8/16-bit Data Bus Static RAM Card

MF38M1-L6DAGXX

Connector Type

Two- piece 68-pin

DESCRIPTION

Mitsubishi's Static RAM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm×54mm×5.0mm).
The cards use an 8/16 bit data bus.
Availabale in 8MB capacities, Mitsubishi's SRAM cards conform to the JEIDA/PCMCIA standard.
Mitsubishi acheived high density memory, while maintaining credit size by using a thin small outline packaging technology(TSOP).
The TSOP surpasses conventional memory card chip-on-board packaging technology where larger, surface-mount devices result in a tradeoff between card size and optimum memory density. This allows up to 16 memory Ics (plus interface circuitry) to be mounted in a card that in only 5.0mm thick.

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size.
- One to 16 memory ICs can be mounted in a card that is only 5.0mm thick.
- Electrostatic discharge protection to 15kV
- Buffered interface
- Write protect switch
- Attribute memory
- 68pin JEIDA/PCMCIA

APPLICATIONS

- Office automation
- Industrial
- Data Communication
- Telecommunications
- Computers
- Consumer

PRODUCT LIST

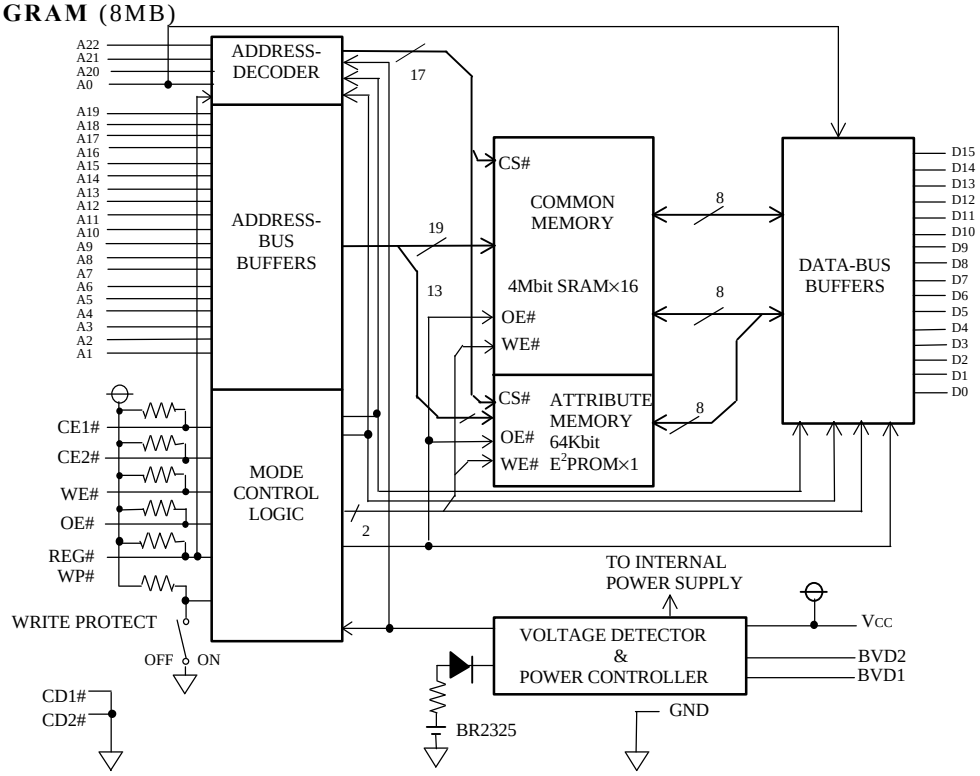
Item / Type name	Memory capacity	Data Bus width(bits)	Attribute memory	Auxialiary battery	Memory organization	Outline drawing	Main battery holder
MF38M1-L6DAGXX	8MB	8/16	YES	NO	4M bit SRAM×16	68P-010	Screw type

PIN ASSIGNMENT
Two-Piece Type (68-pin)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3	Data I/O	36	CD1#	Card detect 1
3	D4		37	D11	Data I/O
4	D5		38	D12	
5	D6		39	D13	
6	D7		40	D14	
7	CE1#	Card enable 1	41	D15	
8	A10	Address input	42	CE2#	Card enable 2
9	OE#	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A9		45	NC	
12	A8		46	A17	Address input
13	A13		47	A18	
14	A14		48	A19	
15	WE#	Write enable	49	A20	
16	NC	No connection	50	A21	
17	VCC	Power supply voltage	51	VCC	Power supply voltage
18	NC	No connection	52	NC	No connection
19	A16	Address input	53	A22	Address input
20	A15		54	NC	No connection
21	A12		55	NC	
22	A7		56	NC	
23	A6		57	NC	
24	A5		58	NC	
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	REG#	REG function
28	A1		62	BVD2	Battery voltage detect 2
29	A0		63	BVD1	Battery voltage detect 1
30	D0	Data I/O	64	D8	Data I/O
31	D1		65	D9	
32	D2		66	D10	
33	WP	Write protect	67	CD2#	Card detect 2
34	GND	Ground	68	GND	Ground

WRITE PROTECT MODE (WP)
When the write protect switch is switched on, this card goes into a write protect mode that can read but not write data.
In this mode, WP pin becomes “H” level.
At the shipment the write protect switch is switched off (Normal mode : The card can be written ; WP pin indicates “L” level).

BLOCK DIAGRAM (8MB)



FUNCTION TABLE

Mode	REG#	CE1#	CE2#	OE#	WE#	A0	I/O (D15~D8)	I/O (D7~D0)	ICC
Standby	X	H	H	X	X	X	High-impedance	High-impedance	standby
Read A (16bit) common	H	L	L	L	H	X	Odd Byte Data out	Even Byte Data out	Active
Write A (16bit) common	H	L	L	H	L	X	Odd Byte Data in	Even Byte Data in	Active
Read B (8bit) common	H	L	H	L	H	L	High-impedance	Even Byte Data out	Active
	H	L	H	L	H	H	High-impedance	Odd Byte Data out	Active
Write B (8bit) common	H	L	H	H	L	L	High-impedance	Even Byte Data in	Active
	H	L	H	H	L	H	High-impedance	Odd Byte Data in	Active
Read C (8bit) common	H	H	L	L	H	X	Odd Byte Data out	High-impedance	Active
Write C (8bit) common	H	H	L	H	L	X	Odd Byte Data in	High-impedance	Active
Output disable	X	X	X	H	H	X	High-impedance	High-impedance	Active
Read A (16bit) attribute	L	L	L	L	H	X	Data out (unknown)	Even Byte Data out	Active
Read B (8bit) attribute	L	L	H	L	H	L	High-impedance	Even Byte Data out	Active
	L	L	H	L	H	H	High-impedance	Data out (unknown)	Active
Read C (8bit) attribute	L	H	L	L	H	X	Data out (unknown)	High-impedance	Active
Write A (16bit) attribute	L	L	L	H	L	X	don't care	Even Byte Data in	Active
Write B (8bit) attribute	L	L	H	H	L	L	don't care	Even Byte Data in	Active
	L	L	H	H	L	H	don't care	don't care	Active
Write C (8bit) attribute	L	H	L	H	L	X	don't care	don't care	Active

Note 1 : H=VIH, L=VIL, X=VIH or VIL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3~6.0	V
Vi	Input voltage		-0.3~V_{CC}+0.3	V
Vo	Output voltage		0~V_{CC}	V
T_{opr1}	Operating temperature 1	Read, Write, Operation	0~70	°C
T_{opr2}	Operating temperature 2	Data retention	0~70	°C
T_{stg}	Storage temperature		-30~80	°C

RECOMMENDED OPERATING CONDITIONS(Ta=0~55°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage	4.75	5.0	5.25	V
GND	System ground		0		V
V_{IH}	High input voltage	2.4		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (Ta=0~55°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	I_{OH}=-1.0mA, Other outputs		2.4			V
V_{OL}	Low output voltage	I_{OL}=2mA				0.4	V
I_{IH}	High input current	V_I=V_{CC} V				10	µA
I_{IL}	Low input current	V_I=0V	CE1#, CE2#, WE#, OE#, REG#	-10		-70	µA
			Other inputs			-10	
I_{OZH}	High output current in off state	CE1#=CE2#=V_{IH} or OE#=V_{IH} WE#=V_{IH}, V_O=V_{CC}				10	µA
I_{OZL}	Low output current in off state	CE1#=CE2#=V_{IH} or OE#=V_{IH} WE#=V_{IH}, V_O=0V				-10	µA
I_{CC} 1・1	Active supply current 1	CE1#=CE2#=V_{IL}, other inputs V_{IH} or V_{IL},Outputs=open				280	mA
I_{CC} 1・2	Active supply current 2	CE1#=CE2# ≤ 0.2V, other inputs ≤ 0.2V or ≥ V_{CC}-0.2V, Outputs=open				270	mA
I_{CC} 2・1	Standby supply current 1	CE1#=CE2#=V_{IH} other inputs=V_{IH} or V_{IL}				10	mA
I_{CC} 2・2	Standby supply current 2	CE1#=CE2# ≥ V_{CC}-0.2V other inputs ≤ 0.2V or ≥ V_{CC}-0.2V				1	mA
VBDET1	Battery detect reference voltage 1*	Vcc=5V,Ta=25°C		2.27	2.37	2.47	V
VBDET2	Battery detect reference voltage 2*	Vcc=5V,Ta=25°C		2.55	2.65	2.75	V

Note 2 : Currents flowing into the IC are taken as positive (unsigned).
3 : Typical values are measured at V_{CC}=5V, Ta=25°C.
*Pin asserted when battery voltage drops below specified level.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I=GND, V_I=25mVrms f=1 MHz, Ta=25°C			30	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms f=1 MHz, Ta=25°C			20	pF

Note 4 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS
Read Cycle (Ta=0~55°C, V_{CC}=5V±5%, unless otherwise noted)

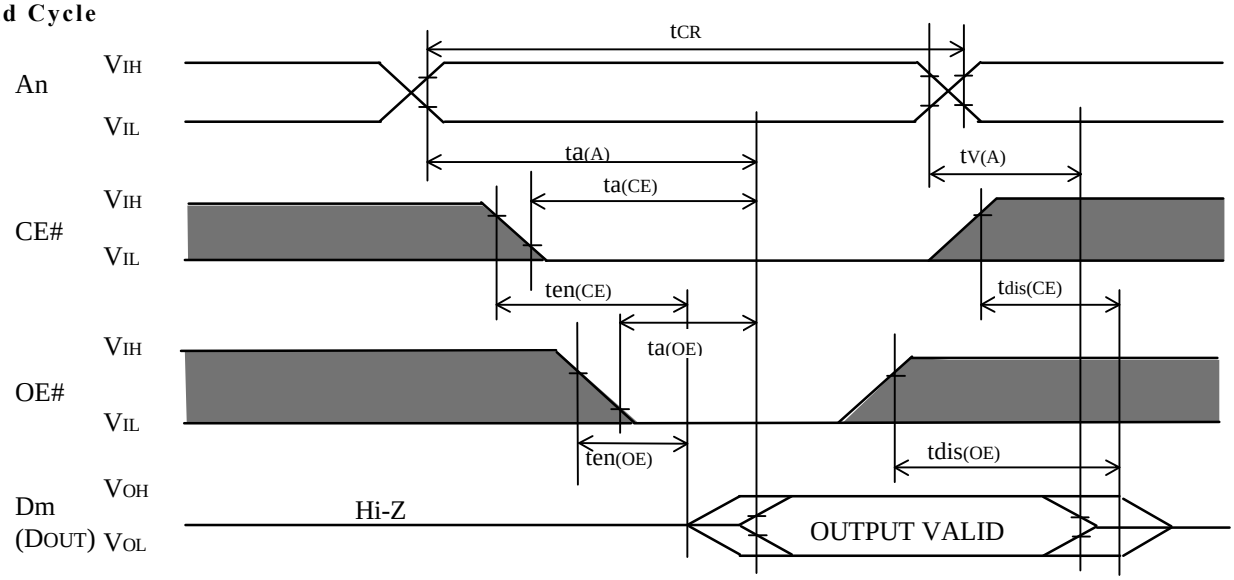
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CR}	Read cycle time	200			ns
t_a(A)	Address access time			200	ns
t_a(CE)	Card enable access time			200	ns
t_a(OE)	Output enable accese time			100	ns
t_{dis}(CE)	Output disable time (from CE#)			90	ns
t_{dis}(OE)	Output disable time (from OE#)			90	ns
t_{en}(CE)	Output enable time (from CE#)	5			ns
t_{en}(OE)	Output enable time (from OE#)	5			ns
t_V(A)	Data valid time (after address change)	0			ns

TIMING REQUIREMENTS
Write Cycle (Ta=0~55°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CW}	Write cycle time	200			ns
$t_{w(WE)}$	Write pulse width	120			ns
$t_{su(A)}$	Address set up time	20			ns
$t_{su(A-WEH)}$	Address set up time with respect to WE# high	140			ns
$t_{su(CE-WEH)}$	Card enable set up time with respect to WE# high	140			ns
$t_{su(D-WEH)}$	Data set up time with respect to WE# high	60			ns
$t_{h(D)}$	Data hold time	30			ns
$t_{rec(WE)}$	Write recovery time	30			ns
$t_{dis(WE)}$	Output disable time (from WE#)			90	ns
$t_{dis(OE)}$	Output disable time (from OE#)			90	ns
$t_{en(WE)}$	Output enable time (from WE#)	5			ns
$t_{en(OE)}$	Output enable time (from OE#)	5			ns
$t_{su(OE-WE)}$	OE# set up time with respect to WE# low	10			ns
$t_{h(OE-WE)}$	OE# hold time with respect to WE# high	10			ns

TIMING DIAGRAM

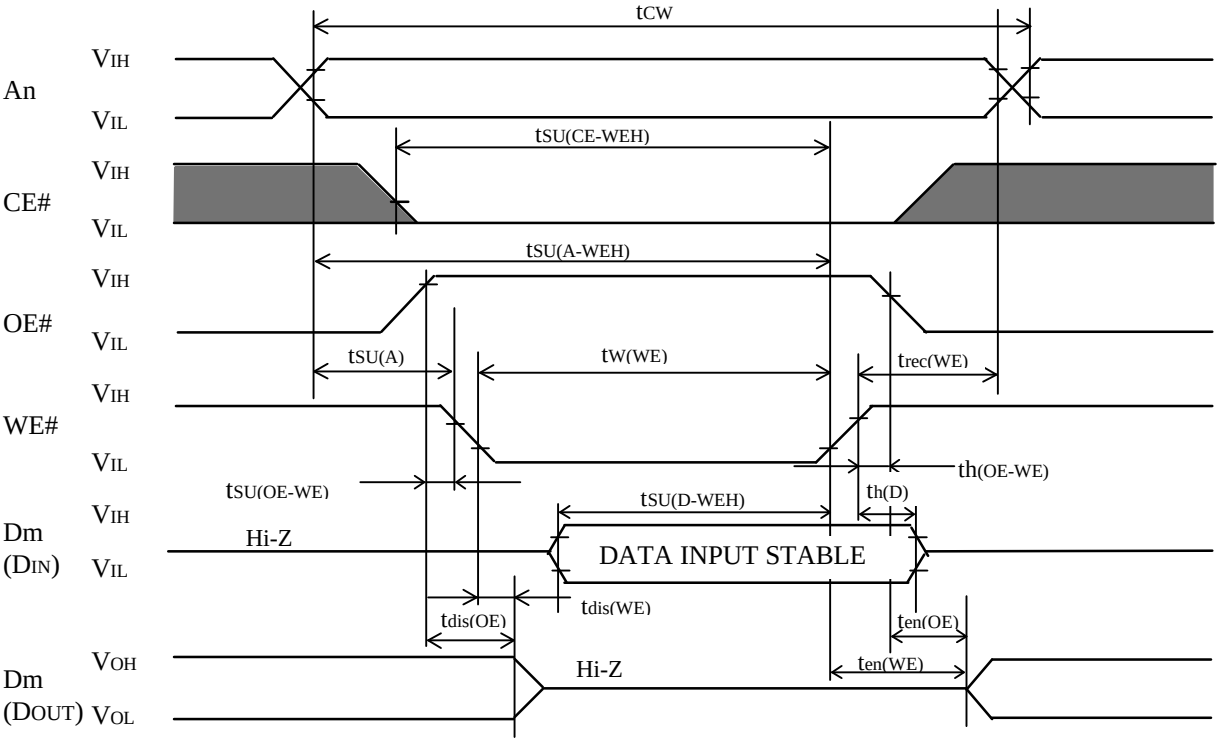
Read Cycle



WE#="H" level
REG#="H" level

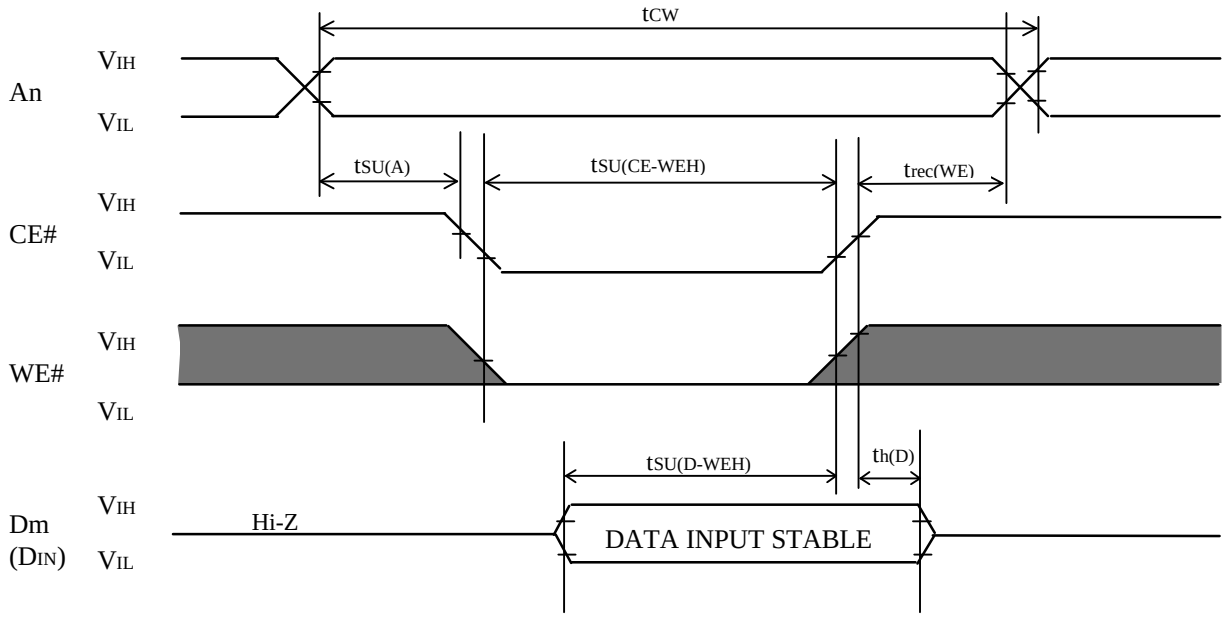
Note 5 : Indicates the don't care input

Write Cycle (WE# control)



REG#="H" level

Write Cycle (CE# control)



OE#="H" level
REG#="H" level

SWITCHING CHARACTERISTICS (Attribute)
Read Cycle (Ta=0~55°C, V_{CC}=5V±5%, unless otherwise noted)

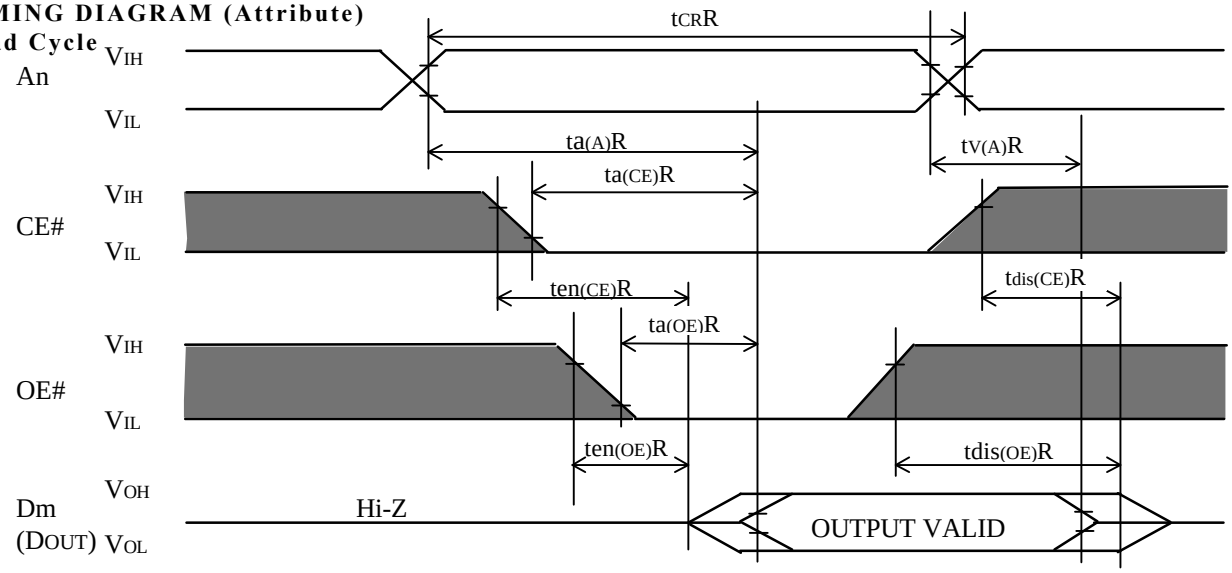
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{CR}R$	Read cycle time	300			ns
$t_{a(A)}R$	Address access time			300	ns
$t_{a(CE)}R$	Card enable access time			300	ns
$t_{a(OE)}R$	Output enable access time			150	ns
$t_{dis(CE)}R$	Output disable time (from CE#)			100	ns
$t_{dis(OE)}R$	Output disable time (from OE#)			100	ns
$t_{en(CE)}R$	Output enable time (from CE#)	5			ns
$t_{en(OE)}R$	Output enable time (from OE#)	5			ns
$t_{V(A)}R$	Data valid time after address change	0			ns

TIMING REQUIREMENTS (Attribute)
Writte Cycle (Ta=0~55°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Paramete	Limits			Unit
		Min.	Typ.	Max.	
$t_{AS}R$	Address setup time	30			ns
$t_{AH}R$	Address hold time	30			ns
$t_{CS}R$	CE# setup time	40			ns
$t_{CH}R$	CE# hold time	30			ns
$t_{DS}R$	Data setup time	120			ns
$t_{DH}R$	Data hold time	40			ns
$t_{ODS}R$	OE# setup time	30			ns
$t_{OEH}R$	OE# hold time	40			ns
$t_{WP}R$	Write pulse width	170			ns
$t_{DL}R$	Data latch time	120			ns
$t_{BL}R$	Byte load time	100			µs
$t_{BLC}R$	Byte load cycle time	0.3		30	µs
$t_{WC}R$	Write cycle time	10			ms
$t_{en(OE)}R$	Output enable time from OE#	5			ns
$t_{DF}R$	Output disable time from OE#	0		100	ns

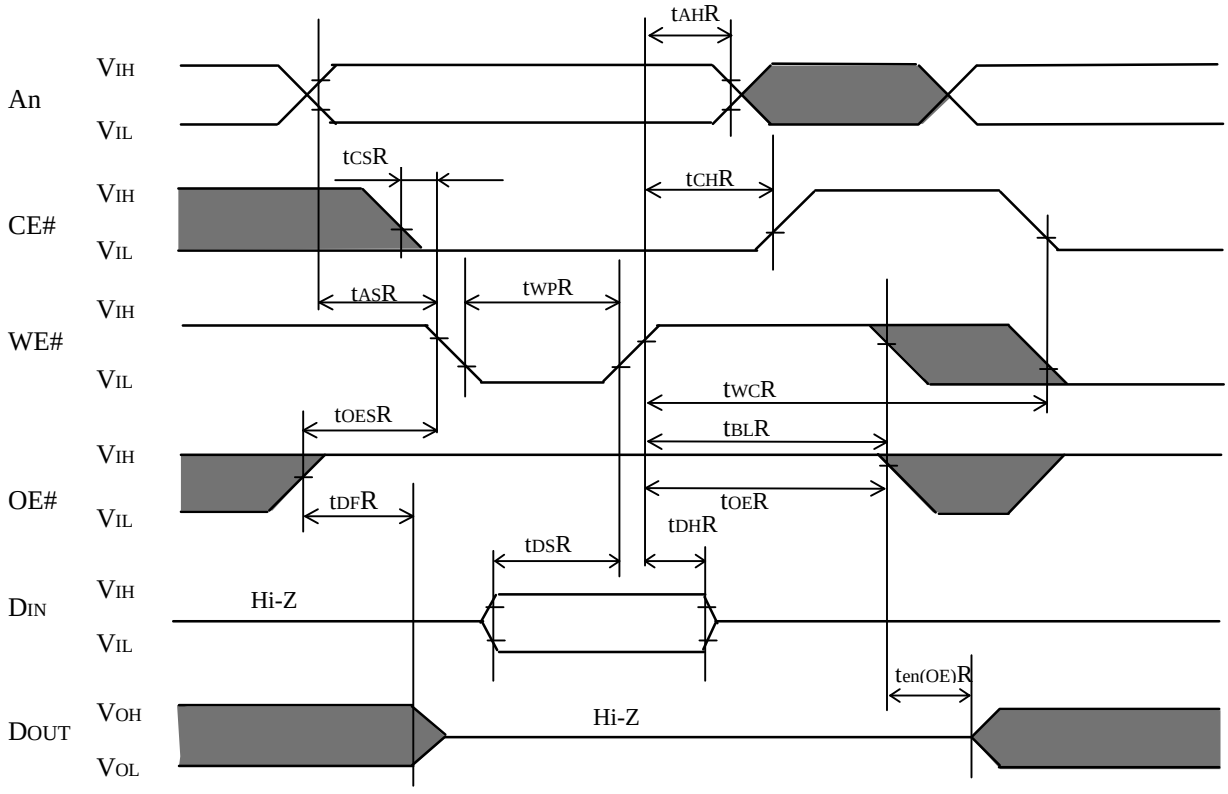
TIMING DIAGRAM (Attribute)

Read Cycle



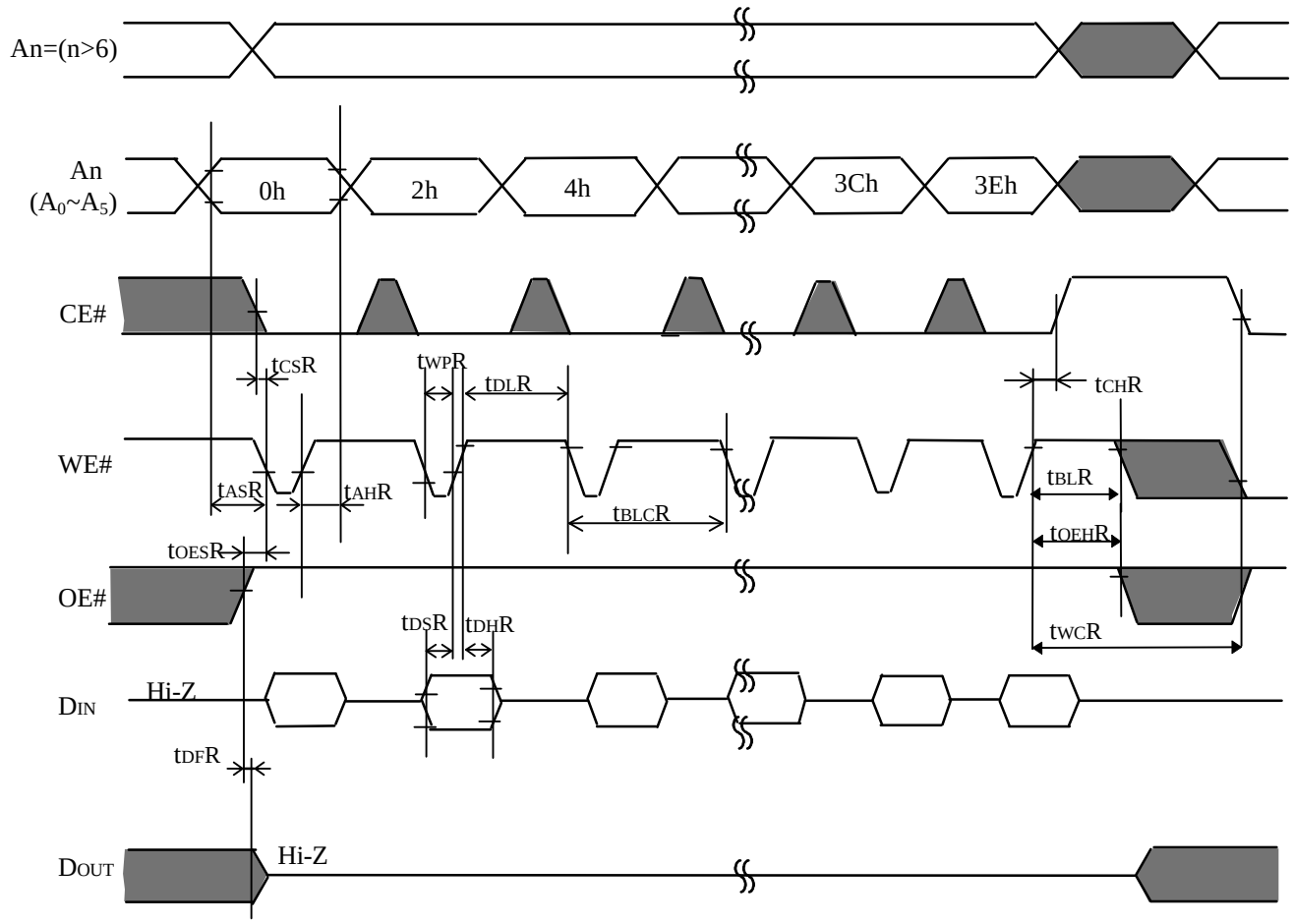
WE#="H" level
REG#="L" level

BYTE WRITE TIMING CHART



REG#="L" level

PAGE MODE WRITE TIMING CHART



REG#="L" level

Note 6 : Test Conditions

Input pulse levels : V_{IL}=0.4V, V_{IH}=2.8V

Input pulse rise, fall time : tr=tf=10ns

Reference voltage

Input : V_{IL}=0.8V, V_{IH}=2.4V

Output : V_{OL}=0.8V, V_{OH}=2.0V

(ten and tdis are measured when output voltage is± 500mV from steady state.)

Load : 100pF+1 TTL gate

5pF+1 TTL gate (at ten and tdis measuring)

7 : Writing is executed in overlap of CE# and WE# are "L" level. (only for Common Memory)

8 : Don't apply inverted phase signal externally when Dm pin is in output mode.

9 : CE# is indicated as follows:

Read A/Write A : CE#=CE1#=CE2#

Read B/Write B : CE#=CE1#, CE2#="H" level

Read C/Write C : CE#=CE2#, CE1#="H" level

ELECTRICAL CHARACTERISTICS

BATTERY BACKUP(Ta=0~55°C, unless otherwise noted)

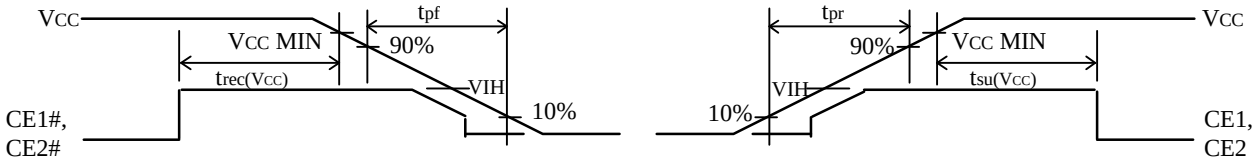
Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{BATT}	Back-up enable battery voltage	All pins open	2.6			V
$V_{I(CE)}$	Card enable voltage	2.4V≤V_{CC}≤5.25V	2.4			V
		0V≤V_{CC}<2.4V	V_{CC}-0.1	V_{CC}	VCC+0.1	
I_{CC}(BUP)	Battery back-up supply current	All pins open, V_{BATT}=3V, Ta=25°C			17	µA
I_{CC}(BUP)	Battery back-up supply current	All pins open, V_{BATT}=3V			400	µA

TIMING REQUIREMENTS(Ta=0~55°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{pr}	Power supply rise time	0.1		300	ms
t_{pf}	Power supply fall time	3		300	ms
$t_{su(VCC)}$	Setup time at power on	20			ms
$t_{rec(VCC)}$	Recovery time at power off	1000			ns

CARD INSERTION/REMOVAL TIMING DIAGRAM

V_{CC} MIN means Minimum Operating Voltage=4.50V.



Note 10: When the card is holding valuable data, the battery must not be removed unless V_{CC} is present.

BATTERY SPECIFICATIONS

A replaceable battery (type BR2325) with a capacity of 165mAH is used:
Estimated battery life when the card is left continuously.

MF38M1-L6DAGXX	1.0years

Conditions
Temperature : 25°C
Humidity : 60%RH