

DESCRIPTION

The M66007 is a semiconductor integrated circuit providing the 12-bit parallel input-serial output shift register function. This product is completely designed with CMOS to sharply reduce power consumption compared with bipolar or Bi-CMOS product. The M66007, developed as an input only expander IC necessary for microcomputer periphery, is widely applicable as a data parallel/serial conversion IC.

FEATURES

- Control signals of only two pins including LE/D and $\overline{\text{CLK}}$
- Low power consumption of 50 μW /package maximum ($V_{\text{cc}}=5\text{V}$, $T_{\text{a}}=25^{\circ}\text{C}$ at time of standstill)
- Schmitt triggered input (LE/D, $\overline{\text{CLK}}$, D0 to D11)
- Wide operating supply voltage range ($V_{\text{cc}}=2\sim 6\text{V}$)
- Wide operating temperature range ($T_{\text{a}}=-20\sim 75^{\circ}\text{C}$)

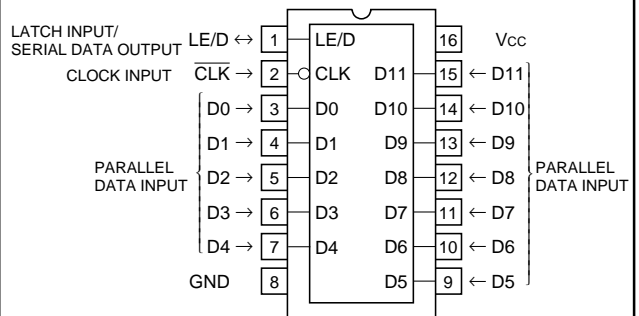
APPLICATION

Parallel/serial data conversion for microcomputer periphery

FUNCTION

The M66007 uses a silicon gate CMOS process to achieve low power consumption and high noise margin. For control signals, this IC adopts only the two pins of latch input/serial data output LE/D and clock input $\overline{\text{CLK}}$. Each bit of shift register of 12-bit parallel input-serial output consists of flip-flop for shift. When LE/D is placed in input mode, $\overline{\text{CLK}}$ is set to "H" and LE/D changes from "H" to "L", the status of parallel data inputs D0 to D11 at that time is latched with the flip-flop for shift and LE/D is switched to output mode to output "L".

PIN CONFIGURATION (TOP VIEW)



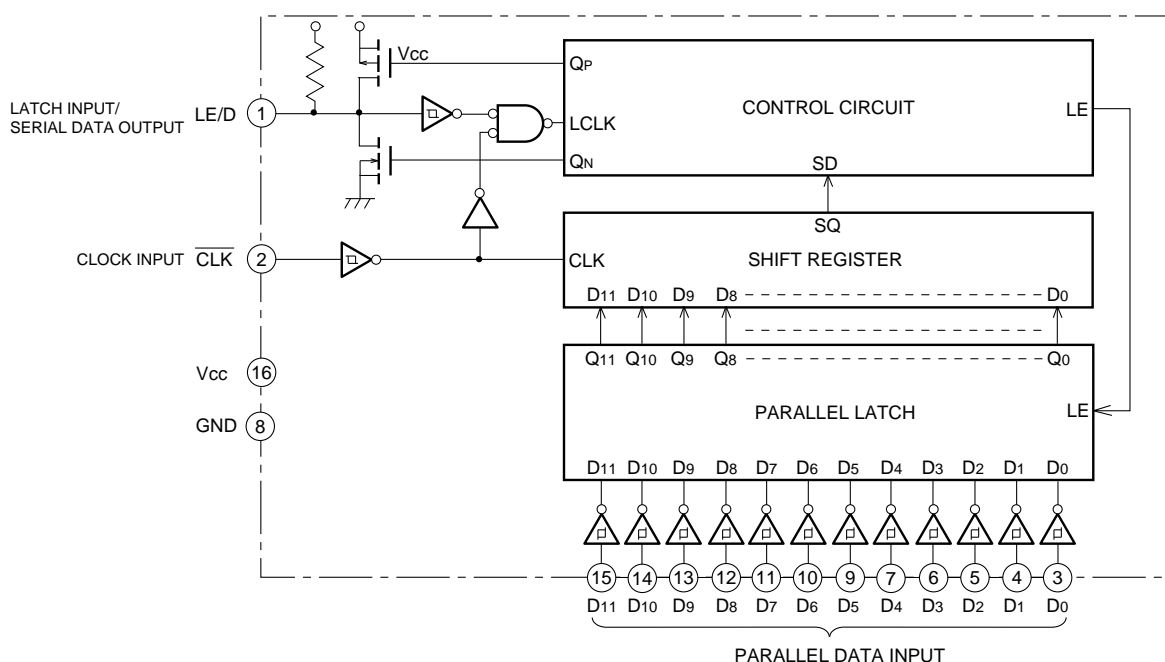
Outline 16P4
 16P2N-A

After this, change of $\overline{\text{CLK}}$ from "H" to "L" makes the shift register perform shift operation and LE/D outputs the contents of the shift register from D0 in order.

In addition, the shift operation for up to the 12th bit is carried out and then LE/D is switched to the input mode at the falling edge of $\overline{\text{CLK}}$ of the 13th bit.

When power is turned on, the input/output mode of LE/D is indeterminate. However, detection of 13 or more falling edges of $\overline{\text{CLK}}$ sets LE/D in the input mode.

BLOCK DIAGRAM

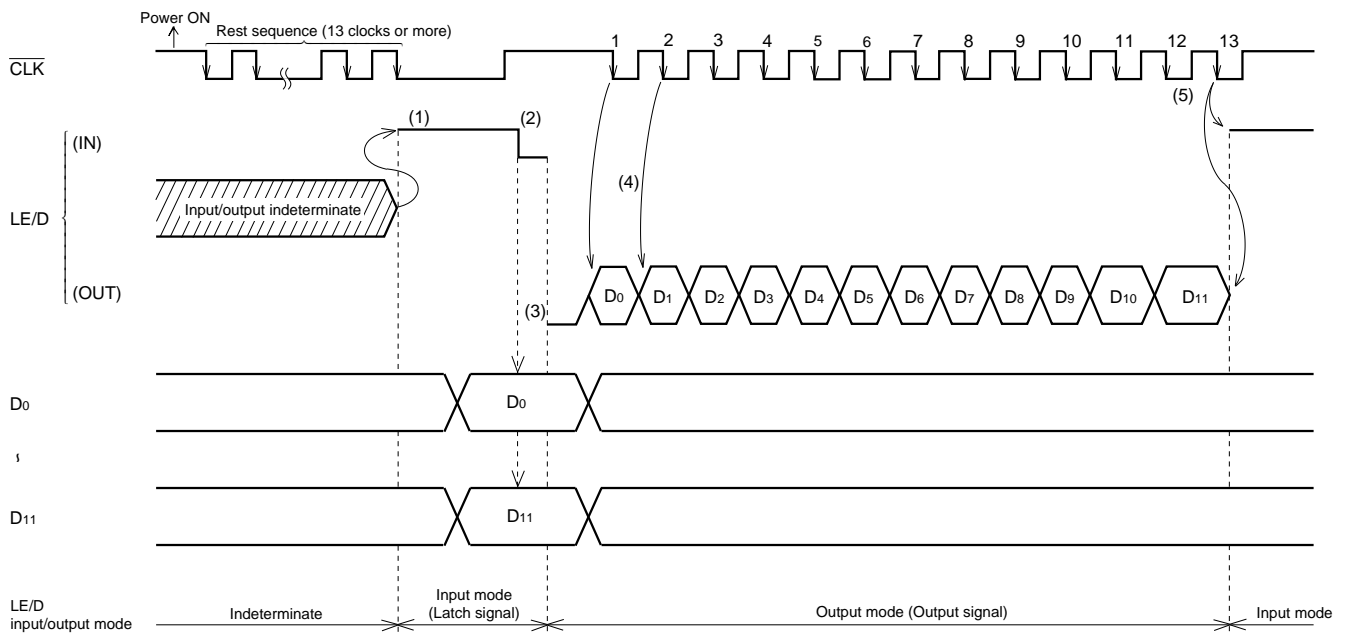


DESCRIPTION OF OPERATION

- (1) When power is turned on, LE/D is placed in input/output indeterminate mode. However, detection of 13 or more of falling edges of CLK sets LE/D in input mode.
- (2) When LE/D is placed in input mode, and $\overline{\text{CLK}}$ is set to "H", access starts at a falling edge of LE/D and the status of D0 to D11 is latched.
- (3) In addition, LE/D switches from input mode to output mode and then outputs "L".

- (4) At a falling edge of $\overline{\text{CLK}}$ from "H" to "L", data latched in step (2) is shifted sequentially and is then output from LE/D in order of D0 to D11.
- (5) After the output of 12-bit data of D0 to D11, LE/D is switched to input mode at the 13th falling edge of CLK to wait for next access. Keep the LE/D pin set to "H" until the next access starts.

OPERATION TIMING CHART



ABSOLUTE MAXIMUM RATINGS (Ta = 20 ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply voltage		-0.5 ~ +7.0	V
VI	Input voltage		-0.5 ~ VCC + 0.5	V
VO	Output voltage		-0.5 ~ VCC + 0.5	V
Iik	Input protection diode current	VI<0V	-20	mA
		VI>VCC	20	
Iok	Output incidental diode current	VO<0V	-20	mA
		VO>VCC	20	
Icc	Power/GND	VCC, GND	±20	mA
Tsig	Storage temperature		-60 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	Supply voltage	2		6	V
VI	Input voltage	0		VCC	V
VO	Output voltage	0		VCC	V
Topr	Operating temperature	-20		75	°C

ELECTRICAL CHARACTERISTICS (VCC = 2 ~ 6V unless otherwise noted)

Symbol	Parameter	Conditions	Limits					Unit
			Ta=25°C		Ta=-20~75°C			
			Min.	Typ.	Max.	Min.	Max.	
VT+	Threshold voltage in positive direction	VO=0.1V, VCC=0.1V, IO=20µA	0.35 × VCC		0.8 × VCC	0.35 × VCC	0.8 × VCC	V
VT-	Threshold voltage in negative direction	VO=0.1V, VCC=0.1V, IO=20µA	0.2 × VCC		0.65 × VCC	0.2 × VCC	0.65 × VCC	V
VOL	Low-level output voltage	VI=VT+, VT- VCC=4.5V	IO=20µA		0.1		0.1	V
			IO=1mA		0.4		0.5	
VOH	High-level output voltage	VI=VT+, VT- VCC=4.5V	IOH=-20µA	4.4		4.4		V
			IOH=-1mA	4.1		4.0		
IO	Maximum output leak current	VI=VT+, VT- VCC=6V	VO=VCC		1.0		10.0	µA
			VO=GND			-0.8		-1.2
Icc	Static consumption current	VI=VCC, GND, VCC=6V, LE/D="H"			10.0		100.0	µA
		VI=VCC, GND, VCC=6V, LE/D="L"			0.8		1.2	mA

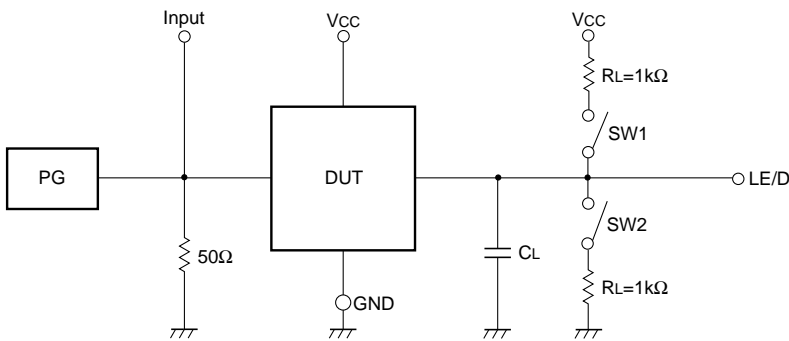
SWITCHING CHARACTERISTICS (VCC=5V)

Symbol	Parameter	Conditions	Limits			Unit
			Ta = -20 ~ 75°C			
			Min.	Typ.	Max.	
fmax	Maximum repetition frequency	CL=50pF (Note 1)	2			MHz
tPLH	Output "L-H", "H-L" propagation time CLK-LE/D				400	ns
tPHL					400	ns
tPLZ					400	ns
tPHZ	Output "L-Z", "H-Z" propagation time CLK-LE/D				400	ns

TIMING REQUIREMENTS ($V_{CC} = 5V$)

Symbol	Parameter	Conditions	Limits			Unit
			$T_a = -20 \sim 75^\circ C$			
			Min.	Typ.	Max.	
tw	CLK pulse width		250			ns
	LE/D pulse width (Input mode)		250			
tsu	CLK set up time for LE/D		100			ns
	D0~D11 set up time for LE/D		100			
th	CLK hold time for LE/D		200			ns
	D0~D11 hold time for LE/D		200			

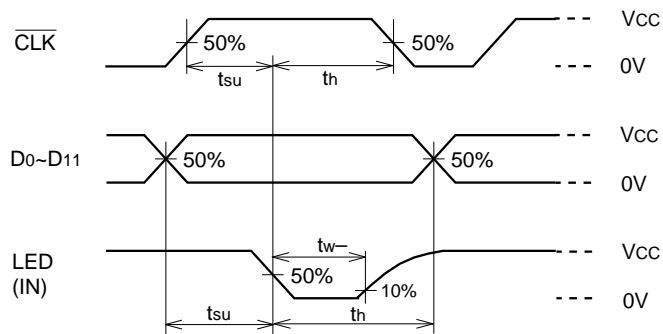
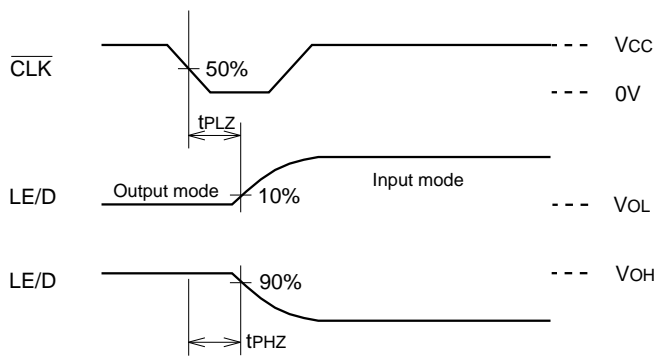
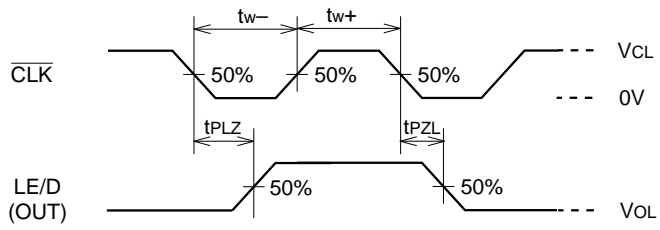
Note 1. Test Circuit



- (1) Characteristics (10%~90%) of pulse generator (PG)
 $t_r = 6ns, t_f = 6ns$
- (2) Electrostatic capacitance C_L includes the floating capacitance of connection and probe input capacitance.

Item	SW1	SW2
tPLH	Open	Open
tPHL	Open	Open
tPLZ	Close	Open
tPHZ	Open	Close

TIMING DIAGRAM



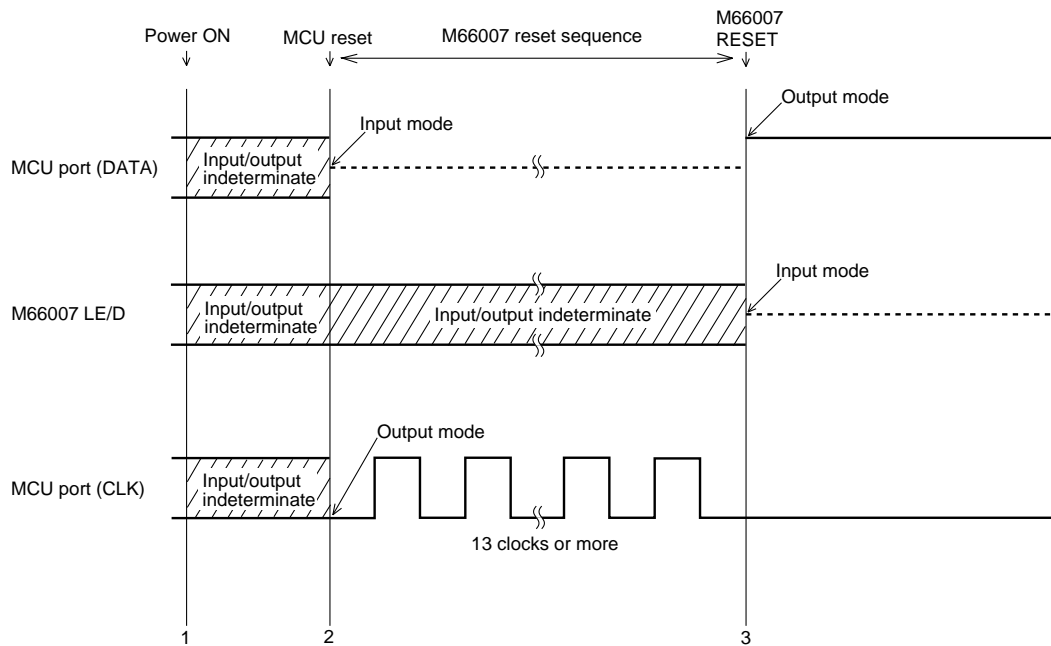
PRECAUTIONS FOR APPLICATION

1. The following timing diagram shows the status of MCU port and LE/D pin of the M66007 when power is turned on. When MCU has been reset to make the collision period of MCU and LE/D line of the M66007 as short as possible, place the port (LE/D) in input mode and execute the reset sequence through the port ($\overline{\text{CLK}}$) promptly to reset the M66007.

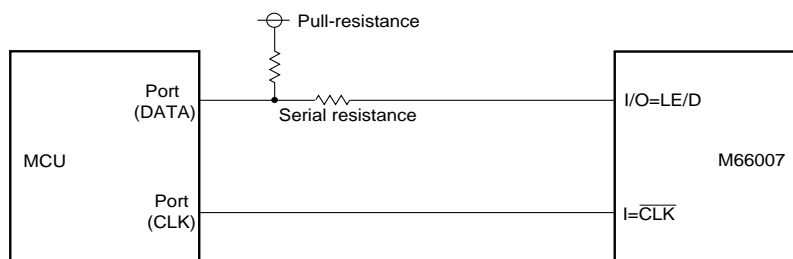
As shown in the diagram, to prevent the IC from being broken due to collision of the LE/D line in the 1-2 section, set in the LE/D line in series a resistance of a degree to which the transmission speed cannot be affected.

2. When the LE/D pin on each of the MPU and M66007 sides switches from input mode to output mode or from output mode to input mode, the LE/D pin may be placed in high impedance status, resulting in oscillation.

To prevent malfunction due to this oscillation, pull up the LE/D line with a high resistance of a degree to which V_{OH} and V_{OL} levels cannot be affected. (with approx. 20kΩ pull-up resistance built-in)



Status of MCU and M66007 with Power Turned on



Connection Example of MCU and M66007