M66006P/FP

12-BIT I/O EXPANDER

DESCRIPTION

The M66006 is a semiconductor integrated circuit which has 12-bit shift register function to execute serial-parallel conversion and parallel-serial conversion.
Because a serial-parallel shift register and a parallel-serial shift register are independently built in this IC, it is possible to read serial input data to a shift register while converting parallel data into serial data. Also, parallel data I/O pins can be set to input mode or output mode bit-by-bit.
The M66006 can be widely used for I/O port expansion of MCU, serial bus system data communication, etc.

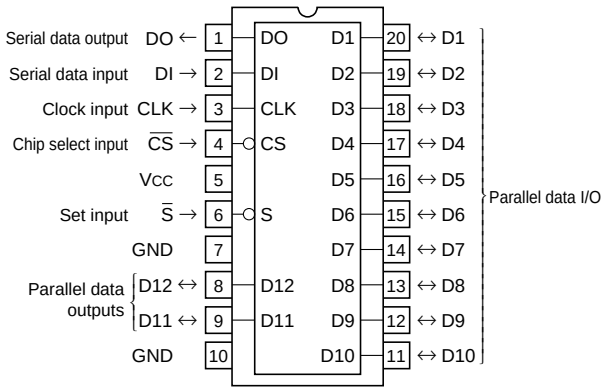
FEATURES

- Bi-directional serial data communication with MCU
- Read of serial data during parallel-serial conversion.
- Bit resolution of serial data I/O
- Low power dissipation (50μW/package max.)
  (V_{CC}=5V, T_a=25°C, in quiescing)
- Schmitt input (DI, CLK, $\overline{S}$, $\overline{CS}$)
- Open drain output (DO, from D1 to D12)
- Parallel data I/O (from D1 to D12)
- Wide operating supply voltage range (V_{CC}=2 to 6V)
- Wide operating temperature range (T_a=–20 to 75°C)

APPLICATION

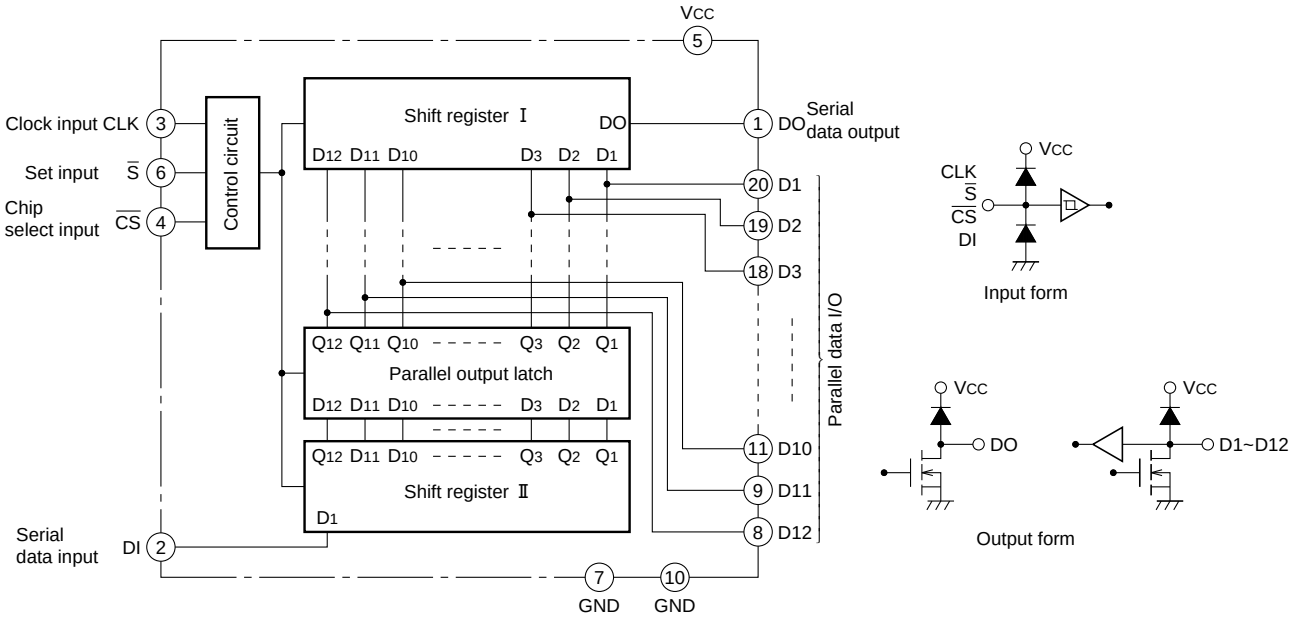
Serial-parallel data conversion, parallel-serial data conversion, serial bus control by MCU.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4
20P2N-A

BLOCK DIAGRAM



FUNCTION

The M66006 realizes low power dissipation and high noise immunity by applying silicon CMOS process.

Because a 12-bit serial-parallel shift register and a 12-bit parallel-serial shift register are independently built in this IC, it is possible to read serial input data while converting parallel data into serial data.

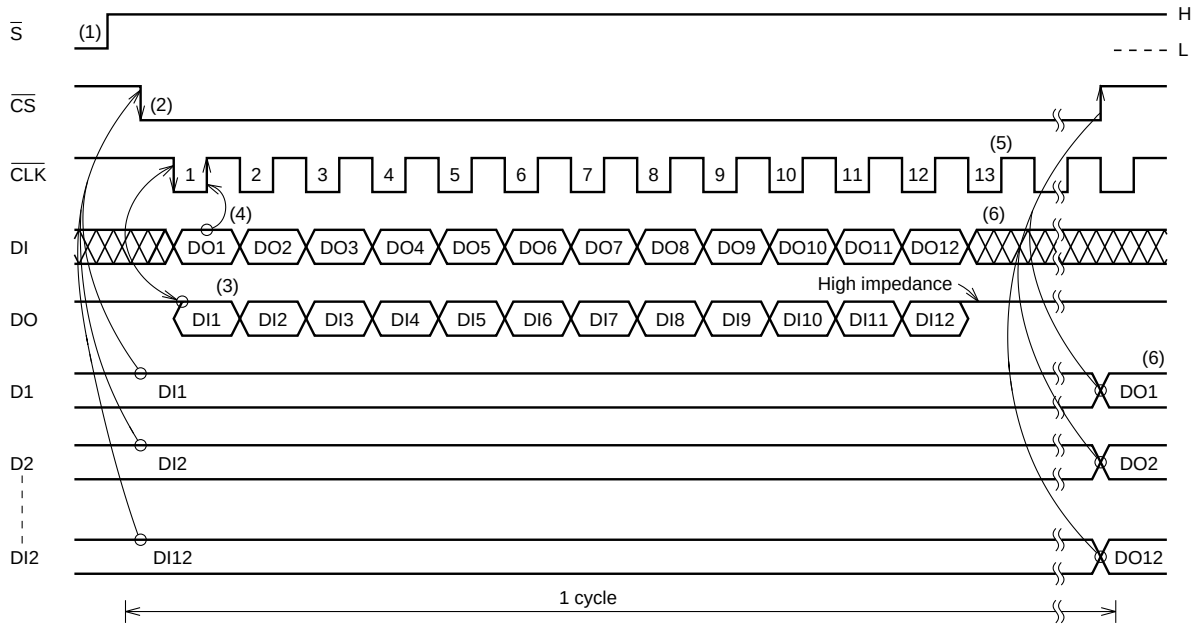
When $\overline{CS}$ changes from "H" to "L", serial output of 12-bit parallel data and read of serial data from the MCU start. That is, 12-bit parallel data is latched at the falling edge of $\overline{CS}$, synchronized with the falling edge of shift clock, and then output to serial output pin DO as serial data. At the same time, serial data from the MCU is read to the internal shift register at the rising edge of shift clock. The shift clock on and after 13th bit is neglected and pin DO is put in the high impedance state when the reading operation is masked. When $\overline{CS}$ changes from "L" to "H", 12-bit serial data read into pin DI is output to parallel output pins from D1 to D12.

Because the output form of parallel output pins is N-channel open drain output, "H" must be written to the pin to set to input mode.

DESCRIPTION OF OPERATION

(1) When power is supplied, pins DO and from D1 to D12 are in undefined state. When $\overline{S}$ changes to "L", those pins are in high impedance state.
(2) At the falling edge of $\overline{CS}$, the status of pins from D1 to D12 is loaded to shift register Ⅰ.
(3) At the falling edge of $\overline{CLK}$, data which is loaded as above (2) is output to pin DO as 12-bit serial data in order.
(4) At the rising edge of $\overline{CLK}$, 12-bit serial data is written from DI to shift register Ⅱ.
(5) CLK on and after the 13th bit is neglected and writing of serial data is not possible. Also, DO is put in the high impedance state.
(6) At the rising edge of $\overline{CS}$, the data which is written as mentioned in (4) is output to pins from D1 to D12.
(7) Shift register Ⅰ loads the data applied externally and the AND-tie data latched by the parallel output latch.
(8) When $\overline{CS}$ rises before $\overline{CLK}$ reaches the 12th bit, the parallel output latch latches the data which has been written to shift register Ⅱ and outputs it to pins from D1 to D12. In this case, shift registers Ⅰ and Ⅱ continues the shift operation and DO outputs serial data until CLK reaches the 12th bit.
(9) Switching of I/O mode of pins from D1 to D12 is controlled by the serial data which is input to pin DI. Pins to which "H" is written operates as input pins.

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = –20 ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
I_{IK}	Input protection diode current	V_I<0V	–20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	–20	mA
		V_O>V_{CC}	20	
I_{GND}	GND current	GND	–48	mA
T_{stg}	Storage temperature		–60 ~ 150	°C

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	–20		75	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 2 ~ 6V unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				T_a=25°C			T_a= –20~75°C		
				Min.	Typ.	Max.	Min.	Max.	
V_{T+}	Positive direction threshold voltage *1	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA		0.35 × V_{CC}		0.8 × V_{CC}	0.35 × V_{CC}	0.8 × V_{CC}	V
V_{T-}	Negative direction threshold voltage *1	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA		0.2 × V_{CC}		0.65 × V_{CC}	0.2 × V_{CC}	0.65 × V_{CC}	V
V_{IH}	"H" input voltage *2	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA		0.75 × V_{CC}			0.75 × V_{CC}		V
V_{IL}	"L" input voltage *2	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA				0.25 × V_{CC}		0.25 × V_{CC}	V
V_{OL}	"L" output voltage	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=3mA			0.4		0.5	V
I_O	Maximum output leak current	V_I=V_{T+}, V_{T-} V_{CC}=6V	V_O=V_{CC}			1.0		10.0	μA
			V_O=GND			–1.0		–10.0	
I_{CC}	Static power dissipation	V_I=V_{CC}, GND, V_{CC}=6V				10.0		100.0	μA

*1: DI, CLK, $\overline{CS}$, $\overline{S}$
*2: D1~D12

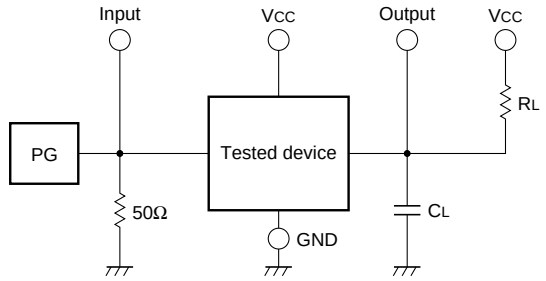
SWITCHING CHARACTERISTICS (V_{CC} = 5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25°C			T_a= –20~75°C		
			Min.	Typ.	Max.	Min.	Max.	
f_{max}	Maximum repeat frequency	C_L=50pF R_L=1kΩ (Note 2)	2.5			1.9		MHz
t_{PLZ}	Output "L-Z", "Z-L" propagation time CLK-DO				300		400	ns
t_{PZL}					300		400	ns
t_{PLZ}	Output "L-Z", "Z-L" propagation time $\overline{CS}$-D1 to D12				300		400	ns
t_{PZL}					300		400	ns
t_{PLZ}	Output "L-Z" propagation time $\overline{S}$-DO, D1 to D12				300		400	ns

TIMING CONDITIONS (V_{CC} = 5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25˚C			T_a= –20~75˚C		
			Min.	Typ.	Max.	Min.	Max.	
t_w	CLK, $\overline{CS}$, $\overline{S}$ pulse width		200			260		ns
t_{su}	Setup time of DI to CLK		100			130		ns
	Setup time of $\overline{CS}$ to CLK		100			130		
	Setup time of D1 to D12 to $\overline{CS}$		100			130		
t_h	Hold time of DI to CLK		100			130		ns
	Hold time of $\overline{CS}$ to CLK		100			130		
	Hold time of D1 to D12 to $\overline{CS}$		100			130		
t_{rec}	Recovery time of $\overline{CS}$ to $\overline{S}$		100			130		ns

NOTE 2: TEST CIRCUIT



(1)Characteristics of pulse generator (PG) (10% to 90%)

t_r=6ns, t_f=6ns, Z_o=50Ω

(2)Static capacitance CL includes floating capacitance of wiring and input capacitance of probe.

TIMING CHARTS