New Product

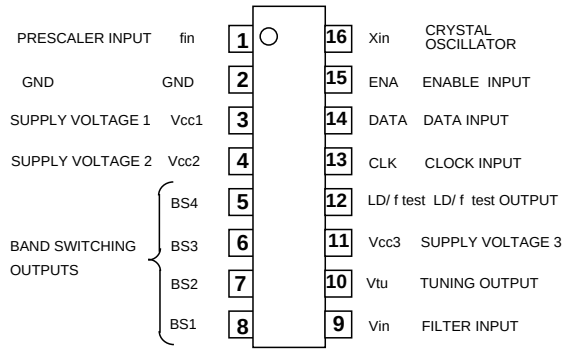
M64893AFP/AGP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

Description

The M64893AFP/AGP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using Bip process. It contains the prescaler with operating up to1.3GHz,4 band drivers and Op.Amp for direct tuning.

PIN CONFIGURATION (TOP VIEW)



OUTLINE 16P2S/16P2Z

16P2S

16P2Z

Features

- 4 integrated PNP band drivers (Io=40mA,Vsat=0.2V typ@Vcc1 to 13.2V)
- Built-in Op.Amp for direct tuning voltage output (33V)
- Low power dissipation (Icc=20mA,Vcc1=5V)
- Built-in prescaler with input amplifier (Fmax=1.3GHz)
- PLL lock/unlock status display out put (Built-in pull up resistor)
- X`tal 4MHz is used to realize 1 type of tuning steps (Division ratio 1/640)
- Serial data input (3 wire bus)
- Built-in Power on reset system
- Small Package(16SOP/16SSOP)

Application

TV,VCR tuners

Recommended operating condition

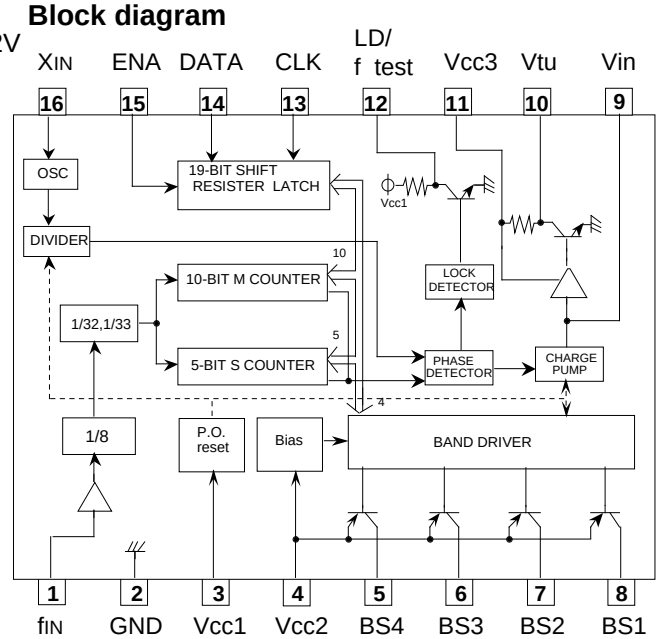
Supply voltage range • • Vcc1=4.5 to 5.5V
Vcc2=Vcc1 to 13.2V
Vcc3=28 to 35V

Rated supply voltage • • Vcc1=5.0V
Vcc2=12V
Vcc3=33V

Function

- 1/32,1/33 dual-modulus prescaler
- 4MHz crystal oscillator,reference divider
- Programmable divider (10-bit M counter,5-bit S counter)
- Tri-state phase comparator
- Lock detector
- Band switch driver
- Op. Amp for direct tuning

Block diagram



Pin description

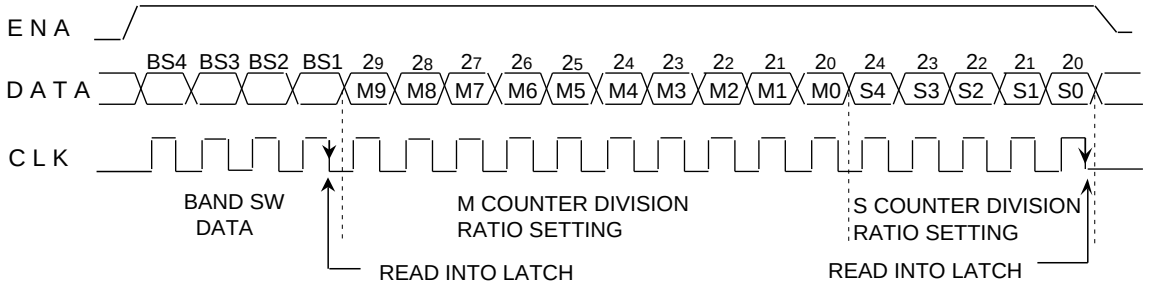
Symbol	Pin No.	Pin name	Function
f in	1	Prescaler input	Input for the VCO frequency.
GND	2	GND	Ground to 0V.
Vcc1	3	Power supply voltage 1	Power supply voltage terminal. 5.0 ±0.5V
Vcc2	4	Power supply voltage 2	Power supply for band switching,Vcc1 to 13.2V
BS4 BS3 BS2 BS1	5 6 7 8	Band switching outputs	PNP open collector method is used. When the band switching data is "H",the output is ON. When it is "L",the output is OFF.
Vin	9	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f 1/N) is ahead compared to the reference frequency (fref), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
Vtu	10	Tuning output	This supplies the tuning voltage.
Vcc3	11	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35V
LD/ f test	12	Lock detect/ Test port	When 19 bit data is input,lock detector is output. When 27 bit data is input, lock detector is output, the programmable freq. Divider output and reference freq. Output is selected by the test mode.
CLOCK	13	Clock input	Data is read into the shift register when the clock signal falls.
DATA	14	Data input	Input for band SW and programmable freq. divider set up.
ENABLE	15	Enable input	This is normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the 19th pulse of the clock signal falls.
X in	16	This is connected to the crystal oscillator.	4.0MHz crystal oscillator is connected.

Method of setting data

The frequency demultiplying ratio uses 15bits. Setting up the band switching output uses 4bits. The test mode data uses 8bits. The total bits used is 27bits.Data is read in when the enable signal is "H" and the clock signal falls.

The band switching data is read in at the 4th pulse of the clock signal.The program counter data is read into the latch by the fall of the 19th pulse of the clock signal. When the enable signal goes to "L" before the 19th pulse of the enable signal, only the band SW data is updated and other data is ignored.

The data is latched at the 19th pulse of the clock signal. At this time, 1/640 frequency division ratio is used. Clock signals after the above are invalid.



How to set the dividing ratio of the programmable divider

Total division N is given by the following formulas in addition to the prescaler used in the previous stage.

N=8 • (32M + S) M : 10 bit main counter division

S : 5 bit swallow counter division

The M and S counters are binary the possible ranges of division are as follows.

$32 \leq M \leq 1023$

$O \leq S \leq 31$

Therefore,the range of division N is 8,192 to 262,136.

The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO} = f_{REF} \times N$

$= 6.25 \times 8 \times (32M + S)$

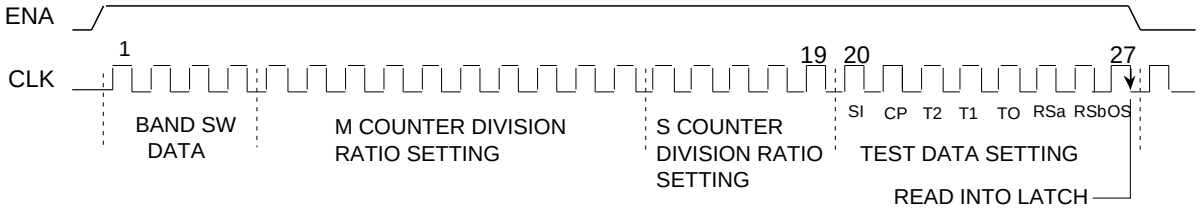
$= 50.0 \times (32M + S)$ [kHz]

But,the tuning frequency range is 51.2MHz to 1300Mz from the maximum prescaler operating frequency.

Test mode data set up method

The data for the test mode uses 20 to 27bits. Data is latched when the 27th clock signal falls.

(1) When transferring 3-wire 27 bit data



(2) Test Mode Bit Set Up

X	:Random, 0 or 1.normal "0"
CP	:Set up the charge pump current value
T0, T1,&T2	:Set up test modes
RSa, Rsa	:Set up for the reference Frequency division ratio
OS	:Set up the tuning amplifier
S I	:1 Only (It is prohibit to "0 ")

Setting up the charge pump current of the phase comparator

CP	Charge pump current	Mode
0	70 uA	Test
1	270 uA	Normal

Setting up for the test mode

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	f_{REF}	Test mode
1	0	1	High impedance	f1/N	Test mode

Set up for the reference Frequency division ratio

RSa	RSb	Division ratio
1	1	1/ 512
0	1	1/ 1024
X	0	1/ 640

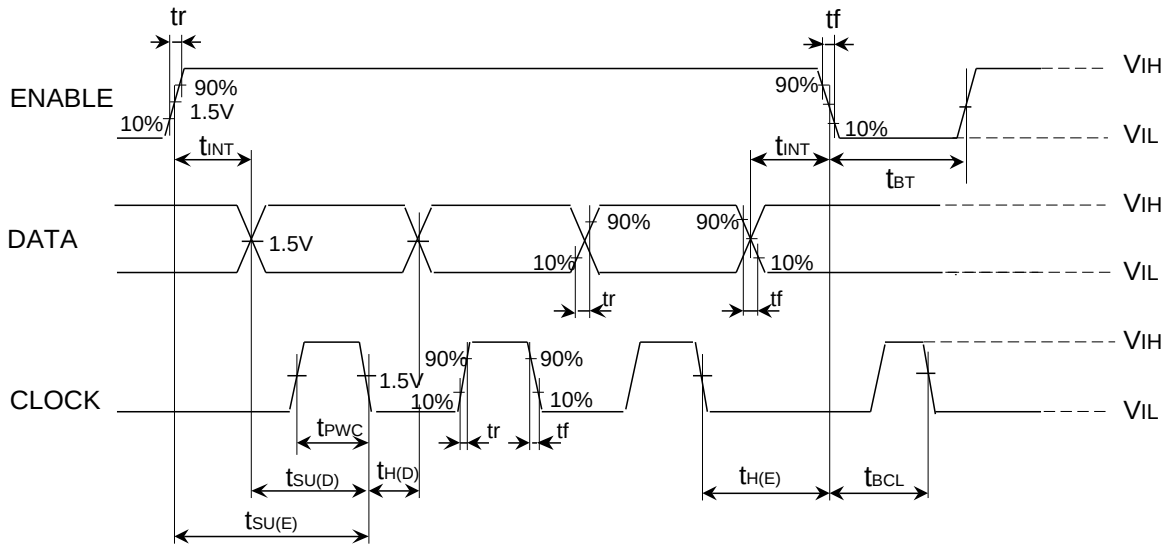
Set up the tuning amplifier

OS	Tuning voltage out put	Mode
0	ON	Normal
1	OFF	Test

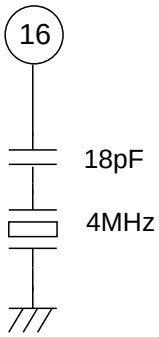
Power on reset operation (Initial state the power is turned ON)

BS4 to BS1 : OFF
Charge pump : High impedance
Tuning amplifier : OFF
Charge pump current : 270uA
Frequency division ratio : 1/640
Lock detect : H

Timing diagram



Crystal oscillator connection diagram



Crystal oscillator characteristics
Actual resistance : less than 3 0 0 Ω
Load capacitance : 2 0 p F

Absolute maximum ratings (Ta=-20°C to +75°C unless otherwise noted)

Parameter	Symbols	Max.ratings	Units	Conditions
Supply voltage 1	Vcc1	6.0	V	Pin3
Supply voltage 2	Vcc2	14.4	V	Pin4
Supply voltage 3	Vcc3	36.0	V	Pin11
Input voltage	VI	6.0	V	Not to exceed Vcc1
Output voltage	Vo	6.0	V	LD output
Voltage applied when the band output is OFF	V_{BSOFF}	14.4	V	
Band output current	I_{BSON}	50.0	mA	per 1 band output circuit
ON the time when the band output is ON	t_{BSON}	10	sec	50mA per 1 band output circuit 3circuits are pn at same time,
Power dissipation	Pd	470	mW	Ta= +75°C
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

Recommended operating conditions (Ta=-20°C to +75°Cunless otherwise noted)

Parameter	Symbol	Ratings	Units	Conditions
Supply voltage 1	Vcc1	4.5 to 5.5	V	Pin3
Supply voltage 2	Vcc2	Vcc1 to 13.2	V	Pin4
Supply voltage 3	Vcc3	28 to 35	V	Pin11
Operating frequency (1)	fopr1	4.0	MHz	Crystal oscillation circuit
Operating frequency (2)	fopr2	80 to 1,300	MHz	
Band output current 5 to 8	I_{BDL}	0 to 40	mA	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.

Electrical characteristics (Ta=-20°C to +75°C unless otherwise noted)
Vcc1=5.0V, Vcc=12V, Vcc3=33V

Parameters	Symbol	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
Input terminals							
"H"input voltage	V_{IH}	13 to 15		3.0	-	Vcc1+0.3	V
"L"input voltage	V_{IL}	13 to 15		-	-	1.5	V
"H"input current	I_{IH}	13 to 15	Vcc1=5.5V ,Vi=4.0V	-	-	10	uA
"L"input current	I_{IL}	13,15	Vcc1=5.5V,Vi=0.4V	-	-6	-10	uA
"L"input current	I_{IL}	14	Vcc1=5.5V ,Vi=0.4V	-	-18	-30	uA
Lock output							
"H"output voltage	V_{OH}	12	Vcc1=5.5V	5.0	-	-	V
"L"output voltage	V_{OL}	12	Vcc1=5.5V	-	0.3	0.5	V
Band SW							
output voltage	V_{BS}	5 to 8	Vcc2=12V Io=-40mA	11.6	11.8	-	V
Leak current	$I_{OIk}2$	5 to 8	Vcc2=12V Band SW is OFF	-	-	-10	uA
Tuning output							
output voltage "H"	V_{toH}	10	Vcc3=33V	32.5	-	-	V
output voltage "L"	V_{toL}	10	Vcc3=33V	-	0.2	0.4	V
Charge pump							
"H" output current	I_{CPH}	9	Vcc1=5.0V Vo=1V	-	±270	±370	uA
"L" output current	I_{CPL}	9	Vcc1=5.0V Vo=1V	-	±70	±110	uA
Leak current	I_{cpLK}	9	Vcc1=5.0V Vo=2.5V	-	-	±50	nA
Supply current 1	I_{cc1}	3	Vcc1=5.5V	-	20	30	mA
Supply current 2							
4 circuits OFF	I_{cc2A}	4	Vcc2=12V	-	-	0.3	mA
1 circuits ON,							
Output open	I_{cc2B}	4	Vcc2=12V	-	6.0	8.0	mA
Output current 40mA	I_{cc2C}	4	Vcc2=12V Io=-40mA	-	46.0	48.0	mA
Supply current 3	I_{cc3}	11	Vcc3=33V Output ON	-	3.0	4.0	mA

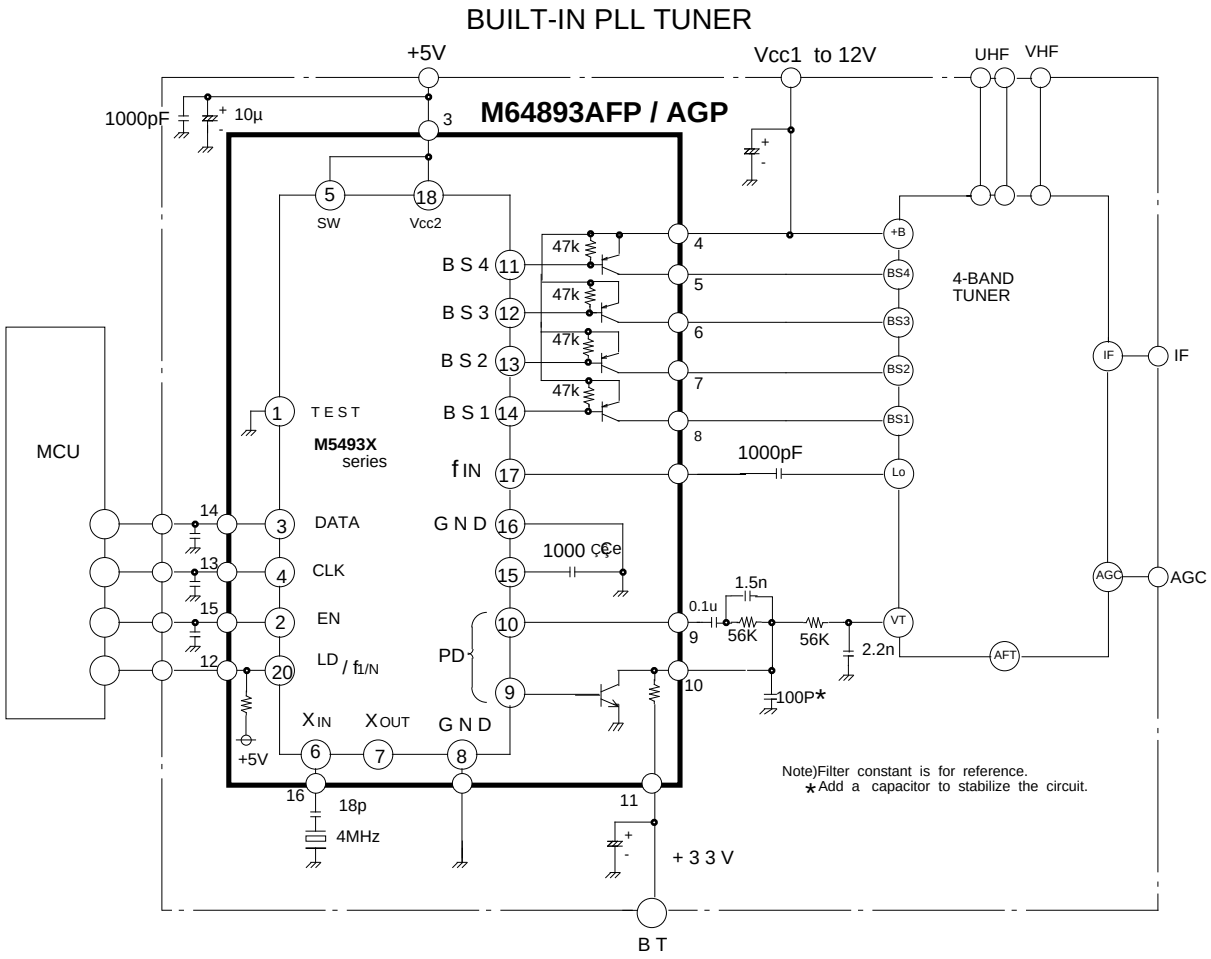
The typical values are at Vcc1=5V,Vcc2=12V,Vcc3=33V,Ta=+25°C

Switching characteristics (Ta=-20°C to +75°C unless otherwise noted)

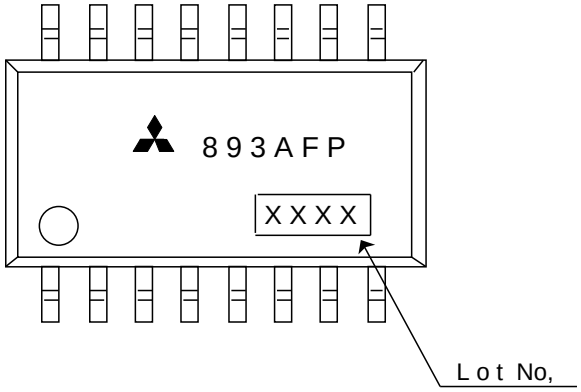
Vcc1=5.0V, Vcc2=12V, Vcc3=33V

Parameter	Symbol	Test pin	Test conditions	Limits			Unit
				Min.	Typ	Max	used
Prescaler operating frequency	f opr2	1	Vcc1=4.5 to 5.5V Vin=Vinmin to Vinmax	80	-	1300	MHz
Operating input voltage	V in	1	Vcc1=4.5 to 5.5V 80 to 100MHz 100 to 200MHz 200 to 800MHz 800 to 1000MHz 1000 to 1300MHz	- 24 - 27 - 30 - 27 - 18	- - - - -	4 4 4 4 4	dBm
Clock pulse width	t PWC	13	Vcc1=4.5 to 5.5V	1	-	-	us
Data setup time	t SU(D)	14	Vcc1=4.5 to 5.5V	2	-	-	us
Data hold time	t H(D)	14	Vcc1=4.5 to 5.5V	1	-	-	us
Enable setup time	t SU(E)	15	Vcc1=4.5 to 5.5V	3	-	-	us
Enable hold time	t H(E)	15	Vcc1=4.5 to 5.5V	3	-	-	us
Enable data interval time	t INT	15,14	Vcc1=4.5 to 5.5V	1	-	-	us
Rise time	t r	13,14,15	Vcc1=4.5 to 5.5V	-	-	1	us
Fall time	t f	13,14,15	Vcc1=4.5 to 5.5V	-	-	1	us
Next enable prohibit time	t BT	15	Vcc1=4.5 to 5.5V	5	-	-	us
Next clock prohibit time	t BCL	13,15	Vcc1=4.5 to 5.5V	5	-	-	us

Application example

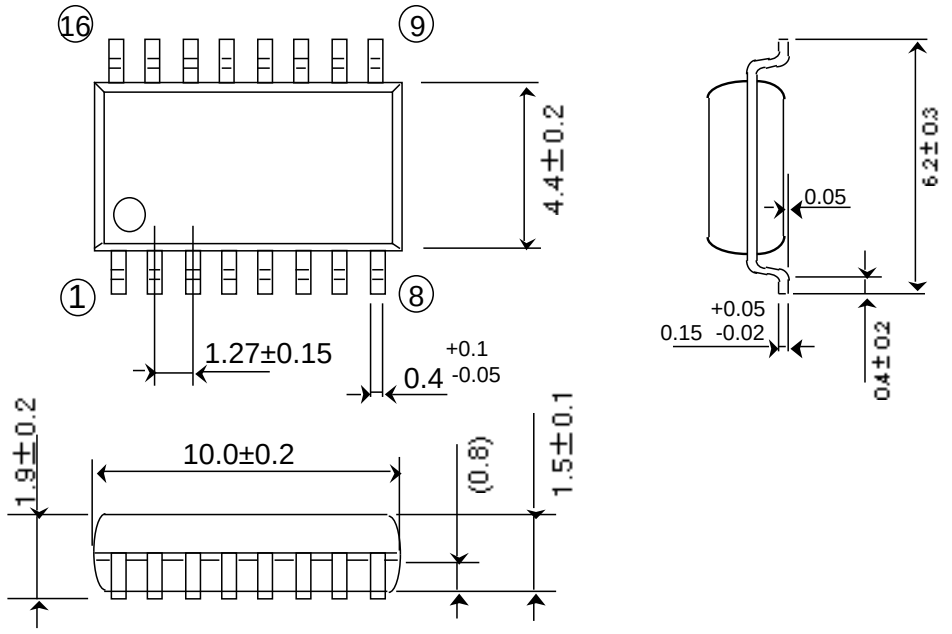


Marking DWG (M 6 4 8 9 3 A F P)

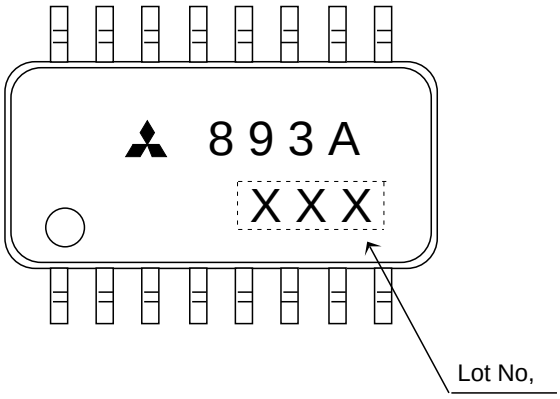


External appearance

16P2S type <16pin plastic mold SOP> Unit:mm



Marking DWG (M 6 4 8 9 3 A G P)



External appearance

16P2Z type <16pin plastic mold SSOP> Unit:mm