MT90840

Distributed Hyperchannel Switch

Advance Information

Features

- Time-slot interchange function between 8 pairs of ST-BUS/GCI/MVIP streams (512 channels) and a Parallel Data Port (PDP)

- Supports star, point to point connections and unidirectional or bidirectional ring topologies for distributed systems

- Input to Output Bypass function with minimum delay for shared ring applications

- Provides an internal latency adjustment buffer for ring applications

- Parallel port data rates up to 19.44Mbyte/s

- Programmable data rates on the serial port side (2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s)

- Unidirectional Parallel switching mode for up to 2430 channels non-blocking

- Per-channel direction control on the serial port side

- Per-channel message mode and high-impedance control on both parallel and serial port sides

- 8-bit multiplexed port compatible with Intel and Motorola microcontrollers

- Guarantees frame integrity when switching wideband channels such as ISDN H0 channel

- Provides external control lines allowing the fast parallel interface to be shared with other devices

Ordering Information

MT90840AK	100 Pin PQFP
MT90840AP	84 Pin PLCC
-40°C to 85°C	

- Special diagnostic alarm functions for statistical analysis

- JTAG boundary scan

Applications

- Bridging ST-BUS/MVIP buses to high speed Time Division Multiplex backplanes at SONET rates (STS-1/3)

- High speed isochronous backbones for distributed PBX and Local Area Network systems

- Switch platforms of up to 2430 channels with guaranteed frame integrity for wideband channels

- Serial bus control and monitoring

- Data multiplexer

- High speed communications interface

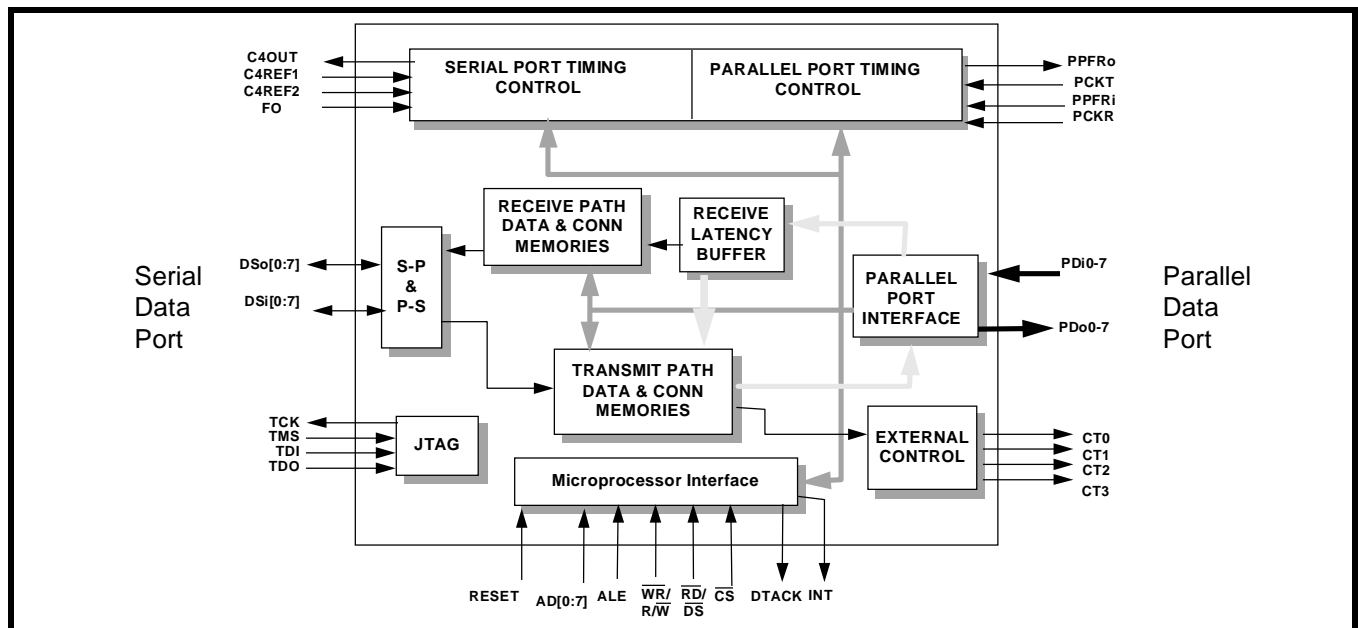- Isochronous switching/multiplexing to support IEEE 802.9 standards

Figure 1 - Functional Block Diagram

Functional Description

Real time multimedia applications require the transmission of mixed voice and data transmission into the same integrated network and transmission media. The network must simultaneously ensure that data (at N x 64 kbit/s) maintains time slot sequence integrity and provide constant delay through the switch.

The MT90840 device bridges existing Mitel ST-BUS components into a new networking environment. Mixed data, voice and video signals can be time-interchanged or multiplexed from serial PCM streams onto a serial high speed Time Division Multiplex (TDM) isochronous backbone operating at SONET rates such as 51 (STS-1) or 155 Mb/s (STS-3). Figure 1 shows the MT90840 functional block diagram.

Today, transmission links operating at SONET rates utilize Serial-to-Parallel and Parallel-to-Serial converter devices (or framers) which perform embedded framing functions and give the user the access to the payload of the high speed frame.

The MT90840 device provides an 8-bit bidirectional parallel data port (PDP) which directly interfaces to the user data interface of typical high speed framers, allowing designers to build distributed networking systems with interconnection speeds up to 155 Mb/s. Figure 2 depicts an example of distributed networking application in Computer Telephony Integration (CTI) systems. Figure 3 shows an example of interconnection between the MT90840 and high speed S/P & P/S framers used when implementing 155 Mb/s transmission links.

The MT90840 device is designed to switch 64 kbit/s or wideband N x 64 kb/s channels from a Serial Data Port (SDP) to the Parallel Data Port (connected to high speed framers) and vice versa. The MT90840 Parallel Data Port is designed to accept data rates up to 19.44 Mbyte/s and the Serial Data Port can be programmed to connect to PCM serial streams at 2.048, 4.096 and 8.192 Mb/s.

Since the parallel and serial ports of the MT90840 device operate at different rates, an internal rate converter circuit associated with a multiple buffer time interchange block is employed to achieve the rate adaptation between the two ports.

The internal time interchange block allows the switching of 512 64 kb/s channels on the serial interface in a flexible connection scheme. This is accomplished by a feature called "per channel direction control" available on the 16 serial streams. For example, in some applications up to 512 channels from the serial port can be time interchanged to the parallel port side. In the opposite direction up to 512 channels coming from the parallel port can be dropped or time interchanged to the serial port side.

The device's clock synchronization and reference options allow many applications and topologies when isochronous TDM backbones are required. Two major clock synchronization schemes provided by the MT90840 allow the serial port interface (ST-BUS) to provide the master clock and frame reference signals for the distributed high speed backbone (master operation) or to derive the entire ST-BUS clock and frame reference signals from the high speed backbone (slave operation). Figure 3 depicts an example of Master Operation.

This type of synchronization scheme may be used in applications such as MVIP multi-chassis level 3 interface (MC-3 system) utilizing point to point or point to multipoint switching connections.

When the MT90840 device operates in a ring type of application like the system depicted in Figure 2, a special mode called Parallel Data Bypass is provided to allow all or part of the received input parallel data to be bypassed to the output parallel port feeding the ring back with the data which is not destined (to be dropped) to the local station. The selection of the data destined (dropped) for the local station can be done through CPU programming. In this mode, the CPU has the full control on managing the outgoing bandwidth (from the serial interface to the high speed link) so that it does not contend with the bypassed data.

For CPU access to the serial channels, the MT90840 device can be programmed using message mode with fast memory access times. By using the Mitel message mode, the microprocessor can access serial input and output TDM data on a per channel basis to control devices such as the Mitel's digital transceivers like MT8972B, MT8930/1, MT8910 and T1/CEPT trunks through the ST-BUS interface.
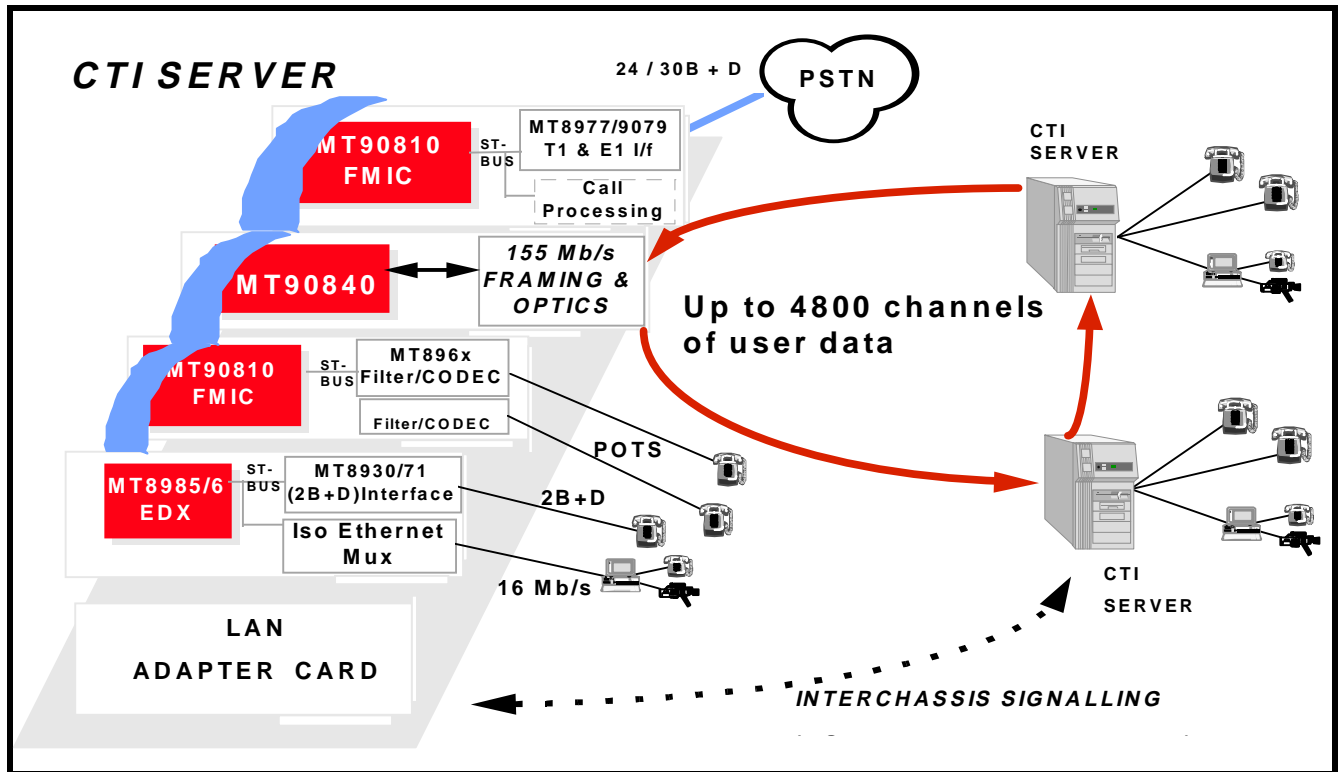
Application Examples
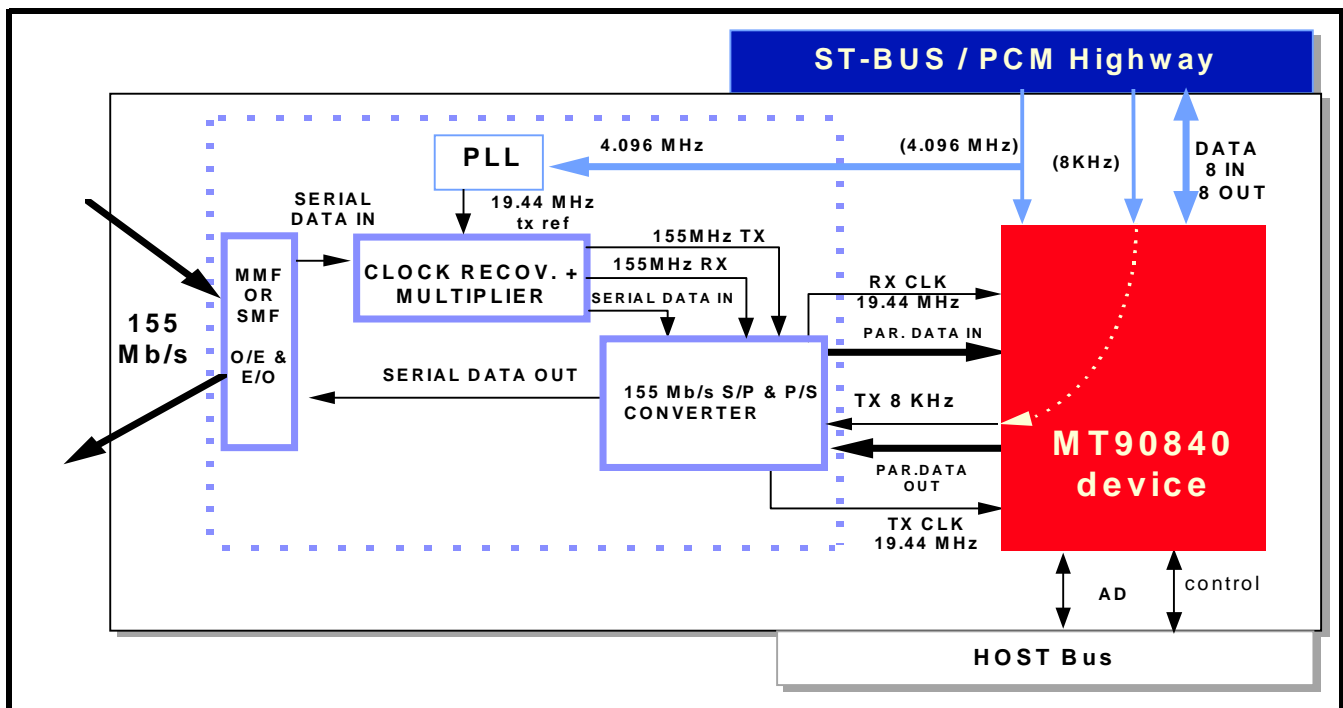

Figure 2 - CTI Multichassis Connection using 155 Mb/s

Figure 3 - Example of a 155 Mb/s Backbone Access Module

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