288Mb SIO REDUCED LATENCY (RLDRAM II)

MT49H16M18C
MT49H32M9C

FEATURES

- 288Mb
- 400 MHz DDR operation (800 Mb/s/pin data rate)
- Organization
  - 16 Meg x 18, 32 Meg x 9 Separate I/O
  - 8 banks
- Cyclic bank switching for maximum bandwidth
- Reduced cycle time (20ns at 400 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM type interface
- Read latency (RL), row cycle time and burst sequence length programmable
- Balanced read and write latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DK, DK#)
- On-chip DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (8K refresh for each bank; 64k refresh command must be issued in total each 32ms)
- 144-ball FBGA package
- HSTL I/O (1.5V or 1.8V nominal)
- 25 ohm–60 ohm matched impedance outputs
- 2.5V VEXT, 1.8V VDD, 1.5V or 1.8V VDDQ I/O
- On-die termination (ODT) RTT

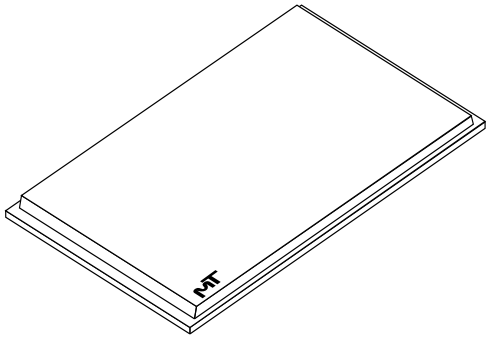
OPTIONS / MARKING

- Clock Cycle Timing
  - 2.5ns (400 MHz) -2.5
  - 3.3ns (300 MHz) -3.3
  - 5ns (200 MHz) -5
- Configuration
  - 16 Meg x 18 MT49H16M18CFM
  - 32 Meg x 9 MT49H32M9CFM
- Package
  - 144-ball, 11mm x 18.5mm FBGA FM

Table 1: Valid Part Numbers

PART NUMBER	DESCRIPTION
MT49H16M18CFM-xx	16 Meg x 18 RLDRAM II
MT49H32M9CFM-xx	32 Meg x 9 RLDRAM II

Figure 1
144-Ball FBGA



GENERAL DESCRIPTION

The Micron® 288Mb Reduced Latency DRAM (RLDRAM) is a high-speed memory device designed for high-bandwidth communication data storage. Applications include, but are not limited to, transmitting or receiving buffers in telecommunication systems and data or instruction cache applications requiring large amounts of memory. The chip's eight-bank architecture is optimized for high speed and achieves a peak bandwidth of 28.8 Gb/s using two separate 18-bit double data rate (DDR) ports and a maximum system clock of 400 MHz.

The double data rate (DDR) separate I/O interface transfers two 18- or 9-bit wide data word per clock cycle at the I/O pins. The read port has dedicated data ouputs to support READ operations, while the write port has dedicated input pins to support WRITE operations. This architecture eliminates the need for high-speed bus turnaround. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock.

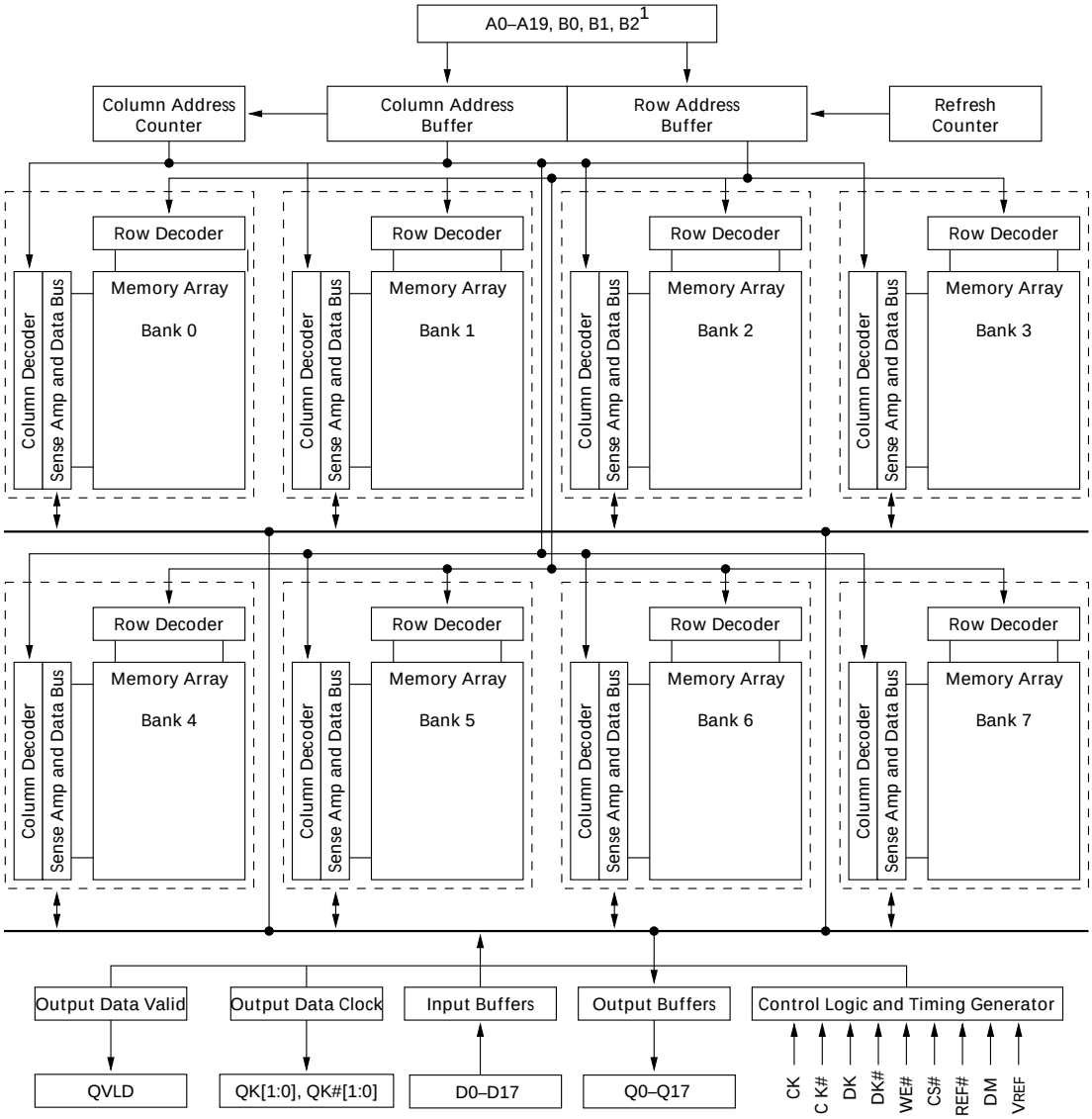
Read and write accesses to the RLDRAM are burst-oriented. The burst length is programmable from 2, 4, or 8 by setting the mode register.

The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

Bank scheduled refresh is supported with row addresses generated internally.

A standard FBGA 144-ball package is used to enable ultra-high-speed data transfer rates and a simple upgrade path from former products.

Figure 2
Functional Block Diagram
16 Meg x 18



NOTE: 1. When the BL8 setting is used, A18 and A19 are "Don't Care."
When the BL4 setting is used, A19 is a "Don't Care."

Figure 3
16 Meg x 18 BALL Assignment (Top View)
144-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	D4	Q4	VSSQ					VSSQ	Q0	D0	VDD
C	VTT	D5	Q5	VDDQ					VDDQ	Q1	D1	VTT
D	(A22)[1]	D6	Q6	VSSQ					VSSQ	QK0#	QK0	VSS
E	(A21)[2]	D7	Q7	VDDQ					VDDQ	Q2	D2	(A20)[2]
F	A5	D8	Q8	VSSQ					VSSQ	Q3	D3	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSS	A4	A3
J	NF[3]	NF[3]	VDD	VDD					VDD	VDD	B0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	D14	Q14	VSSQ					VSSQ	Q9	D9	A19
P	A15	D15	Q15	VDDQ					VDDQ	Q10	D10	DM
R	VSS	QK1	QK1#	VSSQ					VSSQ	Q11	D11	VSS
T	VTT	D16	Q16	VDDQ					VDDQ	Q12	D12	VTT
U	VDD	D17	Q17	VSSQ					VSSQ	Q13	D13	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

NOTE: 1. Reserved for future use. This may optionally be connected to GND.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.
3. No Function. This signal is internally connected and has parasitic characteristics of a clock input signal.

Figure 4
32 Meg x 9 Ball Assignment (Top View)
144-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	VSS	VEXT	VSS					VSS	VEXT	TMS	TCK
B	VDD	DNU[4]	DNU[4]	VSSQ					VSSQ	Q0	D0	VDD
C	VTT	DNU[4]	DNU[4]	VDDQ					VDDQ	Q1	D1	VTT
D	(A22)[1]	DNU[4]	DNU[4]	VSSQ					VSSQ	QK0#	QK0	VSS
E	(A21)[3]	DNU[4]	DNU[4]	VDDQ					VDDQ	Q2	D2	A20
F	A5	DNU[4]	DNU[4]	VSSQ					VSSQ	Q3	D3	QVLD
G	A8	A6	A7	VDD					VDD	A2	A1	A0
H	B2	A9	VSS	VSS					VSS	VSS	A4	A3
J	NF[3]	NF[3]	VDD	VDD					VDD	VDD	B0	CK
K	DK	DK#	VDD	VDD					VDD	VDD	B1	CK#
L	REF#	CS#	VSS	VSS					VSS	VSS	A14	A13
M	WE#	A16	A17	VDD					VDD	A12	A11	A10
N	A18	DNU[4]	DNU[4]	VSSQ					VSSQ	Q4	D4	A19
P	A15	DNU[4]	DNU[4]	VDDQ					VDDQ	Q5	D5	DM
R	VSS	DNU[4]	DNU[4]	VSSQ					VSSQ	Q6	D6	VSS
T	VTT	DNU[4]	DNU[4]	VDDQ					VDDQ	Q7	D7	VTT
U	VDD	DNU[4]	DNU[4]	VSSQ					VSSQ	Q8	D8	VDD
V	VREF	ZQ	VEXT	VSS					VSS	VEXT	TDO	TDI

NOTE: 1. Reserved for future use. This signal is not connected.
2. Reserved for future use. This signal is internally connected and has parasitic characteristics of a clock input signal.
3. No Function. This signal is internally connected and has parasitic characteristics of a clock input signal.
4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND.

Table 2: Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
CK, CK#	Input	Input Clock: CK and CK# are differential clock inputs. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip Select: CS# enables the command decoder when low and disables it when high. When the command decoder is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	Command Inputs: Sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be excuted.
A[0:20]	Input	Address Inputs: A[0:20] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET the address inputs define the register settings. They are sampled at the rising edge of CK. In the x18 configuration, A[20] is reserved for address expansion. These expansion addresses can be treated as address inputs, but they do not effect the operation of the device.
A21	-	Reserved for future use. This signal is internally connected and can be treated as an address input.
A22	-	Reserved for future use. This signal is not connected and may be connected to ground.
BA[0:2]	Input	Bank Address Inputs: Select to which internal bank a command is being applied.
D0–D17	Input	Data Input: The D signals form the 18-bit input data bus. During WRITE commands, data is sampled at both edges of DK.
Q0–Q17	Output	Data Output: The Q signals form the 18-bit output data bus. During READ commands, data is referenced to both edges of QK.
QKx, QKx#	Output	Output Data Clocks: QKx and QKx# are the differential output data clocks. During READs, they are transmitted by the RLDRAM and edge-aligned with data. QKx# is ideally 180 degrees out of phase with QKx. QK0 and QK0# are aligned with Q0–Q8, QK1 and QK1# are aligned with Q9–Q17. Consult the RLDRAM II design guide for more details.
DK, DK#	Input	Input Data Clock: DK and DK# are the differential input data clocks. All input data is referenced to both edges of DK. DK# is ideally 180 degrees out of phase with DK. D0–D17 are referenced to DK and DK#.
DM	Input	Input Data Mask: The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH, along with the WRITE input data. DM is sampled on both edges of DK.
QVLD	Output	Data Valid: The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.
TMS TDI	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 1.8V I/O levels. These pins may be left Not Connected if the JTAG function is not used in the circuit
TCK	Input	IEEE 1149.1 Clock Input: JEDEC-standard 1.8V I/O levels. This pin must be tied to VSS if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 1.8V I/O level.
ZQ	Input/ Output	External Impedance [25Ω–60Ω]: This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 x RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to VDD invokes the maximum impedance mode. Refer to the Mode Register Bit Map to activate this function.
VREF	Input	Input Reference Voltage: Nominally VDDQ/2. Provides a reference voltage for the input buffers.
VEXT	Supply	Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Condidtions for range.

Table 2: Ball Descriptions (continued)

SYMBOL	TYPE	DESCRIPTION
VDD	Supply	Power Supply: 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. Nominally, 1.5V or 1.8V. See DC Electrical Characteristics and Operating Conditions for range.
VSS	Supply	Power Supply: GND.
VSSQ	Supply	Power Supply: Isolated Output Buffer Supply. GND
VTT	Supply	Power Supply: Isolated Termination Supply. Nominally, VDDQ/2. See DC Electrical Characteristics and Operating Conditions for range.
NF	–	No Function: These pins may be connected to ground.
DNU	–	Do Not Use: These pins may be connected to ground.

COMMANDS

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

Table 3: Address Widths at Different Burst Lengths

	CONFIGURATION	
BURST LENGTH	x18	x9
BL = 2	19:0	20:0
BL = 4	18:0	19:0
BL = 8	17:0	18:0

Table 4: Command Table[1]

OPERATION	CODE	CS#	WE#	REF#	A[20:0]	B[2:0]	NOTES
Device Deselect/No Operation	DESEL/NOP	H	X	X	X	X	
Mode Register Set	MRS	L	L	L	OPCODE	X	2
Read	READ	L	H	H	A	BA	3
Write	WRITE	L	L	H	A	BA	3
Auto Refresh	AREF	L	H	L	X	BA	

NOTE: 1. X represents a "Don't Care"; H represents a logic HIGH; L represents a logic LOW; A represents a Valid Address; and BA represents a Valid Bank Address.
2. Only A(17:0) are used for the MRS command.
3. See above table, Address Widths at Different Burst Lengths.

Table 5: Description of Commands

COMMAND	DESCRIPTION
DESEL/NOP[1]	The NOP command is used to perform a no operation to the RLDRAM, which essentially deselects the chip. Use NOP commands to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.
MRS	The mode register is set via the address inputs A(17:0). See the Mode Register Bit Map for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.
READ	The READ command is used to initiate a burst read access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(20:0) selects the data location within the bank.
WRITE	The WRITE command is used to initiate a burst write access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(20:0) selects the data location within the bank. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written).
AREF	The AREF is used during normal operation of the RLDRAM to refresh the memory content of a bank. The command is non persistent, so it must be issued each time a refresh is required. The value on the BA(2:0) inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a "Don't Care" during the AREF command. The RLDRAM requires 64K cycles at an average periodic interval of 0.49µs[2] (MAX). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLDRAM at periodic intervals of 3.9µs[3].

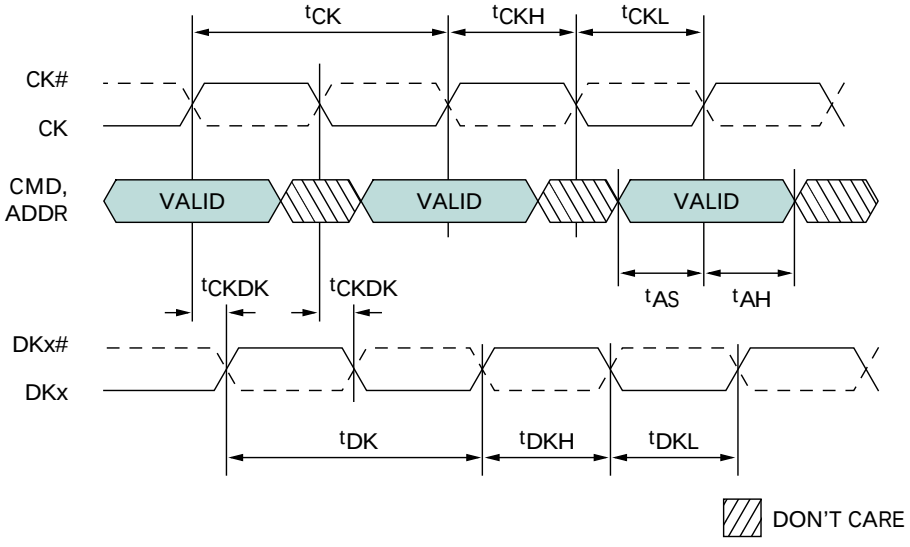
NOTE: 1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
2. Actual refresh is 32ms/8K/8 = 0.488µs.
3. Actual refresh is 32ms/8k = 3.90µs.

Table 6: AC Electrical Characteristics[1]

DESCRIPTION	SYMBOL	-2.5		-3.3		-5		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock cycle time	tCK, tDK	2.5	5.7	3.3	5.7	5.0	5.7	ns	
System frequency	fCK, fDK	175	400	175	300	175	200	MHz	
Clock phase jitter	tCKvar		0.30		0.30		0.30	ns	2
Clock HIGH time	tCKH, tDKH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock LOW time	tCKL, tDKL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock to input data clock	tCKDK	-0.3	0.3	-0.3	0.3	-0.3	0.3	ns	
Mode register set cycle time to any command	tMRSC	6		6		6		tCK	
Setup Times									
Address/command and input setup time	tAS/tCS	0.4		0.5		0.8		ns	
Data-in and data mask to DK setup time	tDS	0.25		0.3		0.4		ns	
Hold Times									
Address/command and input hold time	tAH/tCH	0.4		0.5		0.8		ns	
Data-in and data mask to DK hold time	tDH	0.25		0.3		0.4		ns	
Data and Data Strobe									
Output data clock HIGH time	tQKH	0.9	1.1	0.9	1.1	0.9	1.1	tCKH	
Output data clock LOW time	tQKL	0.9	1.1	0.9	1.1	0.9	1.1	tCKL	
QK edge to clock edge skew	tCKQK	-0.25	0.25	-0.3	0.3	-0.5	0.5	ns	
QK edge to output data edge	tQKQ0, tQKQ1	-0.2	0.2	-0.25	0.25	-0.3	0.3	ns	3
QK edge to data out High-Z	tQKHZ		0.2		0.25		0.3	ns	
QK edge to any output data edge	tQKQ	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns	4
QK edge to QVLD	tQKVLD	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns	

NOTE: 1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with VREF of the command, address, and data signals.
2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
3. tQKQ0 is referenced to Q0–Q8 in x18.
tQKQ1 is referenced to Q9–Q17 in x18.
4. tQKQ takes into account the skew between any QKx and any Q.

Figure 6
Clock/Input Data Clock Command/Address Timings



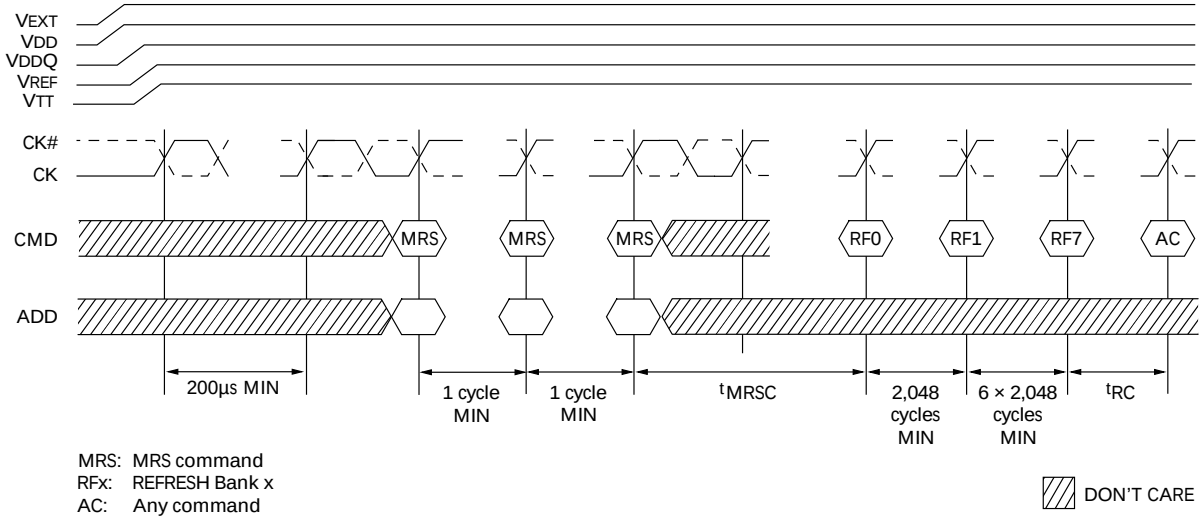
INITIALIZATION

The RLDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

THE FOLLOWING SEQUENCE IS USED FOR POWER-UP:

1. Apply power (VEXT, VDD, VDDQ, VREF, VTT) and start clock as soon as the supply voltages are stable. Apply VDD and VEXT before or at the same time as VDDQ. Apply VDDQ before or at the same time as VREF and VTT. Although there is no timing relation between VEXT and VDD, the chip starts the power-up sequence only after both voltages are at their nominal levels. The pad supply must not be applied before the core supplies. Maintain all remaining pins in NOP conditions.
2. Maintain stable conditions for 200µs (MIN).
3. Issue three Mode Register Set commands: two dummies plus one valid MRS.
4. ^{t}MRSC after the valid MRS, issue eight AUTO REFRESH commands, one on each bank and separated by 2,048 cycles. Initial bank refresh order does not matter.
5. After ^{t}RC, the chip is ready for normal operation.

Figure 6
Power-Up Sequence



PROGRAMMABLE IMPEDANCE OUTPUT BUFFER

The RLDRAM II is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSS. The value of the resistor must be five times the desired impedance. For example, a 300Ω resistor is required for an output impedance of 60Ω. To ensure that output impedance is one-fifth the value of RQ (within 15 percent), the range of RQ is 125Ω to 300Ω.

Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of RQ. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

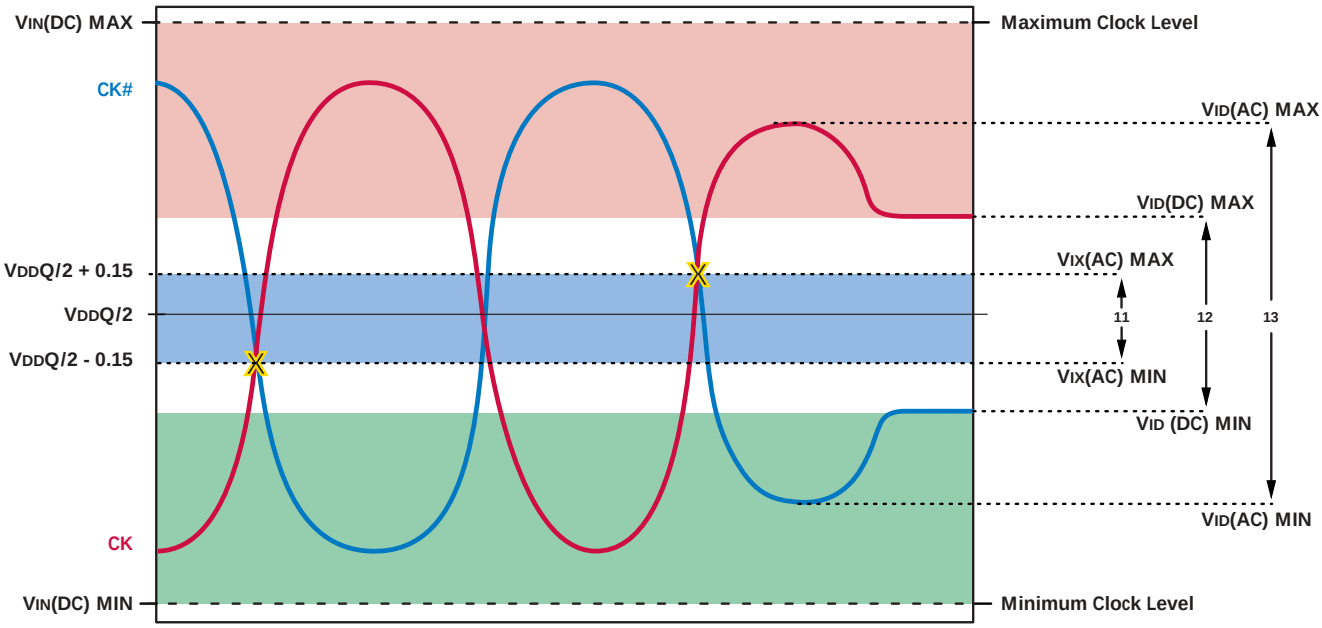
CLOCK CONSIDERATIONS

The RLDRAM II utilizes internal delay-locked loops for maximum output, data valid windows. It can be placed into a stopped-clock state to minimize power with a modest restart time of 1,024 cycles. Circuitry automatically resets the DLL when the absence of an input clock is detected.

Table 7: Clock Input Operating Conditions[1–8]

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Clock Input Voltage Level; CK and CK#	VIN(DC)	-0.3	VDDQ + 0.3	V	
Clock Input Differential Voltage; CK and CK#	VID(DC)	0.2	VDDQ + 0.6	V	9
Clock Input Differential Voltage; CK and CK#	VID(AC)	0.4	VDDQ + 0.6	V	9
Clock Input Crossing Point Voltage; CK and CK#	VIX(AC)	VDDQ/2 - 0.15	VDDQ/2 + 0.15	V	10

Figure 7
Clock Input

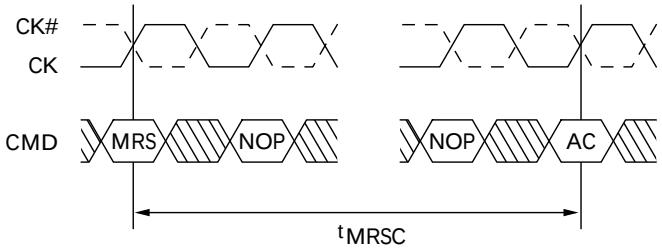


NOTE:
1. DKx and DKx# have the same requirements as CK and CK#.
2. All voltages referenced to VSS.
3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
4. Outputs (except for IDD measurements) measured with equivalent load.
5. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between VIL(AC) and VIH(AC).
6. The AC and DC input level specifications are as defined in the HSTL Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is VREF.
8. CK and CK# input slew rate must be ≥ 2 V/ns (≥4 V/ns if measured differentially).
9. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
10. The value of VIX is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
11. CK and CK# must cross within this region.
12. CK and CK# must meet at least VID(DC)MIN when static and centered around VDDQ/2.
13. Minimum peak-to-peak swing.

MODE REGISTER SET COMMAND (MRS)

The mode register stores the data for controlling the operating modes of the memory. It programs the RLDRAM configuration, burst length, test mode, and I/O options. During a MODE REGISTER SET command, the address inputs A(17:0) are sampled and stored in the mode register. ^{t}MRSC must be met before any command can be issued to the RLDRAM. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete. See the RLDRAM II design guide for more details.

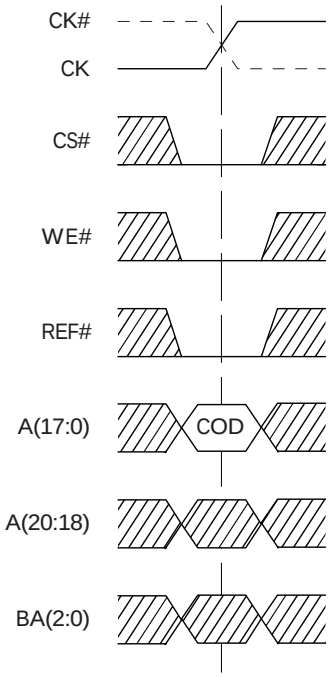
Figure 10
Mode Register Set Timing



Note: MRS: MRS command; AC: Any command

DON'T CARE

Figure 9
Mode Register Set



Note: COD: code to be loaded into the register

DON'T CARE

Figure 11
Mode Register Bit Map

A(17:10)	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Reserved[1]	On-Die Termination	Impedance Matching	DLL Reset	Unused	Address Mux	Burst Length		Configuration		

On-Die Termination

A9	Termination
0	Disabled (default)
1	Enabled

DLL Reset

A7	DLL Reset
0	DLL reset (default)
1	DLL enabled

Burst Length

A4	A3	BL
0	0	2 (default)
0	1	4
1	0	8[2]
1	1	not valid

Configuration

A2	A1	A0	RLDRAM Configuration
0	0	0	1[2] (default)
0	0	1	1[2]
0	1	0	2
0	1	1	3
1	0	0	reserved
1	0	1	reserved
1	1	0	reserved
1	1	1	reserved

Impedance Matching

A8	Resistor
0	internal 50Ω[3] (default)
1	external

Address Mux

A5	Address Mux
0	nonmultiplexed (default)
1	address multiplexed

NOTE: 1. Bits A(17:10) MUST be set to zero.
2. BL = 8 is not available for configuration 1.
3. ±15% temperature variation.

CONFIGURATION TABLE

Table 8 shows, for different operating frequencies, the different RLDRAM configurations that can be programmed into the mode register. The read and write latency (^{t}RL and ^{t}WL) values along with the row cycle times (^{t}RC) are shown in clock cycles as well as in nanoseconds.

The shaded areas correspond to configurations that are not allowed.

Table 8: RLDRAM Configuration Table

		CONFIGURATION			
FREQUENCY	SYMBOL	1[1]	2	3	UNIT
	^{t}RC	4	6	8	cycles
	^{t}RL	4	6	8	cycles
	^{t}WL	5	7	9	cycles
400 MHz	^{t}RC			20.0	ns
	^{t}RL			20.0	ns
	^{t}WL			22.5	ns
300 MHz	^{t}RC		20.0	26.7	ns
	^{t}RL		20.0	26.7	ns
	^{t}WL		23.3	30.0	ns
200 MHz	^{t}RC	20.0	30.0	40.0	ns
	^{t}RL	20.0	30.0	40.0	ns
	^{t}WL	25.0	35.0	45.0	ns

NOTE: 1. BL = 8 is not available for configuration 1.

WRITE BASIC INFORMATION

Write accesses are initiated with a WRITE command, as shown in the WRITE Command figure on the right. Row and bank addresses are provided together with the WRITE command.

During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). A write latency (WL) one cycle longer than the programmed read latency (RL + 1) is present, with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command. Figures 16 and 17 illustrate the timing requirements for a WRITE followed by a READ for bursts of two and four, respectively.

Setup and hold time for incoming DQ relative to the DK edges are specified as ^{t}DS and ^{t}DH. The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for data mask are also ^{t}DS and ^{t}DH.

Figure 12
WRITE Command

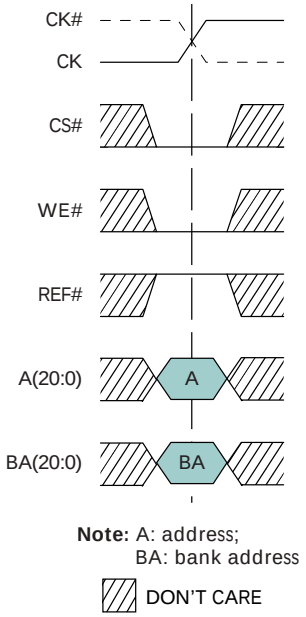


Figure 13
Basic WRITE Burst/DM Timing

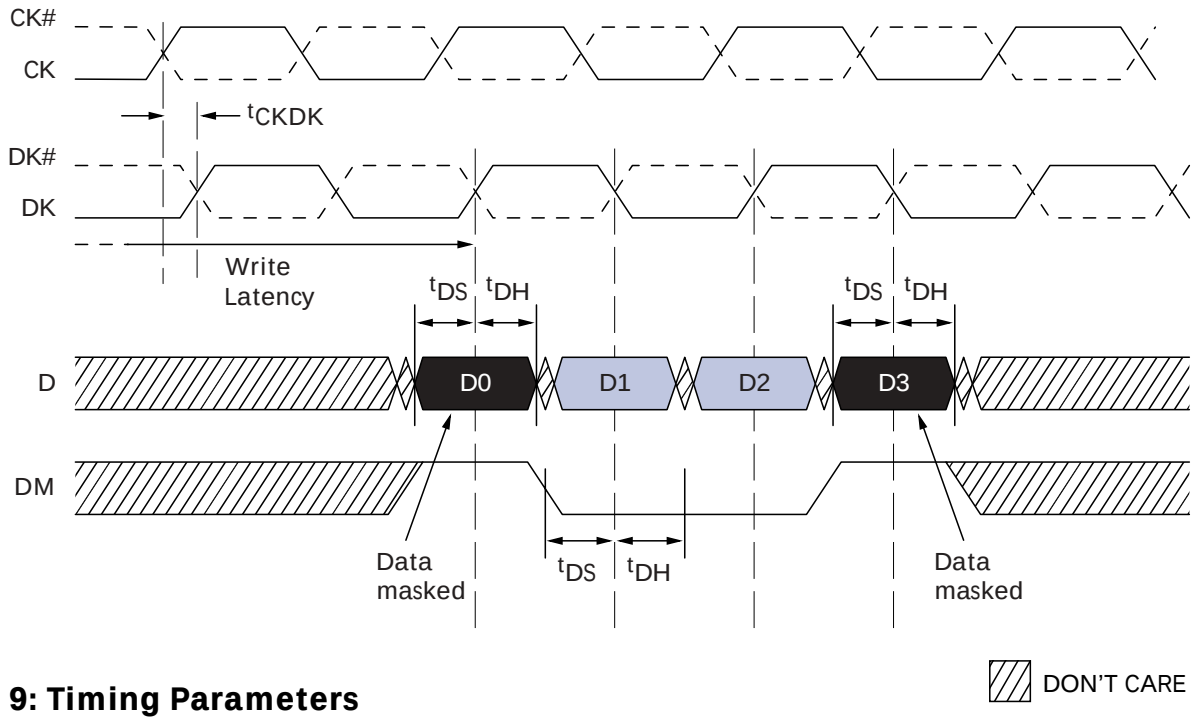
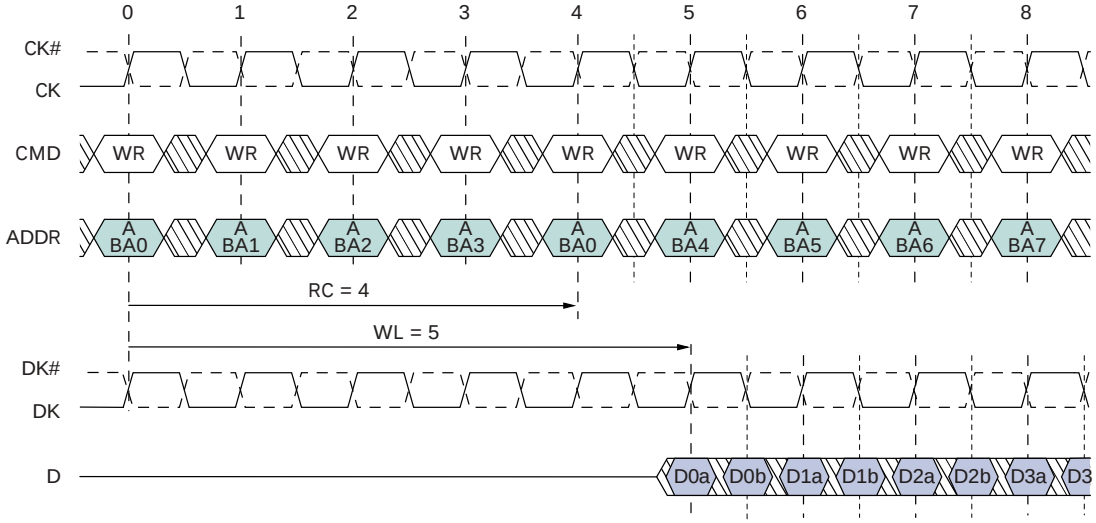


Table 9: Timing Parameters

SYMBOL	-2.5		-3.3		-5		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
^{t}DS	0.25		0.3		0.4		ns
^{t}DH	0.25		0.3		0.4		ns
^{t}CKDK	-0.3	0.3	-0.3	0.3	-0.3	0.3	ns

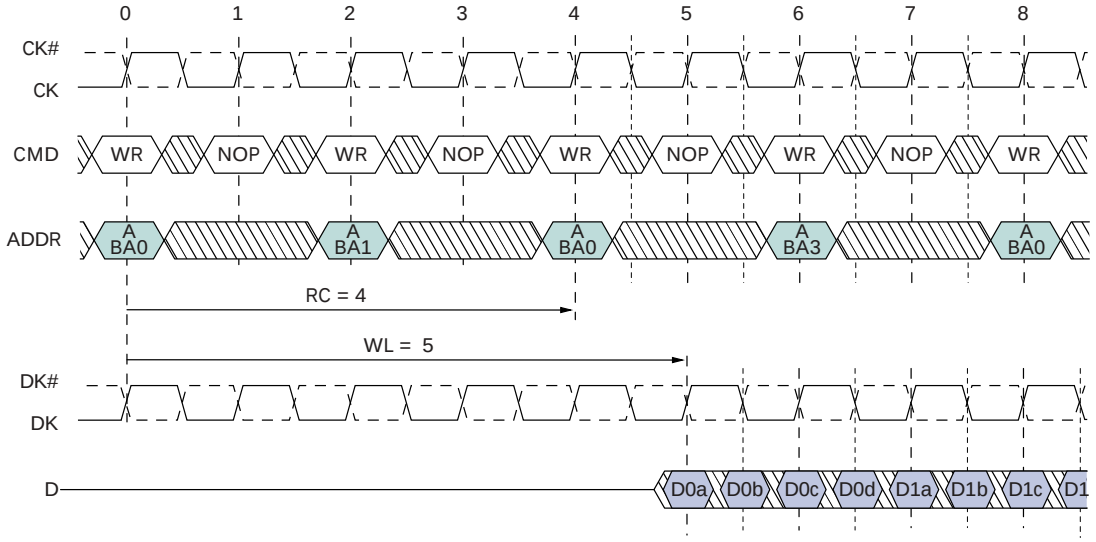
Figure 14
WRITE Burst Basic Sequence: BL = 2, RL = 4, WL = 5, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: Data *y* to bank *x*
RC: row cycle time
WL: write latency

DON'T CARE

Figure 15
WRITE Burst Basic Sequence: BL = 4, RL = 4, WL = 5, Configuration 1

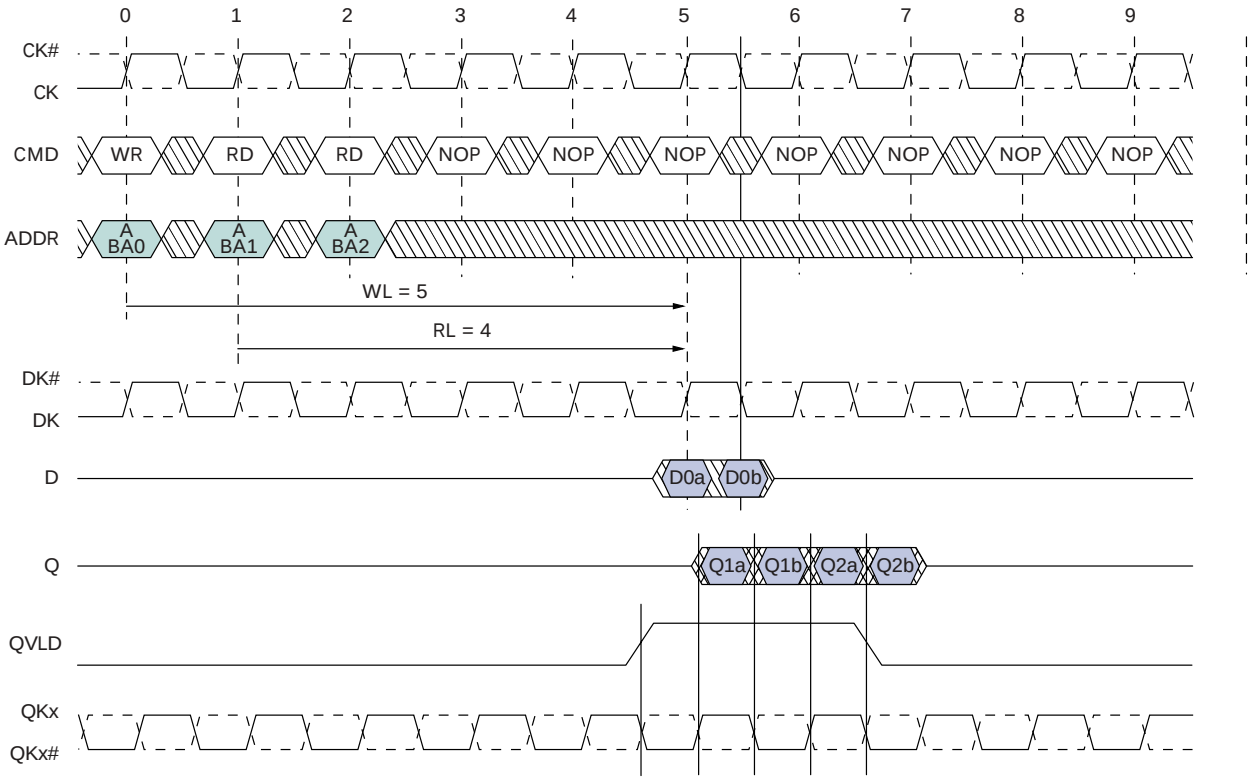


Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: Data *y* to bank *x*
RC: row cycle time
WL: write latency

DON'T CARE

NOTE: Any free bank may be used in any given CMD. The sequence shown is only one example of a back sequence.

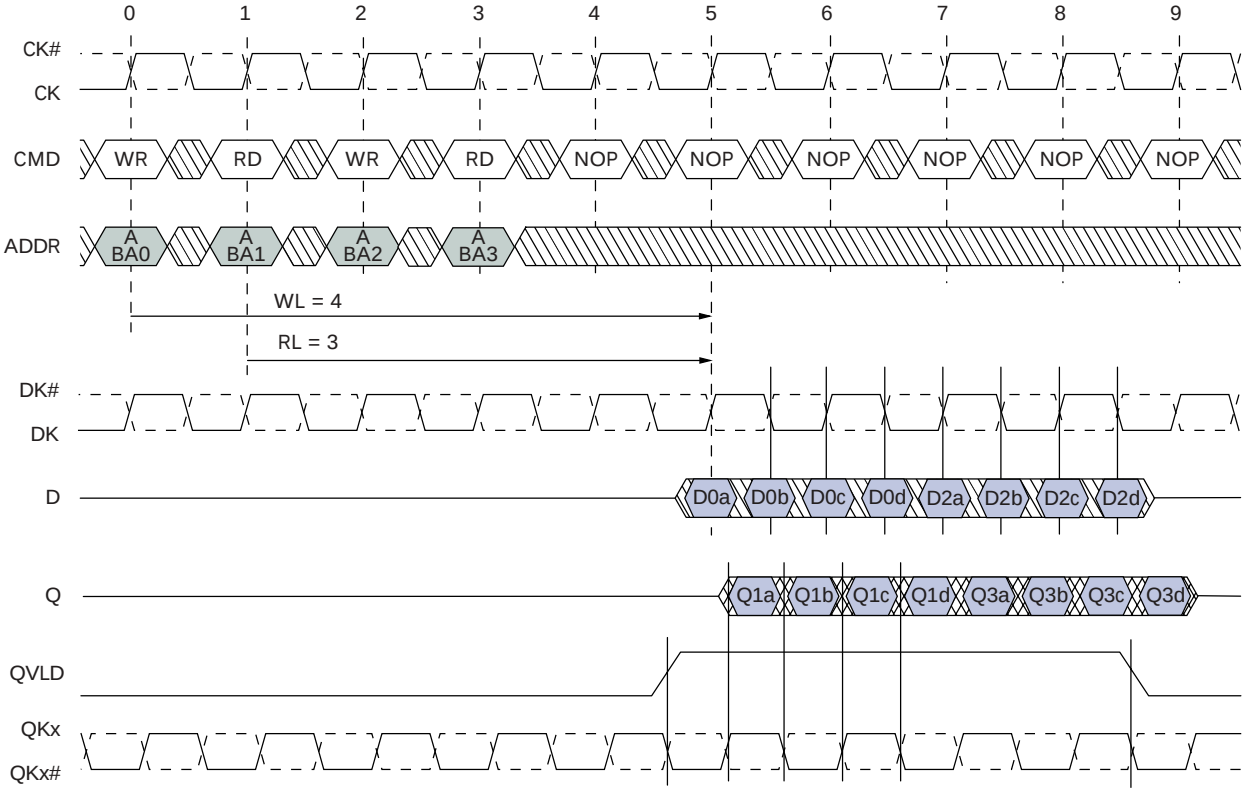
Figure 16
WRITE followed by READ: BL = 2, RL = 4, WL = 5, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: data *y* to bank *x*
WL: write latency
RD: READ command
Q*xy*: data *y* from bank *x*
RL: Read Latency

DON'T CARE UNDEFINED

Figure 17
WRITE followed by READ: BL = 4, RL = 4, WL = 5, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: data y to bank *x*
WL: write latency
RD: READ command
Q*xy*: data *y* from bank *x*
RL: read latency

DON'T CARE UNDEFINED

READ BASIC INFORMATION

Read accesses are initiated with a READ command, as shown in Figure 18. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the QK signal. After a programmable read latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

The skew between QK and the crossing point of CK is specified as ^{t}CKQK. ^{t}QKQ0 is the skew between QK0 and the last valid data edge considered over all the data generated at the Q signals. ^{t}QKQ1 is the skew between QK1 and the last valid data edge considered over all the data generated at the Q signals. ^{t}QKQx is derived at each QKx clock edge and is not cumulative over time. ^{t}QKQ is the maximum of ^{t}QKQ0 and ^{t}QKQ1.

After completion of a burst, assuming no other commands have been initiated, output data (Q) will go High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

The data valid window is derived from each QK transisition and is defined as: MIN(^{t}QKH, ^{t}QKL) - 2(^{t}QKQ(MAX)).

Any READ burst may be followed by a subsequent WRITE command. Figures 22 illustrates the timing requirements for a READ followed by a WRITE.

Figure 18
READ Command

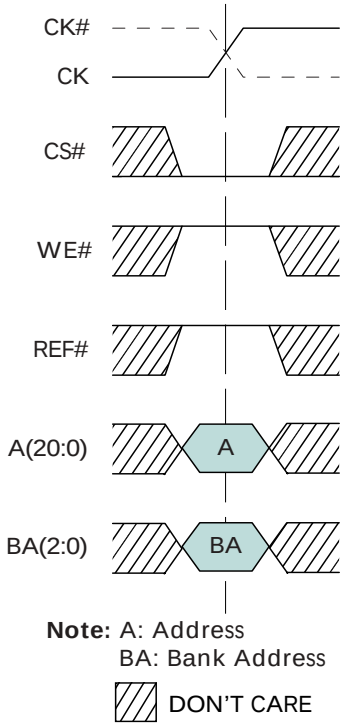


Figure 19
Basic READ Burst Timing

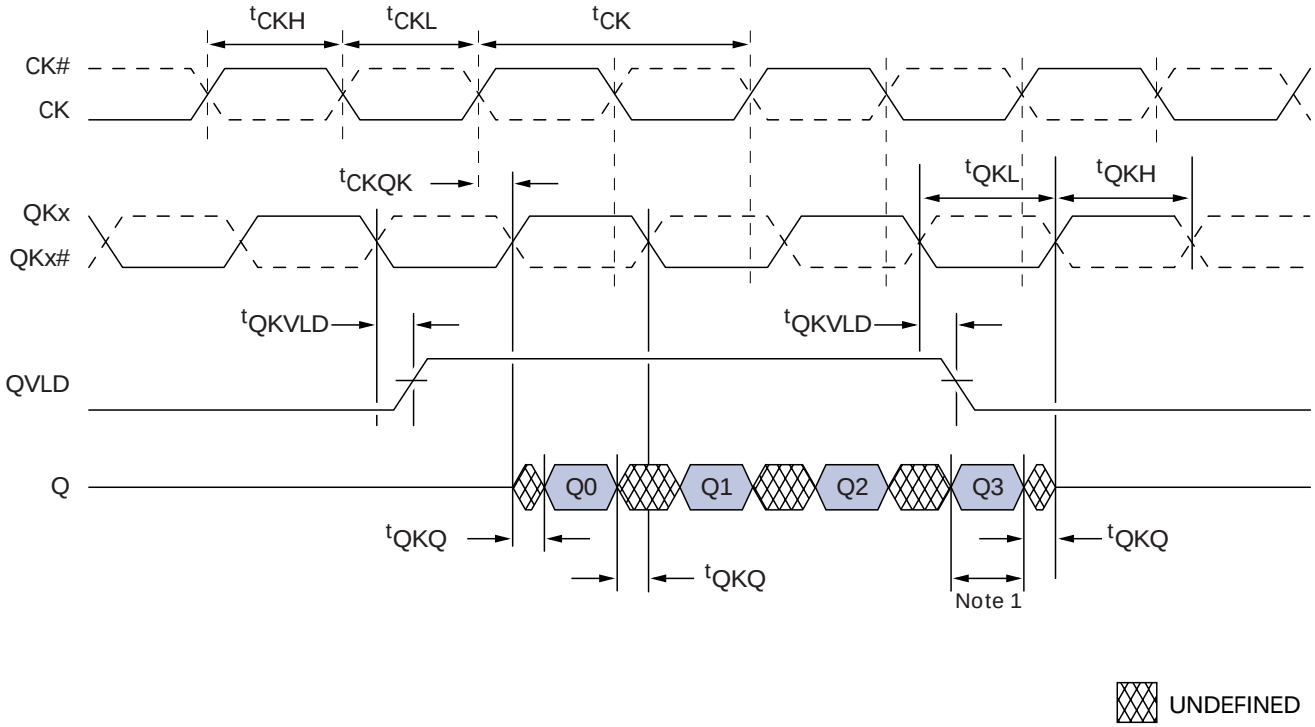


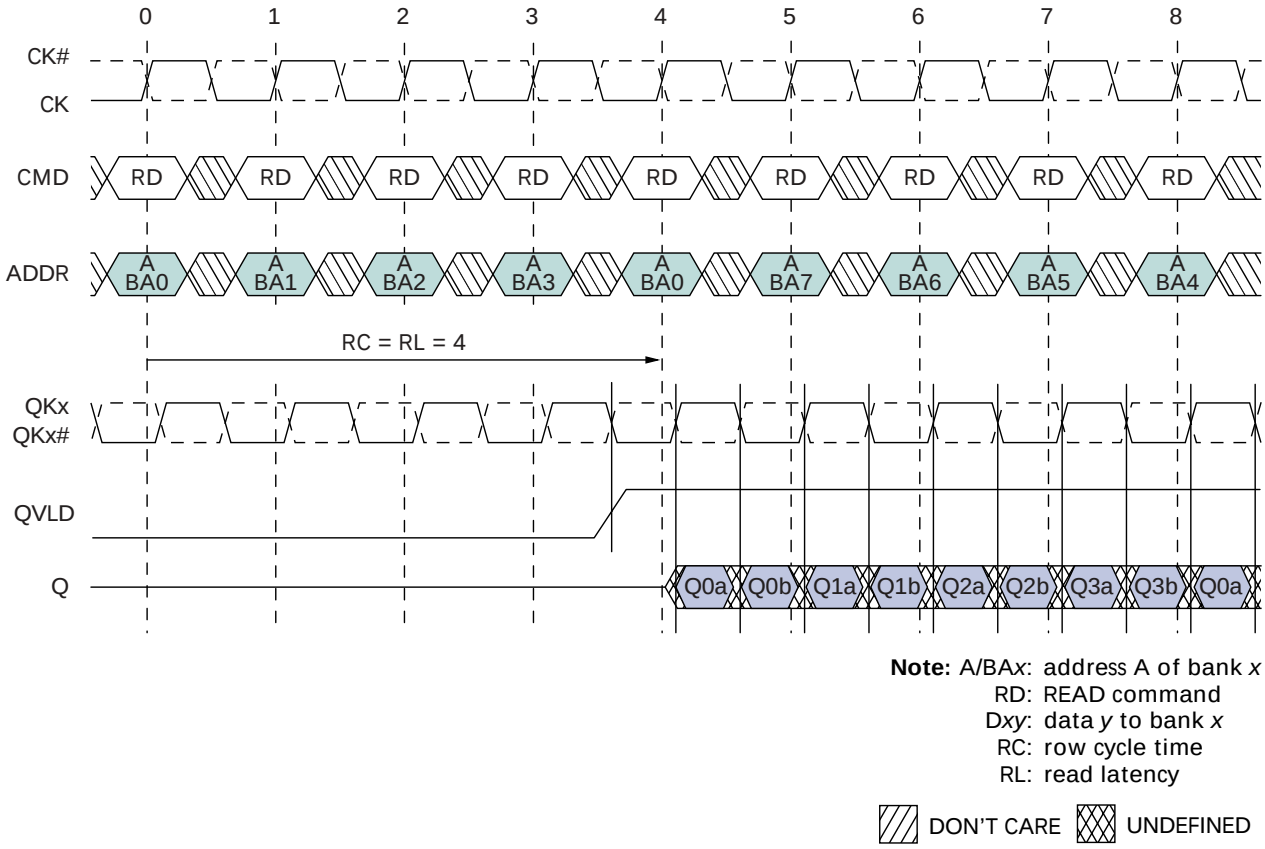
Table 10: Timing Parameters

SYMBOL	-2.5		-3.3		-5		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
tCK	2.5	5.7	3.3	5.7	5.0	5.7	ns
tCKH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tCKL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tCKQK	-0.25	0.25	-0.3	0.3	-0.5	0.5	ns

SYMBOL	-2.5		-3.3		-5		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
tQKQ	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns
tQKQ0, tQKQ1	-0.2	0.2	-0.25	0.25	-0.3	0.3	ns
tQKVLD	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns
tQKH	0.9	1.1	0.9	1.1	0.9	1.1	tCKH
tQKL	0.9	1.1	0.9	1.1	0.9	1.1	tCKL

NOTE: 1. Minimum data valid window can be expressed as MIN(tQKH, tQKL) - 2 x tQKQx(MAX).
2. tQKQ0 is referenced to DQ0–DQ8 in x18.
tQKQ1 is referenced to DQ9–DQ17 in x18.
3. tQKQ takes into account the skew between any QKx and any DQ.

Figure 20
READ Burst: BL = 2, RL = 4, Configuration 1

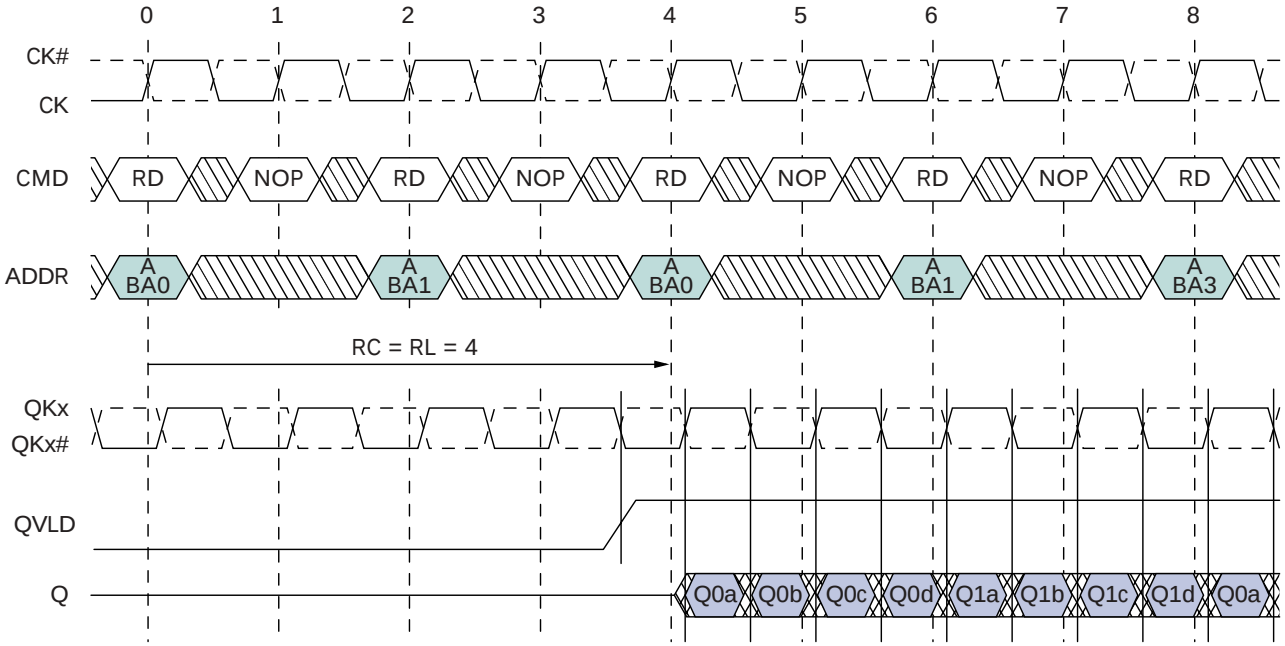


Note: A/BA*x*: address A of bank *x*
RD: READ command
D*xy*: data *y* to bank *x*
RC: row cycle time
RL: read latency

DON'T CARE UNDEFINED

NOTE: Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.

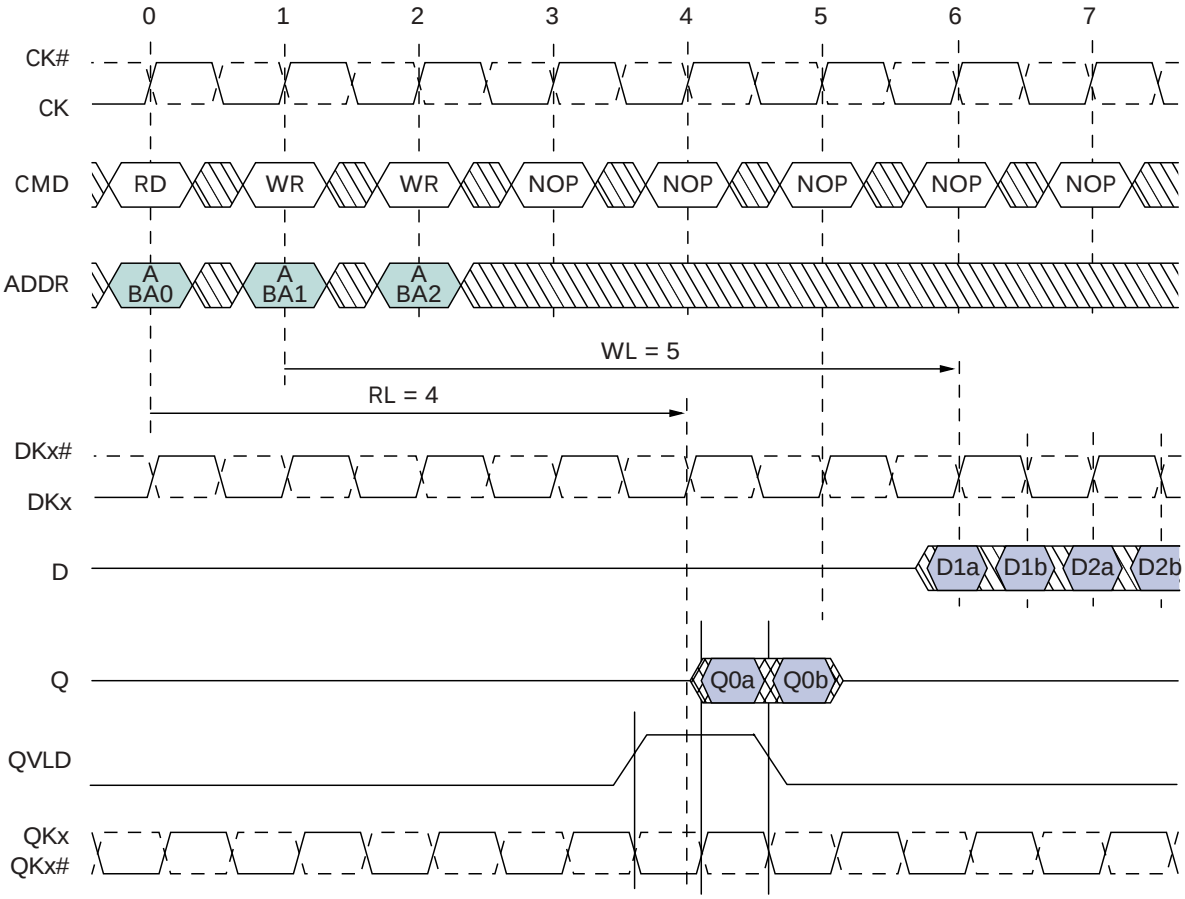
Figure 21
READ Burst: BL = 4, RL = 4, Configuration 1



Note: A/BA*x*: address A of bank *x*
RD: READ command
D*xy*: data *y* to bank *x*
RC: row cycle time
RL: read latency

DON'T CARE UNDEFINED

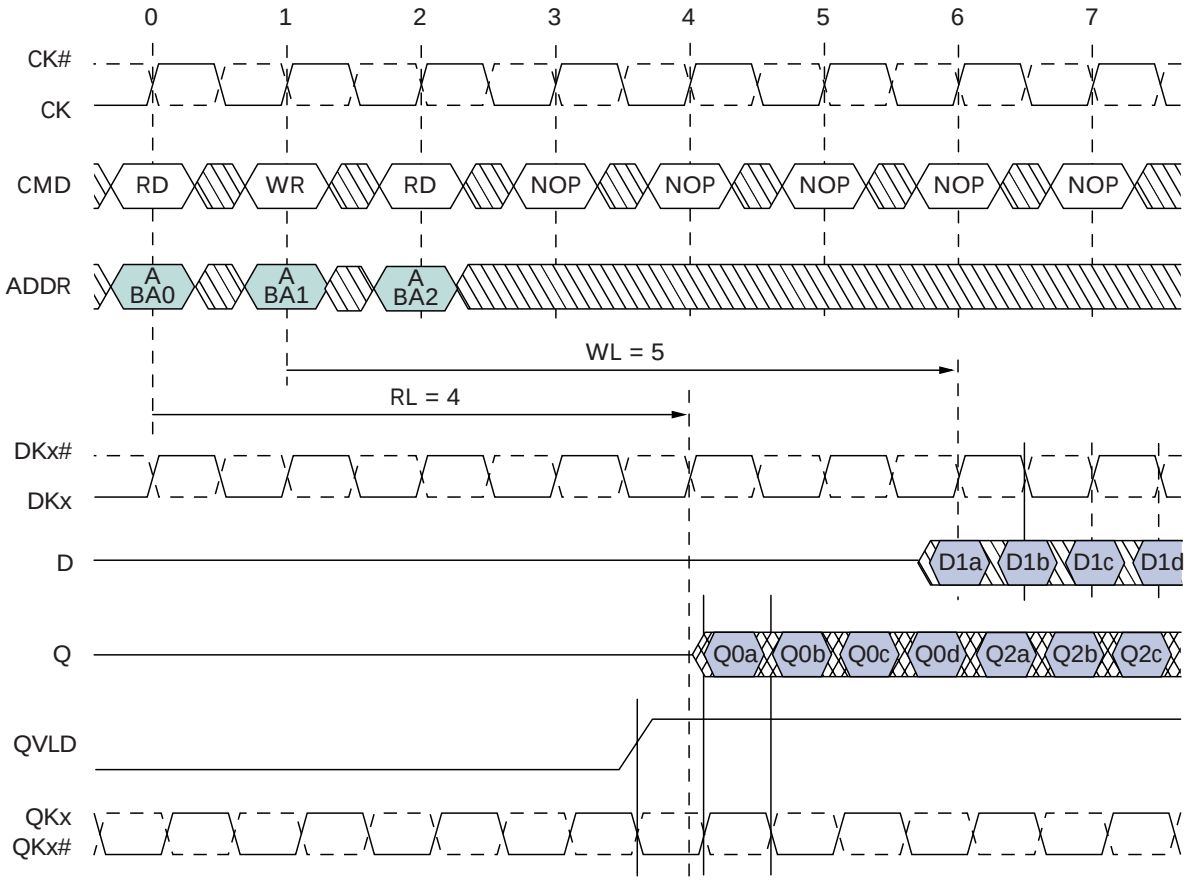
Figure 22
READ followed by WRITE: BL = 2, RL = 4, WL = 5, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: data *y* to bank *x*
WL: write latency
RD: READ command
Q*xy*: data *y* from bank *x*
RL: read latency

DON'T CARE UNDEFINED

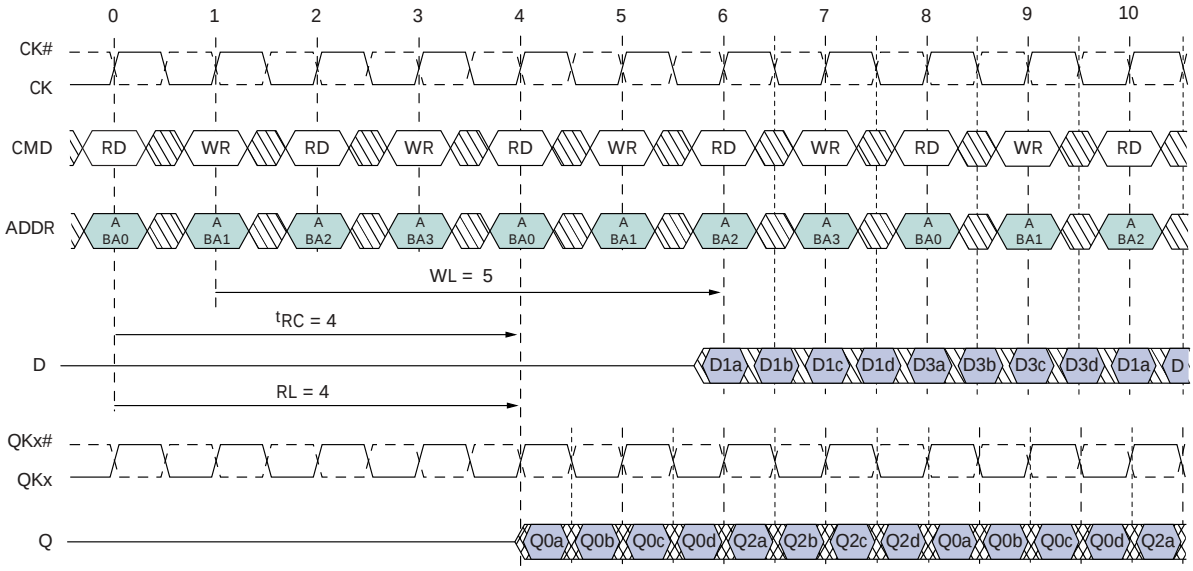
Figure 23
READ followed by WRITE: BL = 4, RL = 4, WL = 5, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
Dxy: data *y* to bank *x*
WL: write latency
RD: READ command
Q*xy*: data *y* from bank *x*
RL: read latency

DON'T CARE UNDEFINED

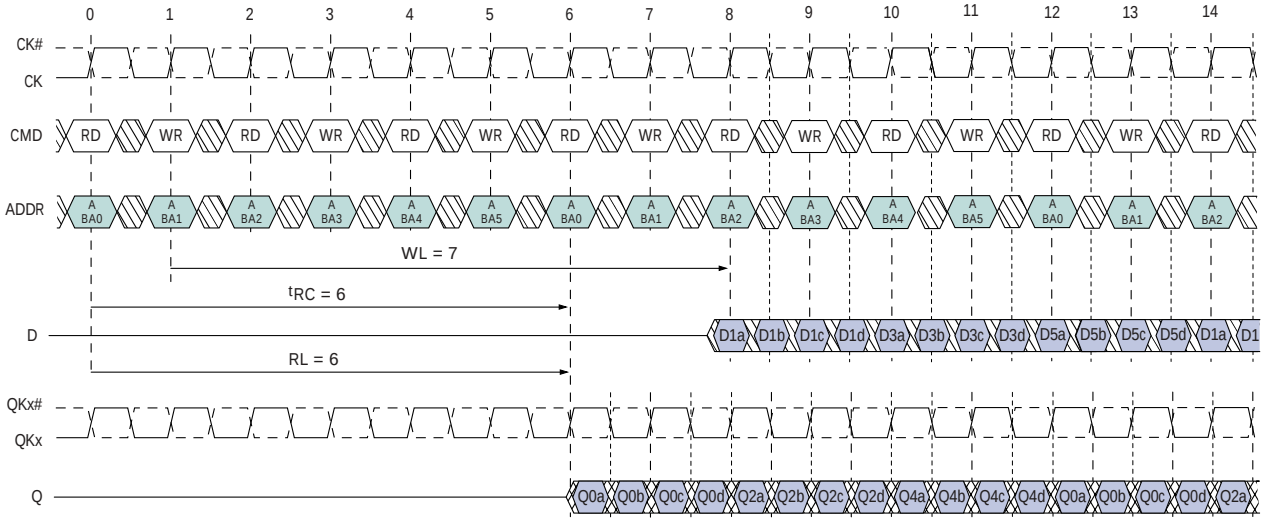
Figure 24
READ/WRITE Interleave: BL = 4, tRC = 4, RL = 4, WL = 5, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: Data *y* to bank *x*
WL: write latency
RD: READ command
Q*xy*: data part *y* from bank *x*
RL: read latency
tRC: row cycle time

DON'T CARE UNDEFINED

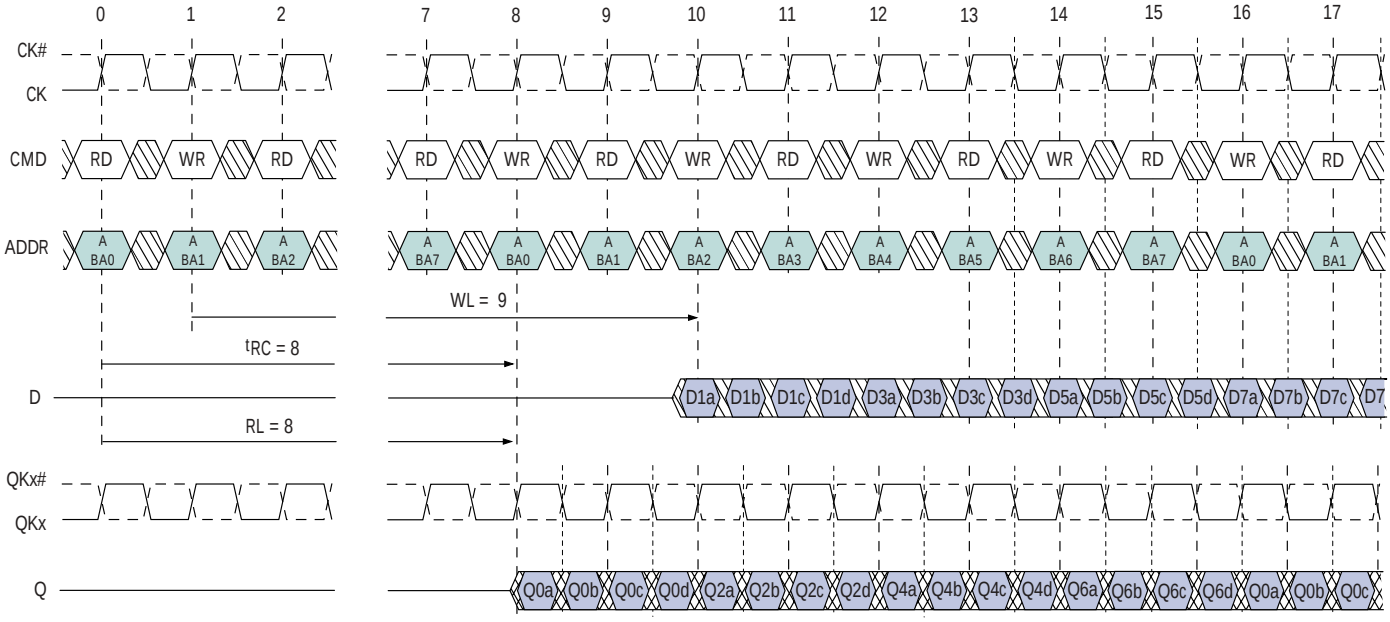
Figure 25
READ/WRITE Interleave: BL = 4, tRC = 6, RL = 6, WL = 7, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: data *y* to bank *x*
WL: write latency
RD: READ command
Q*xy*: data part *y* from bank *x*
RL: read latency
tRC: row cycle time

DON'T CARE UNDEFINED

Figure 26
READ/WRITE Interleave, BL = 4, tRC = 8, RL = 8, WL = 9, Configuration 1



Note: A/BA*x*: address A of bank *x*
WR: WRITE command
D*xy*: data *y* to bank *x*
WL: write latency
RD: READ command

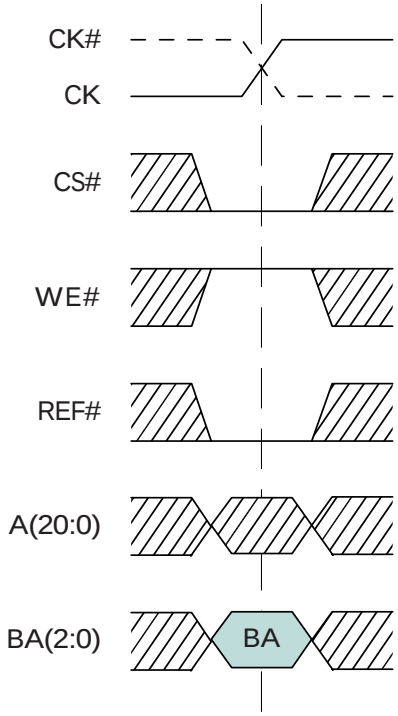
DON'T CARE UNDEFINED

AUTO REFRESH COMMAND (AREF)

AREF is used to perform a refresh cycle on one row in a specific bank. The row addresses are generated by an internal refresh counter for each bank; external address pins are "DON'T CARE." The delay between the AREF command and a subsequent command to the same bank must be at least ^{t}RC.

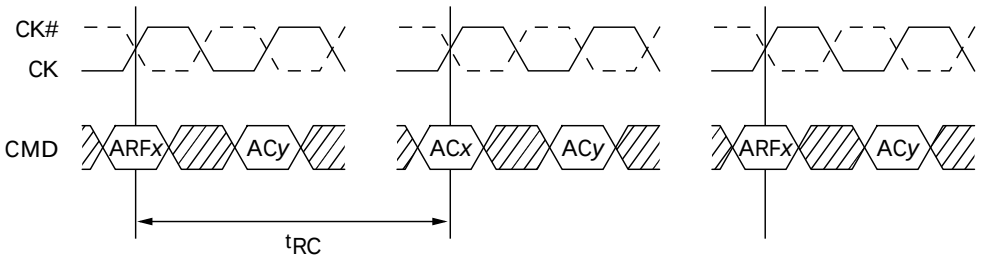
Within a period of 32ms (^{t}REF), the entire memory must be refreshed. Figure 28 illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

Figure 27
AUTO REFRESH Command



Note: BA: bank address

Figure 28
AUTO REFRESH Cycle



Note: ACx: Any command on bank *x*
ARFx: Auto Refresh bank *x*
ACy: Any command on different bank

DON'T CARE

NOTE: ^{t}RC is configuration-dependent. Refer to Table 8 RLDRAM Configuration on page 13.

ON DIE TERMINATION

On-die termination is enabled by setting A9 to one during a MODE REGISTER SET (MRS) command. With on-die termination on, all the DQs are terminated to VTT with a resistance RTT. The command, address, and clock signals are not terminated. Figure 29 shows the equivalent circuit of a DQ receiver with on-die termination. On-die terminations are dynamically switched off during READ commands and are designed to be off prior to the RLDRAM driving the bus. Similarly, on-die terminations are designed to switch on after the RLDRAM has issued the last piece of data.

Table 11: On-Die Termination DC Parameters

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Termination Voltage		VTT	0.95 x VREF	1.05 x VREF	V	1, 2
On-Die Termination		RTT	135	165	Ω	3

NOTE: 1. All voltages referenced to VSS (GND).
2. VTT is expected to be set equal to VREF and must track variations in the DC level of VREF.
3. The RTT value is measured at 70°C T_J.

Figure 29
On-Die Termination-Equivalent Circuit

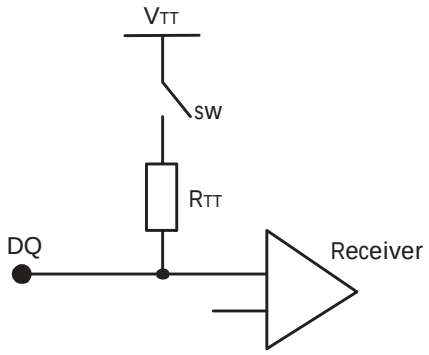
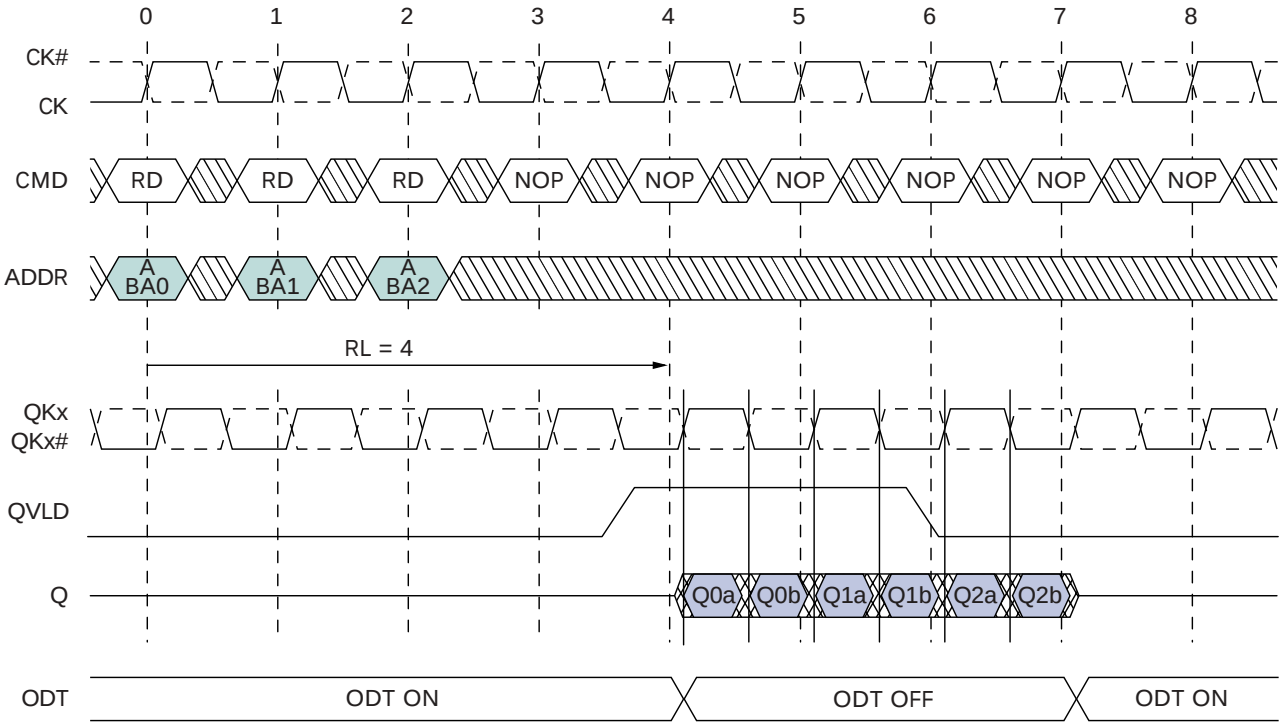


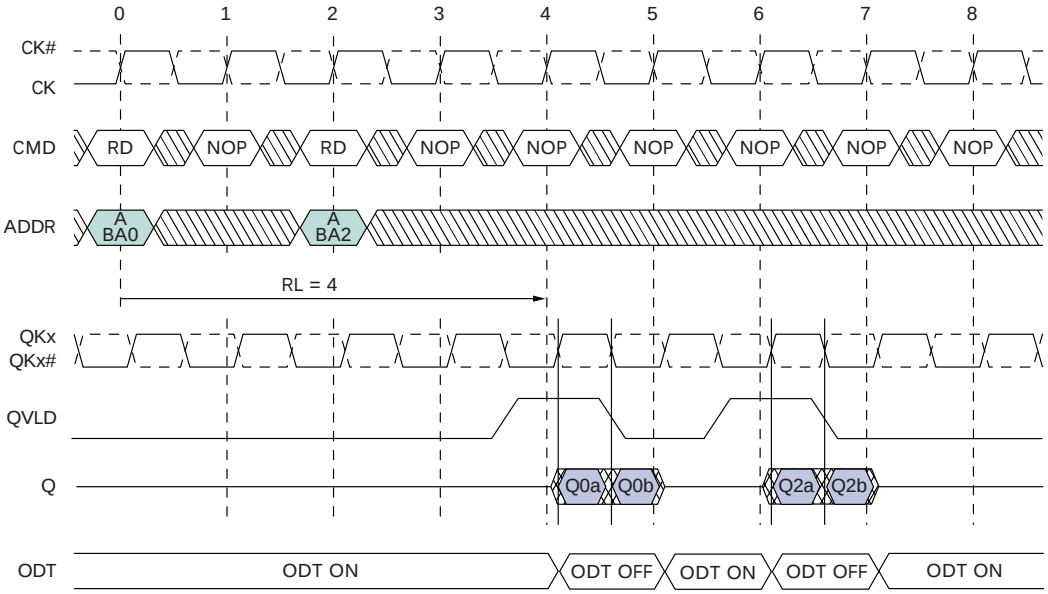
Figure 30
READ Burst with ODT: BL = 2, Configuration 1



Note: A/BA*x*: address A of bank *x*
RD: READ
D*xy*: data *y* to bank *x*
RL: read latency

DON'T CARE UNDEFINED

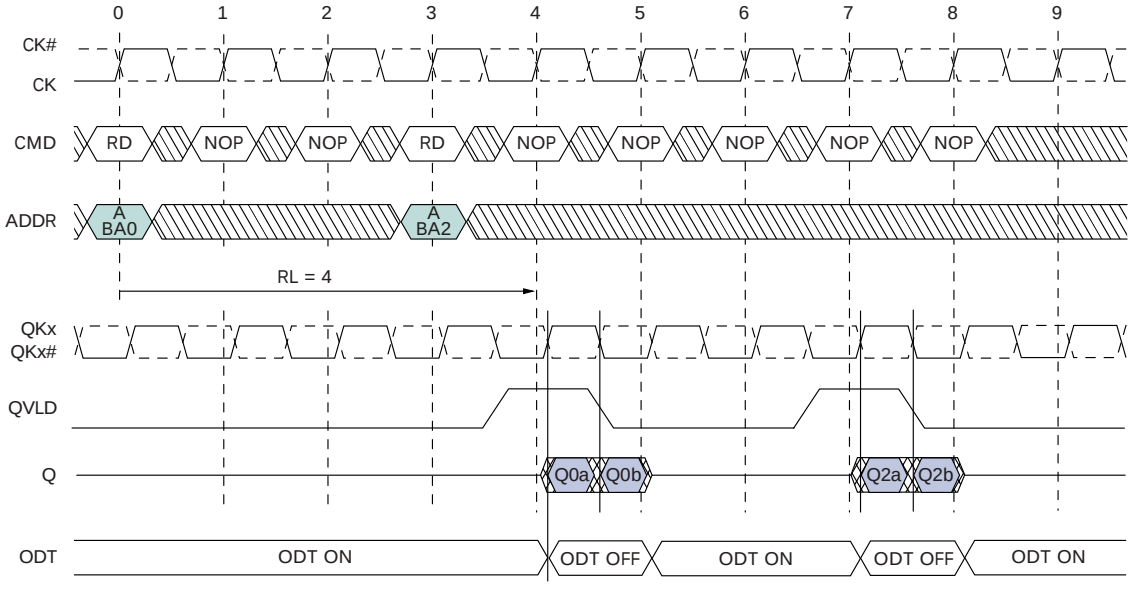
Figure 31
READ-NOP-READ with ODT: BL = 2, Configuration 1



Note: A/BA*x*: address A of bank *x*
RD: READ
D*xy*: data *y* to bank *x*
RL: read latency

DON'T CARE UNDEFINED

Figure 32
READ-NOP-NOP-READ with ODT: BL = 2, Configuration 1



Note: A/BA*x*: address A of bank *x*
RD: READ
D*xy*: data *y* to bank *x*
RL: read latency

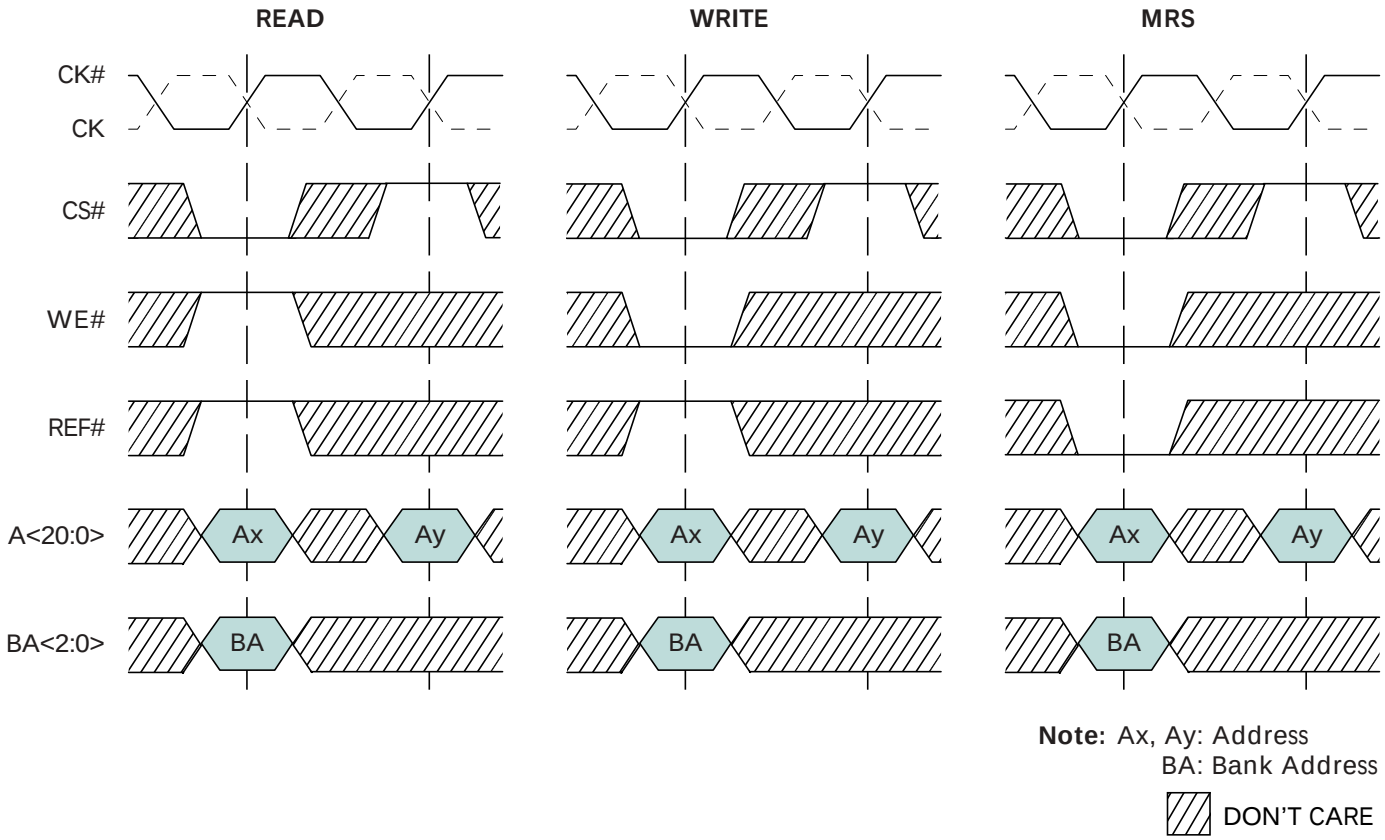
DON'T CARE UNDEFINED

OPERATION WITH MULTIPLEXED ADDRESSES

In multiplexed address mode, the address can be provided to the RLDRAM in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage that a maximim of 11 address pins are required to control the RLDRAM, reducing the number of pins on the controller side. The data bus efficiency in continuous burst mode is not affected for BL4 and BL8 since at least two clocks are required to read the data out of the memory. The bank addresses are delivered to the RLDRAM at the same time as the WRITE command and the first address part, A*x*.

This option is available by setting bit A5 to '1' in the mode register. Once this bit is set the READ, WRITE, and MRS commands follow the format described in Figure 33. See Figure 35 for the power-up sequence.

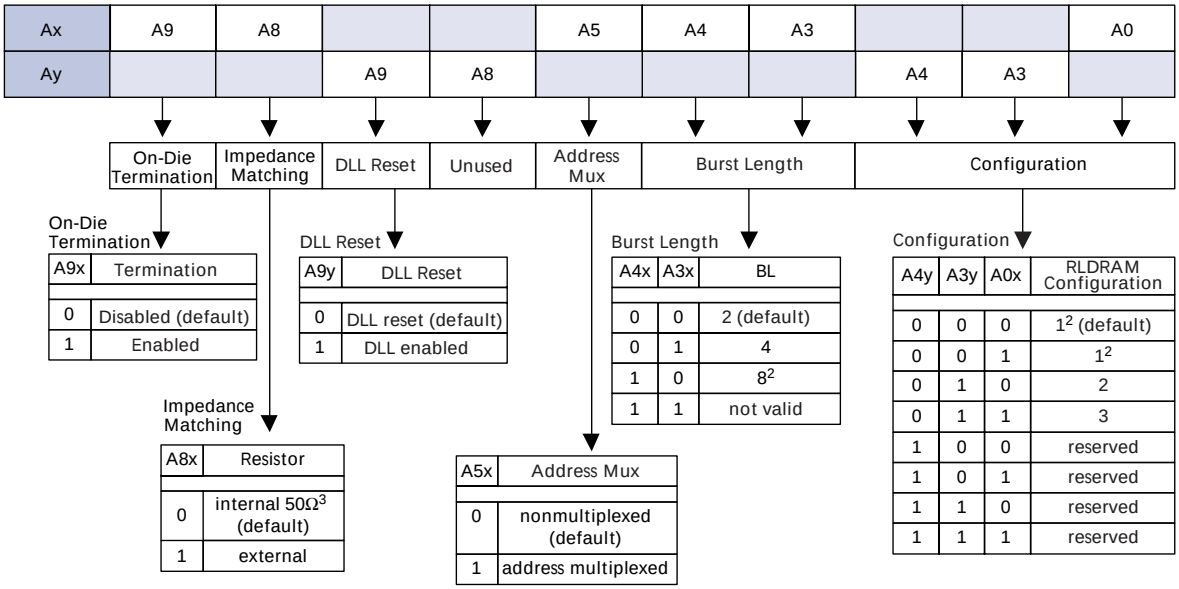
Figure 33
Command Description in Multiplexed Address Mode



NOTE: The minimum setup and hold times of the two address parts are defined ^{t}AS and ^{t}AH.

Figure 34
Mode Register Set Command in Multiplexed Address Mode

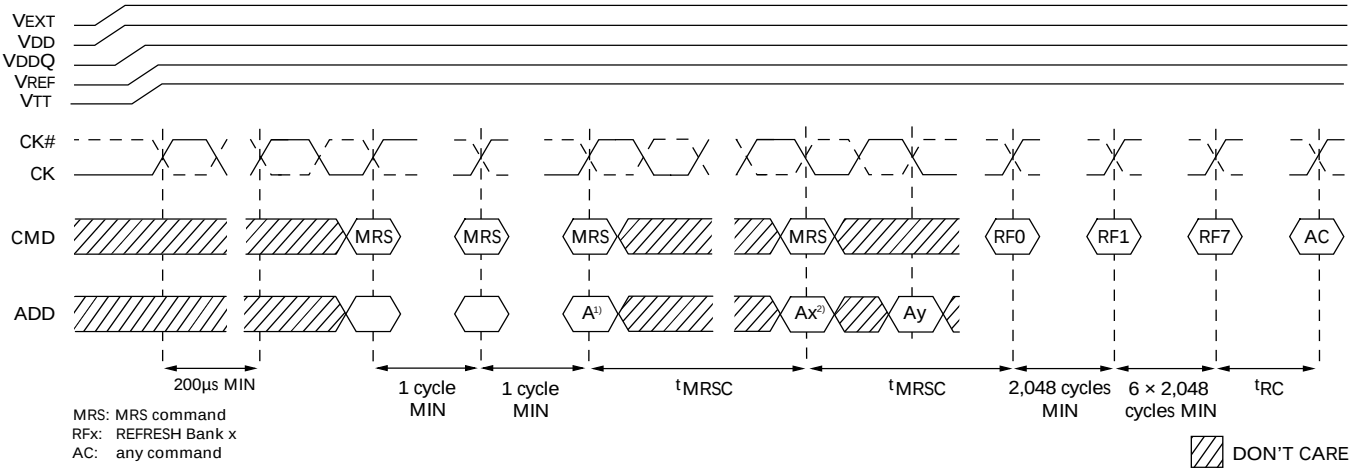
The addresses A0 to A6 must be set as follows in order to activate the Mode Register in the multiplexed address mode.



NOTE: 1. Bits A(17:11) MUST be set to zero.
2. BL = 8 is not available for configuration 1.
3. ±15% temperature variation.

Figure 35
Power-Up Sequence in Multiplexed Address Mode

The following sequence must be respected in order to power up the RLDRAM in the multiplexed address mode.



NOTE: 1. Address A5 must be set HIGH (muxed address mode setting when RLDRAM is in normal mode of operation).
2. Address A5 must be set HIGH (muxed address mode setting when RLDRAM is already in muxed address mode).

ADDRESS MAPPING

The address mapping is described in Table 12 as a function of data width and burst length.

Table 12: Address Mapping in Multiplexed Address Mode[1]

DATA WIDTH	BURST LENGTH	PIN	ADDRESSES										
			A0[2]	A3	A4	A5[3]	A8	A9	A10	A13	A14	A17	A18
x18	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x9	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

NOTE: 1. X means "Don't Care."
2. Reserved for A20 expansion in multiplexed mode.
3. Reserved for A21 expansion in multiplexed mode.

CONFIGURATION TABLE

In this mode, the read and write latencies are increased by one clock cycle. The RLDRAM cycle time remains the same, as described in Table 13.

Table 13: Configuration Table In Multiplexed Address Mode

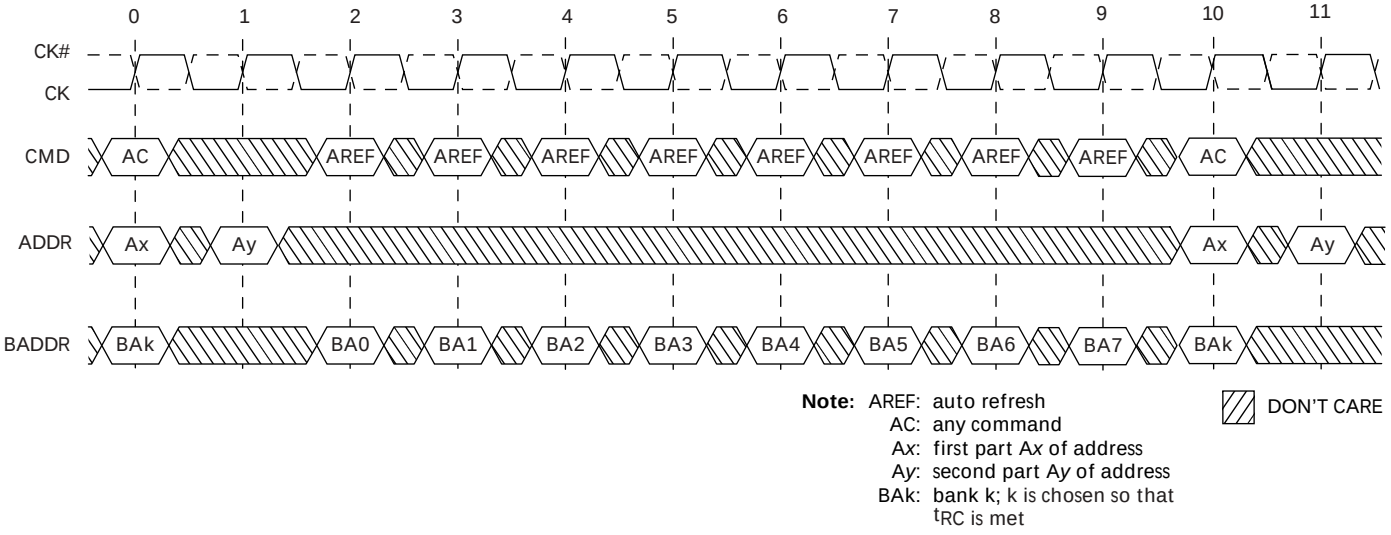
CONFIGURATION					
FREQUENCY	SYMBOL	1[4]	2	3	UNIT
	tRC	4	6	8	cycles
	tRL	5	7	9	cycles
	tWL	6	8	10	cycles
400 MHz	tRC			20.0	ns
	tRL			22.5	ns
	tWL			25.0	ns
300 MHz	tRC		20.0	26.7	ns
	tRL		23.3	30.0	ns
	tWL		26.7	33.3	ns
200 MHz	tRC	20.0	30.0	40.0	ns
	tRL	25.0	35.0	45.0	ns
	tWL	35.0	40.0	50.0	ns

NOTE: 1. X means "Don't Care."
2. Reserved for A20 expansion in multiplexed mode.
3. Reserved for A21 expansion in multiplexed mode.
4. BL = 8 is not available for configuration 1.

REFRESH COMMAND IN MULTIPLEXED ADDRESS MODE

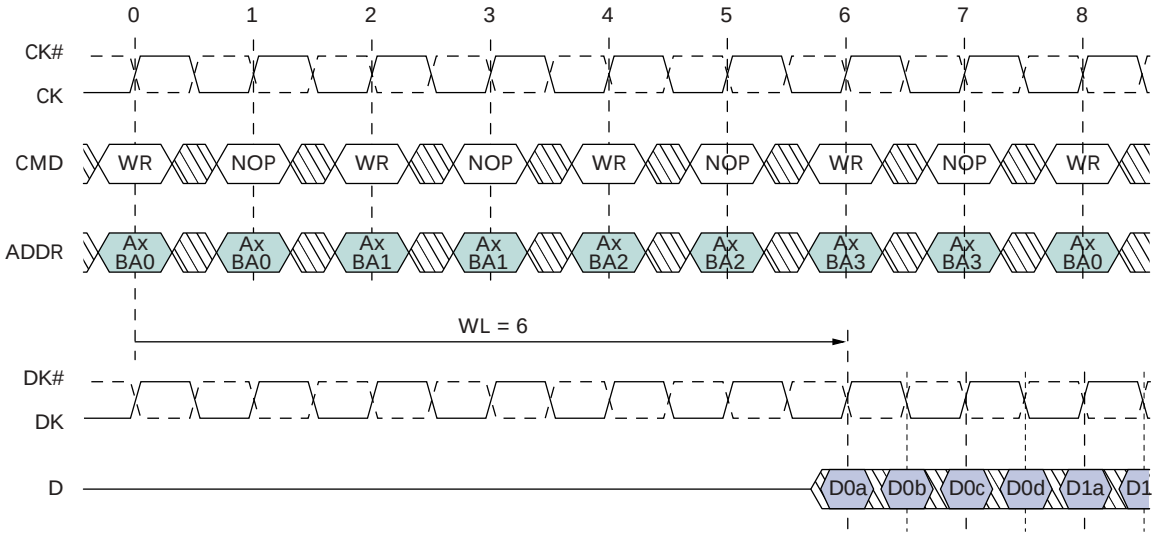
Similar to other commands, the refresh command is executed on the next rising clock edge when in the multiplexed address mode. However, since only bank address is required, the next AREF command can be applied on the following clock. In order to comply with the chip command processing, two clock cycles have to be introduced between the last AREF command and any other command as represented in Figure 36.

Figure 36
Burst Refresh Operation



Note: AREF: auto refresh
AC: any command
Ax: first part *Ax* of address
Ay: second part *Ay* of address
BAk: bank k; k is chosen so that ^{t}RC is met

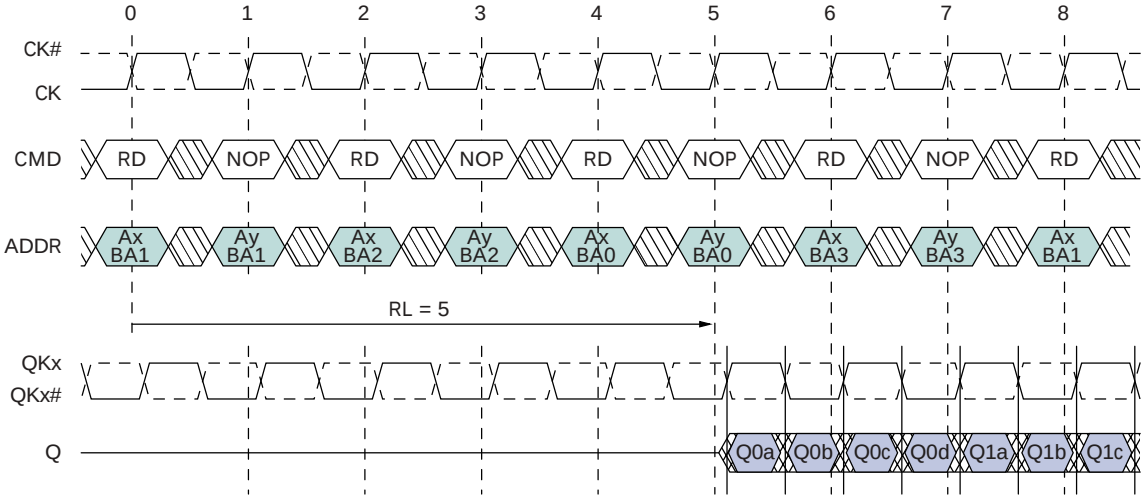
Figure 37
WRITE Burst Basic Sequence: BL = 4, with Multiplexed Addresses, Configuration 1, WL = 6



Note: A*x*/BAk: address A*x* of bank k
A*y*: address A*y* of bank k
WR: WRITE
Djk: data k to bank j
WL: write latency

DON'T CARE

Figure 38
READ Burst Basic Sequence: BL = 4, with Multiplexed Addresses, Configuration 1, RL = 5



Note: A*x*/BAk: address A*x* of bank k
A*y*: address A*y* of bank k
RD: READ
Qjk: data k to bank j
RL: read latency

DON'T CARE UNDEFINED

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

RLDRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-2001. The TAP operates using JEDEC-standard logic levels.

RLDRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

DISABLING THE JTAG FEATURE

It is possible to operate the RLDRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 39. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register (see Figure 40).

TEST DATA-OUT (TDO)

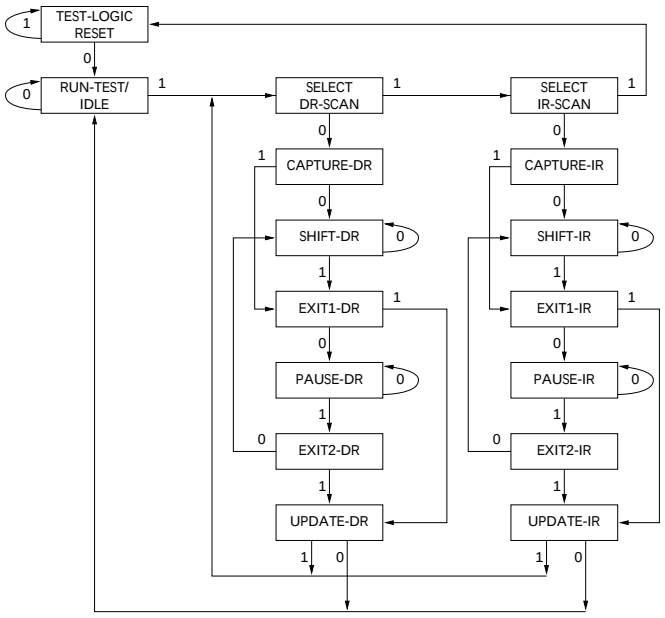
The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Figure 39). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see Figure 40).

PERFORMING A TAP RESET

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the RLDRAM and may be performed while the RLDRAM is operating.

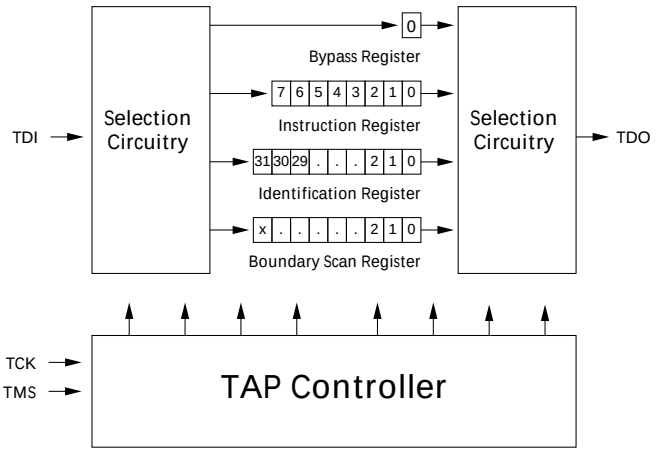
At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

Figure 39
TAP Controller State Diagram



Note: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Figure 40
TAP Controller Block Diagram



Note: x = 112 for all configurations.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the RLDRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

INSTRUCTION REGISTER

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 40. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the RLDRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the RLDRAM. Several pins are also included in the scan register to reserved pins. The RLDRAM has a 113-bit register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the pins on the RLDRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the RLDRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET

OVERVIEW

Many different (2^8) instructions are possible with the eight-bit instruction register. All used combinations are listed in Table18, Instruction Codes. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RLDRAM is fully compliant to the 1149.1 convention.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply a test vector, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instrucion. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output pins.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

HIGH Z

The HIGH Z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RLDRAM outputs into a High-Z state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output pins are determined from the values held in the boundary scan register.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the RLDRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To ensure that the boundary scan register will capture the correct value of a signal, the RLDRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The RLDRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 41
TAP Timing

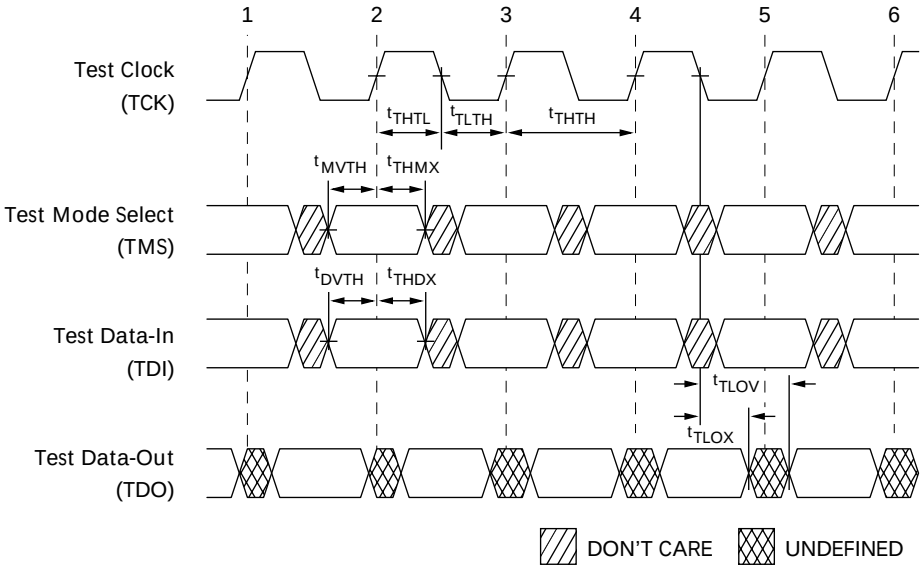


Table 14: TAP AC Electrical Characteristics[1]

(+0°C ≤ T_J ≤ +100°C; +1.7V ≤ V_{DD} ≤ +1.9V)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	20		ns
Clock frequency	^fTF		50	MHz
Clock HIGH time	^tTHTL	10		ns
Clock LOW time	^tTLTH	10		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		10	ns
TDI valid to TCK HIGH	^tDVTH	5		ns
TCK HIGH to TDI invalid	^tTHDX	5		ns
Setup Times				
TMS setup	^tMVTH	5		ns
Capture setup	^tCS	5		ns
Hold Times				
TMS hold	^tTHMX	5		ns
Capture hold	^tCH	5		ns

NOTE: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.

Table 15: TAP DC Electrical Characteristics and Operating Conditions

(+0°C ≤ T_J ≤ 100°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	V_{REF} + 0.15	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	$V_{SS}Q$ - 0.3	V_{REF} - 0.15	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-5.0	5.0	µA	
Output Leakage Current	Output disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$	I_{LO}	-5.0	5.0	µA	
Output Low Voltage	I_{OLC} = 100µA	V_{OL1}		V_{REF} - tbd	V	1
Output Low Voltage	I_{OLT} = 2mA	V_{OL2}		V_{REF} - tbd	V	1
Output High Voltage	|I_{OHC}| = 100µA	V_{OH1}	V_{REF} + tbd		V	1
Output High Voltage	|I_{OHT}| = 2mA	V_{OH2}	V_{REF} + tbd		V	1

NOTE: 1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH}(AC) \leq V_{DD} + 0.7V$ for $t \leq {}^tCK/2$
Undershoot: $V_{IL}(AC) \geq -0.5V$ for $t \leq {}^tCK/2$
During normal operation, $V_{DD}Q$ must not exceed V_{DD}.

Table 16: Identification Register Definitions

INSTRUCTION FIELD	ALL DEVICES	DESCRIPTION
Revision Number (31:28)	abcd	ab = die revision cd = 10 for x36, 01 for x18, 00 for x9.
Device ID (27:12)	00jkidef10100111	def = 000 for 288M, 001 for 576M, 010 for 1G. i = 0 for common I/O, 1 for separate I/O. jk = 00 for RLDRAM, 01 for RLDRAM II.
MICRON JEDEC ID Code (11:1)	00000101100	Allows unique identification of RLDRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Table 17: Scan Register Sizes

REGISTER NAME	BIT SIZE
Instruction	8
Bypass	1
ID	32
Boundary Scan	113

Table 18: Instruction Codes

INSTRUCTION	CODE	DESCRIPTION
Extest	0000 0000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect RLDRAM operations.
ID Code	0010 0001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect RLDRAM operations.
Sample/Preload	0000 0101	Captures I/O ring contents. Places the boundary scan register between TDI and TDO.
Clamp	0000 0111	Selects the bypass register to be connected between TDI and TDO. Data driven by output pins are determined from values held in the boundary scan register.
High Z	0000 0011	Selects the bypass register to be connected between TDI and TDO. All ouputs are forced into high impedance state.
Bypass	1111 1111	Places the bypass register between TDI and TDO. This operation does not affect RLDRAM operations.

Table 19: Boundary Scan (Exit) Order

BIT#	FBGA BALL
1	K1
2	K2
3	L2
4	L1
5	M1
6	M3
7	M2
8	N1
9	P1
10	N3
11	N3
12	N2
13	N2
14	P3
15	P3
16	P2
17	P2
18	R2
19	R3
20	T2
21	T2
22	T3
23	T3
24	U2
25	U2
26	U3
27	U3
28	V2
29	U10
30	U10
31	U11
32	U11
33	T10
34	T10
35	T11
36	T11
37	R10

BIT#	FBGA BALL
38	R10
39	R11
40	R11
41	P11
42	P11
43	P10
44	P10
45	N11
46	N11
47	N10
48	N10
49	P12
50	N12
51	M11
52	M10
53	M12
54	L12
55	L11
56	K11
57	K12
58	J12
59	J11
60	H11
61	H12
62	G12
63	G10
64	G11
65	E12
66	F12
67	F10
68	F10
69	F11
70	F11
71	E10
72	E10
73	E11
74	E11

BIT#	FBGA BALL
75	D11
76	D10
77	C11
78	C11
79	C10
80	C10
81	B11
82	B11
83	B10
84	B10
85	B3
86	B3
87	B2
88	B2
89	C3
90	C3
91	C2
92	C2
93	D3
94	D3
95	D2
96	D2
97	E2
98	E2
99	E3
100	E3
101	F2
102	F2
103	F3
104	F3
105	E1
106	F1
107	G2
108	G3
109	G1
110	H1
111	H2
112	J2
113	J1

NOTE: 1. Any unused pins that are in the order will read as the logic level applied to the ball site. If left floating, a value of '0' is returned.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -55°C to +150°C
I/O Voltage ..... -0.3V to VDDQ + 0.3V
Voltage on VEXT Supply
Relative to VSS ..... -0.3V to +2.8V
Voltage on VDD Supply
Relative to VSS ..... -0.3V to +2.1V
Voltage on VDDQ Supply
Relative to VSS ..... -0.3V to +2.1V
Junction Temperature** ..... 110°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

Table 20: DC Electrical Characteristics and Operating Conditions

(+0°C ≤ T_J ≤ +100°C; +1.7V ≤ VDD ≤ +1.9V, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		VEXT	2.38	2.63	V	1
Supply Voltage		VDD	1.7	1.9	V	1, 4
Isolated Output Buffer Supply		VDDQ	1.4	VDD	V	1, 4, 5
Reference Voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	1–3, 8
Termination Voltage		VTT	0.95 x VREF	1.05 x VREF	V	9, 10
Input High (Logic 1) Voltage		VIH	VREF + 0.1	VDDQ + 0.3	V	1, 4
Input Low (Logic 0) Voltage		VIL	VSSQ - 0.3	VREF - 0.1	V	1, 4
Output High Current	VOH = VDDQ/2	IOH	(VDDQ/2) (1.15 x RQ/5)	(VDDQ/2) (0.85 x RQ/5)	mA	6, 7,11
Output Low Current	VOL = VDDQ/2	IOL	(VDDQ/2) (1.15 x RQ/5)	(VDDQ/2) (0.85 x RQ/5)	mA	6, 7,11
Clock Input Leakage Current	0V ≤ VIN ≤ VDD	ILC	-5	5	µA	
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5	5	µA	
Output Leakage Current	0V ≤ VIN ≤ VDDQ	ILO	-5	5	µA	
Reference Voltage Current		IREF	-5	5	µA	

NOTE:
1. All voltages referenced to VSS (GND).
2. Typically the value of VREF is expect to be 0.5 x VDDQ of the transmitting device. VREF is expected to track variations in VDDQ.
3. Peak-to-peak AC noise on VREF must not exceed 2% VREF(DC).
4. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ $^tCK/2$
   Undershoot: VIL(AC) ≥ -0.5V for t ≤ $^tCK/2$
   During normal operation, VDDQ must not exceed VDD.
   Control input signals may not have pulse widths less than $^tCK/2$ or operate at frequencies exceeding ^tCK (MAX).
5. VDDQ can be set to a nominal 1.5V ± 0.1V or 1.8V ± 0.1V supply
6. IOH and IOL are defined as absolute values and are measured at VDDQ/2. IOH flows from the device, IOL flows into the device.
7. If MRS bit A8 is 0, use RQ = 250Ω in the equation in lieu of presence of an external impedance matched resistor.
8. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on VREF may not exceed ±2 percent of the DC value. Thus, from VDDQ/2, VREF is allowed ±2% VDDQ/2 for DC error and an additional ±2% VDDQ/2 for AC noise. This measurement is to be taken at the nearest VREF by-pass capacitor.
9. VTT is expected to be set equal to VREF and must track variations in the DC level of VREF.
10. On-die termination may be selected using mode register bit 9 (see Mode Register Bit Map on page 10). A resistance RTT from each data input signal to the nearest VTT can be enabled. RTT = 150Ω (± 10%) at 70°C T_J.
11. For VOL and VOH, refer to the Spice Model fro the RLDRAM II Command Driver.

Table 21: AC Electrical Characteristics and Operating Conditions

(+0°C ≤ T_J ≤ +100°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Matched Impedance Mode	V_{IH}	V_{REF} + 0.2	$V_{DD}Q$ + 0.2	V	
Input Low (Logic 0) Voltage	Matched Impedance Mode	V_{IL}	$V_{SS}Q$ - 0.2	V_{REF} - 0.2	V	

Table 22: Capacitance

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	1.5	2.5	pF	
Input/Output Capacitance (DQ)		C_O	3.0	4.0	pF	
Clock Capacitance		C_{CK}	2.0	3.0	pF	

Figure 42
Output Test Conditions

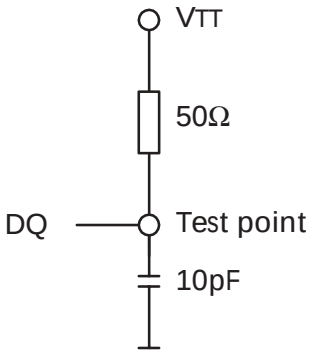


Figure 43
Input Waveform

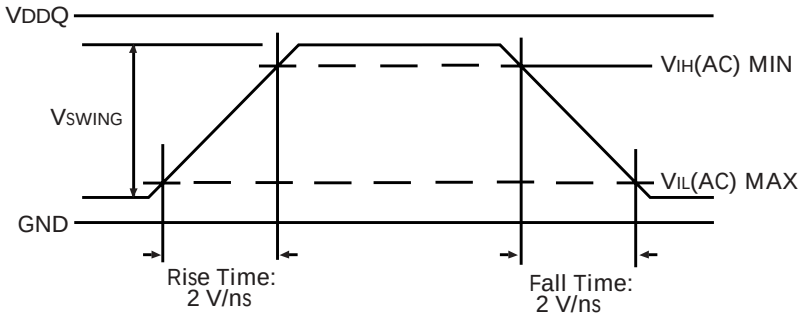
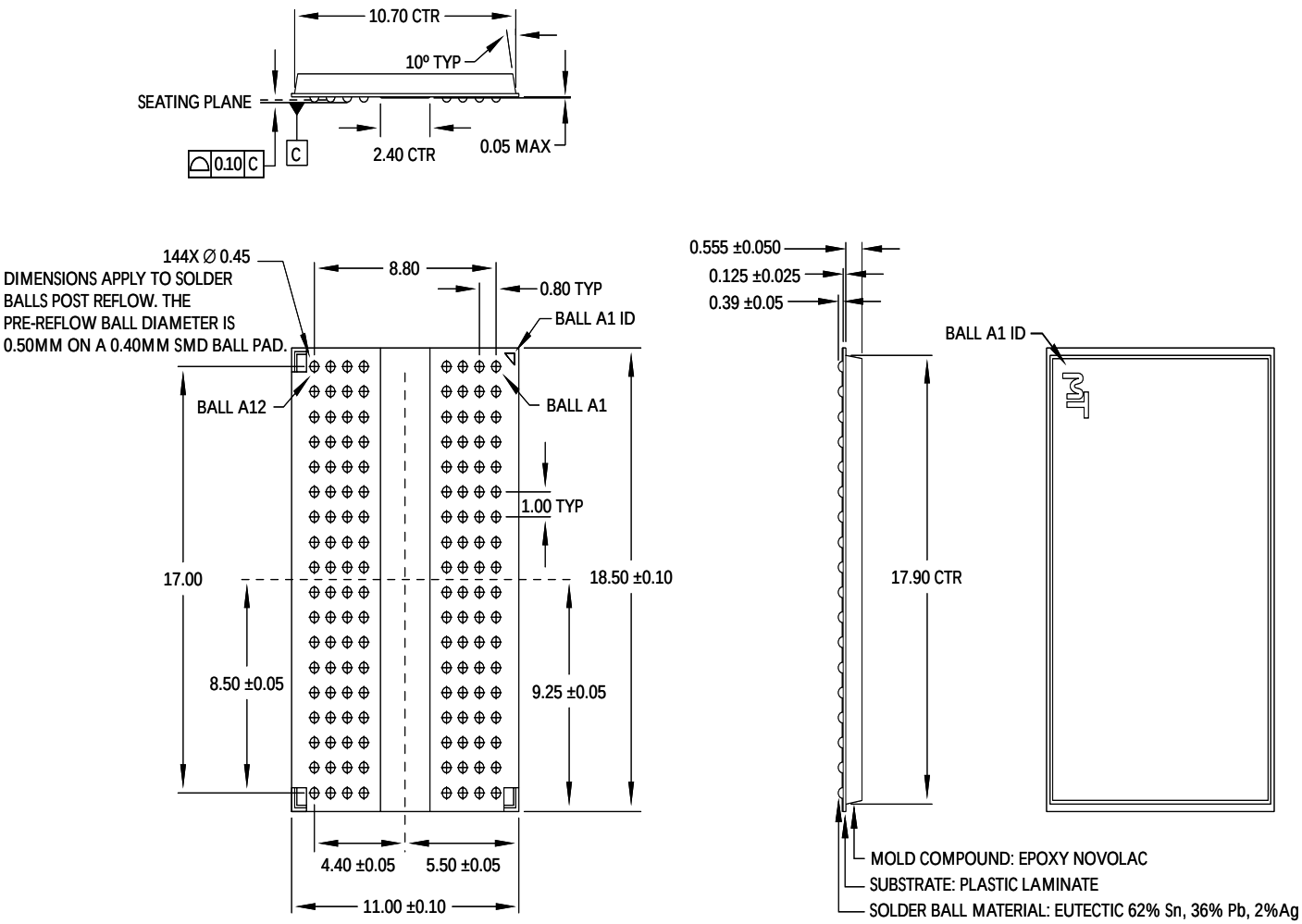


Table 13: IDD Operating Conditions and Maximum Limits

(+0°C ≤ T_J ≤ +100°C; VDD = MAX, unless otherwise noted)

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-2.5	-3.3	-5	UNIT	NOTES
Standby Current	^tCK = Idle All banks idle, no inputs toggling	ISB1 (VDD) ISB1 (VEXT)	TBD TBD	TBD TBD	TBD TBD	mA mA	
Standby Current	^tCK = MIN, CS# = 1 No commands	ISB2 (VDD) ISB2 (VEXT)	TBD TBD	TBD TBD	TBD TBD	mA mA	
Incremental Current	BL = 2, ^tCK = MIN, ^tRC = MIN, 1 bank active	IDD1 (VDD) IDD1 (VEXT)	TBD TBD	TBD TBD	TBD TBD	mA mA	
Incremental Current	BL = 4, ^tCK = MIN, ^tRC = MIN, 1 bank active	IDD2 (VDD) IDD2 (VEXT)	TBD TBD	TBD TBD	TBD TBD	mA mA	
Incremental Current	BL = 8, ^tCK = MIN, ^tRC = MIN, 1 bank active	IDD3 (VDD) IDD3 (VEXT)	TBD TBD	TBD TBD	TBD TBD	mA mA	
Refresh Current	^tCK = MIN	IREF (VDD) IREF (VEXT)	TBD TBD	TBD TBD	TBD TBD	mA mA	
Operating Supply Current Example	BL = 4, ^tCK = MIN, ^tRC = MIN, 4 banks interleave, address change up to 8 times during minimum ^tRC continuous data	IDD4R (VDD) IDD4R (VEXT)	TBD TBD	TBD TBD	TBD TBD	mA mA	

Figure 44
144-Ball FBGA



NOTE: 1. All dimensions in millimeters.

DATA SHEET DESIGNATION

Advance: This data sheet contains initial descriptions of products still under development.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992

REVISION HISTORY

Rev. 3, Pub. 5/03 ..... 5/03

- JTAG numbering order has been reversed. (Page 42)