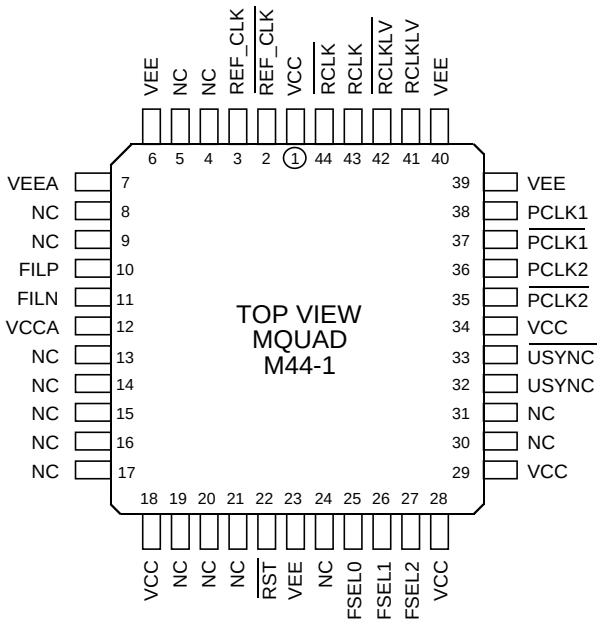
## FEATURES

- 3.3V, –1.9V power suppies
- Differential LVPECL clock input
- Differential HSTL/LVPECL outputs
- Compatible with HP PA-8000 microprocessors
- Low-jitter source for all PA-8000 required timing signals
- Available in 44-pin MQUAD package

## PIN CONFIGURATION




## DESCRIPTION

Micrel-Synergy's SY89801A PLL based clock generator provides, in a single chip, all the necessary clocks for Hewlett-Packard's PA-8000 Microprocessor.

Utilizing Micrel-Synergy's advanced PLL technology, the SY89801A accepts a Positive-ECL (PECL) reference clock input at 100MHz-132MHz, and provides precisely aligned, ultra-low-jitter ratios of frequencies necessary for the operation of the processor. In addition, the SY89801A provides the "USYNC" synchronizing signals as required by the PA-8000. The frequency ratios are 1:1, 4:3, 3:2, 5:3 and 2:1.

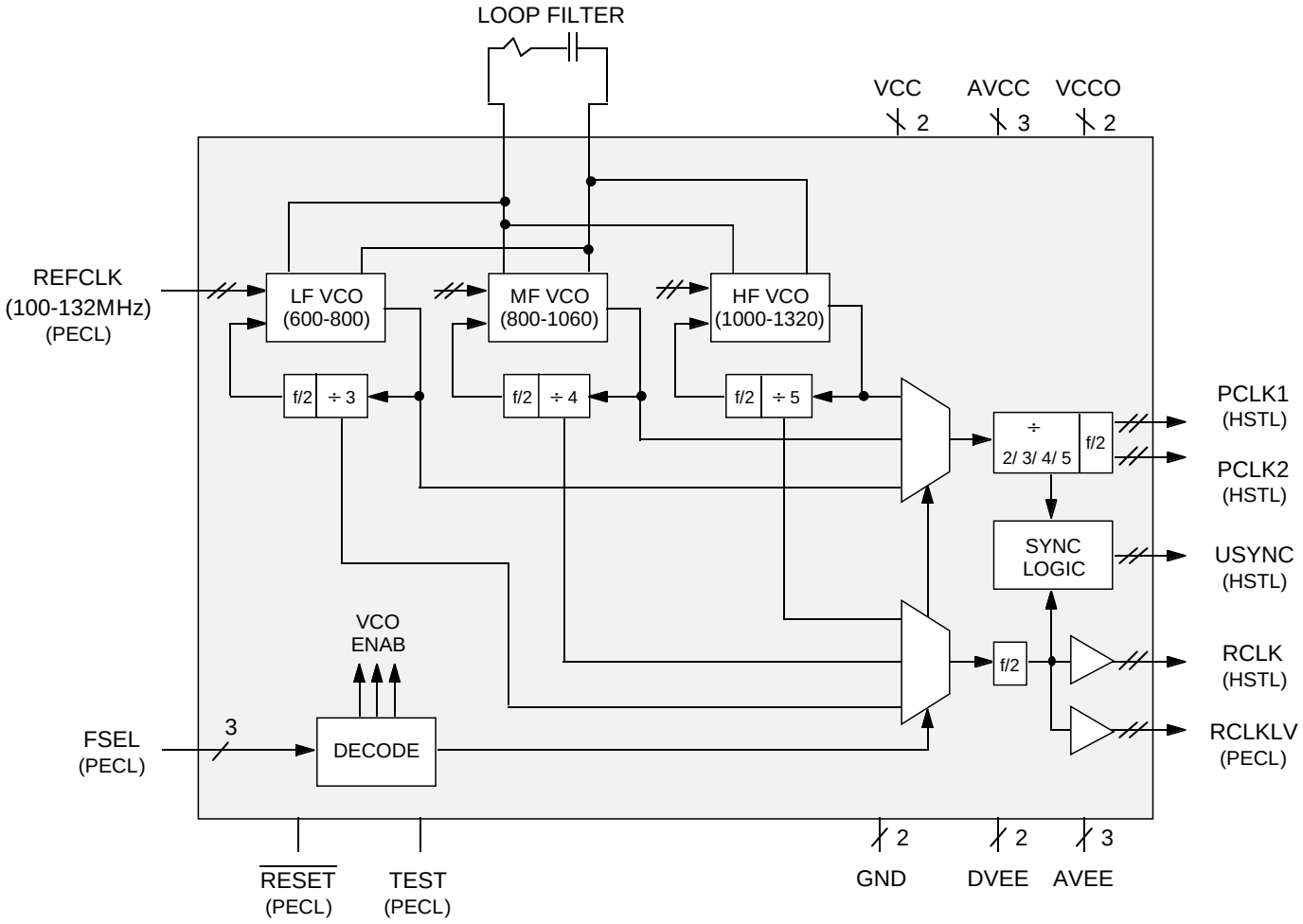
To facilitate direct interfacing to the PA-8000, the SY89801A operates across +3.3 volt and -1.9 volt supplies. The processor clock (PCLK), runway clock (RCLK) , and USYNC outputs are HSTL-compatible. Additionally, there is a PECL-compatible runway clock output (RCLKLV). The SY89801A requires only a simple external series-RC loop filter.

Coupling Micrel-Synergy's advanced PLL technology with our proprietary ASSET bipolar process has produced a Timing Generator IC which meets the stringent requirements of the PA-8000 µP, while setting a new standard for performance and flexibility.

## PIN NAMES

| Pin | Function |
|---|---|
| REF_CLK, $\overline{\text{REF\_CLK}}$ | Differential Input Ref. Clock |
| FILP, FILN | Filter Pins (Positive & Negative) |
| $V_{CCA}$, $V_{EEA}$ | Analog $V_{CC}$, $V_{EE}$ |
| $\overline{\text{RST}}$ | Master Reset |
| FSEL2-0 | LVPECL Frequency Select Pins |
| USYNC, $\overline{\text{USYNC}}$ | Diff. HSTL Sync Signal for PA-8000 |
| PCLK1-2, $\overline{\text{PCLK}}$1-2 | Diff. HSTL Processor Clock Signal |
| RCLK, $\overline{\text{RCLK}}$ | Diff. HSTL Runway Clock Signal |
| RCLKLV, $\overline{\text{RCLKLV}}$ | Diff. LVPECL Clock Signal |

## BLOCK DIAGRAM



## 3.3V DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCA} = 3.3V \pm 10\%$; $V_{EEA} = V_{EE} = -1.9V$

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 3.0 | — | 3.6 | V | $V_{EE} = -1.9V$ |
| $I_{CC}$ | Power Supply Current ($V_{CC}$) | — | 250 | 321 | mA | |

## PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V \pm 10\%$; $V_{EE} = -1.9V$

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} - 1.075$ | — | $V_{CC} - 0.830$ | V | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} - 1.860$ | — | $V_{CC} - 1.570$ | V | |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC} - 1.165$ | — | $V_{CC} - 0.880$ | V | |
| $V_{IL}$ | Input LOW Voltage | $V_{CC} - 1.810$ | — | $V_{CC} - 1.475$ | V | |
| $V_{BB}$ | PECL Threshold | — | $V_{CC} - 1.35$ | — | V | |

## HSTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V \pm 10\%$; $V_{EE} = -1.9V$

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} - 2.3$ | — | $V_{CC} - 2.1$ | V | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} - 3.1$ | — | $V_{CC} - 2.9$ | V | |

## AC ELECTRICAL CHARACTERISTICS[1]

$V_{CC} = 3.3V \pm 10\%$; $V_{EE} = -1.9V$

| | | $T_A = 0°C$ | | | $T_A = +25°C$ | | | $T_A = +70°C$ | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Unit | Condition |
| $f_{VCO}$ | Maximum VCO Frequency | 1320 | — | — | 1320 | — | — | 1320 | — | — | MHz | |
| $f_{MAX}$ | Maximum PCLK Output Frequency<br>Maximum RCLK Output Frequency | 264<br>132 | —<br>— | —<br>— | 264<br>132 | —<br>— | —<br>— | 264<br>132 | —<br>— | —<br>— | MHz<br>MHz | |
| $t_{skew}$[2] | PCLK to PCLK<br>RCLK to RCLKLV<br>PCLK to RCLK<br>PCLK (neg.) to USYNC | —<br>—<br>—<br>— | —<br>—<br>—<br>— | ±50<br>±100<br>±100<br>±500 | —<br>—<br>—<br>— | —<br>—<br>—<br>— | ±50<br>±100<br>±100<br>±500 | —<br>—<br>—<br>— | —<br>—<br>—<br>— | ±50<br>±100<br>±100<br>±500 | ps<br>ps<br>ps<br>ps | Measured at differential crossover |
| tpe | Phase Error<br>RCLK to REF_CLK | — | — | ±250 | — | — | ±250 | — | — | ±250 | ps | |
| tj[2] | Output Jitter | –50 | — | +50 | –50 | — | +50 | –50 | — | +50 | ps | Peak to Peak, Cycle to Cycle |
| tdc[2] | Output Duty Cycle | 49 | — | 51 | 49 | — | 51 | 49 | — | 51 | % | |
| tr [2]<br>tf | Rise/Fall Times<br>(20% to 80%) | 100 | — | 800 | 100 | — | 800 | 100 | — | 800 | ps | |

**NOTES:**

1. All HSTL outputs terminated into 50 ohms in parallel with 3pf to GND.
2. $t_{skew}$, tj, tdc, tr and tf are specified by HP for the PA-8000. This is our best information as of the date of this document.

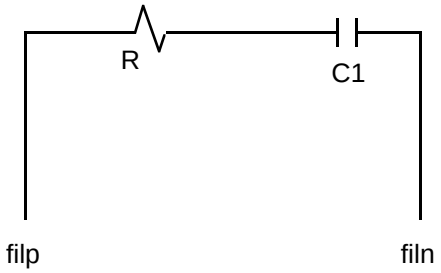
## APPLICATIONS INFORMATION

The following table lists the various PCLK and RCLK ratios supported by the SY89801A and the corresponding PCLK, RCLK, FB and VCO frequencies. The table is arranged in order of increasing PCLK:RCLK ratio. The table was designed to balance several constraints:

- **2.5:1 VCO frequency range**
- **Maximum system frequency of 120MHz plus 10% margin**
- **Maximum output frequency of 264MHz**

| FSEL <2:0> | PCLK:RCLK | fPCLK (MHz) | fRCLK (MHz) | VCO ÷ ratios VCO/P:VCO/R | fVCO (MHz) |
|---|---|---|---|---|---|
| 000 | 1:1 | 100-132 | 100-132 | 8:8 | 800-1056 |
| 001 | 4:3 | 133.3-176 | 100-132 | 6:8 | 800-1056 |
| 010 | 3:2 | 150-198 | 100-132 | 4:6 | 600-792 |
| 011 | 5:3 | 166.7-220 | 100-132 | 6:10 | 1000-1320 |
| 100 | 2:1 | 200-264 | 100-132 | 4:8 | 800-1056 |
| 101 | 1:1 | 100-132 | 100-132 | 6:6 | 600-792 |
| 110 | 1:1 | 100-132 | 100-132 | 10:10 | 1000-1320 |
| 111 | n/a | n/a | n/a | n/a | n/a |

## LOOP FILTER COMPONENT SELECTION




R = 500Ω ±10%

C1 = 1000pF ±10%

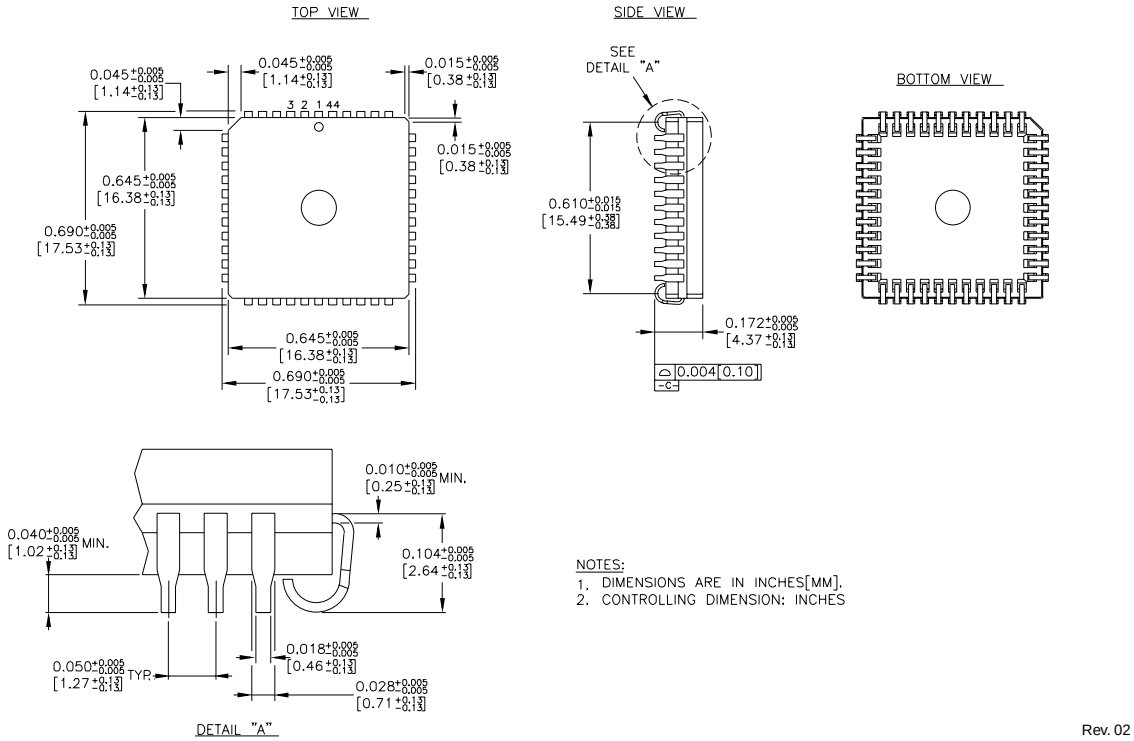
## PRODUCT ORDERING CODE

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| SY89801AMC | M44-1 | Commercial |
| SY89801AMCA(1) | M44-1 | Commercial |

**NOTES:**

1. "A" denotes enhanced 200MHz testing.

## 44 LEAD MLCC (M44-1)




Rev. 02



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