TH8082

Enhanced SoloLIN Transceiver

Features

- Operating voltage V_S = 6 to 18 V
- Very low standby current consumption of typ. 6.5µA in sleep mode
- LIN-Bus Transceiver:
  - Slew rate control for good EMC behavior
  - Fully integrated receiver filter
  - BUS input voltage -27V to 40V
  - Integrated termination resistor for LIN slave nodes (30kΩ)
  - Wake up via LIN bus
  - Baud rate up to 20 kBaud
  - Compatible to LIN Specification 1.3
- Compatible to ISO9141 functions
- Control output for voltage regulator with low on – resistance for switchable master termination
- High EMI immunity
- Bus terminals proof against short-circuits and transients in the automotive environment
- High impedance Bus pin in case of loss of ground and undervoltage condition
- Thermal overload protection
- High signal symmetry for using in RC – based slave nodes up to 2% clock tolerance
- ±4kV ESD protection at Bus pin

Ordering Information

Part No.	*Temperature Range*	*Package*
TH8082	K (-40 to 125 °C)	DC (SOIC8)

General Description

The TH8082 is a physical layer device for a single wire data link capable of operating in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor which use the network. The TH8082 is designed in accordance to the physical layer definition of the LIN Protocol Specification, Rev. 1.3.The IC furthermore can be used in ISO9141 systems.

Because of the very low current consumption of the TH8082 in the sleep mode it's suitable for ECU applications with hard standby current requirements. This mode allows a shutdown of the whole application. The included wake-up function detects incoming dominant bus messages and enables the voltage regulator.

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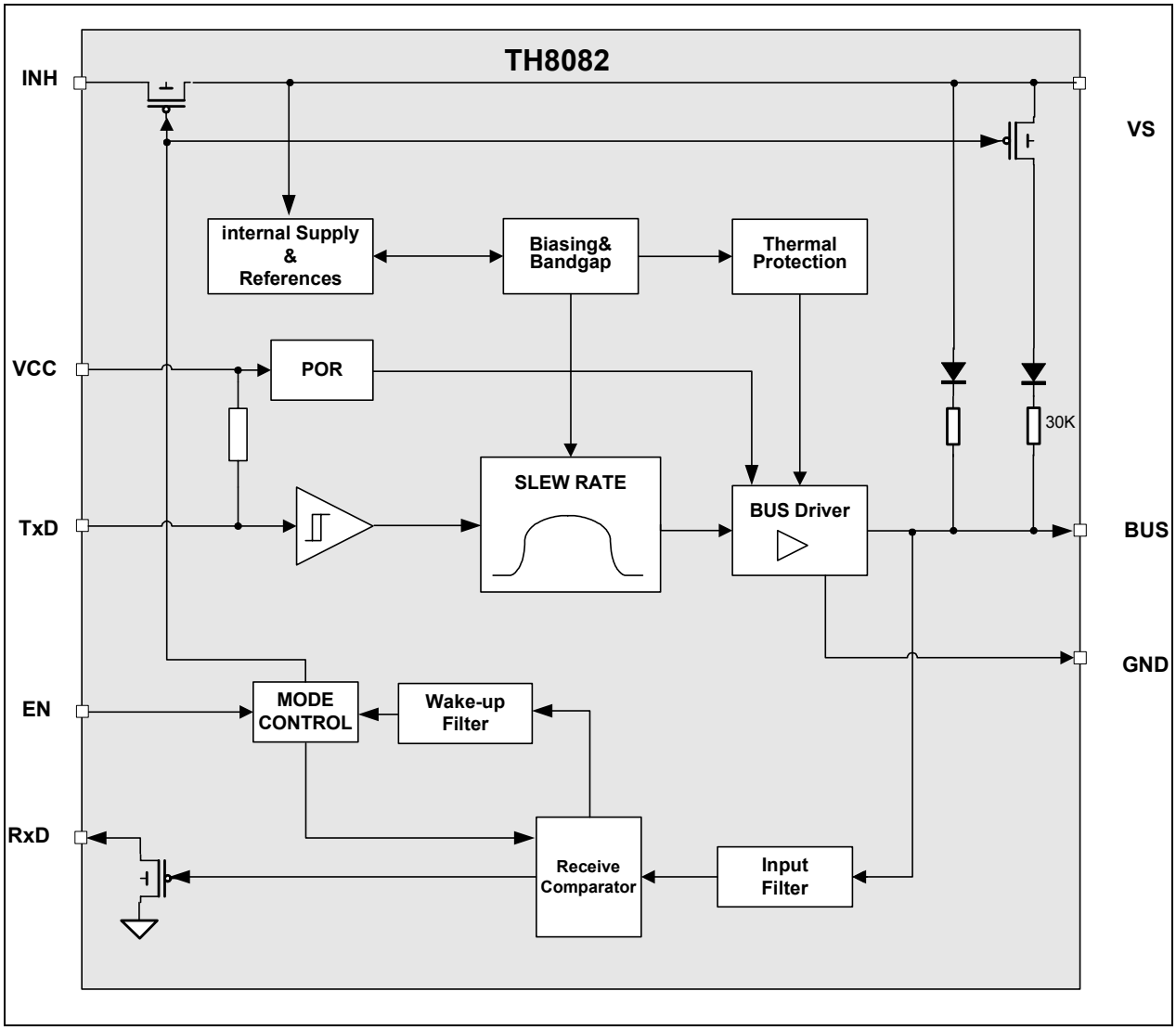


Figure 1 - Block Diagram

2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may effect the reliability of the device.

2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery supply voltage [1]	V_S	6	18	V
Supply voltage	V_{CC}	4.5	5.5	V
Operating ambient temperature	T_{amb}	-40	+125	°C

[1] Vs is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4 to 1V, V_{BAT_ECU} voltage range is 7 to 18V

2.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Battery Supply Voltage	V_S	t < 1 min	-0.3	30	V
		Load dump, t < 500ms		40	
Supply Voltage	V_{CC}		-0.3	+7	V
Transient supply voltage	$V_{S.tr1}$	ISO 7637/1 pulse 1[1]	-150		V
Transient supply voltage	$V_{S..tr2}$	ISO 7637/1 pulses 2[1]		100	V
Transient supply voltage	$V_{S..tr3}$	ISO 7637/1 pulses 3A, 3B	-150	150	V
BUS voltage	V_{BUS}	t < 500ms , Vs = 18V	-27	40	V
		t < 500ms ,Vs = 0V	-40		
Transient bus voltage	$V_{BUS..tr1}$	ISO 7637/1 pulse 1 [2]	-150		V
Transient bus voltage	$V_{BUS.tr2}$	ISO 7637/1 pulses 2 [2]		100	V
Transient bus voltage	$V_{BUS.tr3}$	ISO 7637/1 pulses 3A, 3B [2]	-150	150	V
DC voltage on pins TxD, RxD	V_{DC}		-0.3	7	V
ESD capability of any pin	ESD_{HB}	Human body model, equivalent to discharge 100pF with 1.5kΩ,	-4	4	kV
Maximum latch - up free current at any Pin	I_{LATCH}		-500	500	mA
Maximum power dissipation	P_{tot}	At T_{amb} = 125 °C		197	mW
Thermal impedance	Θ_{JA}	in free air		152	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

[1] ISO 7637 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor .
[2] ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1 nF.

2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for V_S = 6 to 18V, V_{CC} = 4.5 to 5.5V and T_{AMB}= -40 to 125°C. All voltages are referenced to ground (GND), positive currents are flow into the IC.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN VS, VCC						
V_{CC} undervoltage lockout	V_{CC_UV}	EN=H, TxD=L	2.75		4.3	V
Supply current, dominant	I_{Sd}	V_S = 18V,V_{CC} = 5.5V TxD = L		0.9	2	mA
Supply current, dominant	I_{CCd}	V_S = 18V,V_{CC} = 5.5V TxD = L		0.6	2	mA
Supply current, recessive	I_{Sr}	V_S = 18V,V_{CC} = 5.5V TxD = H		25	100	µA
Supply current, recessive	I_{CCr}	V_S = 18V,V_{CC} = 5.5V TxD = H		50	100	µA
Supply current, sleep mode	I_{Ssl}	V_S = 12V,V_{CC} and TxD = 0V, T_{amb}= 25°		6.5		µA
Supply current, sleep mode	I_{Ssl}	V_S = 12V, V_{CC} and TxD = 0V		6.5	14	µA
PIN BUS – Transmitter						
Short circuit bus current	I_{BUS_LIM}	V_{BUS} = V_S, driver on		120	200	mA
Pull up current bus	I_{BUS_PU}	V_{BUS} = 0, V_S = 12V, driver off	-1			mA
Pull up current bus	$I_{BUS\_PU\_SLEEP}$	V_{BUS} = 0, V_S = 12V, sleep mode	-100			µA
Bus reverse current, recessive	$I_{BUS\_PAS\_rec}$	V_{BUS} > V_S, 8V < V_{BUS} < 18V 8V < V_S < 18V, driver off			20	µA
Bus reverse current loss of battery	I_{BUS}	V_S = 0V, 0V < V_{BUS} < 18V			100	µA
Bus current during loss of Ground	$I_{BUS\_NO\_GND}$	V_S = 12V, 0 < V_{BUS} < 18V	-1		1	mA
Transmitter dominant voltage	$V_{BUSdom\_DRV\_1}$	Load = 40mA			1.2	V
Transmitter dominant voltage	$V_{BUSdom\_DRV\_2}$	V_S = 6V, load = 1000Ω	0.6			V
Transmitter dominant voltage	$V_{BUSdom\_DRV\_3}$	V_S = 18V, load = 1000Ω	0.8			V
PIN BUS – Receiver						
Receiver dominant voltage	V_{BUSdom}		0.4 *V_S			V
Receiver recessive voltage	V_{BUSrec}				0.6 *V_S	V
Center point of receiver threshold	V_{BUS_CNT}	V_{BUS_CNT} = (V_{BUSdom} + V_{BUSrec})/2	0.487 *V_S	0.5 *V_S	0.512 *V_S	V
Receiver hysteresis	V_{HYS}	V_{BUS_CNTt} = (V_{BUSrec} -V_{BUSdom})		0.175 *V_S	0.187 *V_S	V
PIN TXD, EN						
High level input voltage	V_{ih}	Rising edge			0.7*V_{CC}	V
Low level input voltage	V_{il}	Falling edge	0.3*V_{CC}			V
TxD pull up current, high level	I_{IH_TXD}	V_{TxD} = 4V	-125	-50	-25	µA
TxD pull up current, low level	I_{IL_TXD}	V_{TxD} = 1V	-500	-250	-100	µA
EN pull down current, high level	I_{IH_EN}	V_{EN} = 4V, Vcc = 0V	50	125	250	µA
EN pull down current, low level	I_{IL_EH}	V_{EN} = 1V, Vcc = 0V	12	25	50	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN RXD						
Low level output voltage	V_{ol_rxd}	I_{RxD} = 2mA			0.9	V
Leakage Current	V_{leak_rxd}	V_{RxD} = 5.5V, recessive	-1		1	µA
PIN INH						
On resistance INH	R_{on_INH}	Normal or standby mode, V_{INH} = V_S-1V , V_S = 12V		20	50	Ω
Leakage current INH	I_{INH_lk}	EN = L ,V_{INH} = 0V	-5		5	µA
Thermal Protection						
Thermal shutdown	T_{sd} [1]		155		180	°C
Thermal recovery	T_{hys} [1]		130		150	°C

[1] No production test, guaranteed by design and qualification

2.4 Dynamic Characteristics

Unless otherwise specified all values in the following table are valid for V_S = 6 to 18V and T_{AMB}= -40 to 125°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation delay transmitter [1] [3]	t_{trans_pd}	Bus loads: 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF			5	µs
Propagation delay transmitter symmetry [3]	t_{trans_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-2		2	µs
Propagation delay receiver [1] [3]	t_{rec_pdf}	C_{RxD} = 25pF			6	µs
Propagation delay receiver symmetry [3]	t_{rec_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-1.5		1.5	µs
Slew rate falling edge [2]	t_{SRF}	Bus load 1KΩ/1nF	-3	-2	-1	V/µs
Slew rate rising edge [2]	t_{SRR}	Bus load 1KΩ/1nF	1	2	3	V/µs
Slope time, transition from recessive to dominant, low battery [4]	t_{sdom_LB}	V_S = 6V , Bus loads: 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF			5.4	µs
Slope time, transition from dominant to recessive, low battery [4]	t_{srec_LB}	V_S = 6V, Bus load 500Ω/10nF			7.2	µs
Slope Symmetry, low battery	T_{ssym_LB}	Calculate t_{sdom} - t_{srec}	-7		+1	µs
Slope time, transition from recessive to dominant, high battery [4]	t_{sdom_HB}	V_S = 18V, Bus loads: 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF			17.2	µs
Slope time, transition from dominant to recessive , high battery [4]	t_{srec_HB}	V_S = 18V , Bus loads: 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF			17.2	µs
Slope Symmetry, high battery	t_{ssym_HB}	Calculate t_{sdom} – t_{srec}	-5		+5	µs
Receiver debounce time [6] [1]	t_{rec_deb}	BUS rising & falling edge	1.5		4	µs
Wake-up filter time	t_{wu}	Sleep mode, BUS rising & falling edge	30		150	µs
EN - debounce time	t_{en_deb}	Normal -> sleep mode transition	10	20	40	µs

[2] Propagation delays are not relevant for LIN protocol transmission, value only information parameter
[3] No production test, guaranteed by design and qualification
[4] See Figure 2 - Input / Output timing
[5] See Figure 8 - Slope time calculation
[6] See Figure 3 – Receiver debouncing

2.5 Timing Diagrams

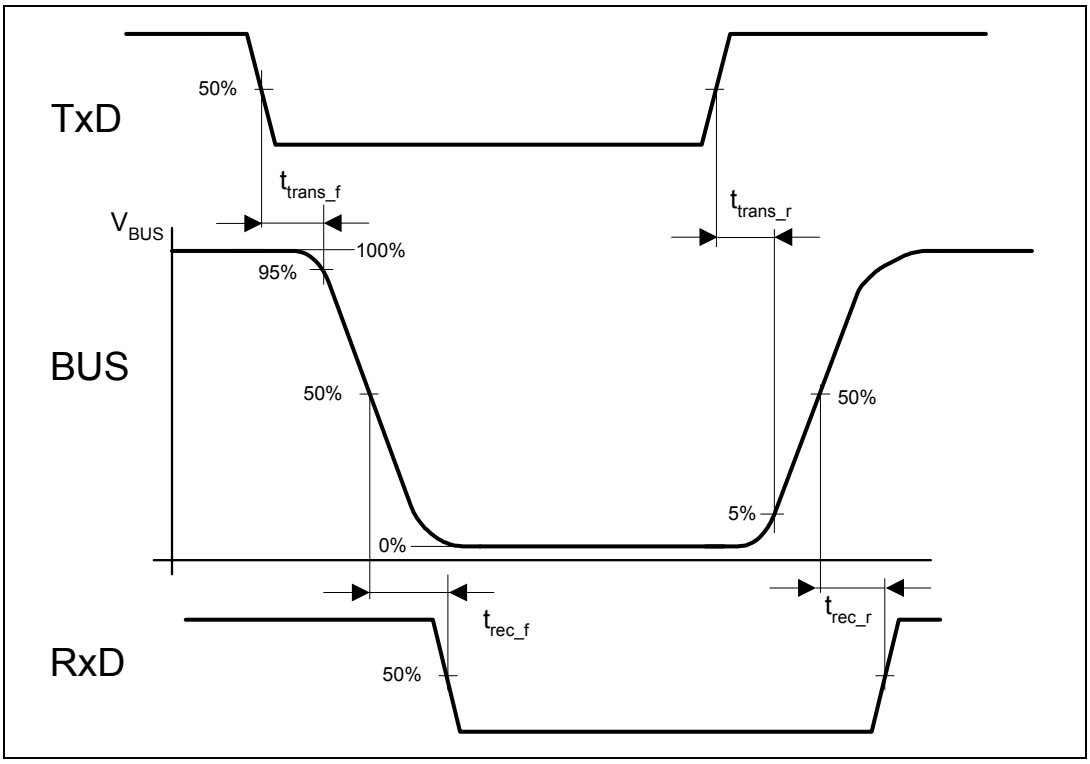


Figure 2 - Input / Output timing

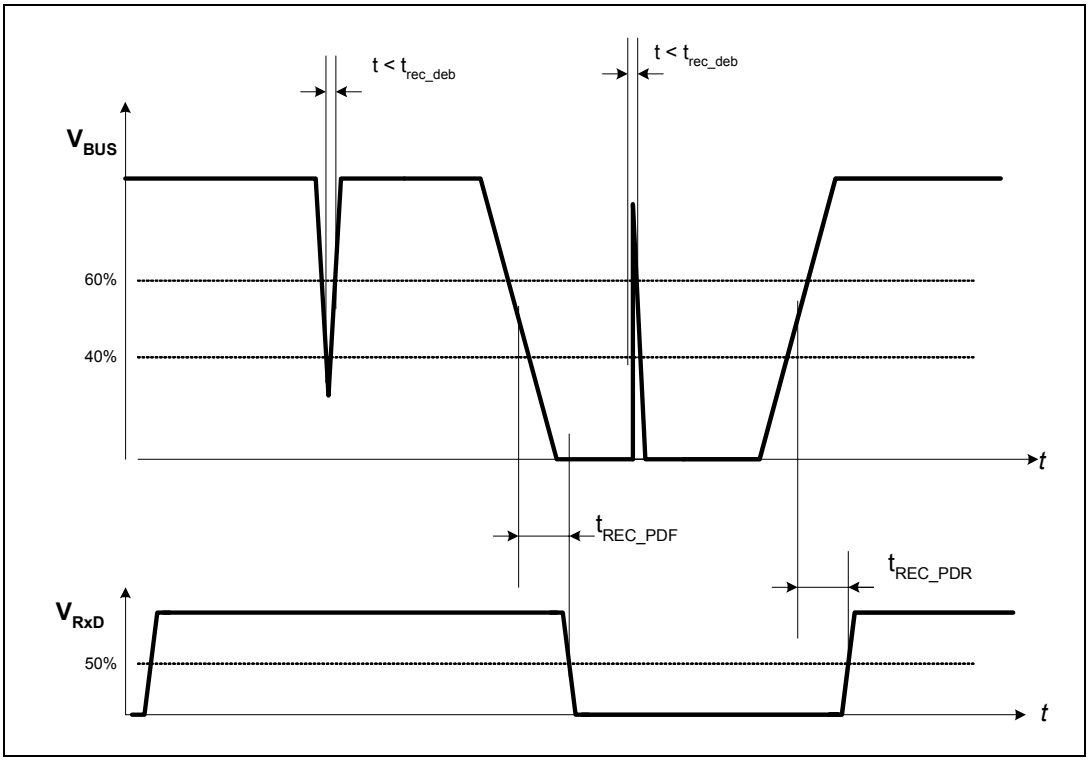


Figure 3 – Receiver debouncing

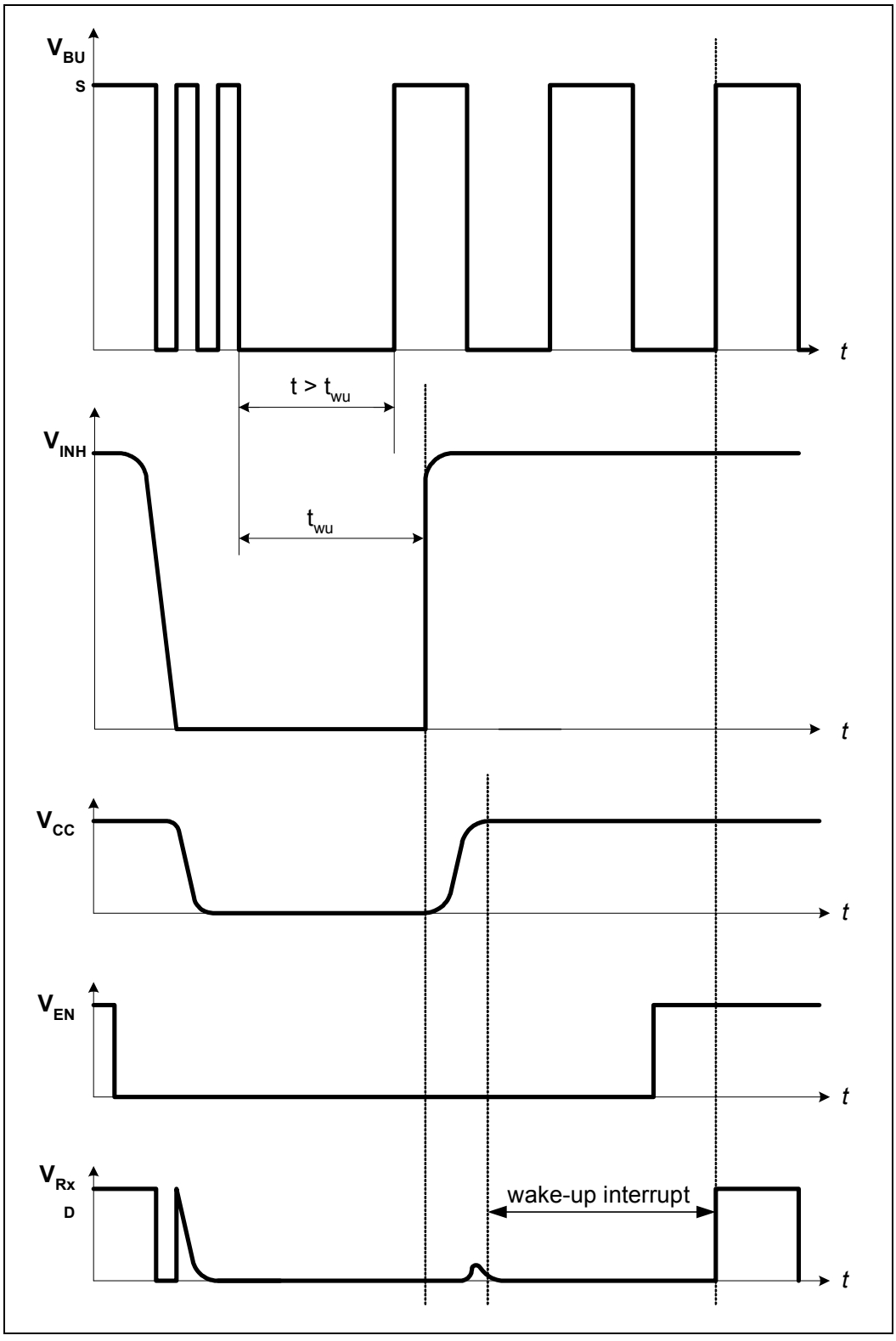


Figure 4 – Sleep mode and wake up procedure

2.6 Test Circuits for Dynamic and Static Characteristics

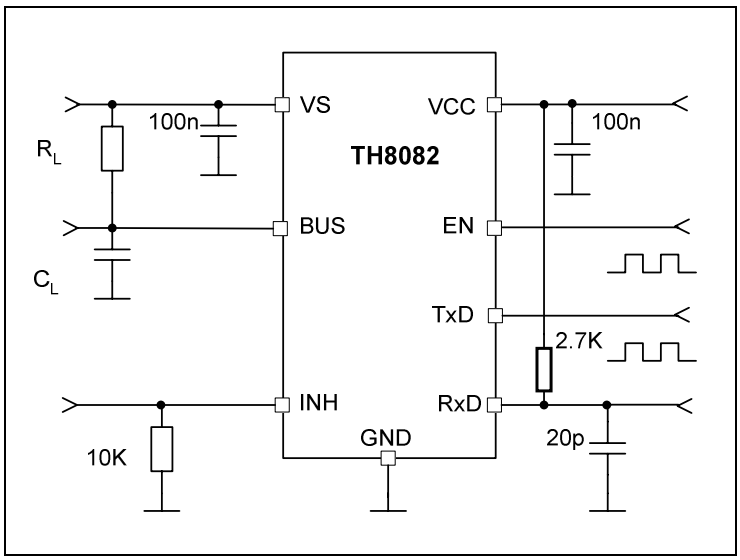


Figure 5 - Test circuit for dynamic characteristics

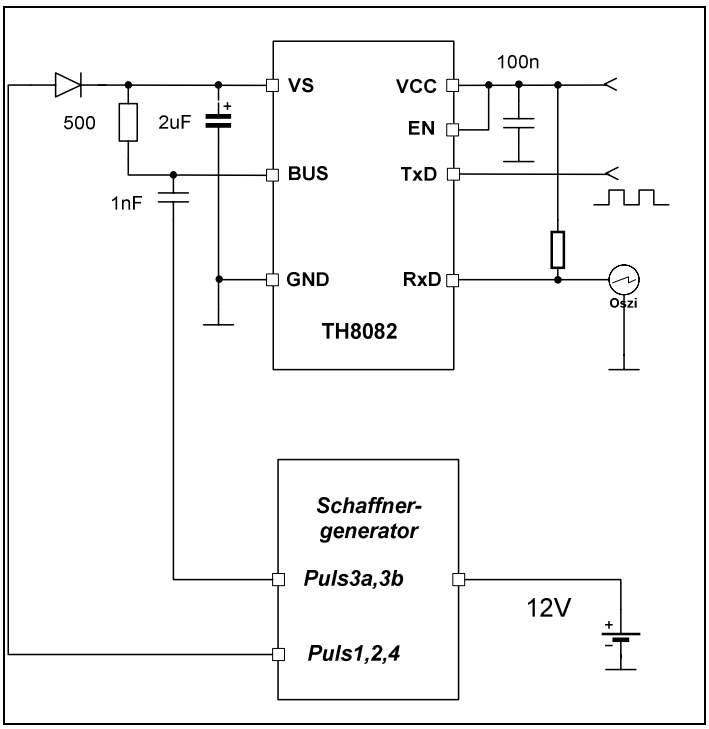


Figure 6 - Test circuit for automotive transients

3. Functional Description

3.1 Initialization

After *power on,* the chip enters automatically the *V_{BAT}-standby mode*. In this intermediate mode the INH output will become HIGH (V_S) and therefore the ECU - voltage regulator will provide the V_{CC} - supply. The transceiver will remain the V_{BAT}-standby mode until the controller sets it to *normal operation* (EN = High). Only in this mode bus communication is possible. The TH8082 switches itself in the V_{BAT}-standby mode if V_{CC} is missing or below the threshold.

3.2 Operating Modes

Via the EN pin it is possible to switch the TH8082 into different operating modes:

Normal Mode

The whole TH8082 is active. Switching to normal mode can only be done via the EN pin with EN=high.

Sleep Mode

The *sleep mode* (EN = LOW) can only be reached from normal mode and permits a very low power consumption because the transceiver and even the external voltage regulator will be disabled. If the V_{CC} has been switched off a wake-up request from the bus line (remote wake up) will cause the TH8082 to enter the V_{BAT}-standby mode (V_{CC} is present again) and sets the RxD output to low until the device enters the normal operation mode (active LOW interrupt at RxD). If the INH pin is not connected to the regulator or the inhibitable external regulator is not the one that provides the V_{CC} - supply, the normal mode is directly accessible by logic high on the EN pin. (wake up via mode change/local wake up)
In order to prevent an unintended wake-up caused by disturbances of the automotive environment incoming dominant signals from the bus have to exceed the wake-up delay time.

Thermal Shutdown Mode

If the junction temperature T_J is higher than 155°C, the TH8082 will be switched into the thermal shutdown mode. The impact of this mode is comparable with the sleep mode.
If T_J falls below the thermal shutdown temperature (typ. 140°C) the TH8082 will be switched to the previous state.

3.3 Mode control

EN	VCC	Comment	INH	RxD
0	0	V_{BAT}-standby , power on	Vs	0
0	1	V_{BAT}-standby , V_{CC} on	Vs	X
1	1	Normal mode	Vs	Vcc = recessive 0 = dominant
0	0	Sleep mode	floating	0
0	1	Sleep mode regulator not disabled directly switch to normal mode with EN = 1	floating	Vcc
0	0/1	Remote wake up request	Vs	0 - Active low wake up interrupt

Table 1 - Mode control

3.4 LIN BUS Transceiver

The transceiver consists a bus-driver (1.2V@40mA) with slew rate control, current limitation and as well in the receiver a high voltage comparator followed by a debouncing unit.

BUS Input/Output

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with a diode This diode prevent the reverse current of V_{BUS} during differential voltage between VS and BUS (V_{BUS}>V_S).
No additional termination resistor is necessary to use the TH8082 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via a external 1kΩ resistor in serial with a diode to VBAT or INH (See chapter 4.4 Short circuit to ground).

TxD Input

During transmission the data at the pin TxD will be transferred to the BUS driver for generating a BUS signal. To minimize the electromagnetic emission of the bus line, the BUS driver is equipped with an integrated slew rate control and wave shaping unit.
Transmitting will be interrupted in the following cases:

- Sleep mode
- Thermal Shutdown active
- V_{BAT} standby

The CMOS compatible input TxD controls directly the BUS level:

TxD = low	->	BUS = low (dominant level)
TxD = high	->	BUS = high (recessive level)

The TxD pin has an internal pull up resistor connected to VCC. This secures that an open TxD pin generates a recessive BUS level.

RxD Output

The data signals from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit.

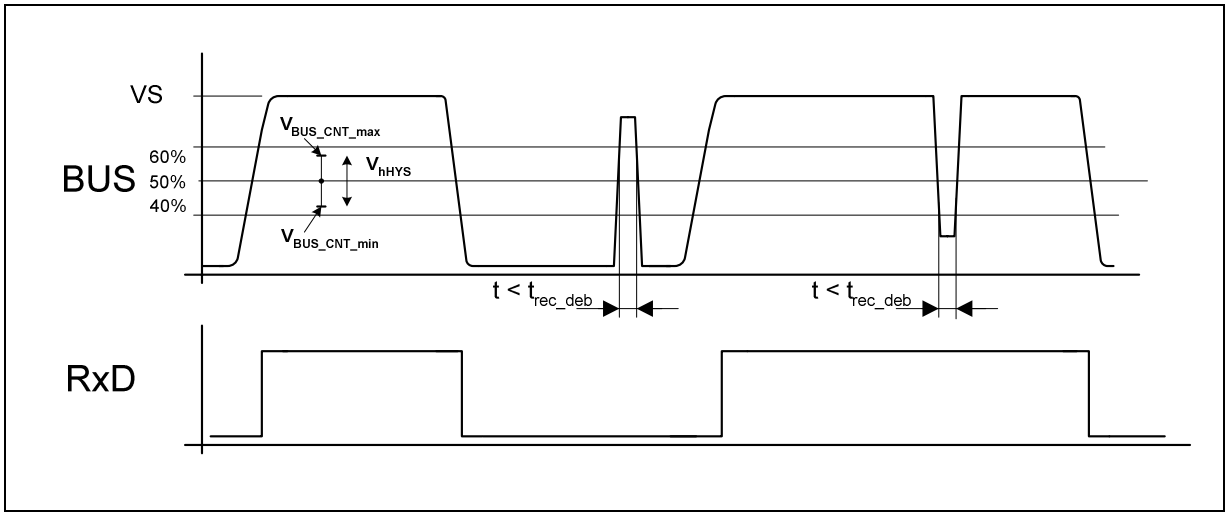


Figure 7 - Receive impulse diagram

The receive threshold values $V_{BUS\_CNT\_max}$ and $V_{BUS\_CNT\_min}$ are symmetrical to the centre voltage of $0.5*V_S$ with a hysteresis of typ. $0.175*V_S$. Including all tolerances the LIN specific receive threshold values of $0.4*V_S$ and $0.6*V_S$ will be secure observed.

The received BUS signal will be output to the RxD pin:

BUS < $V_{BUS\_CNT} - 0.5 * V_{HYS}$	->	RxD = low (BUS dominant)
BUS > $V_{BUS\_CNT} + 0.5 * V_{HYS}$	->	RxD = high, floating (BUS recessive)

This pin is a buffered open drain output with a typical load of:
Resistance: 2.7 kOhm
Capacitance: < 25 pF

EN-Pin

The TH8082 is switched into the sleep mode with a falling edge and into normal mode with a rising edge at the EN pin. The normal mode will be kept as long as EN = high (See Figure 4 – Sleep mode and wake up procedure for more details).
If the TH8082 is switched to sleep mode also a connected voltage regulator via the INH pin is switched off.
The deactivation of TH8082 with EN = low can be done independent from the state of the bus-transceiver.
The EN input is internal pulled down so that it is secured if this pin is not connected a low level will be applied.

Datarate

The TH8082 is a ***constant slew rate*** transceiver that means the bus driver operates with a fixed slew rate range of 1.0 V/µs ≤ $\Delta V/\Delta T$ ≤ 3V/µs. This principle secures a very good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}).
The TH8082 guarantees data rates up to 20kbit within the complete bus load range under worst case conditions. The constant slew rate principle is very robust against voltage drops and can operate with RC-oscillator systems with a clock tolerance up to ±2% between 2 nodes.

4. Operating under Disturbance

4.1 Loss of battery

If the ECU is disconnected from the battery, the bus pin is in high impedance state. There is no impact to the bus traffic and to the ECU itself.

4.2 Loss of Ground

In case of an interrupted ECU ground connection there is no influence to the bus line.

4.3 Short circuit to battery

The transmitter output current is limited to the specified value in case of short circuit to battery in order to protect the TH8082 itself against high current densities .

4.4 Short circuit to ground

If the bus line is shorted to negative shifted ground levels, there is no current flow from the ECU ground to the bus and no distortion of the bus traffic occurs.
The permanent failure current from battery to ground can be reduced dramatically by using the INH pin as termination pin for the master pull up (See Figure 9 - Application Circuitry).
If the controller detects a short circuit of the bus to ground (RxD timeout) the transceiver can be set into sleep mode. The INH pin is floating and in this case the master pull up resistor is disconnected from the bus line. Additionally the internal slave termination resistor is switched off and only a high impedance termination is applied to the bus (typ. 75µA). The failure current of the hole system can be reduced by at least ten times to prevent a fast discharge of the car battery. If the failure disappears, the bus level will become recessive again and will wake up the system even if no local wake up is present or possible.

4.5 Thermal overload

The TH8082 is protected against thermal overloads. If the chip temperature exceeds the specified value, the transmitter is switched off until thermal recovery. The receiver is still working while thermal shutdown.

4.6 Undervoltage Vcc

If the ECU regulated supply voltage is missing or decreases under the specified value, the transmitter is switched off to prevent undefined bus traffic.

5. Application Hints

5.1 LIN System Parameter

5.1.1. Bus loading requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating voltage range	V_{BAT}	8		18	V
Voltage drop of reverse protection diode	V_{Drop_rev}	0.4	0.7	1	V
Voltage drop at the serial diode in pull up path	$V_{SerDiode}$	0.4	0.7	1	V
Battery shift voltage	V_{Shift_BAT}	0		0.1	V_{BAT}
Ground shift voltage	V_{Shift_GND}	0		0.1	V_{BAT}
Master termination resistor	R_{master}	900	1000	1100	Ω
Slave termination resistor	R_{slave}	20	30	60	kΩ
Number of system nodes	N	2		16	
Total length of bus line	LEN_{BUS}			40	m
Line capacitance	C_{LINE}		100	150	pF/m
Capacitance of master node	C_{Master}		220		pF
Capacitance of slave node	C_{Slave}		220	250	pF
Total capacitance of the bus including slave and master capacitance	C_{BUS}	0.47	4	10	nF
Network Total Resistance	$R_{Network}$	500		862	Ω
Time constant of overall system	τ	1		5	µs

Table 2 - Bus loading requirements

5.1.2. Recommendations for system design

The goal of the LIN physical layer standard is to be universal valid definition of the LIN system for plug &play solutions in LIN networks up to 20kbd bus speed.
In case of small and medium LIN networks no problems occurring. It's recommended to adjust the total network capacitance to at least 4nF for good EMC and EMI behavior. This can be done by adapting only the master node capacitance. The slave node capacitance should have a unit load of typically 220pF for good EMC/EMI behavior.
In large networks with long bus lines and the maximum number of nodes some system parameters can exceed the defined limits and an intervention of the LIN system designer is required.
The whole capacitance of a slave node is not only the unit load capacitor itself. Additionally there is a capacitance of wires and connectors and the internal capacitance of the LIN transmitter. This internal capacitance is strongly dependent from the technology of the IC manufacturer and should be in the range of 30 to 150pF. If the bus lines have a total length of nearly 40m, the total bus capacitance can exceed 10nF.
A second reason for exceeding these limits is the tolerance of the integrated slave termination resistor. If most of the slave nodes have a slave termination resistance near by the allowed maximum of 60kΩ, the total

network resistance is more than 700Ω. Even if the total network capacitance is below or equal to the maximum specified value of 10nF, the network time constant is higher than 7µs!
This problem can be removed only by adapting the master termination resistor to realize the required maximum network time constant of 5µs.
The LIN output driver of the TH8082 provides a higher driving capability than necessary within the LIN standard (40mA @ 1.2V). With this driver stage the system designer have more degrees of freedom in case of maximum LIN networks with a total network capacitance of more than 10nF. The total network resistance can be decreased to:

$$R_{tl\_min} = (V_{Bat\_max} - V_{BUSdom}) / I_{BUS\_max} = (18V - 1.2V) / 40mA = 420\Omega$$

Note:
The adaptation of the network time constant is necessary in large networks (Master resistance)and also in small networks (master capacitance).
The intervention in the LIN network has only to be done in the master ECU! The limits of the system have to be known by the system designer and shouldn't have any influence to the LIN physical layer.

The TH8082 meets the requirements for implementation in RC-based slave nodes (oscillator tolerance <2% at baudrate 20Kbit/s)under all worst case conditions in V_{BAT}- or ground shift, operating voltage and load conditions, and independent from the method of reverse polarity protection .

5.2 Min/max slope time calculation

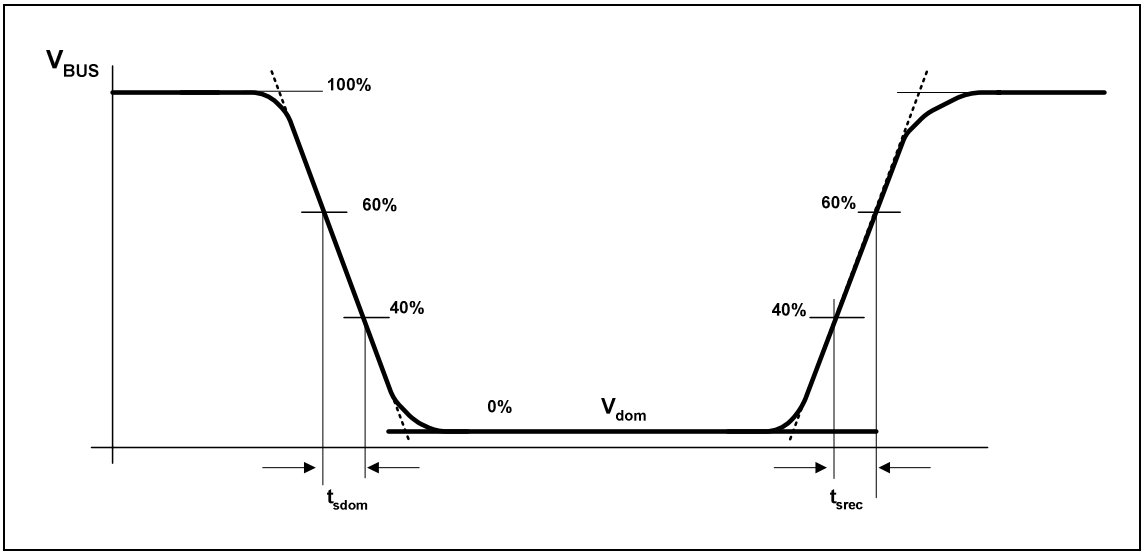


Figure 8 - Slope time calculation

The slew rate of the bus voltage is measured between 40% and 60% of the output voltage swing (linear region). The output voltage swing is the difference between dominant and recessive bus voltage.

$$dV/dt = 0.2*V_{swing} / (t_{40\%} - t_{60\%})$$

The slope time is the extension of the slew rate tangent until the upper and lower voltage swing limits:

$$t_{slope} = 5 * (t_{40\%} - t_{60\%})$$

The slope time of the recessive to dominant edge is directly determined by the slew rate control of the transmitter:

$$t_{slope} = V_{swing} / dV/dt$$

The dominant to recessive edge is influenced from the network time constant and the slew rate control, because it's a passive edge. In case of low battery voltages and high bus loads the rising edge is only determined by the network. If the rising edge slew rate exceeds the value of the dominant one, the slew rate control determines the rising edge.

5.3 Application Circuitry

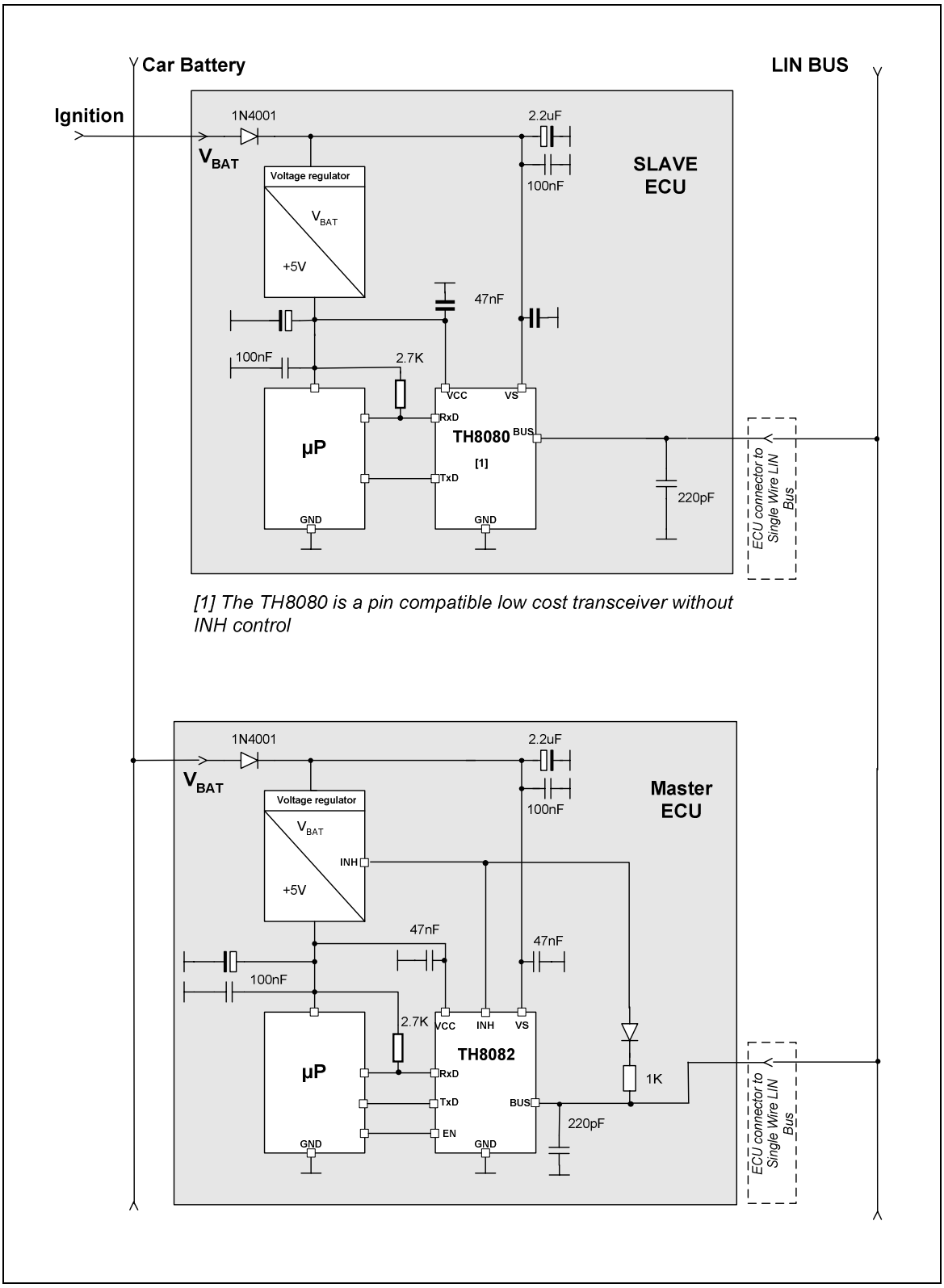


Figure 9 - Application Circuitry

6. Pin Description

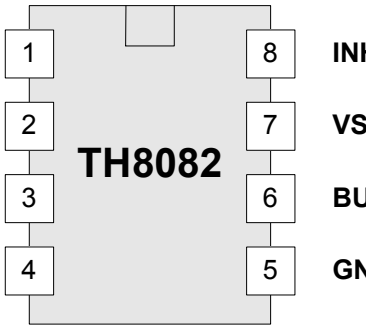
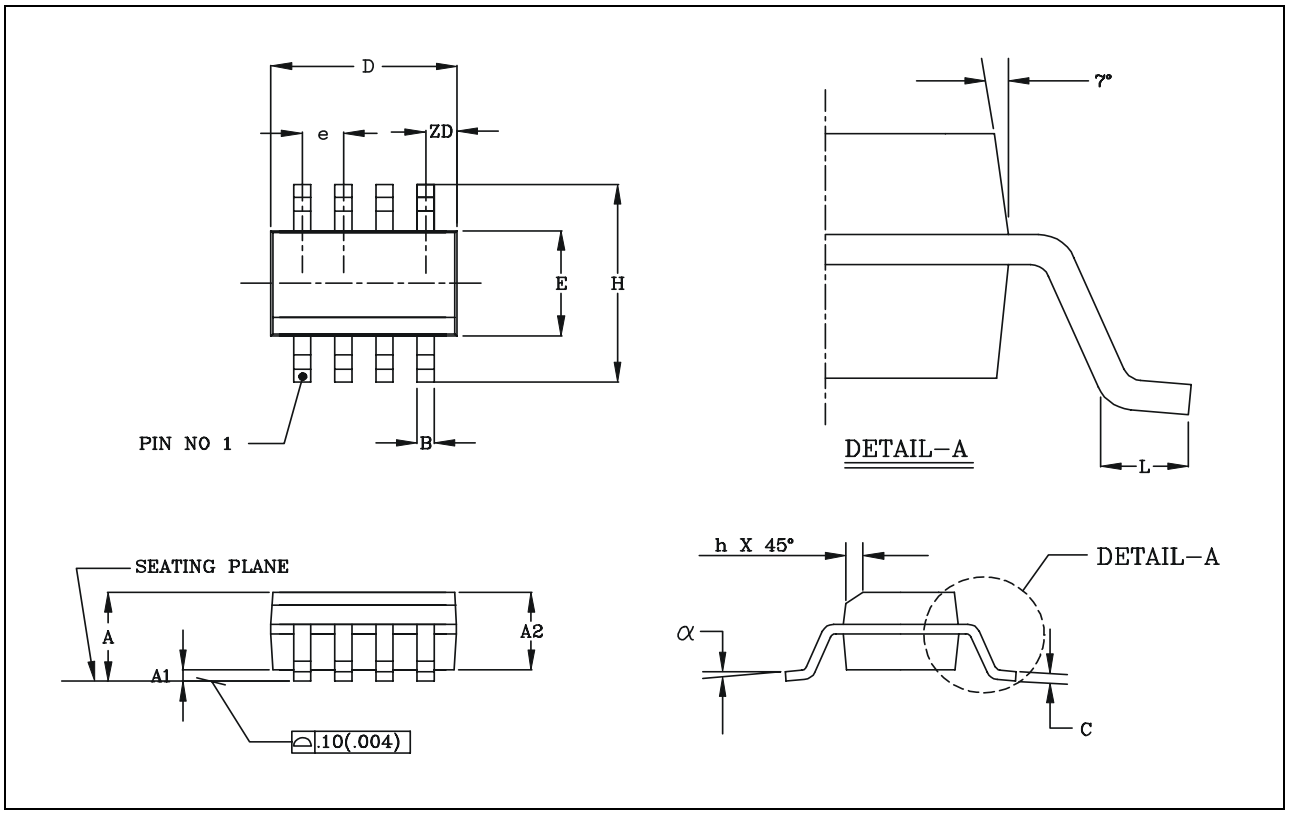


Figure 10 - Pin description SOIC8 package

Pin	Name	IO-Typ	Description
1	RXD	O	Receive data from BUS to core, LOW in dominant state
2	EN	I	Enables the normal operation mode when HIGH
3	VCC	P	5V supply input
4	TXD	I	Transmit data from core to BUS, LOW in dominant state
5	GND	G	Ground
6	BUS	I/O	LIN bus pin, LOW in dominant state
7	VS	P	Battery input voltage
8	INH	O	Control output for voltage regulator, termination pin for master pull up

7. Mechanical Specification SOIC8



Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

	A1	B	C	D	E	e	H	h	L	A	α	ZD	A2
All Dimension in mm, coplanarity < 0.1 mm													
min	0.10	0.36	0.19	4.80	3.81	1.27	5.80	0.25	0.41	1.52	0°	0.53	1.37
max	0.25	0.46	0.25	4.98	3.99		6.20	0.50	1.27	1.72	8°		1.57
All Dimension in inch, coplanarity < 0.004”													
min	0.004	0.014	0.0075	0.189	0.150	0.050	0.2284	0.0099	0.016	0.060	0°	0.021	0.054
max	0.0098	0.018	0.0098	0.196	0.157		0.244	0.0198	0.050	0.068	8°		0.062

8. ESD/EMC Remarks

8.1 General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

8.2 ESD-Test

The TH8082 is tested according MIL883D (human body model).

8.3 EMC

The test on EMC impacts is done according to ISO 7637-1 for power supply pins and ISO 7637-3 for data- and signal pins.

Power Supply pin VS:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	5000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	5000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms / U_P+U_S = 40 V	10 pulses every 1min

Data- and signal pins EN, BUS:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	1000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	1000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1000 burst

9. Reliability Information

Melexis devices are classified and qualified regarding suitability for infrared, vapor phase and wave soldering with usual (63/37 SnPb-) solder (melting point at 183degC).
The following test methods are applied:

- IPC/JEDEC J-STD-020A (issue April 1999)
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
- CECC00802 (issue 1994)
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- MIL 883 Method 2003 / JEDEC-STD-22 Test Method B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

For more information on manufacturability/solderability see quality page at our website: http://www.melexis.com/

10. Disclaimer

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