19-1711; Rev 1; 1/01

MAXIM

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

General Description

The MAX5270 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). On-chip precision output amplifiers provide the voltage outputs. The device operates from +12V/-12V supplies. Its output voltage swing ranges from 0V to +8.192V and is achieved with no external components. The MAX5270 has three pairs of differential reference inputs; two of these pairs are connected to two DACs each, and a third pair is connected to four DACs. The references are independently controlled, providing different full-scale output voltages to the respective DACs. The MAX5270 operates within the following voltage ranges: V_{DD} = +11.4V to +12.6V, V_{SS} = -11.4V to -12.6V, and V_{CC} = +4.75V to +5.25V.

The MAX5270 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single-write instruction. An asynchronous load input ($\overline{LD}$) transfers data from the input latch to the DAC latch. The $\overline{LD}$ input controls all DACs; therefore, all DACs can be updated simultaneously by asserting the $\overline{LD}$ pin.

An asynchronous $\overline{CLR}$ input sets the output of all eight DACs to the respective DUTGND input of the op amp. Note that $\overline{CLR}$ is a CMOS input, which is powered by V_{DD}. All other logic inputs are TTL/CMOS compatible.

The "A" grade of the MAX5270 has a maximum INL of ±2LSBs, while the "B" grade has a maximum INL of ±4LSBs. Both grades are available in 44-pin MQFP packages.

Applications

Industrial Process Controls

Arbitrary Function Generators

Avionics Equipment

Minimum Component Count Analog Systems

Digital Offset/Gain Adjustment

SONET Applications

Automatic Test Equipment (ATE)

Functional Diagram appears at end of data sheet.

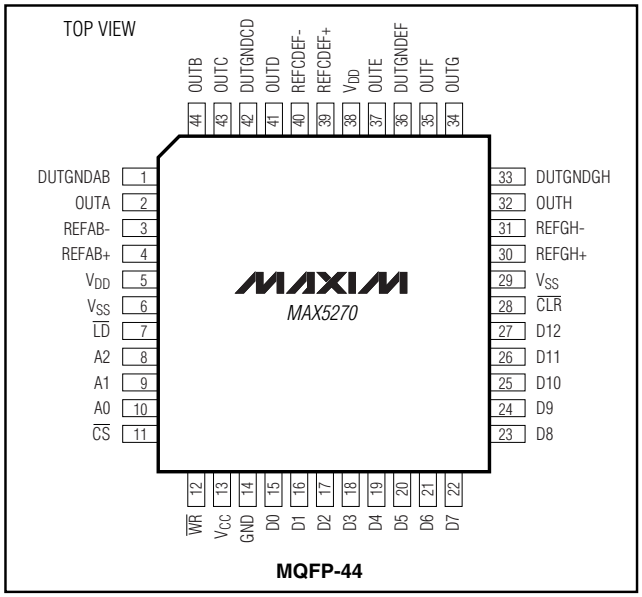
Features

- ♦ **Full 13-Bit Performance Without Adjustments**
- ♦ **Eight DACs in a Single Package**
- ♦ **Buffered Voltage Outputs**
- ♦ **Voltage Swing Between 0 and +8.192V**
- ♦ **22µs Output Settling Time**
- ♦ **Drives up to 10,000pF Capacitive Load**
- ♦ **30mV Low Output Glitch**
- ♦ **Low Power Consumption: 10mA (typ)**
- ♦ **Small 44-Pin MQFP Package**
- ♦ **Double-Buffered Digital Inputs**
- ♦ **Asynchronous Load Updates All DACs Simultaneously**
- ♦ **Asynchronous $\overline{CLR}$ Forces All DACs to DUTGND Potential**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5270ACMH	0°C to +70°C	44 MQFP	±2
MAX5270BCMH	0°C to +70°C	44 MQFP	±4
MAX5270AEMH	-40°C to +85°C	44 MQFP	±2
MAX5270BEMH	-40°C to +85°C	44 MQFP	±4

Pin Configuration



MQFP-44

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +13.2V
V_{SS} to GND ..... -13.2V to +0.3V
V_{CC} to GND ..... -0.3V to +6V
A_, D_, $\overline{WR}$, $\overline{CS}$, $\overline{LD}$, $\overline{CLR}$ to GND.....+0.3V to (V_{CC} + 0.3V)
REF_ _ _ _+, DUTGND_ _ .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
OUT_ .....V_{DD} to V_{SS}
Maximum Current into REF_ _ _ _ _, DUTGND_ _ .....±10mA
Maximum Current into Any Signal Pin ..... ±50mA
OUT_ Short-Circuit Duration to V_{DD}, V_{SS}, and GND 1s

Continuous Power Dissipation (T_A = +70°C)
44-Pin MQFP (derate 11.1mW/°C above +70°C)..... 870mW
Operating Temperature Ranges
MAX5270_CMH ..... 0°C to +70°C
MAX5270_EMH..... -40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +12V, V_{SS} = -12V, V_{CC} = +5V, V_{GND} = $V_{DUTGND\_\ \_}$ = 0, $V_{REF\_\ \_\ \_\ \_+}$ = +4.096V, $V_{REF\_\ \_\ \_\ \_-}$ = 0, R_L = 10MΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (ANALOG SECTION)						
Resolution	N		13			Bits
Relative Accuracy	INL	MAX5270A			±2	LSB
		MAX5270B			±4	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Zero-Scale Error	ZSE			±2	±4	LSB
Full-Scale Error	FSE			±4	±8	LSB
Gain Error				±2	±5	LSB
Gain Temperature Coefficient		(Note 1)		0.15	20	ppm FSR/°C
DC Crosstalk		(Note 1)		14	75	µV
REFERENCE INPUTS						
Input Resistance			1			MΩ
Input Current				±1	±10	µA
REF_ _ _ _+ Input			2		4.5	V
REF_ _ _ _- Input		REF_ _ _ _- tied to AGND externally		0		V
(REF_ _ _ _+) - (REF_ _ _ _-) Range			2		4.5	V
ANALOG OUTPUTS						
Maximum Output Voltage			9	V_{DD} - 2		V
Minimum Output Voltage				0		V
Resistive Load to GND			5			kΩ
Capacitive Load to GND		(Note 2)			10,000	pF
DC Output Impedance		(Note 1)			0.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +12V, V_{SS} = -12V, V_{CC} = +5V, V_{GND} = $V_{DUTGND\_\_}$ = 0, $V_{REF\_\_\_\_+}$ = +4.096V, $V_{REF\_\_\_\_-}$ = 0, R_L = 10MΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DUTGND_ _ CHARACTERISTICS						
Input Impedance per DAC			40	84		kΩ
Input Current per DAC		(Note 1)	-165		100	µA
Input Range			-2		2	V
DIGITAL INPUTS						
Input Voltage High	V_{IH}		2.4			V
Input Voltage Low	V_{IL}				0.8	V
Input Capacitance	C_{IN}	(Note 1)			10	pF
Input Current	I_{IN}	V_{IN} = 0 or V_{CC}	-1		1	µA
POWER SUPPLIES						
V_{DD} Analog Power Supply Range	V_{DD}		11.4		12.6	V
V_{SS} Analog Power Supply Range	V_{SS}		-11.4		-12.6	V
Digital Power Supply	V_{CC}		4.75	5	5.25	V
Positive Supply Current	I_{DD}	(Note 3)		10	13	mA
Negative Supply Current	I_{SS}	(Note 4)		10	13	mA
Digital Supply Current	I_{CC}	(Note 3)			0.5	mA
		(Note 4)			5	
PSRR, ΔV_{OUT} / ΔV_{DD}		V_{DD} = 14V ±5%		94		dB
PSRR, ΔV_{OUT} / ΔV_{SS}		V_{SS} = -9V ±5%		98		dB

INTERFACE TIMING CHARACTERISTICS

(V_{DD} = +12V, V_{SS} = -12V, V_{CC} = +5V, V_{GND} = $V_{DUTGND\_\_}$ = 0, $V_{REF\_\_\_\_+}$ = +4.096V, $V_{REF\_\_\_\_-}$ = 0, R_L =10MΩ, C_L = 50pF, Figure 2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width Low	t_1		50			ns
$\overline{WR}$ Pulse Width Low	t_2		50			ns
$\overline{LD}$ Pulse Width Low	t_3		50			ns
$\overline{CS}$ Low to $\overline{WR}$ Low	t_4		0			ns
$\overline{CS}$ High to $\overline{WR}$ High	t_5		0			ns
Data Valid to $\overline{WR}$ Setup	t_6		50			ns
Data Valid to $\overline{WR}$ Hold	t_7		0			ns
Address Valid to $\overline{WR}$ Setup	t_8		15			ns
Address Valid to $\overline{WR}$ Hold	t_9		0			ns

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

DYNAMIC CHARACTERISTICS

(V_{DD} = +12V, V_{SS} = -12V, V_{CC} = +5V, V_{GND} = $V_{DUTGND\_\_}$ = 0, $V_{REF\_\_\_\_+}$ = +4.096V, $V_{REF\_\_\_\_-}$ = 0, R_L = 10MΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

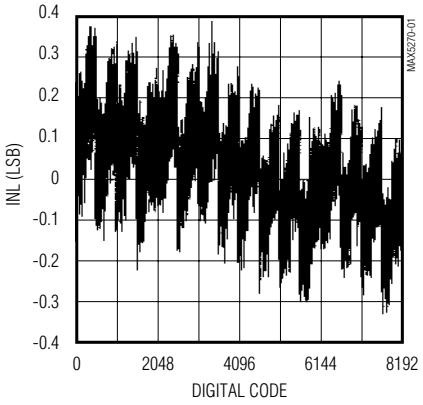
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Settling Time		To ±1/2LSB of full scale		22		µs
Output Slew-Rate				1		V/µs
Digital Feedthrough		(Note 5)		3		nV/s
Digital Crosstalk		(Note 6)		3		nV/s
Digital-to-Analog Glitch Impulse				120		nV/s
DAC-to-DAC Crosstalk				3		nV/s
Channel-to-Channel Isolation				100		dB
Output Noise Spectral Density		At f = 1kHz		120		nV/√Hz

Note 1: Guaranteed by design. Not production tested.
Note 2: Guaranteed by design when 220Ω resistor is in series with C_L = 10,000pF.
Note 3: All digital inputs (D_, A_, $\overline{WR}$, $\overline{CS}$, $\overline{LD}$, and $\overline{CLR}$) at GND or V_{CC} potential.
Note 4: All digital inputs (D_, A_, $\overline{WR}$, $\overline{CS}$, $\overline{LD}$, and $\overline{CLR}$) at +0.8V or +2.4V.
Note 5: All data inputs (D0 to D12) transition from GND to V_{CC}, with $\overline{WR}$ = V_{CC}.
Note 6: All digital inputs (D_, A_, $\overline{WR}$, $\overline{CS}$, $\overline{LD}$, and $\overline{CLR}$) at +0.8V or +2.4V.

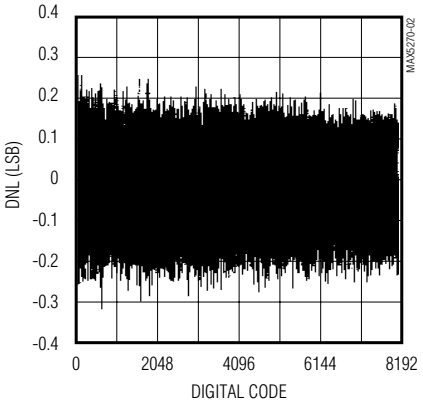
Typical Operating Characteristics

(V_{DD} = +12V, V_{SS} = -12V, V_{CC} = +5V, V_{GND} = $V_{DUTGND\_\_}$ = 0, $V_{REF\_\_\_\_+}$ = +4.096V, $V_{REF\_\_\_\_-}$ = 0, T_A = +25°C, unless otherwise noted.)

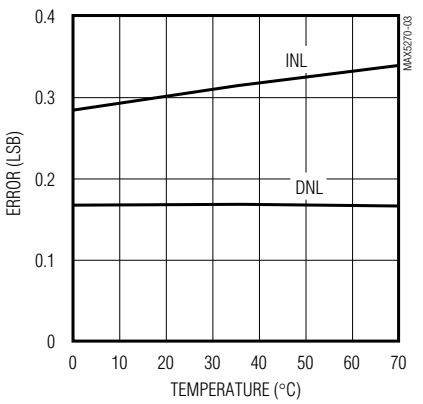
INTEGRAL NONLINEARITY vs. DIGITAL CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



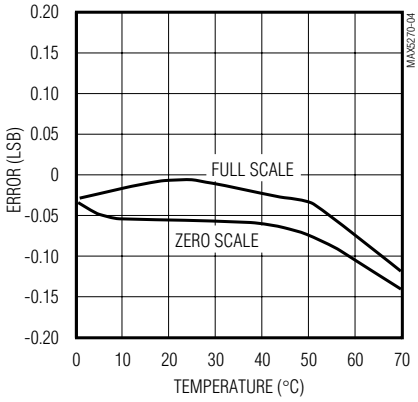
INL AND DNL ERROR vs. TEMPERATURE



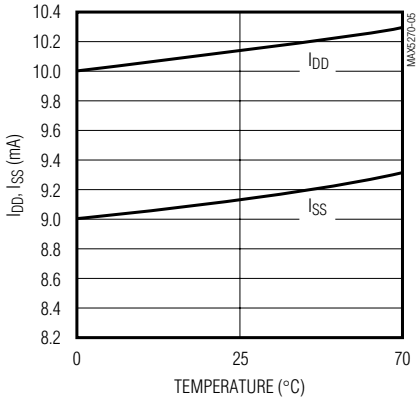
Typical Operating Characteristics (continued)

(V_{DD} = +12V, V_{SS} = -12V, V_{CC} = +5V, V_{GND} = $V_{DUTGND\_\_}$ = 0, $V_{REF\_\_\_\_+}$ = +4.096V, $V_{REF\_\_\_\_-}$ = 0, T_A = +25°C, unless otherwise noted.)

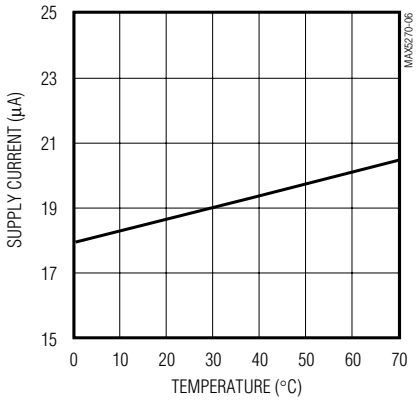
ZERO-SCALE AND FULL-SCALE ERROR vs. TEMPERATURE



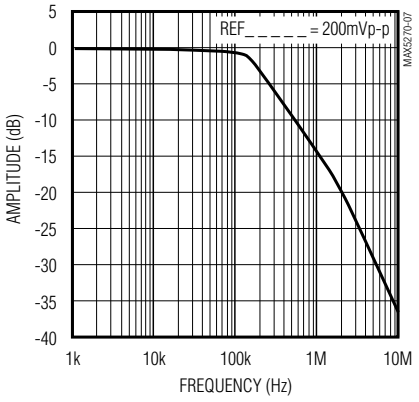
I_{DD} AND I_{SS} vs. TEMPERATURE (UNLOADED)



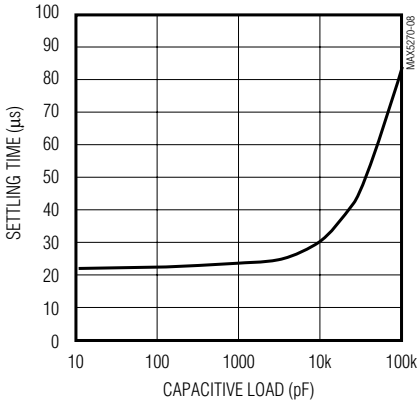
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



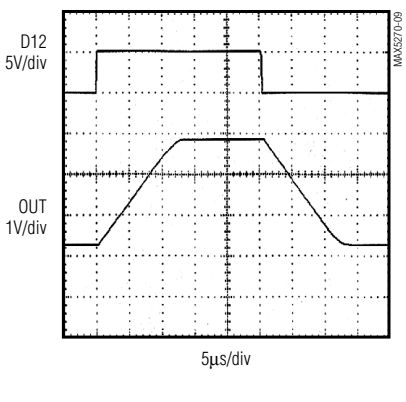
REFERENCE INPUT FREQUENCY RESPONSE



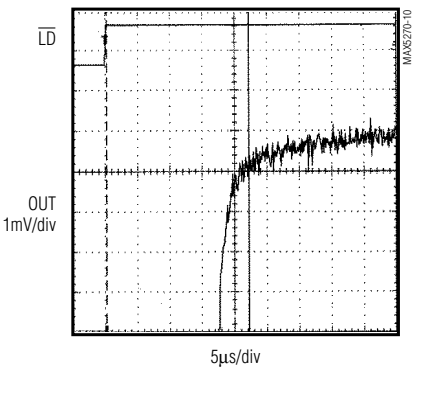
SETTLING TIME vs. CAPACITIVE LOAD



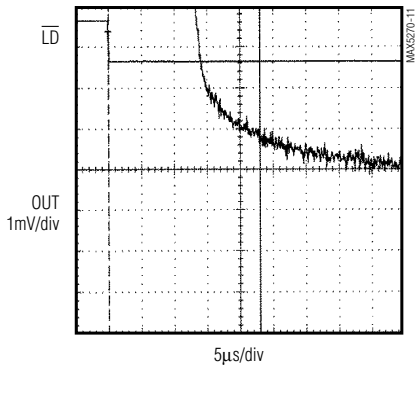
LARGE-SIGNAL STEP RESPONSE



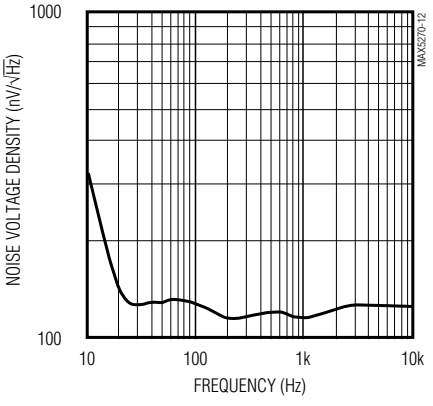
POSITIVE SETTLING TIME



NEGATIVE SETTLING TIME



NOISE VOLTAGE DENSITY vs. FREQUENCY

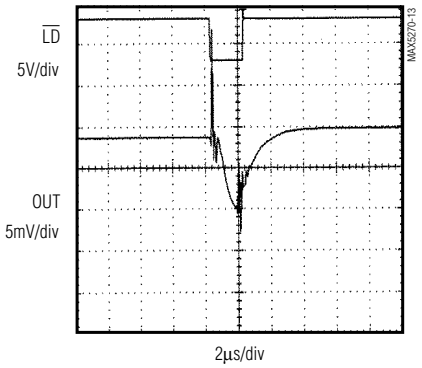


Octal, 13-Bit Voltage-Output DAC with Parallel Interface

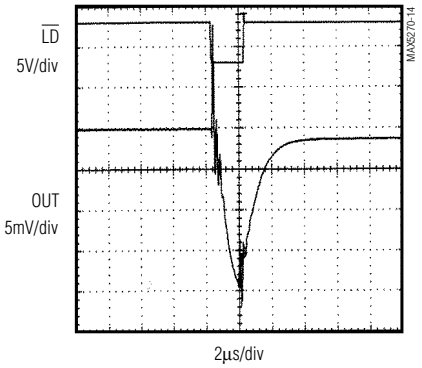
Typical Operating Characteristics (continued)

(V_{DD} = +12V, V_{SS} = -12V, V_{CC} = +5V, V_{GND} = $V_{DUTGND\_\_}$ = 0, $V_{REF\_\_\_\_+}$ = +4.096V, $V_{REF\_\_\_\_-}$ = 0, T_A = +25°C, unless otherwise noted.)

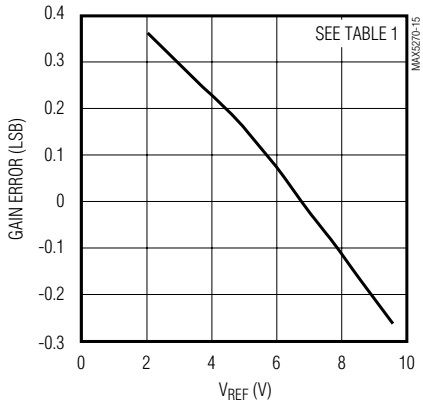
MAJOR CARRY GLITCH IMPULSE (0xFFFF–0x10000)



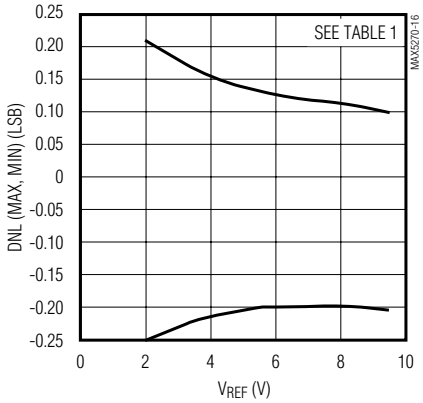
MAJOR CARRY GLITCH IMPULSE (0x1000–0xFFF)



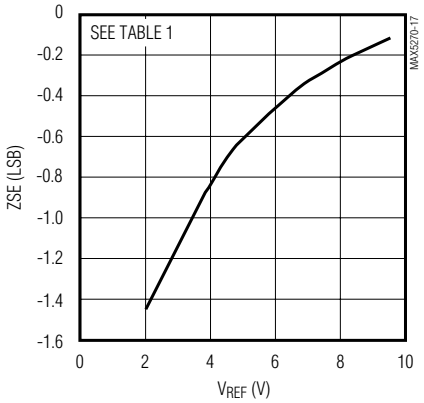
GAIN ERROR vs. V_{REF} (V_{REF+} - V_{REF-})



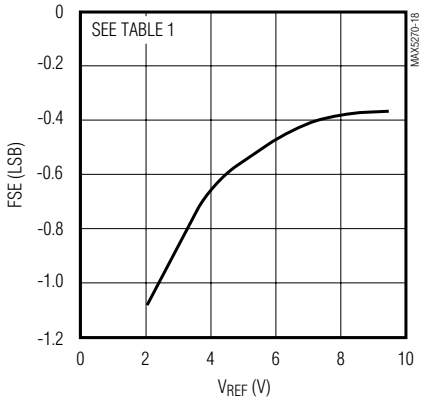
DIFFERENTIAL NONLINEARITY (MAX, MIN) vs. V_{REF} (V_{REF+} - V_{REF-})



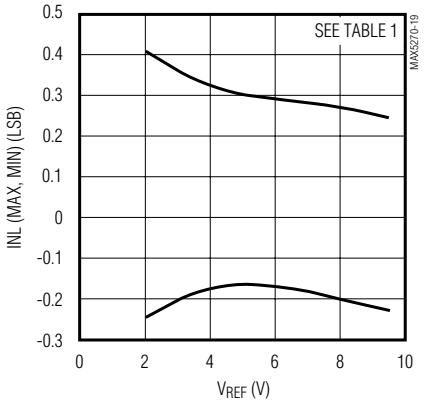
ZERO-SCALE ERROR vs. V_{REF} (V_{REF+} - V_{REF-})



FULL-SCALE ERROR vs. V_{REF} (V_{REF+} - V_{REF-})



INTEGRAL NONLINEARITY (MAX, MIN) vs. V_{REF} (V_{REF+} - V_{REF-})



Pin Description

PIN	NAME	FUNCTION
1	DUTGNDAB	Device Sense Ground Input for OUTA and OUTB. In normal operation, OUTA and OUTB are referenced to DUTGNDAB. When $\overline{CLR}$ is low, OUTA and OUTB are forced to the potential on DUTGNDAB.
2	OUTA	DAC A Buffered Output Voltage
3	REFAB-	Negative Reference Input for DACs A and B. It is externally tied to AGND.
4	REFAB+	Positive Reference Input for DACs A and B
5, 38	V_{DD}	Positive Analog Power Supply. Normally set to +14V. Connect both pins to the supply voltage. See *Grounding and Bypassing* section for bypass requirements.
6, 29	V_{SS}	Negative Analog Power Supply. Normally set to -9V. Connect both pins to the supply voltage. See *Grounding and Bypassing* section for bypass requirements.
7	$\overline{LD}$	Load Input. Drive this asynchronous input low to transfer the contents of the input latches to their respective DAC latches. DAC latches are transparent when $\overline{LD}$ is low and latched when $\overline{LD}$ is high.
8	A2	Address Bit 2 (MSB)
9	A1	Address Bit 1
10	A0	Address Bit 0 (LSB)
11	$\overline{CS}$	Chip Select. Active-low input.
12	$\overline{WR}$	Write Input. Active-low strobe for conventional memory write sequence. Input data latches are transparent when $\overline{WR}$ and $\overline{CS}$ are both low. $\overline{WR}$ latches data into the DAC input latch selected by A2, A1, and A0 on the rising edge of $\overline{CS}$.
13	V_{CC}	Digital Power Supply. Normally set to +5V. See *Grounding and Bypassing* section for bypass requirements.
14	GND	Ground
15–27	D0–D12	Data Bits 0–12. Offset binary coding.
28	$\overline{CLR}$	Clear Input. Drive $\overline{CLR}$ low to force all DAC outputs to the voltage on their respective DUTGND _ _. Does not affect the status of internal registers. All DACs return to their previous levels when $\overline{CLR}$ goes high.
30	REFGH+	Positive Reference Input for DACs G and H
31	REFGH-	Negative Reference Input for DACs G and H. It is externally tied to AGND.

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Pin Description (continued)

PIN	NAME	FUNCTION
32	OUTH	DAC H Buffered Output Voltage
33	DUTGNDGH	Device Sense Ground Input for OUTG and OUTH. In normal operation, OUTG and OUTH are referenced to DUTGNDGH. When $\overline{CLR}$ is low, OUTG and OUTH are forced to the potential on DUTGNDGH.
34	OUTG	DAC G Buffered Output Voltage
35	OUTF	DAC F Buffered Output Voltage
36	DUTGNDEF	Device Sense Ground Input for OUTE and OUTF. In normal operation, OUTE and OUTF are referenced to DUTGNDEF. When $\overline{CLR}$ is low, OUTE and OUTF are forced to the potential on DUTGNDEF.
37	OUTE	DAC E Buffered Output Voltage
39	REFCDEF+	Positive Reference Input for DACs C, D, E, and F
40	REFCDEF-	Negative Reference Input for DACs C, D, E, and F. It is externally tied to AGND.
41	OUTD	DAC D Buffered Output Voltage
42	DUTGNDCD	Device Sense Ground Input for OUTC and OUTD. In normal operation, OUTC and OUTD are referenced to DUTGNDCD. When $\overline{CLR}$ is low, OUTC and OUTD are forced to the potential on DUTGNDCD.
43	OUTC	DAC C Buffered Output Voltage
44	OUTB	DAC B Buffered Output Voltage

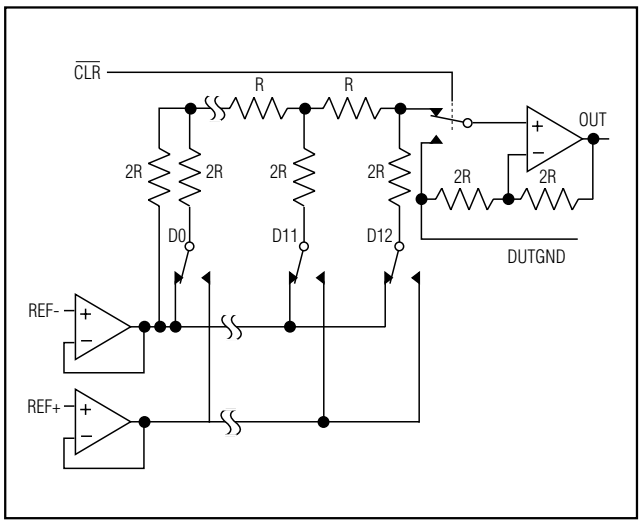
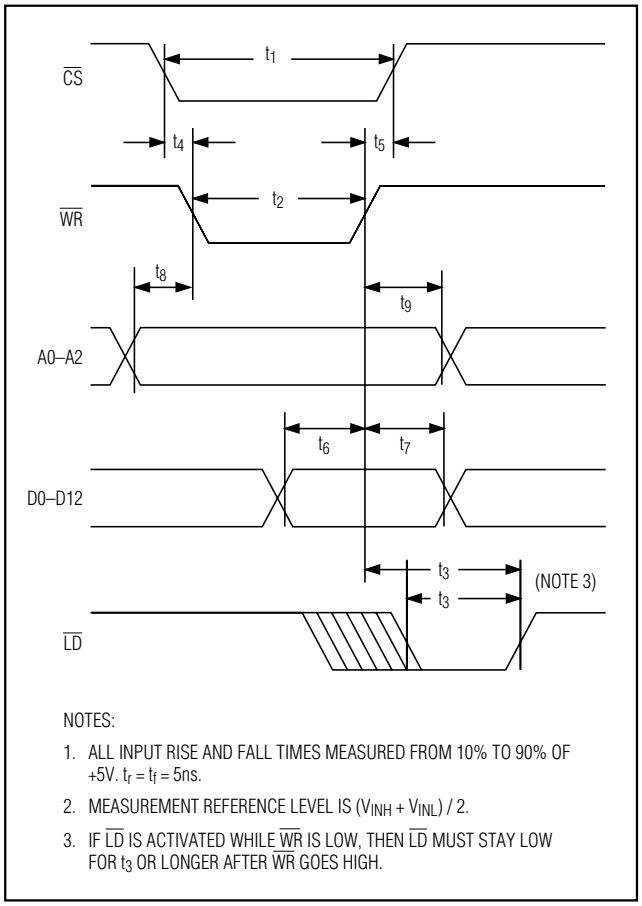


Figure 1. DAC Simplified Circuit



NOTES:

1. ALL INPUT RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 5ns$.
2. MEASUREMENT REFERENCE LEVEL IS $(V_{INH} + V_{INL}) / 2$.
3. IF $\overline{LD}$ IS ACTIVATED WHILE $\overline{WR}$ IS LOW, THEN $\overline{LD}$ MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 2. Digital Timing Diagram

Detailed Description

Analog Section

The MAX5270 contains eight 13-bit voltage-output DACs. These DACs are "inverted" R-2R ladder networks that convert 13-bit digital inputs into equivalent analog output voltages, in proportion to the applied reference voltages (Figure 1). The MAX5270 has three positive reference inputs (REF_ _ _ _+) and three negative reference inputs (REF_ _ _ _-). The difference from REF_ _ _ _+ to REF_ _ _ _- , multiplied by 2, sets the DAC output span.

In addition to the differential reference inputs, the MAX5270 has four analog-ground input pins (DUTGND_ _). When $\overline{CLR}$ is high (unasserted), the voltage on DUTGND_ _ offsets the DAC output voltage range. If $\overline{CLR}$ is asserted, the output amplifier is forced to the voltage present on DUTGND_ _.

Reference and DUTGND Inputs

All of the MAX5270's reference inputs are buffered with precision amplifiers. This allows the flexibility of using resistive dividers to set the reference voltages. Because of the relatively high multiplying bandwidth of the reference input (188kHz), any signal present on the reference pin within this bandwidth is replicated on the DAC output.

The DUTGND pins of the MAX5270 are connected to the negative source resistor (nominally 84kΩ) of the output amplifier. The DUTGND pins are typically connected directly to analog ground. Each of these pins has an input current that varies with the DAC digital code. If the DUTGND pins are driven by external circuitry, budget ±200µA per DAC for load current.

Output Buffer Amplifiers

The MAX5270's voltage outputs are internally buffered by precision gain-of-two amplifiers with a typical slew rate of 1V/µs. With a full-scale transition at its output, the typical settling time to $\pm 1/2$LSB is 22µs. This settling time does not significantly vary with capacitive loads less than 10,000pF.

Output Deglitching Circuit

The MAX5270's internal connection from the DAC ladder to the output amplifier contains special deglitch circuitry. This glitch/deglitch circuitry is enabled on the falling edge of $\overline{LD}$ to remove the glitch from the R-2R DAC. This enables the MAX5270 to exhibit a fraction of the glitch impulse energy of parts without the deglitching circuit.

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Digital Inputs and Interface Logic

All digital inputs are compatible with both TTL and CMOS logic. The MAX5270 interfaces with microprocessors using a data bus at least 13 bits wide. The interface is double buffered, allowing simultaneous updating of all DACs. There are two latches for each DAC (see *Functional Diagram*): an input latch that receives data from the data bus, and a DAC latch that receives data from the input latch. Address lines A0, A1, and A2 select which DAC's input latch receives data from the data bus, as shown in Table 1. Both the input latches and the DAC latches are transparent when $\overline{CS}$, $\overline{WR}$, and $\overline{LD}$ are all low. Any change of D0–D12 during this condition appears at the output instantly. Transfer data from the input latches to the DAC latches by asserting the asynchronous $\overline{LD}$ signal. Each DAC's analog output reflects the data held in its DAC latch. All control inputs are level triggered. Table 2 is an interface truth table.

Table 1. MAX5270 DAC Addressing

A2	A1	A0	FUNCTION
0	0	0	DAC A input latch
0	0	1	DAC B input latch
0	1	0	DAC C input latch
0	1	1	DAC D input latch
1	0	0	DAC E input latch
1	0	1	DAC F input latch
1	1	0	DAC G input latch
1	1	1	DAC H input latch

Table 2. Interface Truth Table

$\overline{CLR}$	$\overline{LD}$	$\overline{WR}$	$\overline{CS}$	FUNCTION
X	X	0	0	Input register transparent
X	X	X	1	Input register latched
X	X	1	X	Input register latched
X	0	X	X	DAC register transparent
X	1	X	X	DAC register latched
0	X	X	X	Outputs of DACs at DUTGND_ _
1	1	X	X	Outputs of DACs set to voltage defined by the DAC register, the references, and the corresponding DUTGND_ _

X = Don't care

Input Write Cycle

Data can be latched or transferred directly to the DAC. $\overline{CS}$ and $\overline{WR}$ control the input latch, and $\overline{LD}$ transfers information from the input latch to the DAC latch. The input latch is transparent when $\overline{CS}$ and $\overline{WR}$ are low, and the DAC latch is transparent when $\overline{LD}$ is low. The address lines (A0, A1, A2) must be valid for the duration that $\overline{CS}$ and $\overline{WR}$ are low (Figure 2) to prevent data from being inadvertently written to the wrong DAC. Data is latched within the input latch when either $\overline{CS}$ or $\overline{WR}$ is high.

Loading the DACs

Taking $\overline{LD}$ high latches data into the DAC latches. If $\overline{LD}$ is brought low when $\overline{WR}$ and $\overline{CS}$ are low, the DAC addressed by A0, A1, and A2 is directly controlled by the data on D0–D12. This allows the maximum digital update rate; however, it is sensitive to any glitches or skew in the input data stream.

Asynchronous Clear

The MAX5270 has an asynchronous clear pin ($\overline{CLR}$) that, when asserted, sets all DAC outputs to the voltage present on their respective DUTGND pins. Deassert $\overline{CLR}$ to return the DAC output to its previous voltage. Note that $\overline{CLR}$ does not clear any of the internal digital registers.

Applications Information

Multiplying Operation

The MAX5270 can be used for multiplying applications. Its reference accepts both DC and AC signals. Since the reference inputs are unipolar, multiplying operation is limited to two quadrants. See the graphs in the *Typical Operating Characteristics* section for dynamic performance of the DACs and output buffers.

Digital Code and Analog Output Voltage

The MAX5270 uses offset binary coding. A 13-bit two's complement code is converted to a 13-bit offset binary code by adding $2^{12} = 4096$.

Output Voltage Range

For typical operation, connect DUTGND to signal ground, V_{REF+} to +4.096V, and V_{REF-} to 0V. Table 3 shows the relationship between digital code and output voltage.

The DAC digital code controls each leg of the 13-bit R-2R ladder. A code of 0x0 connects all legs of the ladder to REF-, corresponding to a DAC output voltage (V_{DAC}) equal to REF-. A code of 0x1FFF connects all legs of the ladder to REF+, corresponding to a V_{DAC} approximately equal to REF+.

Table 3. Analog Voltage vs. Digital Code

INPUT CODE	OUTPUT VOLTAGE (V)
1 1111 1111 1111	+8.191
1 0000 0000 0000	+4.096
0 1111 1111 1111	+4.095
0 0000 0000 0001	+0.001
0 0000 0000 0000	0

Note: *Output voltage is based on REF+ = +4.096V, REF- = 0V, and DUTGND = 0.*

The output amplifier multiplies V_{DAC} by 2, yielding an output voltage range of 2 × REF- to 2 × REF+ (Figure 1). Further manipulation of the output voltage span is accomplished by offsetting DUTGND. The output voltage of the MAX5270 is described by the following equation:

$$V_{OUT} = 2\left[\left(V_{REF+} - V_{REF-}\right)\frac{DATA}{2^{13}} + V_{REF-}\right] - V_{OUTGND}$$

where DATA is the numeric value of the DAC's binary input code, and DATA ranges from 0 (2^0) to 8191 (2^{13} - 1). The resolution of the MAX5270, defined as 1LSB, is described by the following equation:

$$LSB = \frac{2\left(REF+ - REF-\right)}{2^{13}}$$

Reference Selection

Since the MAX5270 has precision buffers on its reference inputs, the requirements for interfacing to these inputs are minimal. Select a low-drift, low-noise reference within the recommended REF+ and REF- voltage ranges. The MAX5270 does not require bypass capacitors on its reference inputs. Add capacitors only if the reference voltage source requires them to meet system specifications.

Minimizing Output Glitch

The MAX5270's internal deglitch circuitry is enabled on the falling edge of $\overline{LD}$. Therefore, to achieve optimum performance, drive $\overline{LD}$ low after the inputs are either latched or steady state. This is best accomplished by having the falling edge of $\overline{LD}$ occur at least 50ns after the rising edge of $\overline{CS}$.

Power Supplies, Grounding, and Bypassing

For optimum performance, use a multilayer PC board with an unbroken analog ground. For normal operation, connect the four DUTGND pins directly to the ground plane. Avoid sharing the connections of these sensitive pins with other ground traces.

As with any sensitive data-acquisition system, connect the digital and analog ground planes together at a single point, preferably directly underneath the MAX5270. Avoid routing digital signals underneath the MAX5270 to minimize their coupling into the IC.

For normal operation, bypass V_{DD} and V_{SS} with 0.1µF ceramic chip capacitors to the analog ground plane. To enhance transient response and capacitive drive capability, add 10µF tantalum capacitors in parallel with the ceramic capacitors. Note, however, that the MAX5270 does not require the additional capacitance for stability. Bypass V_{CC} with a 0.1µF ceramic chip capacitor to the digital ground plane.

Power-Supply Sequencing

To guarantee proper operation of the MAX5270, ensure that power is applied to V_{DD} before V_{SS} and V_{CC}. Also ensure that V_{SS} is never more than 300mV above ground. To prevent this situation, connect a Schottky diode between V_{SS} and the analog ground plane, as shown in Figure 3. Do not power-up the logic input pins before establishing the supply voltages. If this is not possible and the digital lines can drive more than 10mA, place current-limiting resistors (e.g., 470Ω) in series with the logic pins.

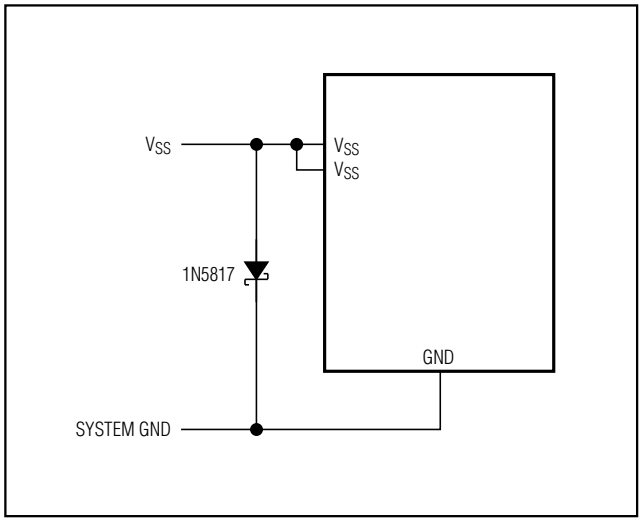
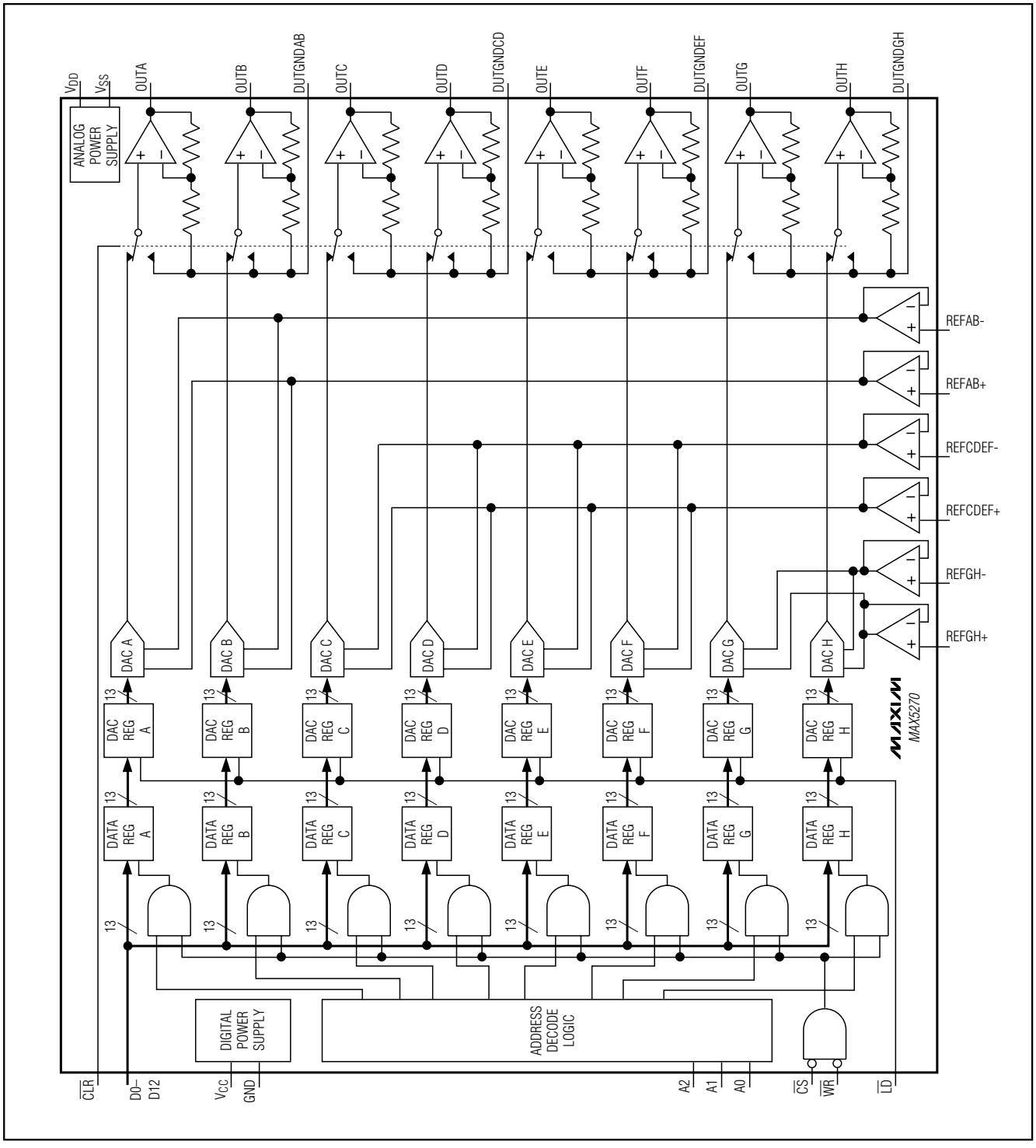


Figure 3. Schottky Diode Between V_{SS} and GND

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Functional Diagram



Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Driving Capacitive Loads

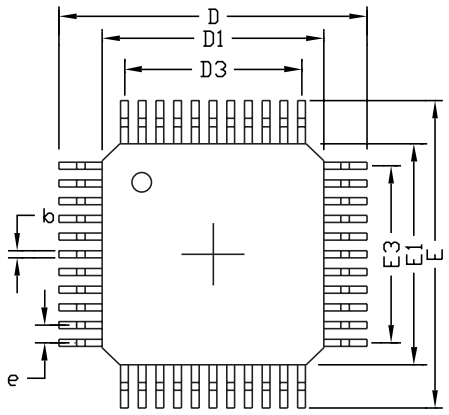
The MAX5270 typically drives capacitive loads up to 0.01µF without a series output resistor. However, whenever driving high capacitive loads, it is prudent to use a 220Ω series resistor between the MAX5270 output and the capacitive load.

Chip Information

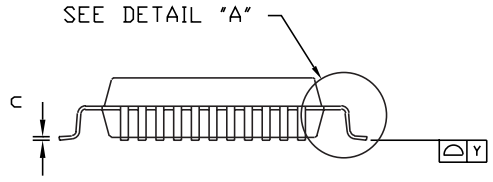
TRANSISTOR COUNT: 10,973

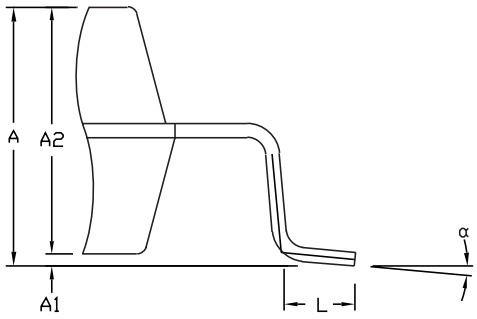
Package Information

MQFP44.EPS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.032	2.388	0.080	0.094
A1	0.102	0.254	0.004	0.010
A2	1.930	2.134	0.076	0.084
b	0.305	0.457	0.012	0.018
c	0.102	0.254	0.004	0.010
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.000 REF		0.315 REF	
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.000 REF		0.315 REF	
e	0.800 REF		0.0315 REF	
L	0.635	0.940	0.025	0.037
α	°0	°10	°0	°10





DETAIL "A"

NOTES:

1. D1&E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-AA-2.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, MQFP, 44L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0826	C	1/1