DS3160

JT 6312kbps Secondary-Rate Line Interface Unit and Framer/Formatter

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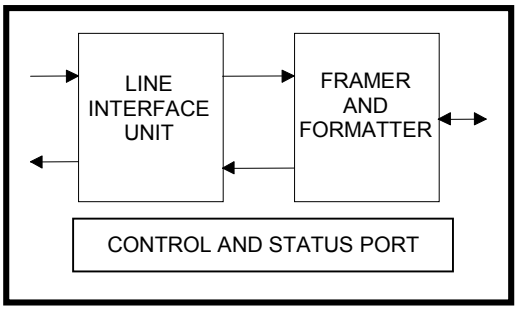
FEATURES

- Single-chip JT 6312kbps secondary-rate line interface unit (LIU) and framer/formatter
- Supports G.704 and NTT J2 frame formats
- Transmit and receive path-monitor outputs
- B8ZS encoder and decoder
- Generates and detects alarms
- Integrated HDLC controller handles LAPD messages without host intervention
- Integrated BERT supports performance monitoring
- Supports 8-bit or 16-bit control
- 3.3V supply with 5V tolerant I/O; low-power CMOS
- Available in 100-pin LQFP package
- IEEE 1149.1 JTAG support

ORDERING INFORMATION

DS3160	100-pin LFQP	0°C to +70°C
DS3160C01	100-pin LFQP	0°C to +85°C
DS3160N	100-pin LFQP	-40°C to +85°C

FUNCTIONAL DIAGRAM



APPLICATIONS

- Routers
- Switches
- Test Equipment
- Aggregators/Concentrators
- PBX
- Base Stations

DESCRIPTION

The DS3160 device, which combines a line interface unit (LIU) with a formatter and framer, is compliant with the JT 6312kbps secondary-rate user-network interface and supports the G.704 and NTT J2 frame formats. A full-featured LIU with integrated jitter attenuator supports a software-programmable framer and formatter. Framer features include alarm and error detection, on-chip HDLC controller for processing of M-bit information, and programmable timeslot data-enable signal for 1.5Mbps, 3Mbps, 4.5Mbps, and 6Mbps frame formats. The formatter adds the required overhead to the user data and has the additional capability of generating diagnostic errors. Loopback features, together with an on-chip bit-error-rate test (BERT) function, allow easy isolation and monitoring of network segments.

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://www.maxim-ic.com/errata.

1. MAIN FEATURES

Line Interface Unit

- Integrated transmit and receive 6312kbps line interface
- Requires no special external components other than 1:1 transformers
- Transmit and receive signal-monitor outputs
- Transmit, receive, and monitor paths use the same transformer (1:1)
- Nominal pulse waveform: $2V_{o-p}$ ±0.3V, 50% pulse width
- Electrical characteristics in accordance with TTC Standard JT-G703
- Adaptive receive equalizer adapts to coax cable loses from 0 to 15dB
- Performs clock/data recovery and wave shaping
- Transmit line-driver monitoring checks for faulty transmitter or a shorted output
- Jitter attenuator that can be placed either in the receive path or the transmit path or disabled
- On-board B8ZS coder/decoder with the option to be disabled
- Analog and digital loopbacks
- Analog loss of signal detector
- Tri-state-capable transmit and signal monitor line drivers for power management options
- Commercial temperature operating range: 0°C to +70°C

Framer/Formatter

- Provides frame synchronization and insertion
- Frame structure in accordance with TTC Standard JT-G704
- Frame alignment and cyclic redundancy check (CRC) in accordance with TTC Standard JT-G706
- Alarm detection and generation
- AIS and RAI generation
- Supports maintenance data link using an integrated HDLC controller
- Supports generation of gapped receive and transmit clocks for interface to devices that only need access to selected timeslots
- Programmable fractional circuit rates:
  – TS1-24 (1.5Mbps)
  – TS1-48 (3Mbps)
  – TS1-72 (4.5Mbps)
  – TS1-96 (6Mbps)

Path-Maintenance Data-Link HDLC Controller

- Designed to handle multiple LAPD messages without host intervention
- 256-byte receive and transmit buffers
- Handles all of the normal Layer 2 tasks such as zero stuffing/destuffing, CRC generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high and low watermarks for the FIFO

BERT

- Can generate and detect the pseudorandom patterns of 2^7 - 1, 2^{11} - 1, 2^{15} - 1, and quasirandom signal source (QRSS) as well as repetitive patterns from 1 to 32 bits in length
- Large error counter (24 bits) allows testing to proceed for long periods without host intervention
- Errors can be inserted into the generated BERT patterns for diagnostic purposes

Diagnostics

- Diagnostic loopbacks (transmit to receive)
- Line loopbacks (receive to transmit)
- Payload loopback
- Error counters for bipolar violations, code violations, loss of frame (LOF), framing bit errors, and CRC errors
- Error counters can be either updated automatically on 1-second boundaries as timed by the DS3160, or by software control, or by an external hardware pulse
- Can insert the bipolar violation errors and framing bit errors
- Inserted errors can be either controlled by software or by an external hardware pulse
- Generates loss of frame

Control Port

- Nonmultiplexed or multiplexed 16-bit control port (with an optional 8-bit mode)
- Intel and Motorola bus compatible

Packaging and Power

- 3.3V low-power CMOS with 5V tolerant inputs and outputs
- 100-pin LQFP package
- IEEE 1149.1 JTAG test port

Table 1A. APPLICABLE STANDARDS

1) Telecommunications Technique Council (TTC) **JT-G.703**, 1989 “Physical/Electrical Characteristics of Hierarchical Digital Interfaces”
2) Telecommunications Technique Council (TTC) **JT-G.704**, 1989 “Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels”
3) Telecommunications Technique Council (TTC) **JT-G.706**, 1989 “Frame Synchronization and CRC Procedure”
4) International Telecommunication Union (ITU) **G.703**, April 1991 “Physical/Electrical Characteristics of Hierarchical Digital Interfaces”
5) International Telecommunication Union (ITU) **G.704**, July 1995 “Synchronous Frame Structures Used at 1544kbps, 6312kbps, 2048kbps, 8488kbps, and 44736kbps Hierarchical Levels”
6) International Telecommunication Union (ITU) **G.775**, November 1994 “Loss-of-Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria”
7) International Telecommunication Union (ITU) **G.783**, January 1994 “Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks”
8) International Telecommunication Union (ITU) **O.151**, October 1992 “Error Performance Measuring Equipment Operating at the Primary Rate and Above”
9) International Telecommunication Union (ITU) **O.153**, October 1992 “Basic Parameters for the Measurement of Error Performance at Bit Rates Below the Primary Rate”
10) International Telecommunication Union (ITU) **O.161**, 1984 “In-Service Code Violation Monitors for Digital Systems”

Figure 1A. BLOCK DIAGRAM

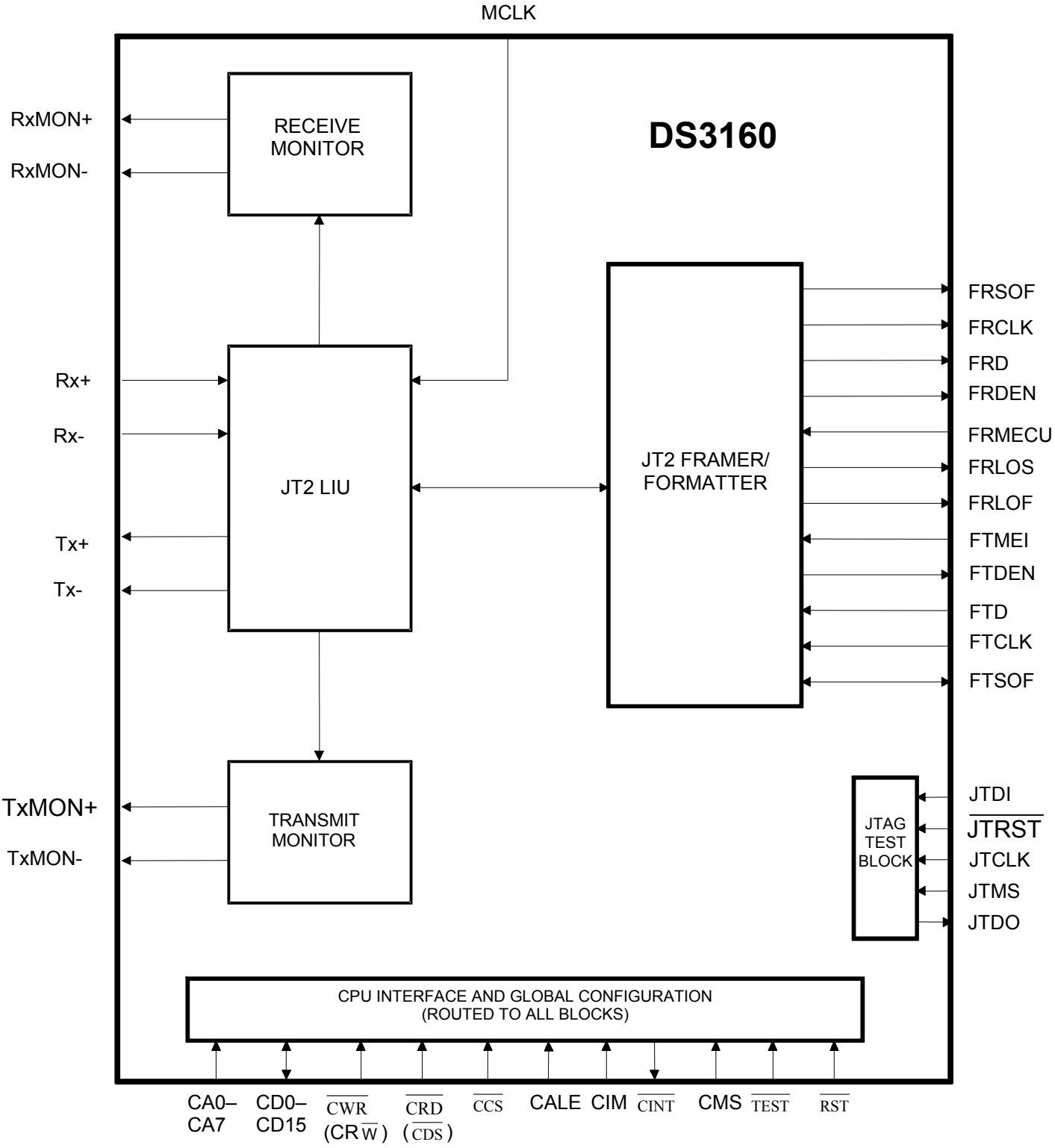


Figure 1B. LINE INTERFACE UNIT (LIU) BLOCK DIAGRAM

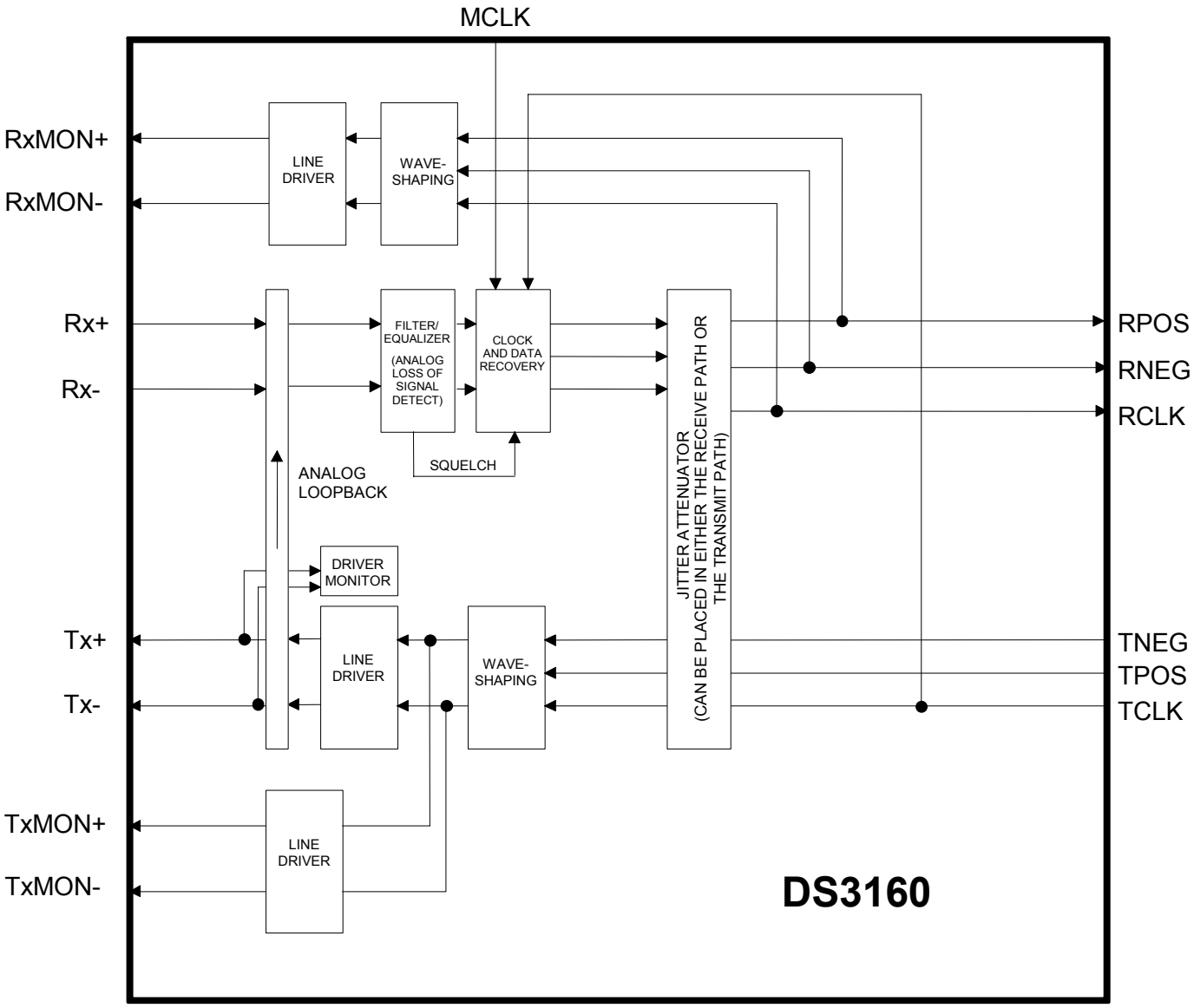
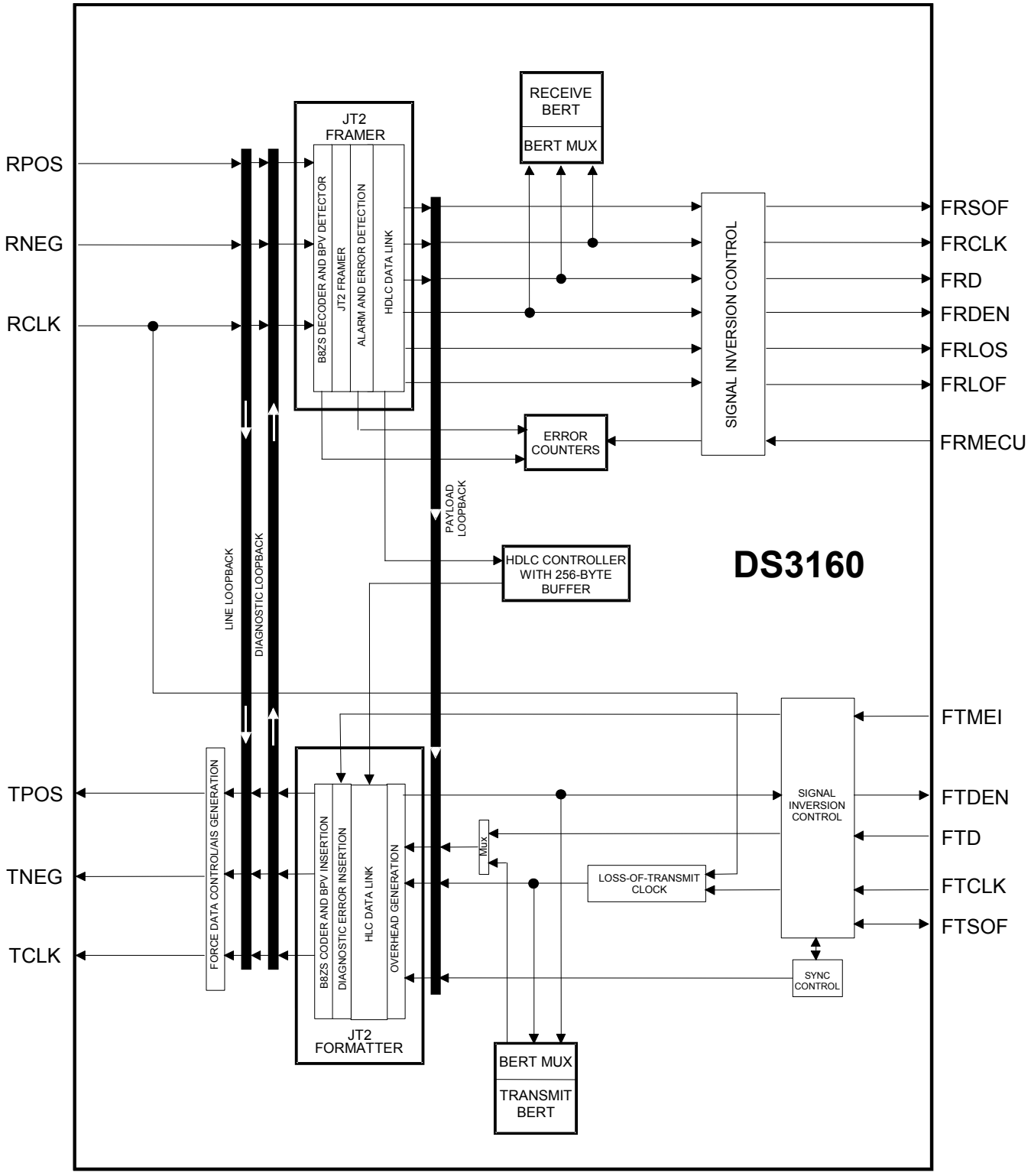


Figure 1C. FRAMER AND FORMATTER BLOCK DIAGRAM



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2. SIGNAL DESCRIPTION

2.1 Overview/Signal Pin List

This section describes the input and output signals on the DS3160. Signal names follow a convention that is shown in Table 2.1A. Table 2.1B lists all of the signals, their signal type, description, and pin location.

Table 2.1A. SIGNAL NAMING CONVENTION

FIRST LETTERS	SIGNAL CATEGORY	SECTION
C	CPU/Host Control Access Port	2.2
FR	Receive Framer	2.3
FT	Transmit Formatter	2.4
Rx	Receive LIU	2.5
Tx	Transmit LIU	2.6
J	JTAG Test Port	2.7

Table 2.1B. SIGNAL DESCRIPTION/PIN LIST (PRELIMINARY PIN ASSIGNMENT, SORTED BY PIN NUMBER)

PIN	SYMBOL	TYPE	FUNCTION
1, 11, 18, 19, 24, 25, 88, 100	AVDD	—	Positive Supply, 3.3V (±5%)
2	Rx+	I	Receive Positive or NRZ Data Input
3	Rx-	I	Receive Negative Data Input
4, 5, 14, 22, 23, 31, 32, 90	AVSS	—	Ground
6	LPOSO	O	LIU POS Factory Test Signal
7	LNEGO	O	LIU NEG Factory Test Signal
8	LCLKO	O	LIU CLK Factory Test Signal
9	TESTIO1	I/O	Factory Test I/O 1
10	TESTIO2	I/O	Factory Test I/O 2
12	RxMON+	O	Receive-Monitor Positive-Data Output
13	RxMON-	O	Receive-Monitor Negative-Data Output
15	LPOSI	I	LIU POS Factory Test Signal
16	LNEGI	I	LIU NEG Factory Test Signal
17	LCLKI	I	LIU CLK Factory Test Signal
20	Tx+	O	Transmit Positive or NRZ Data Output
21	Tx-	O	Transmit Negative Data Output
26	$\overline{\text{RST}}$	I	Reset
27	$\overline{\text{TEST}}$	I	Factory Test Input
28	$\overline{\text{HIZ}}$	I	Tri-State Output Pins Enable
29	TxMON+	O	Transmit-Monitor Positive-Data Output
30	TxMON-	O	Transmit-Monitor Negative-Data Output
33	$\overline{\text{JTRST}}$	I	JTAG IEEE 1149.1 Test Reset
34	JTMS	I	JTAG IEEE 1149.1 Test Mode Select
35	JTDO	O	JTAG IEEE 1149.1 Test Serial Data Output
36	JTDI	I	JTAG IEEE 1149.1 Test Serial Data Input
37	JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock
38, 52, 75, 86	DVDD	—	Positive Supply, 3.3V (±5%)
39	CALE	I	CPU Bus Address Latch Enable
40	CA0	I	CPU Bus Address Bit 0, LSB
41	CA1	I	CPU Bus Address Bit 1
42	CA2	I	CPU Bus Address Bit 2
43	CA3	I	CPU Bus Address Bit 3
44	CA4	I	CPU Bus Address Bit 4
45	CA5	I	CPU Bus Address Bit 5
46	CA6	I	CPU Bus Address Bit 6
47	CA7	I	CPU Bus Address Bit 7, MSB
48, 60, 66, 79	DVSS	—	Ground
49	CD0	I/O	CPU Bus Data Bit 0, LSB
50	CD1	I/O	CPU Bus Data Bit 1
51	CD2	I/O	CPU Bus Data Bit 2
53	CD3	I/O	CPU Bus Data Bit 3
54	CD4	I/O	CPU Bus Data Bit 4
55	CD5	I/O	CPU Bus Data Bit 5
56	CD6	I/O	CPU Bus Data Bit 6

PIN	SYMBOL	TYPE	FUNCTION
57	CD7	I/O	CPU Bus Data Bit 7
58	CD8	I/O	CPU Bus Data Bit 8
59	CD9	I/O	CPU Bus Data Bit 9
61	CD10	I/O	CPU Bus Data Bit 10
62	CD11	I/O	CPU Bus Data Bit 11
63	CD12	I/O	CPU Bus Data Bit 12
64	CD13	I/O	CPU Bus Data Bit 13
65	CD14	I/O	CPU Bus Data Bit 14
67	CD15	I/O	CPU Bus Data Bit 15, MSB
68	$\overline{\text{CCS}}$	I	CPU Bus Chip Select
69	$\overline{\text{CRD}}$ ($\overline{\text{CDS}}$)	I	CPU Bus Read Enable (CPU Bus Data Strobe)
70	$\overline{\text{CRW}}$ (CR/$\overline{\text{W}}$)	I	CPU Bus Write Enable (CPU Bus Read/Write Select)
71	$\overline{\text{CINT}}$	O	CPU Bus Interrupt
72	CIM	I	CPU Bus Intel/Motorola Bus Select
73	CMS	I	CPU Bus Mode Select
74	FTMEI	I	Transmit Formatter Manual Error Insert Pulse
76	FTSOF	I/O	Transmit Formatter Start-of-Frame Pulse
77	FTDEN	O	Transmit Formatter Data-Enable Output
78	FTD	I	Transmit Formatter Data Input
80	FRMECU	I	Receive Framer Manual Error-Counter Update
81	FRLOS	O	Receive Framer Loss-of-Signal output
82	FRLOF	O	Receive Framer Loss-of-Frame output
83	FRSOF	O	Receive Framer Start-of-Frame Pulse
84	FRDEN	O	Receive Framer Data-Enable Output
85	FRD	O	Receive Framer Data Output
87	FRCLK	O	Receive Framer Clock Output
89	FTCLK	I	Transmit Formatter Clock Input
91	MCLK	I	LIU Master Clock
92	$\overline{\text{TENA2}}$	I	Factory Test Enable 2
93	$\overline{\text{TENA1}}$	I	Factory Test Enable 1
94	DCLKO	O	Digital CLK Factory Test Signal
95	DNEGO	O	Digital NEG Factory Test Signal
96	DPOSO	O	Digital POS Factory Test Signal
97	DCLKI	I	Digital CLK Factory Test Signal
98	DNEGI	I	Digital NEG Factory Test Signal
99	DPOSI	I	Digital POS Factory Test Signal

Table 2.1C. SIGNAL DESCRIPTION/PIN LIST (PRELIMINARY PIN ASSIGNMENT, SORTED BY SIGNAL)

PIN	SYMBOL	TYPE	FUNCTION
1, 11, 18, 19, 24, 25, 88, 100	AVDD	—	Positive Supply, 3.3V (±5%)
4, 5, 14, 22, 23, 31, 32, 90	AVSS	—	Ground
40	CA0	I	CPU Bus Address Bit 0, LSB
41	CA1	I	CPU Bus Address Bit 1
42	CA2	I	CPU Bus Address Bit 2
43	CA3	I	CPU Bus Address Bit 3
44	CA4	I	CPU Bus Address Bit 4
45	CA5	I	CPU Bus Address Bit 5
46	CA6	I	CPU Bus Address Bit 6
47	CA7	I	CPU Bus Address Bit 7, MSB
39	CALE	I	CPU Bus Address Latch Enable
68	$\overline{\text{CCS}}$	I	CPU Bus Chip Select
49	CD0	I/O	CPU Bus Data Bit 0, LSB
50	CD1	I/O	CPU Bus Data Bit 1
61	CD10	I/O	CPU Bus Data Bit 10
62	CD11	I/O	CPU Bus Data Bit 11
63	CD12	I/O	CPU Bus Data Bit 12
64	CD13	I/O	CPU Bus Data Bit 13
65	CD14	I/O	CPU Bus Data Bit 14
67	CD15	I/O	CPU Bus Data Bit 15, MSB
51	CD2	I/O	CPU Bus Data Bit 2
53	CD3	I/O	CPU Bus Data Bit 3
54	CD4	I/O	CPU Bus Data Bit 4
55	CD5	I/O	CPU Bus Data Bit 5
56	CD6	I/O	CPU Bus Data Bit 6
57	CD7	I/O	CPU Bus Data Bit 7
58	CD8	I/O	CPU Bus Data Bit 8
59	CD9	I/O	CPU Bus Data Bit 9
72	CIM	I	CPU Bus Intel/Motorola Bus Select
71	$\overline{\text{CINT}}$	O	CPU Bus Interrupt
73	CMS	I	CPU Bus Mode Select
69	$\overline{\text{CRD}}$ ($\overline{\text{CDS}}$)	I	CPU Bus Read Enable (CPU Bus Data Strobe)
70	$\overline{\text{CWR}}$ (CR/$\overline{\text{W}}$)	I	CPU Bus Write Enable (CPU Bus Read/Write Select)
97	DCLKI	I	Digital CLK Factory Test Signal
94	DCLKO	O	Digital CLK Factory Test Signal
98	DNEGI	I	Digital NEG Factory Test Signal
95	DNEGO	O	Digital NEG Factory Test Signal
99	DPOSI	I	Digital POS Factory Test Signal
96	DPOSO	O	Digital POS Factory Test Signal
38, 52, 75, 86	DVDD	—	Positive Supply, 3.3V (±5%)
48, 60, 66, 79	DVSS	—	Ground
87	FRCLK	O	Receive Framer Clock Output
85	FRD	O	Receive Framer Data Output
84	FRDEN	O	Receive Framer Data-Enable Output

PIN	SYMBOL	TYPE	FUNCTION
82	FRLOF	O	Receive Framer Loss-of-Frame Output
81	FRLOS	O	Receive Framer Loss-of-Signal Output
80	FRMECU	I	Receive Framer Manual Error-Counter Update
83	FRSOF	O	Receive Framer Start-of-frame Pulse
89	FTCLK	I	Transmit Formatter Clock Input
78	FTD	I	Transmit Formatter Data Input
77	FTDEN	O	Transmit Formatter Data-Enable Output
74	FTMEI	I	Transmit Formatter Manual Error-Insert Pulse
76	FTSOF	I/O	Transmit Formatter Start-of-Frame Pulse
28	$\overline{\text{HIZ}}$	I	Tri-State Output Pins Enable
37	JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock
36	JTDI	I	JTAG IEEE 1149.1 Test Serial Data Input
35	JTDO	O	JTAG IEEE 1149.1 Test Serial Data Output
34	JTMS	I	JTAG IEEE 1149.1 Test Mode Select
33	$\overline{\text{JTRST}}$	I	JTAG IEEE 1149.1 Test Reset
17	LCLKI	I	LIU CLK Factory Test Signal
8	LCLKO	O	LIU CLK Factory Test Signal
16	LNEGI	I	LIU NEG Factory Test Signal
7	LNEGO	O	LIU NEG Factory Test Signal
15	LPOSI	I	LIU POS Factory Test Signal
6	LPOSO	O	LIU POS Factory Test Signal
91	MCLK	I	LIU Master Clock
26	$\overline{\text{RST}}$	I	Reset
3	Rx-	I	Receive Negative Data Input
2	Rx+	I	Receive Positive or NRZ Data Input
13	RxMON-	O	Receive Monitor Negative Data Output
12	RxMON+	O	Receive Monitor Positive Data Output
93	$\overline{\text{TENA1}}$	I	Factory Test Enable 1
92	$\overline{\text{TENA2}}$	I	Factory Test Enable 2
27	$\overline{\text{TEST}}$	I	Factory Test Input
9	TESTIO1	I/O	Factory Test I/O 1
10	TESTIO2	I/O	Factory Test I/O 2
21	Tx-	O	Transmit Negative Data Output
20	Tx+	O	Transmit Positive or NRZ Data Output
30	TxMON-	O	Transmit Monitor Negative Data Output
29	TxMON+	O	Transmit Monitor Positive Data Output

2.2 CPU Bus Signal Description

Signal Name: **CMS**
Signal Description: **CPU Bus Mode Select**
Signal Type: **Input**
This signal should be connected low when the device is to be operated as a 16-bit bus. This signal should be connected high when the device is to be operated as an 8-bit bus.

0 = CPU bus is in the 16-bit mode
1 = CPU bus is in the 8-bit mode

Signal Name: **CIM**
Signal Description: **CPU Bus Intel/Motorola Bus Select**
Signal Type: **Input**
The signal determines whether the CPU bus operates in the Intel mode (CIM = 0) or the Motorola mode (CIM = 1). The signal names in parenthesis are operational when the device is in the Motorola mode.

0 = CPU bus is in the Intel mode
1 = CPU bus is in the Motorola mode

Signal Name: **CD0 to CD15**
Signal Description: **CPU Bus Data Bus**
Signal Type: **Input/Output (Tri-State Capable)**
The external host configures the device and obtains real-time status information about the device through these signals. When reading data from the CPU bus, these signals are outputs. When writing data to the CPU bus, these signals become inputs. When the CPU bus is operated in the 8-bit mode (CMS = 1), CD8 to CD15 are inactive and should be connected low.

Signal Name: **CA0 to CA7**
Signal Description: **CPU Bus Address Bus**
Signal Type: **Input**
These input signals determine which internal device configuration register that the external host wishes to access. When the CPU bus is operated in the 16-bit mode (CMS = 0), CA0 is inactive and should be connected low. When the CPU bus is operated in the 8-bit mode (CMS = 1), CA0 is the least significant address bit.

Signal Name: $\overline{\text{CWR}}$ **(CR/**$\overline{\text{W}}$**)**
Signal Description: **CPU Bus Write Enable (CPU Bus Read/Write Select)**
Signal Type: **Input**
In Intel mode (CIM = 0), this signal determines when data is to be written to the device. In Motorola mode (CIM = 1), this signal is used to determine whether a read or write is to occur.

Signal Name: $\overline{\text{CRD}}$ **(**$\overline{\text{CDS}}$**)**
Signal Description: **CPU Bus Read Enable (CPU Bus Data Strobe)**
Signal Type: **Input**
In Intel mode (CIM = 0), this signal determines when data is to be read from the device. In Motorola mode (CIM = 1), a rising edge is used to write data into the device.

Signal Name: $\overline{\text{CINT}}$
Signal Description: **CPU Bus Interrupt**
Signal Type: **Output**
This output signal is driven low or open (float) during normal operation. It is driven low if one or more unmasked interrupt sources within the device are active. The signal remains low until the interrupt is either serviced or masked. This pin can be driven high in JTAG test modes.

Signal Name: $\overline{\text{CCS}}$
Signal Description: **CPU Bus Chip Select**
Signal Type: **Input**
This active-low signal must be asserted for the device to accept a read or write command from an external host.

Signal Name: **CALE**
Signal Description: **CPU Bus Address Latch Enable**
Signal Type: **Input**
This input signal controls a latch that exists on the CA0 to CA7 inputs. When CALE is high, the latch is transparent. The falling edge of CALE causes the latch to sample and hold the CA0 to CA7 inputs. In nonmultiplexed bus applications, CALE should be connected high. In multiplexed bus applications, CA[7:0] should be connected to CD[7:0] and the falling edge of CALE latches the address.

2.3 Receive Framer Signal Description

Signal Name: **FRSOF**
Signal Description: **Receive Framer Start-of-Frame Sync Signal**
Signal Type: **Output**
This signal pulses for one FRCLK period to indicate a frame or multiframe boundary. When configured in the frame mode, FRSOF indicates the position of the first bit (bit position 1) in each J2 frame. When configured in the multiframe mode, FRSOF indicates the position of the first bit (bit position 1) in each J2 multiframe. This signal can be configured to be either active high (normal mode) or active low (inverted mode). See Figure 2.3B.

Signal Name: **FRCLK**
Signal Description: **Receive Framer Clock**
Signal Type: **Output**
This signal outputs the clock that is used to pass data through the receive framer. It can be sourced from either the recovered receive clock, MCLK, or FTCLK inputs. During an LIU loss of signal (LIULOS = 1), the clock applied at MCLK (or FTCLK if MCLK is connected high) appears at this signal. This signal is used to clock the receive data out of the device at the FRD output. Data can be either updated on a rising edge (normal mode) or a falling edge (inverted mode).

Signal Name: **FRD**
Signal Description: **Receive Framer Serial Data**
Signal Type: **Output**
This signal outputs data from the receive framer. This signal is updated either on the rising edge of FRCLK (normal mode) or the falling edge of FRCLK (inverted mode). In addition, this signal can be internally inverted. FRD is forced to all 1's during a LOS and/or LOF condition.

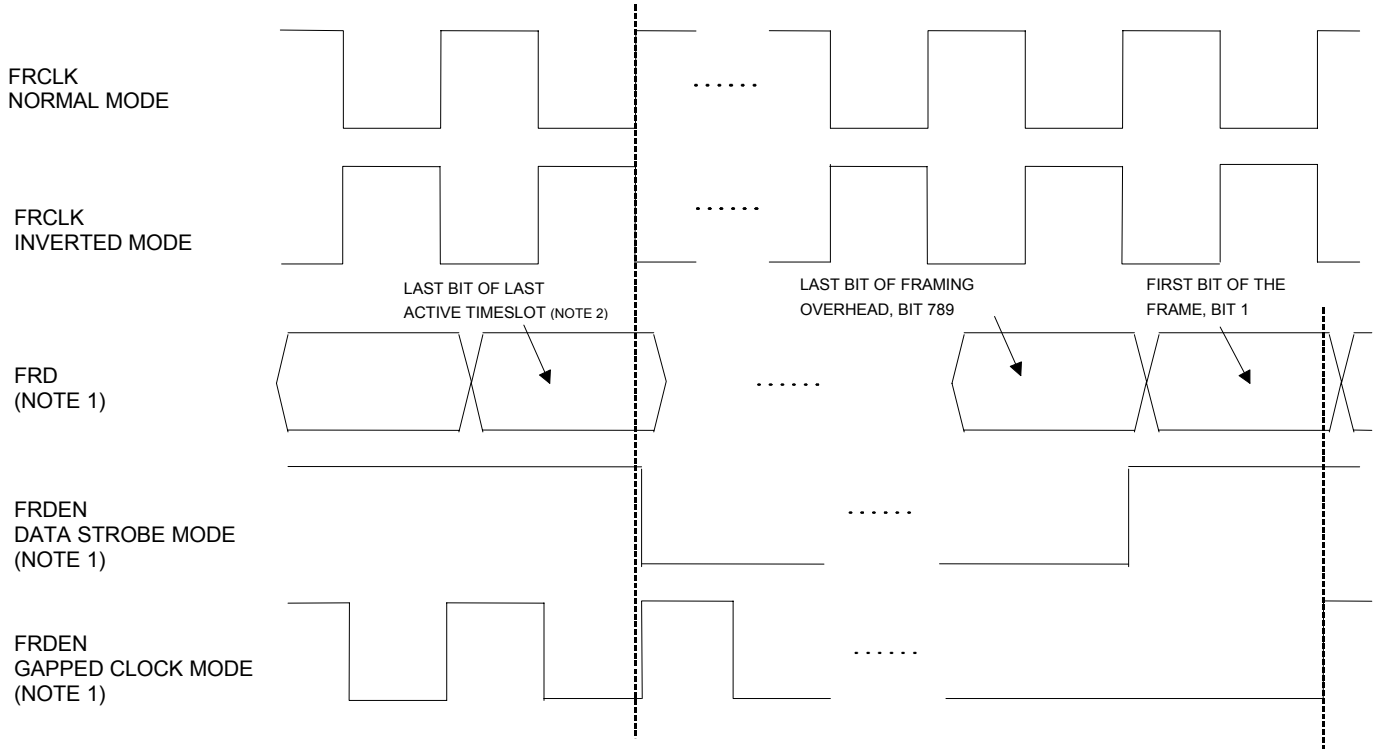
Signal Name: **FRDEN**
Signal Description: **Receive Framer Serial Data-Enable or Gapped Clock Output**
Signal Type: **Output**
This signal can be configured to either output a data enable or a gapped clock. In the data-enable mode, this signal goes active when enabled timeslots are available at the FRD output and is inactive when disabled timeslots or F-bits are being output at the FRD output. In the gapped clock mode, this signal transitions for each bit contained in enabled timeslots and is suppressed for each bit of disabled timeslots and the F-bits. This signal can be internally inverted (Figure 2.3A).

Signal Name: **FRMECU**
Signal Description: **Receive Framer Manual Error-Counter Update Strobe**
Signal Type: **Input**
The DS3160 can be configured to use this asynchronous input to initiate an updating of the internal error counters. A 0-to-1 transition on this input causes the device to begin loading the internal error counters with the latest error counts. This signal must be returned low before a subsequent updating of the error counters can occur. The host must wait at least 100ns before reading the error counters to allow the device time to update the error counters.

Signal Name: **FRLOS**
Signal Description: **Receive Framer Loss of Signal**
Signal Type: **Output**
This signal is forced high when the receive framer is in a loss-of-signal (LOS) state. It remains high as long as the LOS state persists and returns low when the framer exits the LOS state.

Signal Name: **FRLOF**
Signal Description: **Receive Framer Loss of Frame**
Signal Type: **Output**
This signal is forced high when the receive framer is in a loss-of-frame (LOF) state. It remains high as long as the LOF state persists and returns low when the framer synchronizes.

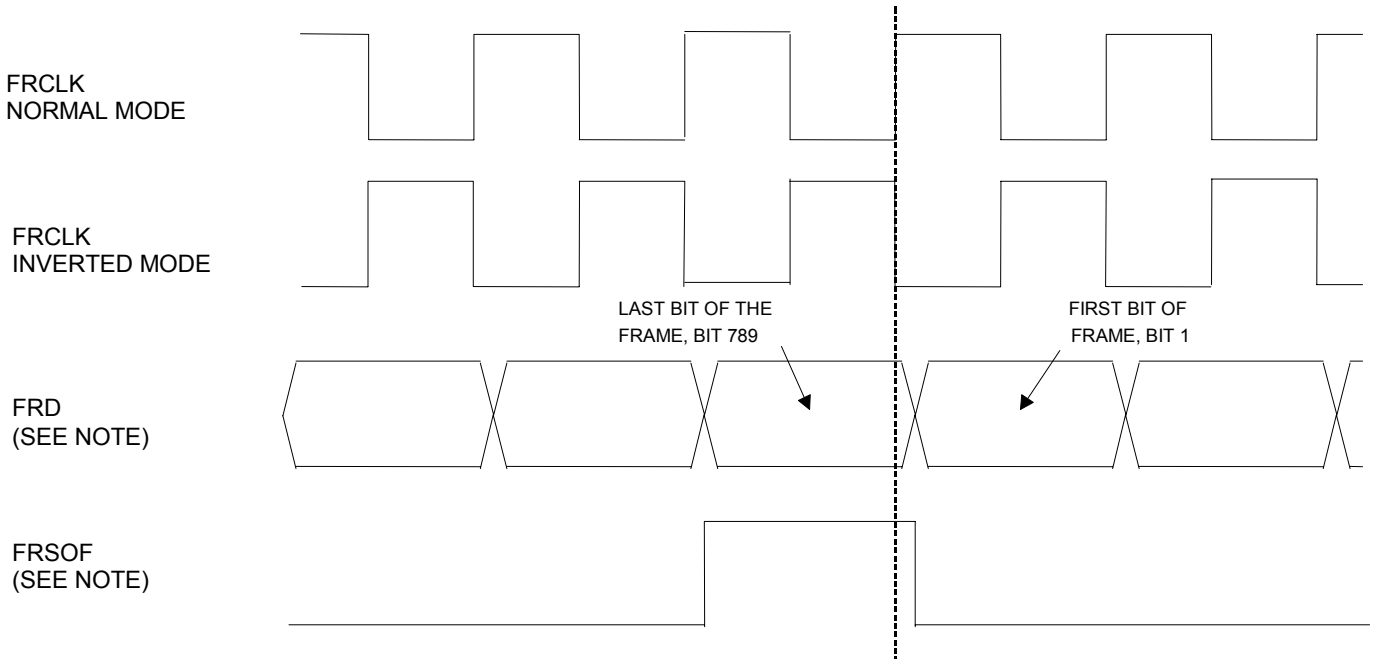
Figure 2.3A. RECEIVE FRAMER TIMING



NOTES:

1) FRCLK, FRD, and FRDEN can be inverted by Master Configuration Register 2 (MC2).
2) Valid last active timeslots include TS24, TS48, TS72, and TS96.

Figure 2.3B. RECEIVE FRAMER TIMING



NOTES:

1) FRCLK, FRD, and FRSOF can be inverted by Master Configuration Register 2 (MC2).

2.4 Transmit Formatter Signal Description

Signal Name: **FTSOF**
Signal Description: **Transmit Formatter Start-of-Frame Sync Signal**
Signal Type: **Output/Input (with internal 10kΩ pullup)**
This signal can be configured to be either an input or output. When FTSOF is an input (default state), a 1-to-0 transition sets the first framing bit in each frame or multiframe. When FTSOF is an input, a pulse is not required at every frame or multiframe boundary. The FTSOF as an input must not be less than a frame cycle of 125µs, or must be configured as an output. When this signal is an output, it pulses for one FTCLK period to indicate frame or multiframe boundary. When configured as an output and in the frame mode, FTSOF pulses high for one out of every 789 clock cycles, providing a frame reference. When configured as an output and in the multiframe mode, FTSOF pulses high for one out of every 3156 clock cycles, providing a multiframe reference. This signal can be configured to be either active high (normal mode) or active low (inverted mode) (Figure 2.4B).

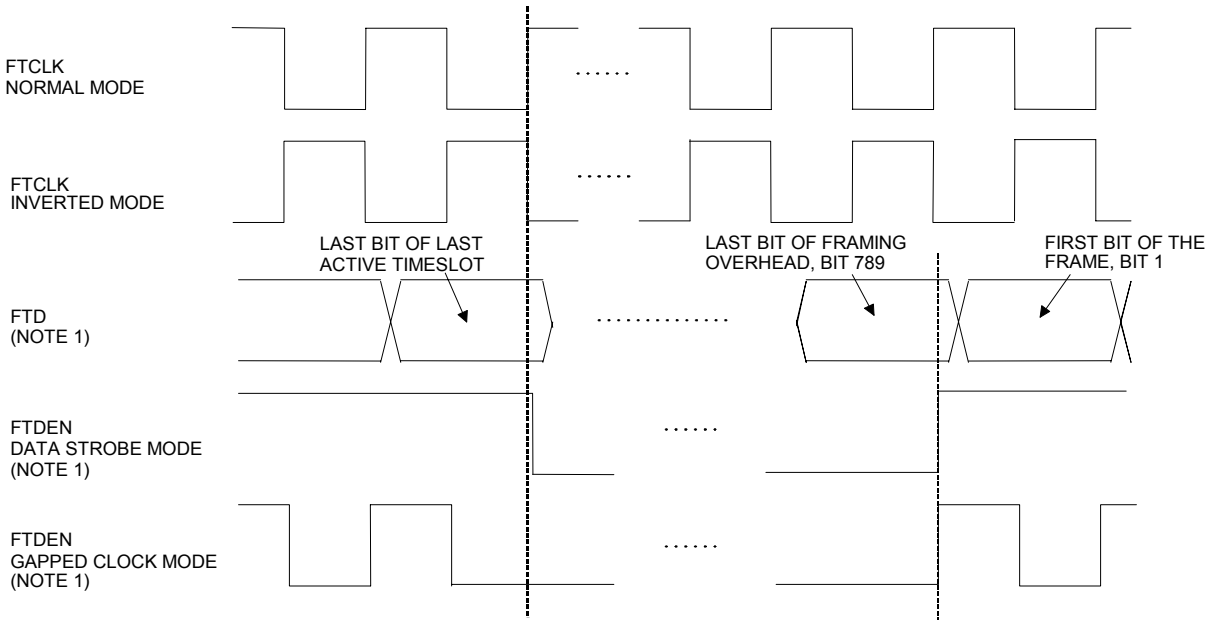
Signal Name: **FTCLK**
Signal Description: **Transmit Formatter Clock**
Signal Type: **Input**
An accurate 6.312MHz ±30ppm clock should be applied at this signal. This signal is used to clock data into the transmit formatter. Transmit data can be clocked into the device either on a rising edge (normal mode) or a falling edge (inverted mode).

Signal Name: **FTD**
Signal Description: **Transmit Formatter Serial Data**
Signal Type: **Input**
This signal inputs data into the transmit formatter. This signal can be sampled either on the rising edge of FTCLK (normal mode) or the falling edge of FTCLK (inverted mode). In addition, the data input to this signal can be internally inverted.

Signal Name: **FTDEN**
Signal Description: **Transmit Formatter Serial Data-Enable or Gapped Clock Output**
Signal Type: **Output**
This signal can be configured to either output a data enable or a gapped clock and use FTSOF for an alignment reference or ignore FTSOF (free-running option, see ALTFTDEN in MC2). When using FTSOF as a reference and in the data enable mode, this signal goes active when data should be made available at the FTD input. When using FTSOF as a reference and in the gapped clock mode, this signal acts as a demand clock for the FTD input and it transitions for each bit of data needed at the FTD input and it is suppressed when the transmit formatter inserts overhead data and, therefore, no data is needed at the FTD input. When the free-running mode is enabled, there is no correlation of FTDEN and when data is made available at FTD. This signal can be internally inverted (Figure 2.4A).

Signal Name: **FTMEI**
Signal Description: **Transmit Formatter Manual Error Insert Strobe**
Signal Type: **Input**
The DS3160 can be configured to use this asynchronous input to cause errors to be inserted into the transmitted data stream. A 0-to-1 transition on this input causes the device to begin the process of causing errors to be inserted. This signal must be returned low before any subsequent errors can be generated. If this signal is not used, then it should be connected low.

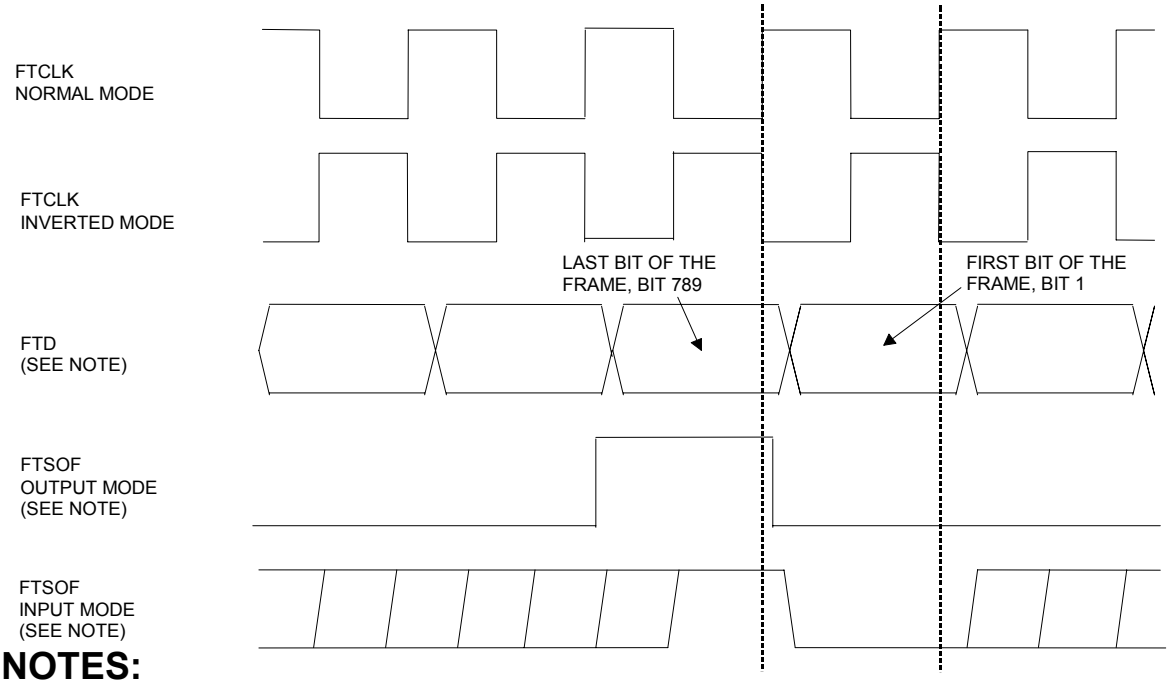
Figure 2.4A. TRANSMIT FORMATTER TIMING



NOTES:

1) FTCLK, FTD, and FTDEN can be inverted by Master Configuration Register 2 (MC2).
2) Valid last active timeslots include TS24, TS48, TS72, and TS96.

Figure 2.4B. TRANSMIT FORMATTER TIMING



NOTES:

1) FTD and FTSOF can be inverted by Master Configuration Register 2 (MC2).

2.5 Receive LIU Signal Description

Signal Name: **MCLK**
Signal Description: **Master Clock**
Signal Type: **Input**
The clock input at this signal is used by the clock-and-data recovery machine. A 6.312MHz ±30ppm clock should be applied at this signal. The DS3160 requires a clock signal to always be present at MCLK for correct device operation.

Signal Name: **Rx+**
Signal Description: **Receive Analog Input**
Signal Type: **Input**
This analog signal is coupled from the user-network interface by a 1:1 transformer.

Signal Name: **Rx-**
Signal Description: **Receive Analog Input**
Signal Type: **Input**
This analog signal is coupled from the user-network interface by a 1:1 transformer.

Signal Name: **RxMON+**
Signal Description: **Receive Monitor Analog Output**
Signal Type: **Output**
This analog output drives the receive monitor port by a 1:1 transformer.

Signal Name: **RxMON-**
Signal Description: **Receive Monitor Analog Output**
Signal Type: **Output**
This analog output drives the receive monitor port by a 1:1 transformer.

2.6 Transmit LIU Signal Description

Signal Name: **Tx+**
Signal Description: **Transmit Analog Output**
Signal Type: **Output**
This analog output drives the user-network interface by a 1:1 transformer (Figure 8A).

Signal Name: **Tx-**
Signal Description: **Transmit Analog Output**
Signal Type: **Output**
This analog output drives the user-network interface by a 1:1 transformer (Figure 8A).

Signal Name: **TxMON+**
Signal Description: **Transmit Monitor Analog Output**
Signal Type: **Output**
This analog output drives the transmit monitor port by a 1:1 transformer (Figure 8A).

Signal Name: **TxMON-**
Signal Description: **Transmit Monitor Analog Output**
Signal Type: **Output**
This analog output drives the transmit monitor port by a 1:1 transformer (Figure 8A).

2.7 JTAG Signal Description

Signal Name: **JTCLK**
Signal Description: **JTAG IEEE 1149.1 Test Serial Clock**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, this signal should be pulled high.

Signal Name: **JTDI**
Signal Description: **JTAG IEEE 1149.1 Test Serial Data Input**
Signal Type: **Input (with internal 10kΩ pullup)**
Test instructions and data are clocked into this signal on the rising edge of JTCLK. If not used, this signal should be left open-circuited.

Signal Name: **JTDO**
Signal Description: **JTAG IEEE 1149.1 Test Serial Data Output**
Signal Type: **Output**
Test instructions are clocked out of this signal on the falling edge of JTCLK. If not used, this signal should be left open-circuited.

Signal Name: $\overline{\text{JTRST}}$
Signal Description: **JTAG IEEE 1149.1 Test Reset**
Signal Type: **Input (with internal 10kΩ pullup)**
This signal is used to asynchronously reset the test access port controller. At power-up, JTRST must be set low and then high. This action sets the device into the boundary-scan bypass mode allowing normal device operation. If boundary scan is not used, this signal should be held low.

Signal Name: **JTMS**
Signal Description: **JTAG IEEE 1149.1 Test Mode Select**
Signal Type: **Input (with internal 10kΩ pullup)**
This signal is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. If not used, this signal should be left open-circuited.

2.8 Supply, Factory Test, and Reset Signal Descriptions

Signal Name: $\overline{\text{RST}}$
Signal Description: **Global Hardware Reset**
Signal Type: **Input (with internal 10kΩ pullup)**
This active-low asynchronous signal causes the device to be reset. When this signal is forced low, it causes all of the internal registers to be forced to their default states. The device is held in a reset state as long as this signal is low. This signal should be activated after the clocks MCLK and FTCLK are valid, and must be returned high before the device can be configured for operation.

Signal Name: $\overline{\text{HIZ}}$
Signal Description: **Tri-State All Output Pins Enable**
Signal Type: **Input (with internal 10kΩ pullup)**
This input should be left open-circuited by the user.

Signal Name: $\overline{\text{TEST}}$, $\overline{\text{TENA1}}$, $\overline{\text{TENA2}}$
Signal Description: **Factory Test Enable**
Signal Type: **Input (with internal 10kΩ pullup)**
These inputs should be left open-circuited by the user.

Signal Names: **LCLKI, LPOSI, LNEGI, DCLKI, DPOSI, DNEGI**
Signal Description: **Factory Test Signal**
Signal Type: **Input (with internal 10kΩ pullup)**
These inputs should be left open-circuited by the user.

Signal Names: **LCLKO, LPOSO, LNEGO, DCLKO, DPOSO, DNEGO**
Signal Description: **Factory Test Signal**
Signal Type: **Output**
These outputs should be left open-circuited by the user.

Signal Names: **TESTIO1, TESTIO2**
Signal Description: **Factory Test Signal**
Signal Type: **Input/Output (tri-state capable)**
These signals should be left open-circuited by the user.

Signal Name: **DVDD**
Signal Description: **Digital Positive Supply**
Signal Type: **N/A**
3.3V (±5%). All DVDD signals should be connected together.

Signal Name: **DVSS**
Signal Description: **Digital Ground Reference**
Signal Type: **N/A**
All DVSS signals should be connected together.

Signal Name: **AVDD**
Signal Description: **Analog Positive Supply**
Signal Type: **N/A**
3.3V (±5%). All AVDD signals should be connected together.

Signal Name: **AVSS**
Signal Description: **Analog Ground Reference**
Signal Type: **N/A**
All AVSS signals should be connected together.

3. MEMORY MAP AND REGISTER NOMENCLATURE

3.1 Memory Map

ADDRESS	ACRONYM	R/W	REGISTER NAME	DATA SHEET SECTION
00	MRID	R/W	Master Reset and ID Register	4.1
02	MC1	R/W	Master Configuration Register 1	4.2
04	MC2	R/W	Master Configuration Register 2	4.2
06	MSR	R	Master Status Register	4.3
08	IMSR	R/W	Interrupt Mask Register for MSR	4.3
0A	CR1	R/W	Control Register 1	5.2
0C	CR2	R/W	Control Register 2	5.2
0E	TXTS9798	R/W	TX TS97 and TS98 Signaling Insertion	5.2
10	RXTS9798	R	RX TS97 and TS98 Signaling Monitor	5.2
12	SR1	R	Status Register	5.3
14	ISR1	R/W	Interrupt Mask for SR	5.3
16	INFO	R	Information Register	5.3
18	BPVCR	R	Bipolar Violation (BPV) Count Register	5.4
1A	EXZCR	R	Excessive Zero (EXZ) Count Register	5.4
1C	FECR	R	Frame Error Count Register	5.4
1E	CRCCR	R	CRC Error Count Register	5.4
20	BERTMC	R/W	BERT Mux Control Register	6.2
22	BERTC0	R/W	BERT Control Register 0	6.2
24	BERTC1	R/W	BERT Control Register 1	6.2
26	BERTRP0	R/W	BERT Repetitive Pattern 0	6.2
28	BERTRP1	R/W	BERT Repetitive Pattern 1	6.2
2A	BERTBC0	R	BERT 32-Bit Bit Counter	6.2
2C	BERTBC1	R	BERT 32-Bit Bit Counter	6.2
2E	BERTEC0	R	BERT 24-Bit Error Counter (lower) and Status Information	6.2
30	BERTEC1	R	BERT 24-Bit Error Counter	6.2
32	HCR	R/W	HDLC Control Register	7.2
34	RHDLC	R	Receive HDLC FIFO	7.2
36	THDLC	R/W	Transmit HDLC FIFO	7.2
38	HSR	R	HDLC Status Register	7.2
3A	IHSR	R/W	Interrupt Mask for HDLC Status Register	7.2
3C	—	—	*Reserved*	—
3E	—	—	*Reserved*	—
40	TEST1	R/W	Test Register 1	10
42	TEST2	R/W	Test Register 2	10
44	TEST3	R/W	Test Register 3	10
46	TEST4	R/W	Test Register 4	10
48–4E	—	—	*Reserved*	—

Note: Address banks 5x, 6x, 7x, 8x, 9x, Ax, Bx, Cx, Dx, Ex, and Fx are not assigned.

3.2 Register Description

The DS3160 register set consists of configuration registers and status registers. Configuration registers are read-write except where noted as read-only; status registers are read-only. In this data sheet, registers are described using the following descriptors:

Table 3.2A. REGISTER DESCRIPTION LABEL DEFINITIONS

TEXT	FUNCTION
Register Name	Register label
Register Description	Full register name
Register Address	Physical address
Bit #	Bit number in register, range 0 through 15; bit 15 is the MSB
Name	Bit label
Default	Value of the bit immediately after a reset has been issued to the DS3160

NOTES:

1) The DS3160 ignores data written to bit locations with the name of "N/A."
2) Reading bit locations with the name of "N/A" returns the value of zero.
3) Writing into read-only bit locations does not affect device operation.

4. MASTER DEVICE CONFIGURATION AND STATUS/INTERRUPT

4.1 Master Reset and ID Register Descriptions

The master reset and ID (MRID) register can be used to globally reset the device. When the RST bit is set to 1, all of the internal registers are placed into their default state. A reset can also be invoked by the $\overline{RST}$ hardware signal.

The upper byte of the MRID register is read-only and can be read by the host to determine the chip revision. Contact the factory for specifics on the meaning of the value read from the ID0 to ID7 bits.

Register Name: **MRID**
Register Description: **Master Reset and ID Register**
Register Address: **00h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	N/A	N/A	N/A	RST
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default	*	*	*	*	*	*	*	*

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Master Software Reset (RST). When this bit is set to a 1 by the host, it forces all of the internal registers to their default states. This bit must be set high for a minimum of 100ns. This software bit is logically OR'ed with the hardware signal $\overline{RST}$.

0 = normal operation
1 = force all internal registers to their default values

Bits 8 to 15/Chip Revision ID Bit 0 to 7 (ID0 to ID7). Read-only. Contact the factory for details on the meaning of the ID bits. MRID bits 15 (MSB) to 8 (LSB) are a binary coded hexidecimal number that represents the die revision according to the product top brand. Example: 10100010 = A2.

** Contact factory.*

4.2 Master Configuration Registers Description

Register Name: **MC1**
Register Description: **Master Configuration Register 1**
Register Address: **02h**

Bit #	7	6	5	4	3	2	1	0
Name	LLB	DLB	DENMS	TAIS	LOTCMC	MECU	AECU	ZCSD
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	FRDAIS	N/A	ALB	JASEL	JAEN	RMONEN	TMONEN	TDRVEN
Default	1	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Zero Code Suppression Disable (ZCSD)

0 = enable the B8ZS
1 = disable the B8ZS

Bit 1/Automatic One-Second Error Counters Update Defeat (AECU). When this bit is set low, the device automatically updates the performance error counters on an internally created 1-second boundary. The host is notified of the update by the setting of the OST status bit in the master status register. In this mode, the host has a full 1-second period to retrieve the error information before it is overwritten with the next update. When this bit is set high, the device defeats the automatic 1-second update and enables a manual update mode. In the manual update mode, the device relies on either the framer manual error-counter update (FRMECU) hardware-input signal or the MECU control bit to update the error counters. The FRMECU hardware input signal and MECU control bit are logically OR'ed and hence a 0-to-1 transition on either initiates an error-counter update to occur. After either the FRMECU signal or MECU bit has toggled, the host must wait at least 100ns before reading the error counters to allow the device time to complete the update.

0 = enable the automatic update mode and disable the manual update mode
1 = disable the automatic update mode and enable the manual update mode

Bit 2/Manual Error-Counter Update (MECU). A 0-to-1 transition on this bit causes the device to update the performance error counters. This bit is ignored if the AECU control bit is set low. This bit must be cleared and set again for a subsequent update. This bit is logically OR'ed with the external FRMECU hardware input signal. After this bit has toggled, the host must wait at least 100ns before reading the error counters to allow the device time to complete the update.

Bit 3/Loss-of-Transmit Clock Mux Control (LOTCMC). The DS3160 can detect if the FTCLK fails to transition. If this bit is set low, the device takes no action (other than setting the LOTC status bit) when the FTCLK fails to transition. When this bit is set high, the device automatically switches to the internal receive clock (RCLK) when the FTCLK fails and transmit AIS.

0 = do not switch to the RCLK signal if FTCLK fails to transition
1 = automatically switch to the RCLK signal if the FTCLK fails to transition and send AIS

Bit 4/Transmit Alarm Indication Signal (TAIS). When this bit is set high, the transmitter generates an unframed all 1's. When this bit it set low, normal data is transmitted.

0 = do not transmit AIS
1 = transmit AIS

Bit 5/Data Enable Mode Select (DENMS). When this bit is set low, the FRDEN and FTDEN outputs are asserted during enabled timeslots and deasserted during the disabled timeslots and F-bits of the frame. When this bit is high, FRDEN and FTDEN are gapped clocks that pulse only during the enabled timeslots of the frame.

0 = FRDEN and FTDEN are data enables
1 = FRDEN and FTDEN are gapped clocks

Bit 6/Diagnostic Loopback Enable (DLB). See Figures 1A and 1B for a visual description of this loopback.

0 = disable loopback
1 = enable loopback

Bit 7/Line Loopback Enable (LLB). See Figures 1A and 1B for a visual description of this loopback.

0 = disable loopback
1 = enable loopback

Bit 8/Transmit Driver Output Enable (TDRVEN). When this bit is set low, the Tx+ and Tx- analog outputs are tri-stated. When this bit is high, the Tx+ and Tx- analog outputs are enabled.

0 = Tx+ and Tx- outputs tri-stated
1 = Tx+ and Tx- outputs enabled

Bit 9/Transmit Monitor Output Enable (TMONEN). When this bit is set low, the TxMON+ and TxMON- analog outputs are tri-stated. When this bit is high, the TxMON+ and TxMON- analog outputs are enabled.

0 = TxMON+ and TxMON- outputs tri-stated
1 = TxMON+ and TxMON- outputs enabled

Bit 10/Receive Monitor Output Enable (RMONEN). When this bit is set low, the RxMON+ and RxMON- analog outputs are tri-stated. When this bit is high, the RxMON+ and RxMON- analog outputs are enabled.

0 = RxMON+ and RxMON- outputs tri-stated
1 = RxMON+ and RxMON- outputs enabled

Bit 11/Jitter Attenuator Enable (JAEN). When this bit is set low, the jitter attenuator is disabled. When this bit is high, the jitter attenuator is enabled.

0 = jitter attenuator disabled
1 = jitter attenuator enabled

Bit 12/Jitter Attenuator Path Select (JASEL). When this bit is set low, the jitter attenuator is enabled in the receive path. When this bit is high, the jitter attenuator is enabled in the transmit path.

0 = jitter attenuator in receive path
1 = jitter attenuator in transmit path

Bit 13/Analog Loopback Enable (ALB). The analog loopback loops the transmit data (Tx+ and Tx- outputs) directly back to the receive side (Rx+ and Rx- inputs). When this loopback is enabled, the data output from the formatter continues to pass through the device, but the incoming receive data is replaced with the data being output from the device. See the block diagrams in Section 1 for a visual description of this loopback.

0 = disable loopback
1 = enable loopback

Bit 15/FRD AIS ENABLE (FRDAIS). When this bit is set high, receive data output at the FRD pin is forced to all 1's. When this bit is low, FRD operates normally.

0 = FRD operates normally
1 = data output at the FRD pin is forced to all 1's

Register Name: **MC2**
Register Description: **Master Configuration Register 2**
Register Address: **04h**

Bit #	7	6	5	4	3	2	1	0
Name	FRCLKI	FRDI	FRDENI	FTMEII	FTSOFI	FTCLKI	FTDI	FTDENI
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	ALTFTDEN	FRSOFM	FTSOFM	FTSOFC	FRMECUI	FRLOFI	FRLOSI	FRSOFI
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/FTDEN Invert Enable (FTDENI)
0 = do not invert the FTDEN signal (normal mode)
1 = invert the FTDEN signal (inverted mode)

Bit 1/FTD Invert Enable (FTDI)
0 = do not invert the FTD signal (normal mode)
1 = invert the FTD signal (inverted mode)

Bit 2/FTCLK Invert Enable (FTCLKI)
0 = do not invert the FTCLK signal (normal mode)
1 = invert the FTCLK signal (inverted mode)

Bit 3/FTSOF Invert Enable (FTSOFI)
0 = do not invert the FTSOF signal (normal mode)
1 = invert the FTSOF signal (inverted mode)

Bit 4/FTMEI Invert Enable (FTMEII)
0 = do not invert the FTMEI signal (normal mode)
1 = invert the FTMEI signal (inverted mode)

Bit 5/FRDEN Invert Enable (FRDENI)
0 = do not invert the FRDEN signal (normal mode)
1 = invert the FRDEN signal (inverted mode)

Bit 6/FRD Invert Enable (FRDI)
0 = do not invert the FRD signal (normal mode)
1 = invert the FRD signal (inverted mode)

Bit 7/FRCLK Invert Enable (FRCLKI)
0 = do not invert the FRCLK signal (normal mode)
1 = invert the FRCLK signal (inverted mode)

Bit 8/FRSOF Invert Enable (FRSOFI)

0 = do not invert the FRSOF signal (normal mode)
1 = invert the FRSOF signal (inverted mode)

Bit 9 / FRLOS Invert Enable (FRLOSI)
0 = do not invert the FRLOS signal (normal mode)
1 = invert the FRLOS signal (inverted mode)

Bit 10/FRLOF Invert Enable (FRLOFI)
0 = do not invert the FRLOF signal (normal mode)
1 = invert the FRLOF signal (inverted mode)

Bit 11/FRMECU Invert Enable (FRMECUI)
0 = do not invert the FRMECU signal (normal mode)
1 = invert the FRMECU signal (inverted mode)

Bit 12/Transmit Frame Sync I/O Control (FTSOFC). When this bit is set low, the FTSOF signal is an input and the DS3160 uses it to determine the frame or multiframe boundaries. When this bit is high, the FTSOF signal is an output and pulses for one FTCLK cycle at the beginning of each frame or multiframe.
0 = FTSOF is an input
1 = FTSOF is an output

Bit 13/Transmit Multiframe Enable (FTSOFM). When FTSOF is configured as an output, this bit determines whether the FTSOF signal indicates frame or multiframe boundaries
0 = FTSOF output indicates frame boundaries
1 = FTSOF output indicates multiframe boundaries

Bit 14/Receive Multiframe Indication Enable (FRSOFM). This bit is used to control whether the FRSOF output indicates frame or multiframe boundaries
0 = FRSOF indicates frame boundaries
1 = FRSOF indicates multiframe boundaries

Bit 15/Alternate Transmit Data Enable (ALTFTDEN). When set low, the FTDEN circuitry uses the FTSOF signal to determine the start of the FTDEN signal (bit 1 of the FTDEN frame). When set high, FTDEN is free-running and ignores FTSOF.
0 = use FTSOF to determine FTDEN start
1 = FTDEN free-running, ignores FTSOF

4.3 Master Status and Interrupt Register Descriptions

Status Registers

The status registers in the DS3160 allow the host to monitor the real-time condition of the device. Most of the status bits in the device can cause a hardware interrupt to occur. Also, most of the status bits within the device are latched to ensure that the host can detect changes in state and the true status of the device. There are three types of status bits in the DS3160. The first type is called an event status bit, which is derived from a momentary condition or state that occurs within the device. The event status bits are always cleared when read and can generate an interrupt when they are asserted. An example of an event status bit is the one-second-timer boundary occurrence (OST).

The second type of status bit is called an alarm status bit, which is derived from conditions that can occur for longer than an instance. The alarm status bits are cleared when read unless the alarm is still present. The alarm status bits generate interrupts on a change in state in the alarm (i.e., when it is asserted or de-asserted). An example of an alarm status bit is the loss of frame (LOF).

The third type of status bit is called a real-time status bit. The real-time status bit remains active as long as the condition exists and generates an interrupt as long as the condition exists. An example of a real-time status bit is the loss-of-transmit clock (LOTC).

Figure 4.3A. EVENT STATUS BIT

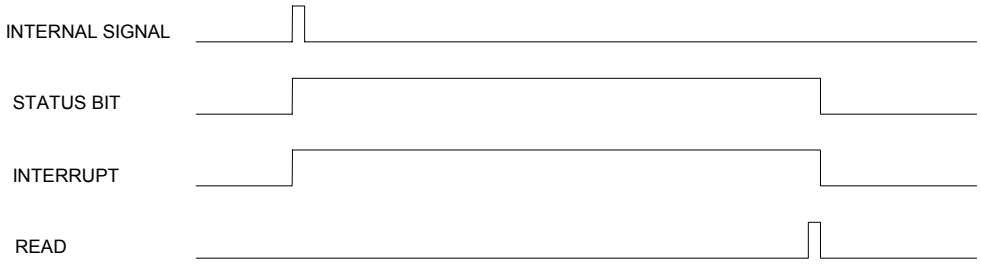
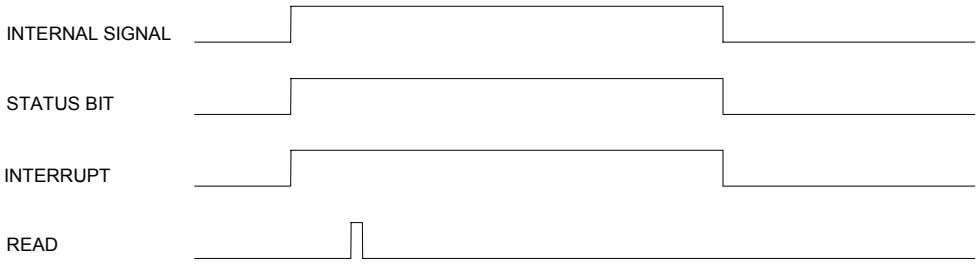


Figure 4.3B. ALARM STATUS BIT

Figure 4.3C. REAL-TIME STATUS BIT



Master Status Register (MSR)

The master status register (MSR) is a special status register that can be used to help the host quickly locate changes in device status. There is a status bit in the MSR for each of the major blocks within the DS3160. When an alarm or event occurs in one of these blocks, the device can be configured to set a bit in the MSR. Status bits in the MSR can also cause a hardware interrupt to occur. In either polled or interrupt-driven software routines, the host can first read the MSR to locate which status registers need to be serviced.

Register Name: **MSR**
Register Description: **Master Status Register**
Register Address: **06h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	SR1	HDLC	BERT	COVF	OST
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	TXDRVR	LIULOS	N/A	LOTC
Default	0	0	0	0	0	1	0	1

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/One-Second-Timer Boundary Occurrence (OST). This latched read-only event status bit is set to a 1 on each 1-second boundary as timed by the DS3160. The device chooses an arbitrary 1-second boundary that is timed from the RCLK signal. This bit is cleared when read and is not be set again until another 1-second boundary has occurred. The setting of this status bit can cause a hardware interrupt to occur if the OST bit in the interrupt mask for MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Bit 1/Counter Overflow Event (COVF). This latched read-only event status bit is set to a 1 if any of the error counters saturate (the error counters saturate when full). This bit is cleared when read even if one or more of the error counters is still saturated. The setting of this status bit can cause a hardware interrupt to occur if the COVF bit in the interrupt mask for MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Bit 2/Change in BERT Status (BERT). This read-only event status bit is set to a 1 if there is a major change of status in the BERT receiver. A major change of status is defined as either a change in the receive synchronization (i.e., the BERT has gone into or out of receive synchronization), a bit error has been detected, or an overflow has occurred in either the bit counter or the error counter. The host must read the status bits of the BERT in the BERT status register (BERTEC0) to determine the change of state. This bit is cleared when read and is not set again until the BERT has experienced another change of state. The setting of this status bit can cause a hardware interrupt to occur if the BERT bit in the interrupt mask for MSR (IMSR) register is set to a 1 (Figure 4.3D).

Bit 3/Change in HDLC Status (HDLC). This read-only event status bit is set to a 1 if there is a change of status in the HDLC controller. The host must read the status bits of the HDLC controller in the HDLC status register (HSR) to determine the change of state. This bit is cleared when read and is not set again until the HDLC controller has experienced another change of state. The setting of this status bit can cause

a hardware interrupt to occur if the HDLC bit in the interrupt mask (IMSR) register is set to a 1 (Figure 4.3E).

Bit 4/Change in Framer Status (SR1). This read-only event-status bit is set to a 1 if there is a change of status in the framer or formatter. The host must read the contents of SR1 to determine the change of state. This bit is cleared when read and is not set again until the framer or formatter has experienced another change of state. The setting of this status bit can cause a hardware interrupt to occur if the SR1 bit in the interrupt mask (IMSR) register is set to a 1 (Figure 4.3F).

Bit 8/Loss-of-Transmit Clock Detected (LOTC). This latched read-only alarm status bit is set to a 1 when the device detects that the FTCLK clock has not toggled for 200ns (±100ns). This bit is cleared when a clock is detected at the FTCLK input. The setting of this status bit can cause a hardware interrupt to occur if the LOTC bit in the interrupt mask for MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when the device detects a clock at FTCLK. On reset, the LOTC status bit is set and then immediately cleared if the clock is present.

Bit 10/Analog Loss-of-Signal Detected (LIULOS). This latched read-only alarm status bit is set to a 1 when the device detects that the incoming signal has dropped below -20dB of the nominal signal level. When set, the recovered data is squelched and all 0's are output to the framer. The analog loss-of-signal detector is not clear until the signal level is above -16dB of the nominal signal level. Setting this status bit can cause a hardware interrupt to occur if the LIULOS bit in the interrupt mask for MSR (IMSR) register is set to a 1.

Bit 11/Transmit Driver Monitor (TXDRVR). This latched read-only alarm status bit is set to a 1 when the analog-transmit outputs (Tx+ and Tx-) fail. The setting of this status bit can cause a hardware interrupt to occur if the TXDRVR bit in the interrupt mask for MSR (IMSR) register is set to a 1.

Figure 4.3D. BERT STATUS BIT FLOW

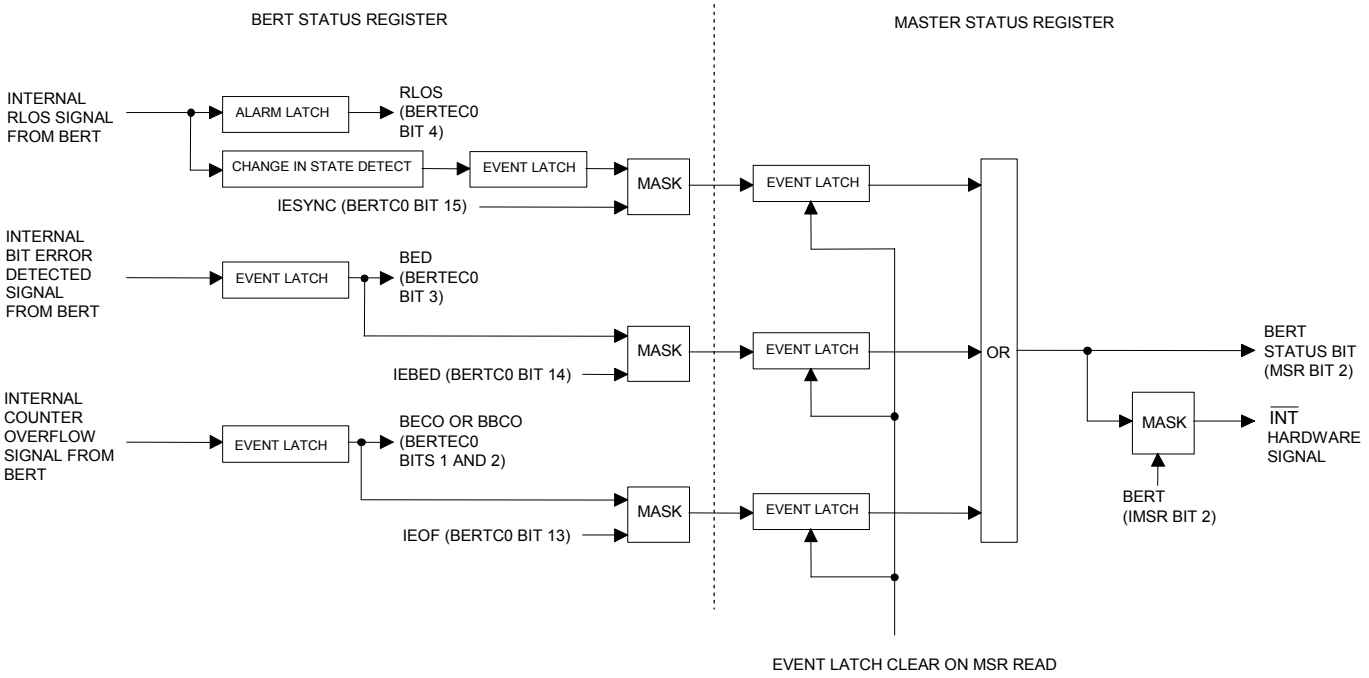


Figure 4.3E. HDLC STATUS BIT FLOW

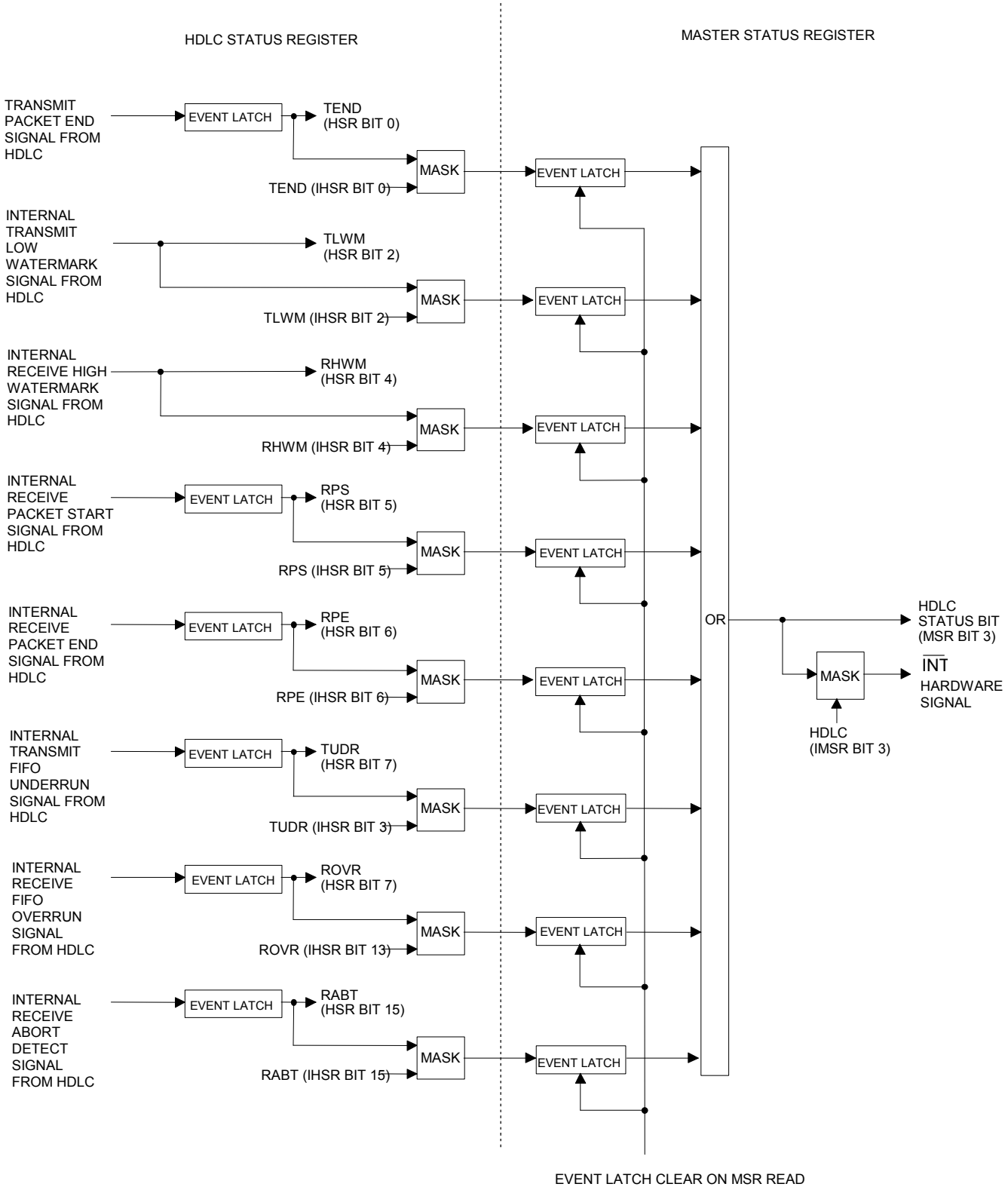
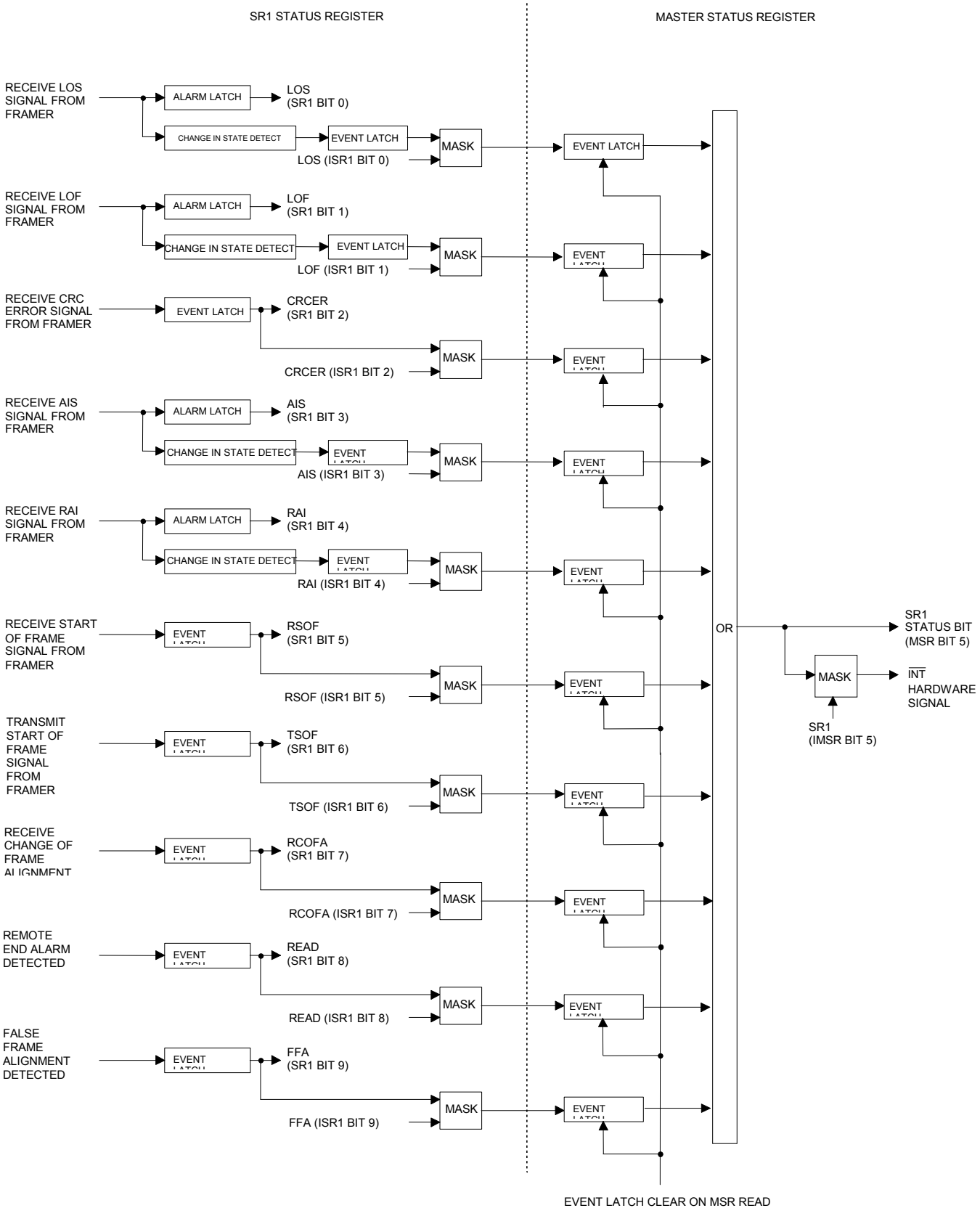


Figure 4.3F. SR1 STATUS BIT FLOW



Register Name: **IMSR**
Register Description: **Interrupt Mask for Master Status Register**
Register Address: **08h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	SR1	HDLC	BERT	COVF	OST
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	TXDRVR	LIULOS	N/A	LOTC
Default	0	0	0	0	0	0	0	0

Bit 0/One-Second-Timer Boundary Occurrence (OST)
0 = interrupt masked
1 = interrupt unmasked

Bit 1/Counter Overflow Event (COVF)
0 = interrupt masked
1 = interrupt unmasked

Bit 2/Change in BERT Status (BERT)
0 = interrupt masked
1 = interrupt unmasked

Bit 3/Change in HDLC Status (RHDLC)
0 = interrupt masked
1 = interrupt unmasked

Bit 4/Change in Framer/Formatter Status (SR1)
0 = interrupt masked
1 = interrupt unmasked

Bit 8/Loss-of-Transmit Clock (LOTC)
0 = interrupt masked
1 = interrupt unmasked

Bit 10/Analog Loss-of-Signal Detected (LIULOS)
0 = interrupt masked
1 = interrupt unmasked

Bit 11/Transmit Driver Monitor (TXDRVR)
0 = interrupt masked
1 = interrupt unmasked

5. FRAMER

5.1 General Description

On the receive side, the framer locates the frame boundaries of the incoming data stream and monitors the data stream for alarms and errors. Alarms are detected and reported in status register 1 (SR1) and the information register (INFO), which are described in Section 5.3. Errors are accumulated in a set of error counters (Section 5.4). The host can force the framer to resynchronize by the REFRM control bit in CR1 (Section 5.2). On the transmit side, the device formats the outgoing data stream with the proper framing pattern and overhead and can generate alarms. It can also inject errors for diagnostic testing purposes (see the EIC register). The transmit side of the framer is called the formatter.

Line Loopback

The line loopback loops the incoming data (i.e., RCLK, RPOS, and RNEG inputs) directly back to the transmit side (i.e., TCLK, TPOS, and TNEG outputs; Figure 1B). When this loopback is enabled, the incoming receive data continues to pass through the device, but the data output from the formatter is replaced with the data being input to the device. (See the block diagrams in Section 1 for a visual description of this loopback.)

Diagnostic Loopback

The diagnostic loopback loops the outgoing data from the formatter back to the receive side framer. When this loopback is enabled, the incoming receive data at RCLK, RPOS, and RNEG is ignored. (See the block diagrams in Section 1 for a visual description of this loopback.) Note that the device can still generate AIS at the TCLK, TPOS, and TNEG outputs when this loopback is invoked. This is important to keep the data that is being looped back from disturbing downstream equipment.

Payload Loopback

The payload loopback loops the framed data from the receive side framer back to the transmit side formatter. When this loopback is enabled, the incoming receive data continues to pass through the device but the data normally being input to the formatter is ignored. The overhead bits are regenerated by the formatter and inserted into the transmit stream. During payload loopback, the DS3160 internally connects FRCLK to FTCLK and FRSOF to FTSOF (FTSOF is set to the input mode). Clock and start-of-frame configurations are returned to user values when the loopback is disabled. (See the block diagrams in Section 1 for a visual description of this loopback.)

5.2 Framer Control Register Description

Register Name: **CR1**
Register Description: **Control Register 1**
Register Address: **0Ah**

Bit #	7	6	5	4	3	2	1	0
Name	TRAILOF	TRAILOS	TRAI	TSLOT1	TSLOT0	TPT	SIGPASS	PLB
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	AREFRM	REFRM	N/A	N/A	N/A	CRC5FM	ECC	FECC
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Payload Loopback Enable (PLB). See Figures 1A and 1B for a visual description of this loopback.

0 = disable loopback
1 = enable loopback

Bit 1/TS97 and TS98 Signaling Pass Through Enable (SIGPASS). Setting the SIGPASS bit allows the signaling bits contained in timeslots 97 and 98 on the FTD stream to pass transparently through the transmit formatter. When SIGPASS is a logic 0, timeslots 97 and 98 are sourced from the transmit TS97 and TS98 signaling insertion register (TXTS9798).

Bit 2/Transmit Pass Through Enable (TPT).

0 = enable the formatter to insert framing and overhead bits
1 = formatter does not insert any framing or overhead bits

Bits 3 and 4/Timeslot Select Bits 0 and 1 (TSLOT0 and TSLOT1). These bits are used to determine what timeslots are considered active by the signals FRDEN and FTDEN.

TSLOT1	TSLOT0	TIMESLOTS SELECTED
0	0	6Mbps (TS1–TS96)
0	1	4.5Mbps (TS1–TS72)
1	0	3Mbps (TS1–TS48)
1	1	1.5Mbps (TS1–TS24)

Figure 5.2A. FRDEN AND FTDEN 6Mbps TIMING

Bit #	1–8	9–16	17–24	753–760	761–768	769–776	777–784	785	786	787	788	789
Frame 1	TS1	TS2	TS3	TS95	TS96	TS97	TS98	1	1	0	0	m
Frame 2	TS1	TS2	TS3	TS95	TS96	TS97	TS98	1	0	1	0	0
Frame 3	TS1	TS2	TS3	TS95	TS96	TS97	TS98	x1`	x2	x3	a	m
Frame 4	TS1	TS2	TS3	TS95	TS96	TS97	TS98	e1	e2	e3	e4	e5

Figure 5.2B. FRDEN AND FTDEN 4.5Mbps TIMING

Bit #	1–8	569–576	577–584	761–768	769–776	777–784	785	786	787	788	789
Frame 1	TS1	TS72	TS73	TS96	TS97	TS98	1	1	0	0	m
Frame 2	TS1	TS72	TS73	TS96	TS97	TS98	1	0	1	0	0
Frame 3	TS1	TS72	TS73	TS96	TS97	TS98	x1`	x2	x3	a	m
Frame 4	TS1	TS72	TS73	TS96	TS97	TS98	e1	e2	e3	e4	e5

Figure 5.2C. FRDEN AND FTDEN 3Mbps TIMING

Bit #	1–8	377–384	385–392	761–768	769–776	777–-784	785	786	787	788	789
Frame 1	TS1	TS48	TS49	TS96	TS97	TS98	1	1	0	0	m
Frame 2	TS1	TS48	TS49	TS96	TS97	TS98	1	0	1	0	0
Frame 3	TS1	TS48	TS49	TS96	TS97	TS98	x1`	x2	x3	a	m
Frame 4	TS1	TS48	TS49	TS96	TS97	TS98	e1	e2	e3	e4	e5

Figure 5.2D. FRDEN AND FTDEN 1.5Mbps TIMING

Bit #	1–8	185–192	193–200	761–768	769–776	777–784	785	786	787	788	789
Frame 1	TS1	TS24	TS25	TS96	TS97	TS98	1	1	0	0	m
Frame 2	TS1	TS24	TS25	TS96	TS97	TS98	1	0	1	0	0
Frame 3	TS1	TS24	TS25	TS96	TS97	TS98	x1`	x2	x3	a	m
Frame 4	TS1	TS24	TS25	TS96	TS97	TS98	e1	e2	e3	e4	e5

Bit 5/Transmit Remote Alarm Indication (TRAI). When this bit is set high, the RAI pattern is sent on the M-bit.

0 = do not transmit RAI
1 = transmit RAI

Bit 6/Automatic Transmit Remote Alarm Indication on LOS (TRAILOS). When this bit is set high, the RAI pattern is sent on the M-bit automatically when the framer declares a loss-of-signal (LOS) occurrence. Transmission of RAI terminates when LOS is cleared.

0 = disable automatic RAI transmit
1 = enable automatic RAI transmit

Bit 7/Automatic Transmit Remote Alarm Indication on LOF (TRAILOF). When this bit is set high, the RAI pattern is sent on the M-bit automatically when the framer declares a loss-of-frame (LOF) occurrence. Transmission of RAI terminates when LOF is cleared.

0 = disable automatic RAI transmit
1 = enable automatic RAI transmit

Bits 8/Frame Error-Counting Control Bit (FECC). This bit is used to control what events are counted by the frame error counter. When this bit is set low, the counter accumulates LOF occurrences. When this bit is set high, the counter accumulates F-bit errors.

Bit 9/Error-Counting Control (ECC). This bit is used to control whether the device increments the error counters during LOF conditions. It affects the frame error counter only when it is configured to count frame errors, not LOF occurrences. When this bit is set low, the frame error counter and CRC error counter are not allowed to increment during LOF conditions. When this bit is set high, both counters are allowed to increment during LOF conditions.

0 = stop the FECR and CRCCR error counters from incrementing during LOF
1 = allow the FECR and CRCCR error counters to increment during LOF

Bit 10/CRC-5 Framing Mode (CRC5FM). When set, this bit enables an alternate framing algorithm that uses the CRC-5 check bits to validate framing in addition to the FAS bits. This reduces the chances of falsely framing to an emulator pattern in the frame. This algorithm declares frame synchronization after two or more of the first four FAS valid frames have correct CRC-5 check bits. If these criteria are not met, reframe is initiated at the FAS level. If CRC5FM is set to 0, the framing algorithm only searches for three consecutive multiframes with correct FAS patterns to declare frame synchronization.

0 = disable CRC qualified framing
1 = enable CRC qualified framing

Bit 14/Reframe (REFRM). The reframe bit forces the DS3160's receiver to begin searching for a new frame alignment. If the new frame alignment matches the previous alignment, there is no disruption in data or movement of the data-enable and start-of-frame signals. A 0-to-1 transition triggers the reframing.

Bit 15/Auto Reframe (AREFRM). Setting the auto-reframe bit to a 0 allows the DS3160 to begin searching for new frame alignment when an LOF has been declared.

0 = enable automatic reframe
1 = disable automatic reframe

Register Name: **CR2**
Register Description: **Control Register 2**
Register Address: **0Ch**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	ALTAIS	MEIMS	CRCI	LOFI	FBEI	EXZI	BPVI
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	IDLEFILL	LOSTHR1	LOSTHR0	RALMTH	X3	X2	X1	A
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Bipolar Violation Insert (BPVI). A 0-to-1 transition on this bit causes a single BPV to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive 1's to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted. In the manual-error-insert mode (MEIMS = 1), errors are inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors are inserted.

Bit 1/Excessive Zero Insert (EXZI). A 0-to-1 transition on this bit causes a single EXZ event to be inserted into the transmit data stream. An EXZ event is defined as eight or more consecutive 0's. Once this bit has been toggled from a 0 to a 1, the device waits for the next possible B8ZS code word insertion and it suppresses that code word from being inserted and, hence, this creates the EXZ event. This bit must be cleared and set again for a subsequent error to be inserted. In the manual-error-insert mode (MEIMS = 1), errors are inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors are inserted.

Bit 2/Frame Bit-Error Insert (FBEI). A 0-to-1 transition on this bit causes the transmit formatter to generate a framing bit error. Once this bit has been toggled from a 0 to a 1, the device waits for the next possible framing bit to insert the error. This bit must be cleared and set again for a subsequent error to be inserted. In the manual-error-insert mode (MEIMS = 1), errors are inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors are inserted. Only FAS bits are corrupted by this function.

Bit 3/Loss-of-Frame Error Insert (LOFI). A 0-to-1 transition on this bit causes the transmit formatter to generate seven consecutive multiframes with errors in the FAS pattern. Once this bit has been toggled from a 0 to a 1, the device waits for the next multiframe to begin error insertion. This bit must be cleared and set again for a subsequent error to be inserted. In the manual-error-insert mode (MEIMS = 1), errors are inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors are inserted. Only FAS bits are corrupted by this function.

Bit 4/CRC Error Insert (CRCI). A 0-to-1 transition on this bit causes the transmit formatter to generate a CRC-5 error. Once this bit has been toggled from a 0 to a 1, the device waits for the next possible CRC-5 word to insert the error. This bit must be cleared and set again for a subsequent error to be inserted. In the manual-error-insert mode (MEIMS = 1), errors are inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors are inserted. Only CRC-5 bits are corrupted by this function.

Bit 5/Manual-Error-Insert Mode Select (MEIMS). When this bit is set low, the device inserts errors on each 0-to-1 transition of the BPVI, EXZI, or FBEI control bits. When this bit is set high, the device inserts errors on each 0-to-1 transition of the FTMEI input signal. The appropriate BPVI, EXZI, or FBEI control bit must be set to 1 for this to occur. If all of the BPVI, EXZI, and FBEI control bits are set to 0, no errors are inserted.

0 = use 0-to-1 transition on the BPVI, EXZI, or FBEI control bits to insert errors
1 = use a 0-to-1 transition on the FTMEI input signal to insert errors

Bit 6/Alternate AIS Enable (ALTAIS). When set low, the device determines AIS using the default criteria. When set high, the device determines AIS using the alternate criteria. See Table 5.3A, *Alarm Criteria*, for additional details.

ALTAIS	SET CRITERIA	CLEAR CRITERIA
0	Two or fewer 0's among the four frames received	Three or more 0's among the four frames received
1	One or fewer 0's among 96 frames (75,744 bits) received	Two or more 0's among 96 frames (75,744 bits) received

Bit 8/Remote-End Alarm Bit (A). When set low, the device inserts a 0 in the A-bit position (bit 788 of the third frame in the multiframe). When set high, the device inserts a 1 in the A-bit position.

0 = set the A-bit to 0
1 = set the A-bit to 1

Bits 9, 10, 11/Spare Bits (X1, X2, X3). These control register bits determine what values are loaded into the spare bit locations (bits 785, 786, 787) of the third frame in the multiframe. X1 maps into bit 785; X2 maps into bit 786; X3 maps into bit 787. These bits should be set to a 1 if not used.

0 = set the X-bit to 0
1 = set the X-bit to 1

Bit 12/Remote-End Alarm-Detected Threshold (RALMTH). This bit selects the number of consecutive A-bits required to set and clear the remote-end alarm-detected status bit found in SR1.

0 = alarm set when the A-bit has been a logic 1 for three consecutive frames and reset when the A-bit has been a logic 0 for three consecutive frames
1 = alarm set when the A-bit has been a logic 1 for five consecutive frames and reset when the A-bit has been a logic 0 for five consecutive frames

Bits 13 and 14/Loss-of-Signal Threshold Select Bits 0 and 1 (LOSTHR0 and LOSTHR1). These bits are used to determine how many consecutive 0's must be received in order to declare a loss-of-signal (LOS) condition. See Table 5.3A, *Alarm Criteria*, for additional details.

LOSTHR1	LOSTHR0	CONSECUTIVE 0's REQUIRED
0	0	15
0	1	31
1	0	63
1	1	255

Bit 15/Idle Timeslot Fill Select (IDLEFILL). This bit determines whether 1's or 0's are inserted into the unused timeslots in the transmit path when the DS3160 is operated at fractional line rates. When this bit is set low, the unused channels are filled with 1's. When this bit is set high, the unused channels are filled with 0's.

ACTIVE TIMESLOTS	TIMESLOTS TO BE FILLED
6Mbps (TS1–TS96)	None
4.5Mbps (TS1–TS72)	TS73–TS96
3Mbps (TS1–TS48)	TS49–TS96
1.5Mbps (TS1–TS24)	TS25–TS96

Register Name: **TXTS9798**
Register Description: **Transmit TS97 and TS98 Signaling Insertion**
Register Address: **0Eh**

Bit #	7	6	5	4	3	2	1	0
Name	TS97_1	TS97_2	TS97_3	TS97_4	TS97_5	TS97_6	TS97_7	TS97_8
Default	1	1	1	1	1	1	1	1

Bit #	15	14	13	12	11	10	9	8
Name	TS98_1	TS98_2	TS98_3	TS98_4	TS98_5	TS98_6	TS98_7	TS98_8
Default	1	1	1	1	1	1	1	1

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 7/Transmit TS97 Signaling (TS97_1:TS97_8). These bits are used to set the contents of timeslot 97 (TS97) in the transmit data path. TS97_1 is the first bit of TS97 transmitted.

Bits 8 to 15/Transmit TS98 Signaling (TS98_1:TS98_8). These bits are used to set the contents of timeslot 98 (TS98) in the transmit data path. TS98_1 is the first bit of TS98 transmitted.

Note: No synchronization of the insertion of the TXTS9798 register contents with respect to the frame or timeslot is provided.

Register Name: **RXTS9798**
Register Description: **Receive TS97 and TS98 Monitor**
Register Address: **10h**

Bit #	7	6	5	4	3	2	1	0
Name	TS97_1	TS97_2	TS97_3	TS97_4	TS97_5	TS97_6	TS97_7	TS97_8
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit #	15	14	13	12	11	10	9	8
Name	TS98_1	TS98_2	TS98_3	TS98_4	TS98_5	TS98_6	TS98_7	TS98_8
Default	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 7/Receive TS97 Signaling (TS97_1:TS97_8). These bits contain the contents of timeslot 97 (TS97) in the receive data path. TS97_1 is the first bit of TS97 received.

Bits 8 to 15/Receive TS98 Signaling (TS98_1:TS98_8). These bits contain the contents of timeslot 98 (TS98) in the receive data path. TS98_1 is the first bit of TS98 received.

Note: The RXTS9798 register contents are real-time and are not integrated. Register content updates are not synchronized with byte, frame, or multiframe boundaries.

5.3 Framer Status and Interrupt Register Descriptions

Note: See Figure 5.3A for details about the signal flow for the status bits in the SR register.

Register Name: **SR1**
Register Description: **Status Register**
Register Address: **12h**

Bit #	7	6	5	4	3	2	1	0
Name	RCOFA	RSOF	TSOF	RAI	AIS	CRCER	LOF	LOS
Default	0	0	0	0	0	0	1	1

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	N/A	N/A	FFA	READ
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Loss-of-Signal Occurrence (LOS). This latched read-only alarm-status bit is set to a 1 when the framer detects a loss of signal. The signal FRD is forced to all 1's during an LOS condition. This bit is cleared when read unless an LOS condition still exists. A change in state of the LOS can cause a hardware interrupt to occur if the LOS bit in the interrupt mask for the SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read. The LOS alarm criteria is described in Table 5.3A.

Bit 1/Loss-of-Frame Occurrence (LOF). This latched read-only alarm-status bit is set to a 1 when the framer detects a loss of frame. This bit is cleared when read unless an LOF condition still exists. A change in state of the LOF can cause a hardware interrupt to occur if the LOF bit in the interrupt mask for the SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read. The LOF alarm criteria is described in Table 5.3A.

Bit 2/Receive CRC Error Detected (CRCER). This latched read-only event-status bit is set to a 1 as a result of detecting a CRC error in a received multiframe. This bit is cleared when read. The setting of this bit can cause a hardware interrupt to occur if the CRCER bit in the interrupt mask for the SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for the MSR (IMSR) register is set to a 1.

Bit 3/Alarm Indication Signal Detected (AIS). This latched read-only alarm-status bit is set to a 1 when the framer detects an incoming alarm indication signal. This bit is cleared when read unless an AIS signal is still present. A change in state of the AIS detection can cause a hardware interrupt to occur if the AIS bit in the interrupt mask for SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read. The AIS alarm detection criteria is described in Table 5.3A.

Bit 4/Remote Alarm Indication Detected (RAI). This latched read-only alarm-status bit is set to a 1 when the framer detects an incoming remote alarm indication (RAI) signal. This bit is cleared when read unless an RAI signal is still present. A change in state of the RAI detection can cause a hardware interrupt to occur if the RAI bit in the interrupt mask for SR1 (ISR1) register is set to a 1 and the SR1 bit in the

interrupt mask for MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read. The RAI alarm detection criteria is described in Table 5.3A.

Bit 5/Transmit Start of Frame (TSOF). This latched read-only event-status bit is set to a 1 on each transmit frame or multiframe boundary (see FTSOFM). This bit is a software version of the FTSOF hardware signal and it is cleared when read. The setting of this bit can cause a hardware interrupt to occur if the TSOF bit in the interrupt mask for SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for MSR (IMSR) register is set to a 1.

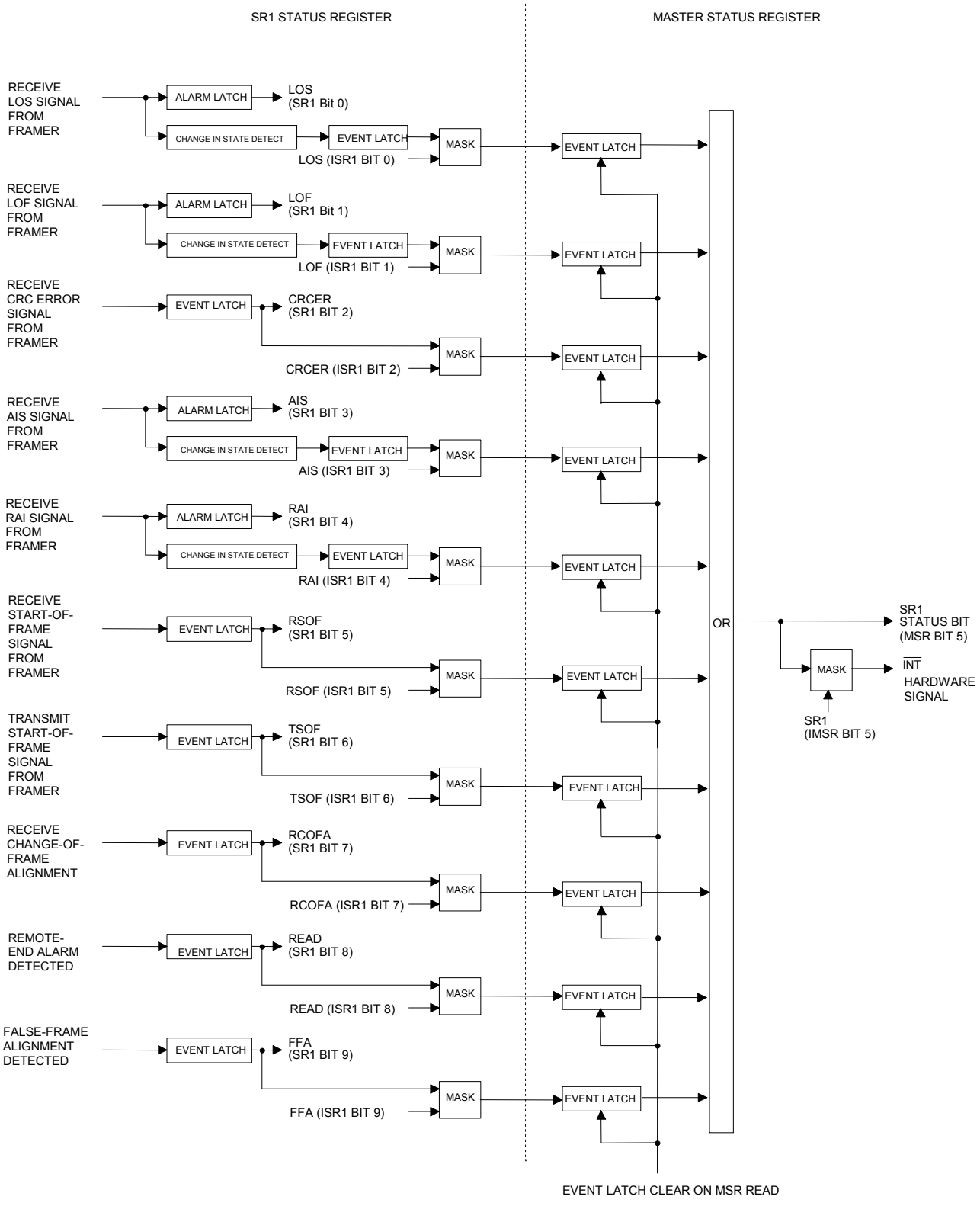
Bit 6/Receive Start of Frame (RSOF). This latched read-only event-status bit is set to a 1 on each receive frame or multiframe boundary (see FRSOFM). This bit is a software version of the FRSOF hardware signal and it is cleared when read. The setting of this bit can cause a hardware interrupt to occur if the RSOF bit in the interrupt mask for SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for MSR (IMSR) register is set to a 1.

Bit 7/Receive Change-of-Frame Alignment (RCOFA). This latched read-only event-status bit is set to a 1 when the framer has experienced a change-of-frame alignment (COFA). A COFA occurs when the device achieves synchronization in a different alignment than it had previously. If the device has never acquired synchronization before, then this status bit is meaningless. This bit is cleared when read and is not set again until the framer has lost synchronization and reacquired synchronization in a different alignment. The setting of this bit can cause a hardware interrupt to occur if the RCOFA bit in the interrupt mask for SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for MSR (IMSR) register is set to a 1.

Bit 8/Remote-End Alarm Detected (READ). This latched read-only alarm-status bit is set to a 1 when the framer detects a remote-end alarm (A-bit set to 1). This bit is cleared when read unless the remote-end alarm signal is present. A change in state of the remote-end alarm can cause a hardware interrupt to occur if the READ bit in the interrupt mask for SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read. The READ threshold can be set in CR2.

Bit 9/False-Frame Alignment (FFA). This latched read-only event-status bit is set to a 1 when 32 consecutive super frames have bad CRC. This feature can be used to assist in monitoring for false-frame alignment as described in JT-G706. This bit is cleared when read. The setting of this bit can cause a hardware interrupt to occur if the RSOF bit in the interrupt mask for SR1 (ISR1) register is set to a 1 and the SR1 bit in the interrupt mask for the MSR (IMSR) register is set to a 1.

Figure 5.3A. SR1 STATUS BIT FLOW



Register Name **ISR1**
Register Description: **Interrupt Mask for Status Register**
Register Address: **14h**

Bit #	7	6	5	4	3	2	1	0
Name	RCOFA	RSOF	TSOF	RAI	AIS	CRCER	LOF	LOS
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	N/A	N/A	FFA	READ
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Loss-of-Signal Occurrence (LOS)
0 = interrupt masked
1 = interrupt unmasked

Bit 1/Loss-of-Frame Occurrence (LOF)
0 = interrupt masked
1 = interrupt unmasked

Bit 2/Receive Multiframe CRC Error Occurrence (CRCER)
0 = interrupt masked
1 = interrupt unmasked

Bit 3/Alarm Indication Signal Detected (AIS)
0 = interrupt masked
1 = interrupt unmasked

Bit 4/Remote Alarm Indication Detected (RAI)
0 = interrupt masked
1 = interrupt unmasked

Bit 5/Transmit Start of Frame (TSOF)
0 = interrupt masked
1 = interrupt unmasked

Bit 6/Receive Start of Frame (RSOF)
0 = interrupt masked
1 = interrupt unmasked

Bit 7/Receive Change-of-Frame Alignment (RCOFA)
0 = interrupt masked
1 = interrupt unmasked

Bit 8/Remote-End Alarm Detected (READ)
0 = interrupt masked
1 = interrupt unmasked

Bit 9/False-Frame Alignment (FFA)
0 = interrupt masked
1 = interrupt unmasked

Table 5.3A. ALARM CRITERIA

ALARM/ CONDITION	DESCRIPTION	CRITERIA	
		SET	CLEAR
AIS	Alarm Indication Signal	Two or fewer “0” among the four frames received.	Three or more “0” among the four frames received.
ALTAIS	Alternate Alarm Indication Signal	One or fewer “0” among 96 frames (75,744 bits) received.	Two or more “0” among 96 frames (75,744 bits) received.
LOS	Loss of Signal	User-selectable threshold of 15, 31, 63, or 255 consecutive “0.”	No excessive 0 (EXZ) events over the selected threshold that starts with the first “1” received.
LOF	Loss of Frame	Reception of seven or more consecutive multiframes with erred frame alignment signal (FAS).	Reception of three or more consecutive multiframes with correct FAS patterns. Alternately, if CRC5FM is enabled, frame synchronization is declared after two or more of the first four FAS valid frames have correct CRC-5 check bits.
RAI	Remote Alarm Indication	Detection of “1111111100000000” pattern for 16 times or more continuously on the M-bit of the received frames.	When a pattern other than “1111111100000000” is detected four times or more consecutively on the M-bit in the received frames.

Register Name: **INFO**
Register Description: **Information Register**
Register Address: **16h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	X1	X2	X3	EXZ	FBE	ZSCD
Default	0	0	1	1	1	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	RAIC	AISC	LOFC	LOSC
Default	0	0	0	0	0	0	0	0

Note 1: Bits that are underlined are read-only; all other bits are read-write.

Note 2: The status bits in the INFO cannot cause a hardware interrupt to occur.

Bit 0/Zero Suppression Code Word Detected (ZSCD). This latched read-only event-status bit is set to a 1 when the framer has detected a B8ZS code word. This bit is cleared when read and is not set again until the framer has detected another B8ZS code word.

Bit 1/F-Bit or FAS Error Detected (FBE). This latched read-only event-status bit is set to a 1 when the DS3160 detects an error in the F-bits. This bit is cleared when read and is not set again until the device detects another error.

Bit 2/Excessive Zeros Detected (EXZ). This latched read-only event-status bit is set to a 1 each time the DS3160 detects a consecutive string of either eight or more 0's. A 0 is defined as no signal (pulses) on the line for one clock period. This bit is cleared when read and is not set again until the device detects another excessive zero event.

Bits 3, 4, 5/Spare Bits (X1, X2, X3). These register bits contain the real-time values of the spare bit locations (bits 785, 786, 787) of the third frame in the multiframe. X1 maps into bit 785. X2 maps into bit 786. X3 maps into bit 787. The DS3160 performs no integration on the spare bits.

Bit 8/Loss-of-Signal Clear Detected (LOSC). This latched read-only event-status bit is set to a 1 each time the framer exits an LOS state. This bit is cleared when read and is not set again until the device once again exits the LOS state. The LOS alarm criteria is described in Table 5.3A.

Bit 9/Loss-of-Frame Clear Detected (LOFC). This latched read-only event status bit is set to a 1 each time the framer exits an LOF state. This bit is cleared when read and is not be set again until the device once again exits the LOF state. The LOF alarm criteria is described in Table 5.3A.

Bit 10/Alarm Indication Signal Clear Detected (AISC). This latched read-only event-status bit is set to a 1 each time the framer no longer detects the AIS alarm state. This bit is cleared when read and is not set again until the device once again exits the AIS alarm state. The AIS alarm criteria is described in Table 5.3A.

Bit 11/Remote Alarm Indication Clear Detected (RAIC). This latched read-only event-status bit is set to a 1 each time the framer no longer detects the RAI alarm state. This bit is cleared when read and is not set again until the device once again exits the RAI alarm state. The RAI alarm criteria is described in Table 5.3A.

5.4 Performance Error Counters

There are four error counters in the DS3160. All of the error counters are 16 bits in length. The host has three options as to how these error counters are updated. The device can be configured to automatically update the counters once per second or manually by either an internal software bit (MECU) or an external signal (FRMECU). See Section 4.2 for details. All the error counters saturate when full and do not roll over.

Register Name: **BPVCR**
Register Description: **Bipolar Violation Count Register**
Register Address: **18h**

Bit #	7	6	5	4	3	2	1	0
Name	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 15/16-Bit Bipolar Violation Counter (BPV0 to BPV15). These bits report the number of bipolar violations (BPV). A BPV is defined as consecutive pulses (or marks) of the same polarity that are not part of a B8ZS code word.

Register Name: **EXZCR**
Register Description: **Excessive Zero Count Register**
Register Address: **1Ah**

Bit #	7	6	5	4	3	2	1	0
Name	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 15/16-Bit Excessive Zero Counter (EXZ0 to EXZ15). These bits report the number of excessive zero occurrences (EXZ). An EXZ occurrence is defined as eight or more consecutive 0's. A 0 is defined as no signal (pulses) on the line for one clock period. As an example, a string of 20 consecutive 0's would only increment this counter once.

Register Name: **FECR**
Register Description: **Frame Error-Count Register**
Register Address: **1Ch**

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 15/16-Bit Framing Bit Error Counter (FE0 to FE15). These bits report either the number of LOF occurrences or the number of framing bit errors received. The FECR is configured through the host by the frame-error-counting control bit (FECC) in the control register 1 (Section 5.2). The possible configurations are shown below.

FECC	FRAME ERROR-COUNT REGISTER (FECR) CONFIGURATION
0	Count LOF Occurrences
1	Count Only F-Bit Errors

When the FECR is configured to count LOF occurrences, the FECR increments by one each time the device loses receive synchronization. When the FECR is configured to count frame bit errors, it can be configured through the ECC control bit in the control register (Section 5.2) to either continue counting frame bit errors during an LOF or not.

Register Name: **CRCCR**
Register Description: **CRC Error-Count Register**
Register Address: **1Eh**

Bit #	7	6	5	4	3	2	1	0
Name	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 15/16-Bit CRC Error Counter (CRC0 to CRC15). These bits report the number of CRC errors received. The CRCCR can be configured by the ECC control bit in the control register (Section 5.2) to either continue counting CRC errors during an LOF or not.

6. BERT

6.1 General Description

The BERT block is capable of generating and detecting the following patterns:

- the pseudorandom patterns 2^7 - 1, 2^{11} - 1, 2^{15} - 1, and QRSS
- a repetitive pattern from 1 to 32 bits in length
- alternating (16-bit) words that flip every 1 to 256 words

The BERT receiver has a 32-bit bit counter and a 24-bit error counter. It can generate interrupts on detecting a bit error, a change in synchronization, or if an overflow occurs in the bit and error counters. See Section 6.2 for details on status bits and interrupts from the BERT block. To activate the BERT block, the host must configure the BERT mux by the BERT mux control register (Section 6.2).

6.2 BERT Register Description

Register Name: **BERTMC**
Register Description: **BERT Mux Control Register**
Register Address: **20h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	N/A	N/A	N/A	TBS1	TBS0	RBS1	RBS0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 1/Receive BERT Select Bits 0 to 1 (RBS0 to RBS1). These bits enable/disable the BERT receiver and select how BERT data is sent to the receiver (active timeslot bits only or active timeslot and the overhead bits).

RBSI	RBS0	DESCRIPTION
0	0	Disabled
0	1	Active Timeslots Only 6Mbps: TS1–TS96 4.5Mbps: TS1–TS72 3Mbps: TS1–TS48 1.5Mbps: TS1–TS24
1	0	Entire Frame including F-Bits (all 789 bits)
1	1	Illegal State

Bits 2 to 3/Transmit BERT Select Bits 0 to 1 (TBS0 to TBS1). These bits determine if the transmit BERT is used to replace the normal transmit data at the transmit formatter. If these bits are set to 01, data from the transmit BERT is only placed in the active timeslot bit positions of the data stream. If these bits are set to 10, then data from the transmit BERT is placed into all bit positions of the data stream (all timeslots and the overhead bits).

TBSI	TBS0	DESCRIPTION
0	0	Disabled
0	1	Active Timeslots Only 6Mbps: TS1–TS96 4.5Mbps: TS1–TS72 3Mbps: TS1–TS48 1.5Mbps: TS1–TS24
1	0	Entire Frame including F-Bits (all 789 bits)
1	1	Illegal State

Register Name: **BERTC0**
Register Description: **BERT Control Register 0**
Register Address: **22h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	TINV	RINV	PS2	PS1	PS0	LC	RESYNC
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	IESYNC	IEBED	IEOF	N/A	RPL3	RPL2	RPL1	RPL0
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Force Resynchronization (RESYNC). A low-to-high transition forces the receive BERT synchronizer to resynchronize to the incoming data stream. This bit should be toggled from low to high whenever the host wishes to acquire synchronization on a new pattern. Must be cleared and set again for a subsequent resynchronization.

Bit 1/Load Bit and Error Counters (LC). A low-to-high transition latches the current bit and error counts into the host accessible registers BERTBC0, BERTBC1 (bit count) and BERTEC0, BERTEC1 (error count), and clears the internal count. This bit should be toggled from low to high whenever the host wishes to begin a new read-acquisition period. Must be cleared and set again for a subsequent loads.

Bit 2/Pattern Select Bit 0 (PS0), Bit 3/Pattern Select Bit 0 (PS1), Bit 4/Pattern Select Bit 1 (PS2)

000 = Pseudorandom Pattern 2^7 - 1 (ANSI T1.403-1999 Annex B)
001 = Pseudorandom Pattern 2^{11} - 1 (ITU O.153)
010 = Pseudorandom Pattern 2^{15} - 1 (ITU O.151)
011 = Pseudorandom Pattern QRSS (2E20 - 1 with a 1 forced if the next 14 positions are 0)
100 = Repetitive Pattern
101 = Alternating Word Pattern
110 = Illegal State
111 = Illegal State

Bit 5/Receive Invert Data-Enable (RINV)

0 = do not invert the incoming data stream
1 = invert the incoming data stream

Bit 6/Transmit Invert Data-Enable (TINV)

0 = do not invert the outgoing data stream
1 = invert the outgoing data stream

Bit 8/Repetitive Pattern Length Bit 0 (RPL0), Bit 9/Repetitive Pattern Length Bit 1 (RPL1), Bit 10/Repetitive Pattern Length Bit 2 (RPL2), Bit 11/Repetitive Pattern Length Bit 3 (RPL3). RPL0 is the LSB and RPL3 is the MSB of a nibble that describes the length of the repetitive pattern. The valid range is 17 (0000) to 32 (1111). These bits are ignored if the receive BERT is programmed for a pseudorandom pattern. To create repetitive patterns less than 17 bits in length, the user must set the length to an integer number of the desired length that is less than or equal to 32. For example, to create a 6-bit pattern, the user can set the length to 18 (0001) or to 24 (0111) or to 30 (1101).

Repetitive Pattern Length Map

LENGTH (bits)	CODE	LENGTH (bits)	CODE	LENGTH (bits)	CODE	LENGTH (bits)	CODE
17	0000	18	0001	19	0010	20	0011
21	0100	22	0101	23	0110	24	0111
25	1000	26	1001	27	1010	28	1011
29	1100	30	1101	31	1101	32	1111

Bit 13/Interrupt Enable for Counter Overflow (IEOF). Allows the receive BERT to cause an interrupt if either the bit counter or the error counter overflows (Figure 6.2A).

0 = interrupt masked
1 = interrupt enabled

Bit 14/Interrupt Enable for Bit Error Detected (IEBED). Allows the receive BERT to cause an interrupt if a bit error is detected (Figure 6.2A).

0 = interrupt masked
1 = interrupt enabled

Bit 15/Interrupt Enable for Change-of-Synchronization Status (IESYNC). Allows the receive BERT to cause an interrupt if there is a change of state in the synchronization status (i.e., the receive BERT either goes into or out of synchronization) (Figure 6.2A).

0 = interrupt masked
1 = interrupt enabled

Register Name: **BERTC1**
Register Description: **BERT Control Register 1**
Register Address: **24h**

Bit #	7	6	5	4	3	2	1	0
Name	EIB2	EIB1	EIB0	SBE	N/A	N/A	N/A	TC
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	AWC7	AWC6	AWC5	AWC4	AWC3	AWC2	AWC1	AWC0
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Transmit Pattern Load (TC). A low-to-high transition loads the pattern generator with the repetitive or pseudorandom pattern that is to be generated. This bit should be toggled from low to high whenever the host wishes to load a new pattern. Must be cleared and set again for subsequent loads.

Bit 4/Single Bit-Error Insert (SBE). A low-to-high transition creates a single bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bit 5/Error Insert Bit 0 (EIB0), Bit 6/Error Insert Bit 1 (EIB1), Bit 7/Error Insert Bit 2 (EIB2). Automatically inserts bit errors at the prescribed rate into the generated data pattern. Useful for verifying error-detection operation.

EIB2	EIB1	EIB0	ERROR RATE INSERTED
0	0	0	No errors automatically inserted
0	0	1	10^{-1} (1 error per 10 bits)
0	1	0	10^{-2} (1 error per 100 bits)
0	1	1	10^{-3} (1 error per 1kb)
1	0	0	10^{-4} (1 error per 10kb)
1	0	1	10^{-5} (1 error per 100kb)
1	1	0	10^{-6} (1 error per 1Mb)
1	1	1	10^{-7} (1 error per 10Mb)

Bits 8 to 15/Alternating Word Count Rate (AWC0 to AWC7). When the BERT is programmed in the alternating word mode, the word in BERTRP0 is transmitted for the count loaded into this register plus one, then flips to the other word loaded in BERTRP1 and again repeats for the same number of times. The valid count range is from 00h to FFh.

AWC VALUE	ALTERNATING COUNT ACTION
00h	Send the word in BERTRP0 **1** time followed by the word in BERTRP1 **1** time…
01h	Send the word in BERTRP0 **2** times followed by the word in BERTRP1 **2** times…
02h	Send the word in BERTRP0 **3** times followed by the word in BERTRP1 **3** times…
06h	Send the word in BERTRP0 **7** times followed by the word in BERTRP1 **7** times…
07h	Send the word in BERTRP0 **8** times followed by the word in BERTRP1 **8** times…
FFh	Send the word in BERTRP0 **256** times followed by the word in BERTRP1 **256** times…

Register Name: **BERTRP0**
Register Description: **BERT Repetitive Pattern 0 (lower word)**
Register Address: **26h**

Bit #	7	6	5	4	3	2	1	0
Name	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
Default	0	0	0	0	0	0	0	0

Register Name: **BERTRP1**
Register Description: **BERT Repetitive Pattern 1 (upper word)**
Register Address: **28h**

Bit #	7	6	5	4	3	2	1	0
Name	RP23	RP22	RP21	RP20	RP19	RP18	RP17	RP16
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RP31	RP30	RP29	RP28	RP27	RP26	RP25	RP24
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 31/BERT Repetitive Pattern Set (RP0 TO RP31). RP0 is the LSB and RP31 is the MSB. These registers must be properly loaded for the BERT to properly generate and synchronize to either a repetitive pattern, a pseudorandom pattern, or an alternating word pattern. For a repetitive pattern that is fewer than 17 bits, the pattern should be repeated so that all 32 bits are used to describe the pattern. For example, if the pattern was the repeating 5-bit pattern …01101… (where the right-most bit is 1, sent first and received first), then BERTRP0 should be loaded with xB5AD and BERTRP1 should be loaded with x5AD6. For a pseudorandom pattern, both registers should be loaded with all 1's (i.e., xFFFF). For an alternating word pattern, one word should be placed into BERTRP0 and the other word should be placed into BERTRP1. For example, if the DDS stress pattern "7E" is to be described, the user would place x0000 in BERTRP0 and x7E7E in BERTRP1 and the alternating word counter would be set to 50 (decimal) to allow 100 bytes of 00h followed by 100 bytes of 7Eh to be sent and received.

Register Name: **BERTBC0**
Register Description: **BERT 32-Bit Bit Counter (lower word)**
Register Address: **2Ah**

Bit #	7	6	5	4	3	2	1	0
Name	BBC7	BBC6	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BBC15	BBC14	BBC13	BBC12	BBC11	BBC10	BBC9	BBC8
Default	0	0	0	0	0	0	0	0

Register Name: **BERTBC1**
Register Description: **BERT 32-Bit Bit Counter (upper word)**
Register Address: **2Ch**

Bit #	7	6	5	4	3	2	1	0
Name	BBC23	BBC22	BBC21	BBC20	BBC19	BBC18	BBC17	BBC16
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BBC31	BBC30	BBC29	BBC28	BBC27	BBC26	BBC25	BBC24
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 31/BERT 32-Bit Bit Counter (BBC0 to BBC31). This 32-bit counter increments for each data bit (i.e., clock received). This counter is not disabled when the receive BERT loses synchronization. It can be cleared by toggling the LC control bit in BERTC0. It saturates and does not rollover. Upon saturation, the BBCO status bit in the BERTEC0 register is set. This error counter starts counting when the BERT goes into receive synchronization (RLOS = 0 or SYNC = 1) and does not stop counting when the BERT loses synchronization. It is recommended that the host toggle the LC bit in the BERTC0 register once the BERT has synchronized and then toggle the LC bit again when the error-checking period is complete. If the device loses synchronization during this period, then the counting results are suspect.

The transition of the LC bit from low to high starts an update cycle. This update cycle has a latency of three clock periods from the setting of the LC bit from (0) to (1). Therefore, each read by the host requires a 475ns period (158.43ns x 3 clocks) to retrieve data from the BERT bit count registers.

Register Name **BERTEC0**
Register Description: **BERT 24-Bit Error Counter (lower) and Status Information**
Register Address: **2Eh**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	RA1	RA0	RLOS	BED	BBCO	BECO	SYNC
Default	0	0	0	1	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Real-Time Synchronization Status (SYNC). Read-only real-time status of the synchronizer (this bit is not latched). It is set when the incoming pattern matches for 32 consecutive bit positions. It is cleared when six or more bits out of 64 are received in error. This bit cannot cause a hardware interrupt to occur.

Bit 1/BERT Error-Counter Overflow (BECO). A latched read-only event-status bit that is set when the 24-bit BERT error counter (BEC) saturates. Cleared when read and is not set again until another overflow occurs (i.e., the BEC counter must be cleared and allowed to overflow again). The setting of this status bit can cause a hardware interrupt to occur if the IEOF bit in BERT control register 0 is set to a 1 and the BERT bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read (Figure 6.2A).

Bit 2/BERT Bit Counter Overflow (BBCO). A latched read-only event-status bit that is set when the 32-bit BERT bit counter (BBC) saturates. Cleared when read and is not set again until another overflow occurs (i.e., the BBC counter must be cleared and allowed to overflow again). The setting of this status bit can cause a hardware interrupt to occur if the IEOF bit in BERT control register 0 is set to a 1 and the BERT bit in the interrupt mask for MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read (Figure 6.2A).

Bit 3/Bit Error Detected (BED). A latched read-only event-status bit that is set when a bit error is detected. The receive BERT must be in synchronization for it to detect bit errors. This bit is cleared when read. The setting of this status bit can cause a hardware interrupt to occur if the IEBED bit in BERT control register 0 is set to a 1 and the BERT bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read (Figure 6.2A).

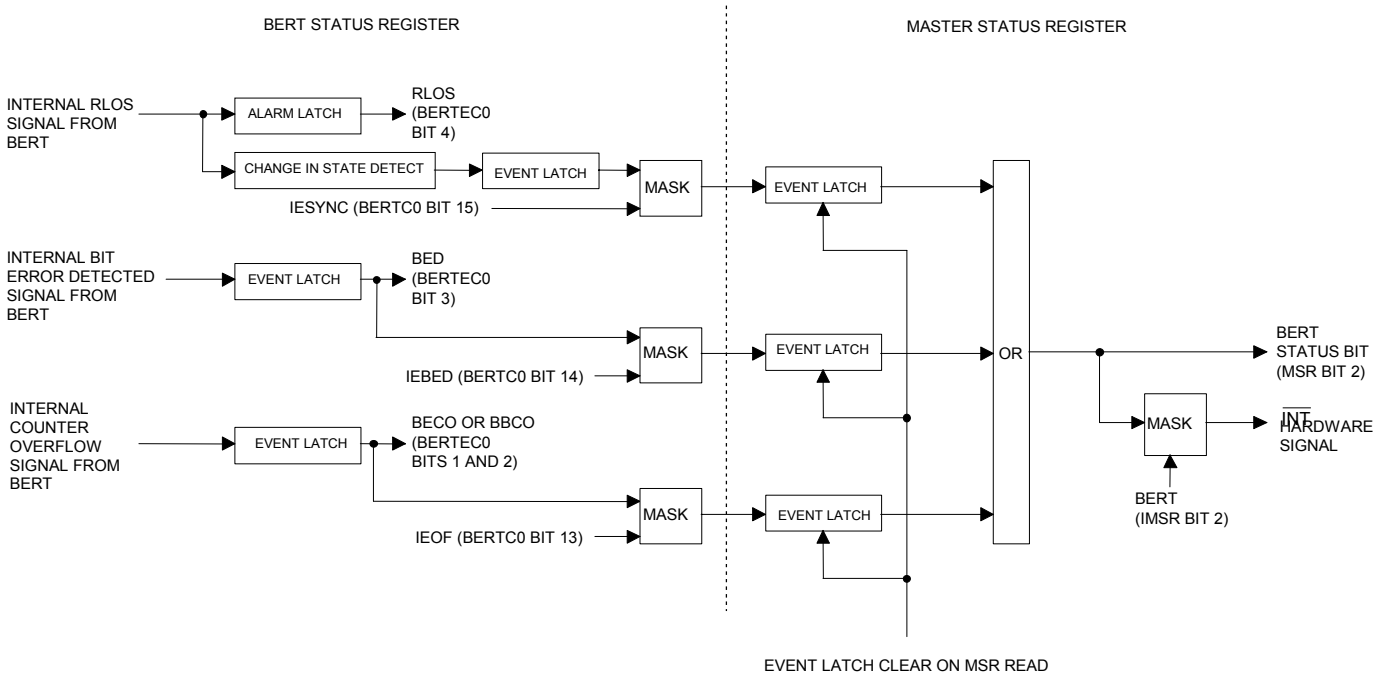
Bit 4/Receive Loss of Synchronization (RLOS). A latched read-only alarm-status bit that is set whenever the receive BERT begins searching for a pattern. Once synchronization is achieved, this bit remains set until read. A change in this status bit (i.e., the synchronizer goes into or out of synchronization) can cause a hardware interrupt to occur if the IESYNC bit in BERT control register 0 is set to a 1 and the BERT bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read (Figure 6.2A).

Bit 5/Receive All 0's (RA0). A latched read-only status bit that is set when 31 consecutive 0's are received. Allowed to be cleared once a 1 is received. This bit cannot cause a hardware interrupt to occur.

Bit 6/Receive All 1's (RA1). A latched read-only status bit that is set when 31 consecutive 1's are received. Allowed to be cleared once a 0 is received. This bit cannot cause a hardware interrupt to occur.

Bits 8 to 15/BERT 24-Bit Error Counter (BEC0 to BEC7). Lower byte of the 24-bit counter. See the BERTEC1 register description for details.

Figure 6.2A. BERT STATUS BIT FLOW



Register Name: **BERTEC1**
Register Description: **BERT 24-Bit Error Counter (upper)**
Register Address: **30h**

Bit #	7	6	5	4	3	2	1	0
Name	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bits 0 to 15/BERT 24-Bit Error Counter (BEC8 to BEC23). Upper two bytes of the 24-bit counter. This 24-bit counter increments for each data bit received in error. This counter is not disabled when the receive BERT loses synchronization; it can be cleared by toggling the LC control bit in BERTC0. This counter saturates and does not rollover. Upon saturation, the BECO status bit in the BERTEC0 register is set. This error counter starts counting when the BERT goes into receive synchronization (RLOS = 0 or SYNC = 1) and it does not stop counting when the BERT loses synchronization. It is recommended that the host toggle the LC bit in BERTC0 register once the BERT has synchronized and then toggle the LC bit again when the error-checking period is complete. If the device loses synchronization during this period, then the counting results are suspect.

As stated in the LC bit description section, the LC bit must be toggled from low to high to begin an update cycle. This update cycle has a latency of three clock periods from the setting of the LC bit from (0) to (1). Therefore, each read by the host requires a 475ns period (158.43ns x 3 clocks) to retrieve data from the BERT error count registers.

7. HDLC CONTROLLER

7.1 General Description

The DS3160 contains an on-board HDLC controller with 256-byte buffers in the transmit and receive paths.

Receive Operation

On reset, the receive HDLC controller flushes the receive FIFO and begins searching for a new incoming HDLC packet. The receive HDLC controller performs a bit by bit search for an HDLC packet and when one is detected, it zero destuffs the incoming data stream and automatically byte aligns to it and places the incoming bytes as they are received into the receive FIFO. The first byte of each packet is marked in the receive FIFO by setting the opening byte (OBYTE) bit. Upon detecting a closing flag, the device checks the 16-bit CRC to see if the packet is valid or not and then marks the last byte of the packet in the receive FIFO by setting the closing byte (CBYTE) bit. The CRC is not passed to the receive FIFO. When the CBYTE is set, the host can obtain the status of the incoming packet through the packet status bits (PS0 and PS1). Incoming packets can be separated by a single flag or even by two flags that share a common 0. If the receive FIFO ever fills beyond capacity, the new incoming packet data is discarded and the receive FIFO overrun (ROVR) status bit is set. If such a scenario occurs, then the last packet in the FIFO is suspect and should be discarded. When an overflow occurs, the receive HDLC stops accepting packets until either the FIFO is completely emptied or reset. If the receive HDLC controller ever detects an incoming abort (seven or more 1's in a row), it sets the receive-abort-sequence-detected (RABT) status bit. If an abort sequence is detected in the middle of an incoming packet, then the receive HDLC controller sets the packet status bits accordingly.

The receive HDLC has been designed to minimize its real-time host-support requirements. The receive FIFO is 256 bytes, which is deep. The host is notified when a new message has begun (receive-packet-start status bit) to be received and when a packet has completed (receive-packet-end status bit). Also the host can be notified when the FIFO has filled beyond a programmable level called the high watermark. The host reads the incoming packet data out of the receive FIFO a byte at a time. When the receive FIFO is empty, the REMPTY bit in the FIFO is set.

Transmit Operation

On reset, the transmit HDLC controller flushes the transmit FIFO and transmits an abort followed by either 7Eh or FFh (depending on the setting of the TFS control bit) continuously. The transmit HDLC then waits until there are at least two bytes in the transmit FIFO before beginning to send the packet. The transmit HDLC automatically adds an opening flag of 7Eh to the beginning of the packet and zero stuffs the outgoing data stream. When the transmit HDLC controller detects that the TMEND bit in the transmit FIFO is set, it automatically calculates and adds in the 16-bit CRC checksum, followed by a closing flag of 7Eh. If the FIFO is empty, then it begins sending either 7Eh or FFh continuously. If there is some more data in the FIFO, then the transmit HDLC automatically adds in the opening flag and sends the next packet. Between consecutive packets there is always at least two flags of 7Eh. If the transmit FIFO ever empties when a packet is being sent (i.e., before the TMEND bit is set), then the transmit HDLC controller sends an abort of seven 1's in a row (FEh), followed by a continuous transmission of either 7Eh (flags) or FFh (idle), and the transmit-FIFO-underrun (TUDR) status bit is set. When the FIFO underruns, the transmit HDLC controller should be reset by the host.

The transmit HDLC has been designed to minimize its real-time host support requirements. The transmit FIFO is 256 bytes. Once the host has loaded an outgoing packet, it can monitor the transmit packet-end (TEND) status bit to know when the packet has finished being transmitted. The host also can be notified when the FIFO has emptied below a programmable level called the low watermark. The host must never overfill the FIFO. To keep this from occurring, the host can obtain the real-time depth of the transmit FIFO by the transmit FIFO level bits in the HDLC status register (HSR).

The transmit remote-alarm indication (TRAI) function shares M-bits with the HDLC controller. Transmission of RAI does not interrupt an outgoing HDLC frame in progress. Transmission of RAI can only occur when the HDLC controller is in the idle state (sending flags or idles between transmit frames). An HDLC packet can interrupt an RAI transmission. Transmission of the RAI resumes when the HDLC packet is finished being sent.

7.2 HDLC Control and FIFO Register Description

Register Name: **HCR**
Register Description: **HDLC Control Register**
Register Address: **32h**

Bit #	7	6	5	4	3	2	1	0
Name	N/A	RHR	THR	TFS	N/A	TCRCI	TZSD	TCRCD
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RHWMS2	RHWMS1	RHWMS0	TLWMS2	TLWMS1	TLWMS0	RID	TID
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Transmit CRC Defeat (TCRCD). When this bit is set low, the HDLC automatically calculates and appends the 16-bit CRC to the outgoing HDLC message. When this bit is set high, the device does not append the CRC to the outgoing message.

0 = enable CRC generation (normal operation)
1 = disable CRC generation

Bit 1/Transmit Zero Stuffer Defeat (TZSD). When this bit is set low, the HDLC automatically enables the zero stuffer in between the opening and closing flags of the HDLC message. When this bit is set high, the device does not enable the zero stuffer under any condition.

0 = enable zero stuffer (normal operation)
1 = disable zero stuffer

Bit 2/Transmit CRC Invert (TCRCI). When this bit is set low, the HDLC allows the CRC to be generated normally. When this bit is set high, the device inverts all 16 bits of the generated CRC. This bit is ignored when the CRC generation is disabled (TCRCD = 1). This bit is useful in testing HDLC operation.

0 = do not invert the generated CRC (normal operation)
1 = invert the generated CRC

Bit 4/Transmit Flag/Idle Select (TFS). This control bit determines whether flags or idle bytes are transmitted in between packets.

0 = 7Eh (flags)
1 = FFh (idle)

Bit 5/Transmit HDLC Reset (THR). A 0-to-1 transition resets the transmit HDLC controller. Must be cleared and set again for a subsequent reset. A reset flushes the current contents of the transmit FIFO and causes one FEh abort sequence (seven 1's in a row) to be sent followed by either 7Eh (flags) or FFh (idle) until a new packet is initiated by writing new data (at least two bytes) into the FIFO.

Bit 6/Receive HDLC Reset (RHR). A 0-to-1 transition resets the receive HDLC controller. Must be cleared and set again for a subsequent reset. A reset flushes the current contents of the receive FIFO and causes the receive HDLC controller to begin searching for a new incoming HDLC packet.

Bit 8/Transmit Invert Data (TID). The control bit determines whether all of the data from the HDLC controller (including flags and CRC checksum) are inverted after processing.

0 = do not invert data (normal operation)
1 = invert all data

Bit 9/Receive Invert Data (RID). The control bit determines whether all of the data into the HDLC controller (including flags and CRC checksum) are inverted before processing.

0 = do not invert data (normal operation)
1 = invert all data

Bits 10 to 12/Transmit Low Watermark Select Bits (TLWMS0 to TLWMS2). These control bits determine when the HDLC controller should set the TLWM status bit in the HDLC status register (HSR). The TLWM status bit is set to a 1 when the transmit FIFO contains less than the number of bytes configured by these bits.

TLWMS2	TLWMS1	TLWMS0	TRANSMIT LOW WATERMARK (BYTES)
0	0	0	16
0	0	1	48
0	1	0	80
0	1	1	112
1	0	0	144
1	0	1	176
1	1	0	208
1	1	1	240

Bits 13 to 15/Receive High Watermark Select Bits (RHWMS0 to RHWMS2). These control bits determine when the HDLC controller should set the RHWM status bit in the HDLC status register (HSR). The RHWM status bit is set to a 1 when the receive FIFO contains more than the number of bytes configured by these bits.

RHWMS2	RHWMS1	RHWMS0	RECEIVE HIGH WATERMARK (BYTES)
0	0	0	16
0	0	1	48
0	1	0	80
0	1	1	112
1	0	0	144
1	0	1	176
1	1	0	208
1	1	1	240

Register Name: **RHDLC**
Register Description: **Receive HDLC FIFO**
Register Address: **34h**

Note: When the CPU bus is operated in the 8-bit mode (CMS = 1), the host should always read the lower byte (bits 0 to 7) first followed by the upper byte (bits 8 to 15).

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	PS1	PS0	CBYTE	OBYTE
Default	0	0	0	0	0	0	0	0

Note 1: Bits that are underlined are read-only; all other bits are read-write.

Note 2: Packets with three or fewer bytes (including the CRC FCS) in between flags are invalid and the data that appears in the FIFO in such instances is meaningless. If only one byte is received between flags, then both the CBYTE and OBYTE bits are set. If two bytes are received, then OBYTE is set for the first one received and CBYTE is set for the second byte received. If three bytes are received, then OBYTE is set for the first one received and CBYTE is set for the third byte received. In all of these cases, the packet status is reported as PS0 = 0 / PS1 = 1, and the data in the FIFO should be ignored.

Bits 0 to 7/Receive FIFO Data (D0 to D7). Data from the receive FIFO can be read from these bits. D0 is the LSB and is received first while D7 is the MSB and is received last.

Bit 8/Opening Byte (OBYTE). This bit is set to a 1 when the byte available at the D0 to D7 bits from the receive FIFO is the first byte of an HDLC packet.

Bit 9/Closing Byte (CBYTE). This bit is set to a 1 when the byte available at the D0 to D7 bits from the receive FIFO is the last byte of an HDLC packet whether the packet is valid or not. The host can use the PS0 and PS1 bits to determine if the packet is valid or not.

Bits 10 and 11/Packet Status Bits 0 and 1 (PS0 and PS1). These bits are only valid when the CBYTE bit is set to a 1. These bits inform the host of the validity of the incoming packet and the cause of the problem if the packet was received in error.

PS1	PS0	PACKET STATUS	REASON FOR INVALID RECEPTION OF THE PACKET
0	0	Valid	—
0	1	Invalid	Corrupt CRC
1	0	Invalid	Incoming packet was either too short (three or fewer bytes including the CRC) or did not contain an integral number of octets
1	1	Invalid	Abort sequence detected

Register Name: **THDLC**
Register Description: **Transmit HDLC FIFO**
Register Address: **36h**

Note: When the CPU bus is operated in the 8-bit mode (CMS = 1), the host should always write to the lower byte (bits 0 to 7) first followed by the upper byte (bits 8 to 15).

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	N/A	N/A	N/A	TMEND
Default	0	0	0	0	0	0	0	0

Note 1: The THDLC is a write-only register.

Note 2: The transmit FIFO can be filled to a maximum capacity of 256 bytes. When the transmit FIFO is full, it does not accept any additional data.

Bits 0 to 7/Transmit FIFO Data (D0 to D7). Data for the transmit FIFO can be written to these bits. D0 is the LSB and is transmitted first while D7 is the MSB and is transmitted last.

Bit 8/Transmit Message End (TMEND). This bit is used to delineate multiple messages in the transmit FIFO. It should be set to a 1 when the last byte of a packet is written to the transmit FIFO. The setting of this bit indicates to the HDLC controller that the message is complete and that it should calculate and add in the CRC check sum and at least two flags. This bit should be set to 0 for all other data written to the FIFO. All HDLC messages must be at least 2 bytes in length.

7.3 HDLC Status and Interrupt Register Description

Note: See Figure 7.2A for details on the signal flow for the status bits in the HSR register.

Register Name: **HSR**
Register Description: **HDLC Status Register**
Register Address: **38h**

Bit #	7	6	5	4	3	2	1	0
Name	TUDR	RPE	RPS	RHWM	N/A	TLWM	N/A	TEND
Default	0	0	0	0	0	1	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RABT	REMPTY	ROVR	TEMPTY	TFL3	TFL2	TFL1	TFL0
Default	0	1	0	1	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Transmit Packet End (TEND). This latched read-only event-status bit is set to a 1 each time the transmit HDLC controller reads a transmit FIFO byte with the corresponding TMEND bit set, or if an FIFO underrun occurs. This bit is cleared when read and is not set again until another message end is detected. The setting of this bit can cause a hardware interrupt to occur if the TEND bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Bit 2/Transmit FIFO Low Watermark (TLWM). This read-only real-time status bit is set to a 1 when the transmit FIFO contains less than the number of bytes configured by the transmit low-watermark setting control bits (TLWMS0 to TLWMS2) in the HDLC control register (HCR). This bit is cleared when the FIFO fills beyond the low watermark. The setting of this bit can cause a hardware interrupt to occur if the TLWM bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1.

Bit 4/Receive FIFO High Watermark (RHWM). This read-only real-time status bit is set to a 1 when the receive FIFO contains more than the number of bytes configured by the receive high-watermark setting control bits (RHWMS0 to RHWMS2) in the HDLC control register (HCR). This bit is cleared when the FIFO empties below the high watermark. The setting of this bit can cause a hardware interrupt to occur if the RHWM bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1.

Bit 5/Receive Packet Start (RPS). This latched read-only event-status bit is set to a 1 each time the HDLC controller detects an opening byte of an HDLC packet. This bit is cleared when read and is not set again until another message is detected. The setting of this bit can cause a hardware interrupt to occur if the RPS bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Bit 6/Receive Packet End (RPE). This latched read-only event-status bit is set to a 1 each time the HDLC controller detects the finish of a message whether the packet is valid (CRC correct) or not (bad

CRC, abort sequence detected, packet too small, not an integral number of octets, or an overrun occurred). This bit is cleared when read and is not set again until another message end is detected. The setting of this bit can cause a hardware interrupt to occur if the RPE bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Bit 7/Transmit FIFO Underrun (TUDR). This latched read-only event-status bit is set to a 1 each time the transmit FIFO underruns and an abort is automatically sent. This bit is cleared when read and is not set again until another underrun occurs (i.e., the FIFO has been written to and then allowed to empty again). The setting of this bit can cause a hardware interrupt to occur if the TUDR bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Bit 8 to 11/Transmit FIFO Level Bits 0 to 3 (TFL0 to TFL3). These read-only real-time status bits indicate the current depth of the transmit FIFO with a 16-byte resolution. These status bits cannot cause a hardware interrupt.

TFL3	TFL2	TFL1	TFL0	TRANSMIT FIFO LEVEL (BYTES)
0	0	0	0	Empty to 15
0	0	0	1	16 to 31
0	0	1	0	32 to 47
0	0	1	1	48 to 63
0	1	0	0	64 to 79
0	1	0	1	80 to 95
0	1	1	0	96 to 111
0	1	1	1	112 to 127
1	0	0	0	128 to 143
1	0	0	1	144 to 159
1	0	1	0	160 to 175
1	0	1	1	176 to 191
1	1	0	0	192 to 207
1	1	0	1	208 to 223
1	1	1	0	224 to 239
1	1	1	1	240 to 256

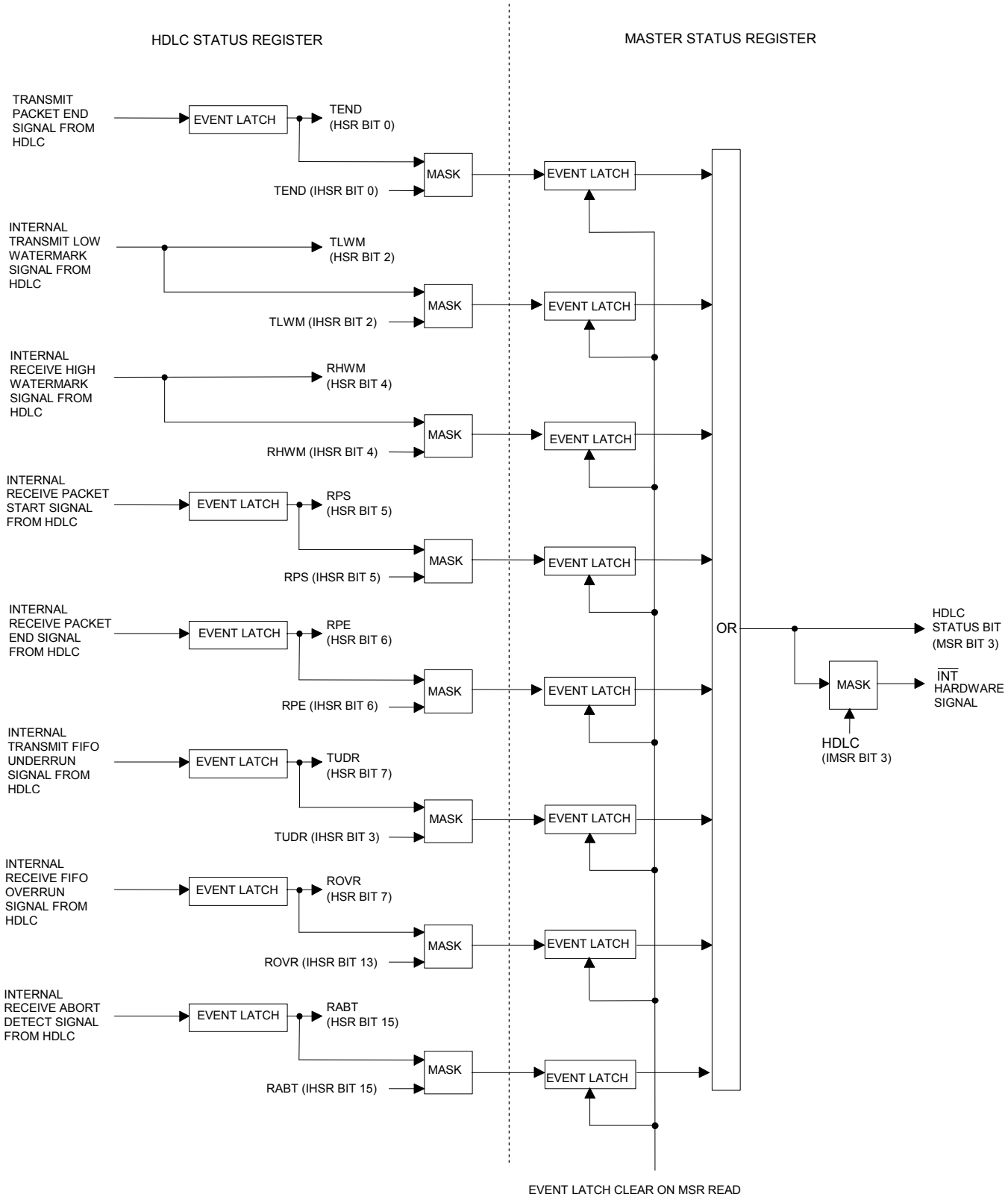
Bit 12/Transmit FIFO Empty (TEMPTY). This read-only real-time status bit is set to a 1 when the transmit FIFO is empty. It is cleared when the transmit FIFO contains one or more bytes. This status bit cannot cause a hardware interrupt.

Bit 13/Receive FIFO Overrun (ROVR). This latched read-only event-status bit is set to a 1 each time the receive FIFO overruns. This bit is cleared when read and is not set again until another overrun occurs (i.e., the FIFO has been read from and then allowed to fill up again). The setting of this bit can cause a hardware interrupt to occur if the ROVR bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Bit 14/Receive FIFO Empty (REMPTY). This read-only real-time bit is set to a 1 when the receive FIFO is empty. It is cleared when the receive FIFO contains one or more bytes. This status bit cannot cause a hardware interrupt.

Bit 15/Receive Abort Sequence Detected (RABT). This latched read-only event-status bit is set to a 1 each time the receive HDLC controller detects seven or more 1's in a row during packet reception. If the receive HDLC is not currently receiving a packet, then seven or more 1's in a row do not trigger this status bit. This bit is cleared when read and is not set again until another abort is detected (at least one valid flag must be detected before another abort can be detected). The setting of this bit can cause a hardware interrupt to occur if the RABT bit in the interrupt mask for the HSR (IHSR) register is set to a 1 and the HDLC bit in the interrupt mask for the MSR (IMSR) register is set to a 1. The interrupt is allowed to clear when this bit is read.

Figure 7.2A. HSR STATUS BIT FLOW



Register Name: **IHSR**
Register Description: **Interrupt Mask for HDLC Status Register**
Register Address: **3Ah**

Bit #	7	6	5	4	3	2	1	0
Name	TUDR	RPE	RPS	RHWM	N/A	TLWM	N/A	TEND
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RABT	N/A	ROVR	N/A	N/A	N/A	N/A	N/A
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read-only; all other bits are read-write.

Bit 0/Transmit Packet End (TEND)
0 = interrupt masked
1 = interrupt unmasked

Bit 2/Transmit FIFO Low Watermark (TLWM)
0 = interrupt masked
1 = interrupt unmasked

Bit 4/Receive FIFO High Watermark (RHWM)
0 = interrupt masked
1 = interrupt unmasked

Bit 5/Receive Packet Start (RPS)
0 = interrupt masked
1 = interrupt unmasked

Bit 6/Receive Packet End (RPE)
0 = interrupt masked
1 = interrupt unmasked

Bit 7/Transmit FIFO Underrun (TUDR)
0 = interrupt masked
1 = interrupt unmasked

Bit 13/Receive FIFO Overrun (ROVR)
0 = interrupt masked
1 = interrupt unmasked

Bit 15/Receive Abort Sequence Detected (RABT)
0 = interrupt masked
1 = interrupt unmasked

8. LINE INTERFACE UNIT

The line interface unit (LIU) performs all of the functions necessary for interfacing at the physical layer lines. The device has independent receive and transmit paths (Figure 1B). The receiver performs clock and data recovery and monitors for the loss of the incoming signal. The transmitter accepts data from the formatter and creates the waveforms that are driven onto the coaxial (coax) cable.

Receiver

The DS3160 interfaces to the receive coax line by a 1:1 transformer (Figure 8A). The receiver automatically adapts to coax cable losses from 0 to 15dB, which translates into 0 to 380m of coax cable (AT&T 734A or equivalent). The receiver has excellent jitter tolerance characteristics.

The receiver contains an analog LOS detector, which resides in the equalizer. If the incoming signal drops below -18dB (typ) of the nominal signal level, the analog LOS detector activates and it squelches the recovered data and forces all 0's out of the data recovery circuitry. The analog LOS detector does not clear until the signal level is above -14dB (typ) of the nominal signal level. While the device is in a loss of signal state, the RCLK output is referenced to the MCLK input.

Tx+ and Tx- Transmitter

The clock applied at the FTCLK input is used to transmit data out onto the JT2 line. Hence, FTCLK must be of transmission quality (i.e., accurate to ±30ppm). The duty cycle of FTCLK is not a key parameter as long as the clock high and low times listed in Section 11 are met.

The DS3160 interfaces to the transmit JT2 coax cable by a 1:1 transformer (Table 8A and Figure 8C). It drives the 75Ω cable and creates the proper waveforms required for interfacing to JT2 lines. The transmitter can be disabled and the Tx+ and Tx- outputs tri-stated by the master configuration register (MC1). See Section 4 for details.

Jitter Attenuator

The DS3160 contains an on-board jitter attenuator that can be placed in either the receive path or the transmit path or disabled. Options are selected through the master configuration register (MC1). See Section 4.2 in this data sheet for selection details and register bit settings.

The jitter attenuator consists of a narrowband PLL to retime the LIU master clock (MCLK), a 16 x 2-bit FIFO to buffer the associated data while the clock is being retimed, and logic to prevent over/underflow of the FIFO in the presence of very large jitter amplitudes. The PLL requires a stable, accurate clock on MCLK. It has a loop bandwidth of 98.1Hz, and attenuates jitter at frequencies higher than the loop bandwidth while allowing jitter (and wander) at lower frequencies to pass through relatively unaffected. Figure 8B shows an example of jitter attenuation versus frequency.

Figure 8A. EXTERNAL CONNECTION

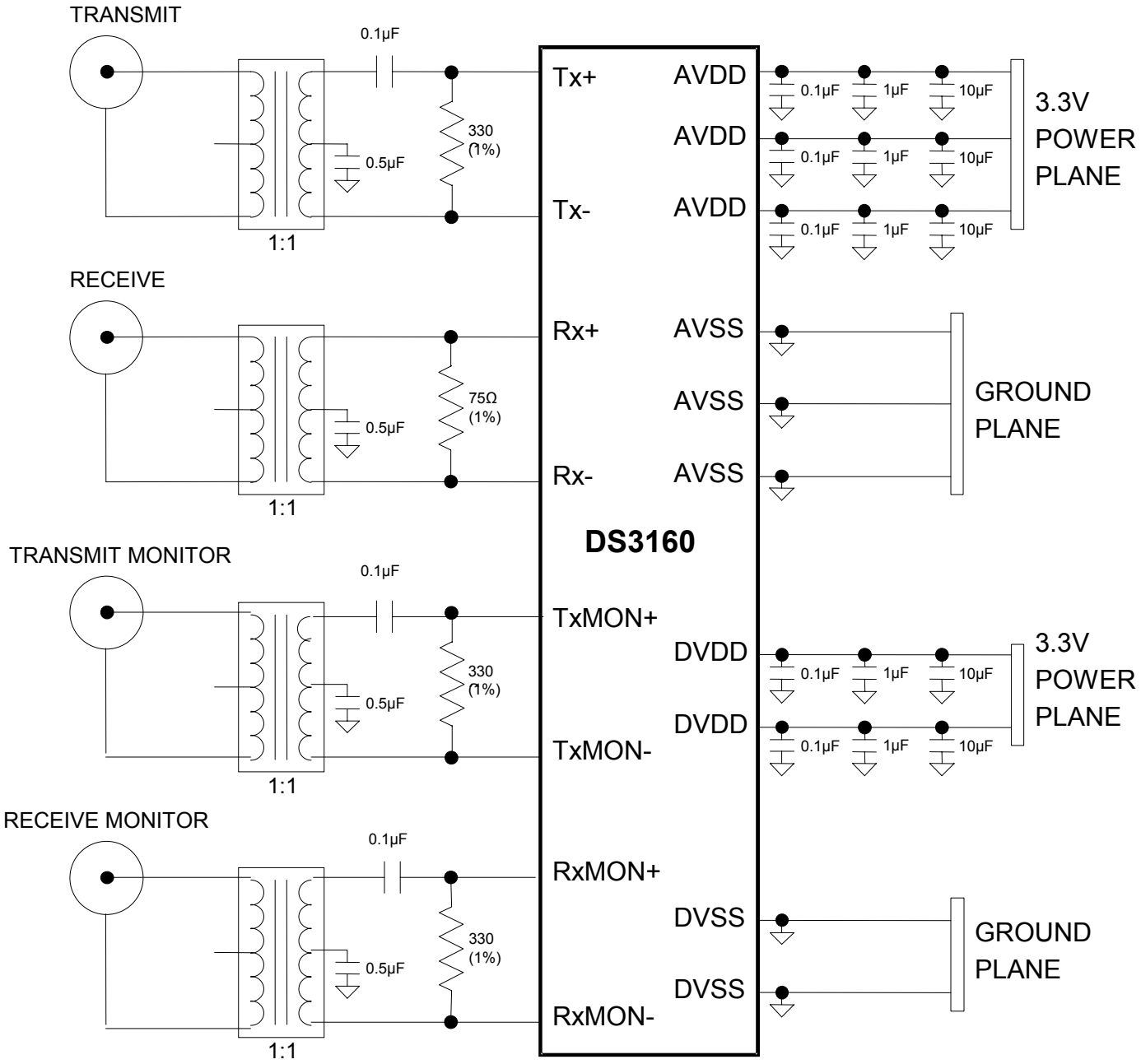


Figure 8B. DS3160 JITTER ATTENUATION/TRANSFER

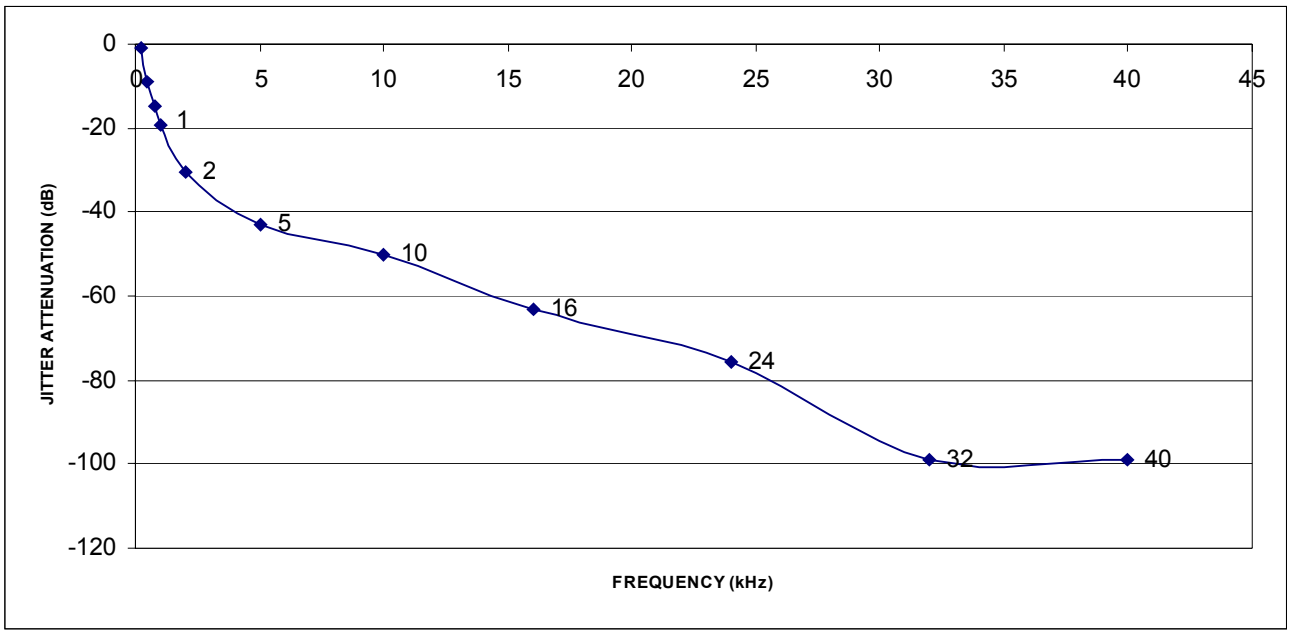


Table 8A. JT2 TRANSMIT WAVEFORM TEST PARAMETERS AND LIMITS

PARAMETER	SPECIFICATION
Rate	6.312Mbps (±30ppm)
Line Code	50% pulse width B8ZS
Transmission Medium	75Ω coax cable
Test Measurement Point	At the output equipment terminal
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	Between $1.7V_{o-p}$ to $2.3V_{o-p}$
Pulse Shape	An isolated pulse (preceded by two 0's and followed by one or more 0's) falls within the curve listed in Figure 8C.

Table 8B. TRANSFORMER SPECIFICATIONS

PARAMETER	RECOMMENDED VALUE AT +25°C
Turns Ratio	1:1
Open Circuit Primary Inductance (L_{MIN})	780µH
Leakage Inductance (L_L)	200nH
DC Resistance (R_{DC})	0.32Ω
Frequency Response	0.005MHz to 100MHz

Note: Transformer recommendation includes Coilcraft WB3010-PC.

Figure 8C. OUTPUT SIGNAL WAVEFORM MASK

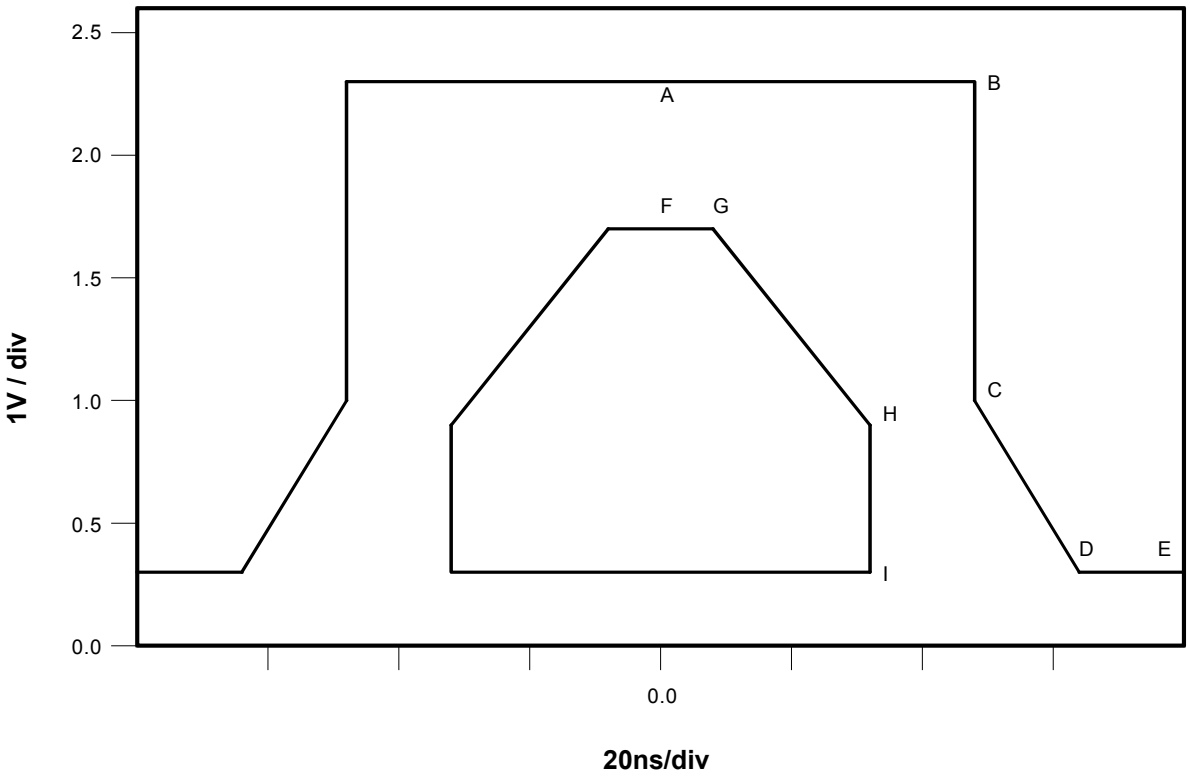


Table 8C. Tx+ and Tx- TEMPLATE CONSTANTS

	HORIZONTAL	VERTICAL
A	0	2.3
B	2.4	2.3
C	2.4	1.0
D	3.2	0.3
E	4.0	0.3

	HORIZONTAL	VERTICAL
F	0	1.7
G	0.4	1.7
H	1.6	0.9
I	1.6	0.3

Table 8D. RxMON+, RxMON-, TxMON+, and TxMON- TEMPLATE CONSTANTS

	HORIZONTAL	VERTICAL
A	0	2.3
B	2.4	2.3
C	2.4	1.0
D	3.2	0.3
E	4.0	0.3

	HORIZONTAL	VERTICAL
F	0	0.85
G	0.4	0.85
H	1.6	0.45
I	1.6	0.15

9. JTAG

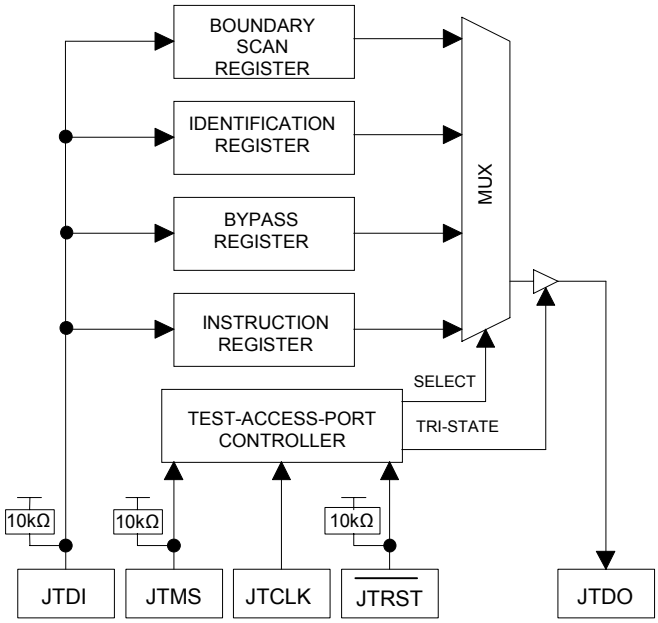
9.1 JTAG Description

The DS3160 device supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGH-Z, CLAMP, and IDCODE (Figure 9.1A). The DS3160 contains the following items that meet the requirements set by the IEEE 1149.1 standard test access port (TAP) and boundary scan architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in Section 2.9. Details about boundary scan architecture and the TAP are found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

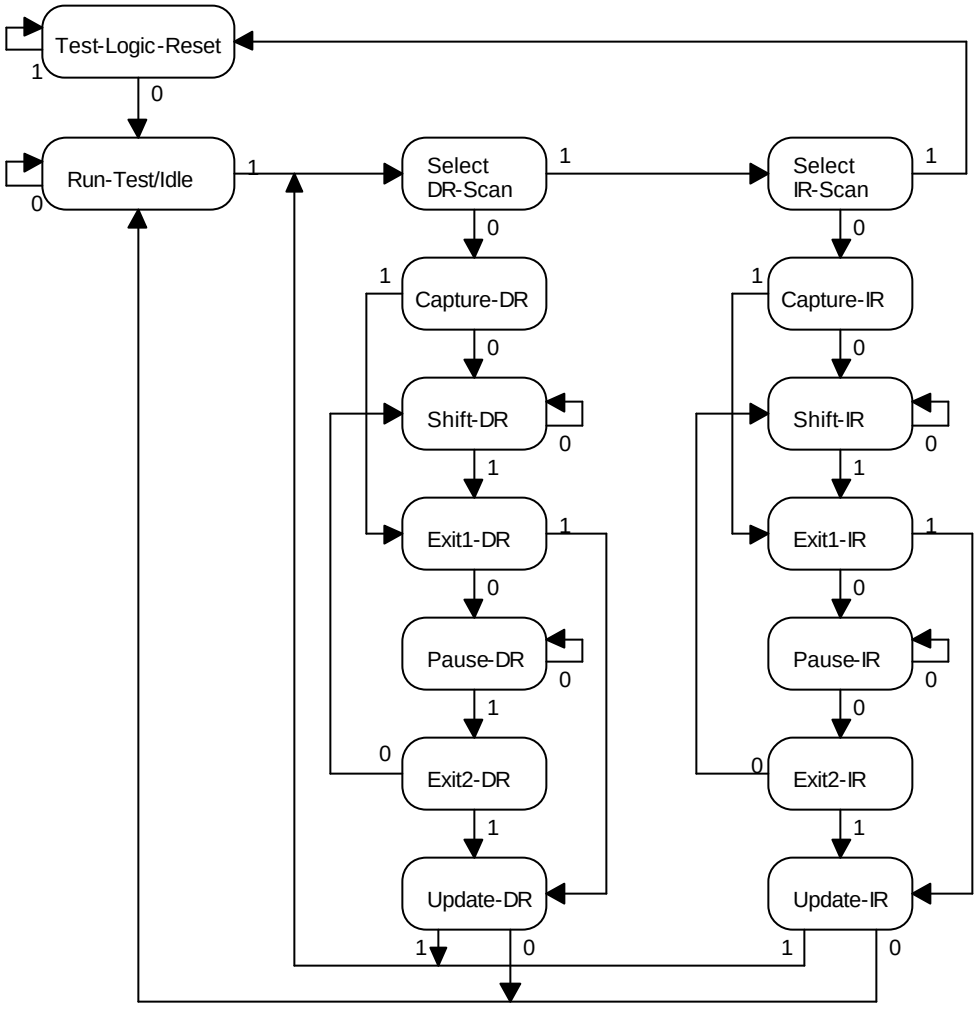
Figure 9.1A. JTAG BLOCK DIAGRAM



9.2 TAP Controller State Machine Description

This section covers the details about the operation of the test-access-port (TAP) controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

Figure 9.2A. TAP CONTROLLER STATE MACHINE



Test-Logic-Reset

Upon power-up of the DS3160, the TAP controller is in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the DS3160 operates normally.

Run-Test-Idle

Run-Test-Idle is used between scan operations or during specific tests. The instruction register and test register remain idle.

Select-DR-Scan

All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR

Data can be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or it goes to the Exit1-DR state if JTMS is high.

Shift-DR

The test data register selected by the current instruction is connected between JTDI and JTDO and shifts data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR

While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state that terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retains their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR

While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low enters the Shift-DR state.

Update-DR

A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan

All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR

The Capture-IR state is used to load the shift register in the Instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register and all test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state while moving data one stage through the instruction shift register.

Exit1-IR

A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR

Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR

A rising edge on JTCLK with JTMS low puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is high during a rising edge of JTCLK in this state.

Update-IR

The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

9.3 Instruction Register and Instructions

The instruction register contains a shift register as well as a latched-parallel output, and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS3160 and their respective operational binary codes are shown in Table 9.3A.

Table 9.3A. INSTRUCTION CODES

INSTRUCTION	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGH-Z	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the DS3160 can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the DS3160 to shift data into the boundary scan register through JTDI using the Shift-DR state.

EXTEST

EXTEST allows testing of all interconnections to the DS3160. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled by the Update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between JTDI and JTDO. The Capture-DR samples all digital inputs into the boundary scan register.

BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the 1-bit bypass test register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially through JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The device ID code always has a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. The device ID code for the DS3160 is 0000D143h.

HIGH-Z
All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP
All digital outputs output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

9.4 Test Registers
IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register has been included in the DS3160 design. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register
This is a single 1-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGH-Z instructions and provides a short path between JTDI and JTDO.

Identification Register
The identification register contains a 32-bit shift register and a 32-bit latched-parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

Boundary Scan Register
This register contains both a shift register path and a latched-parallel output for all control cells and digital I/O cells and is 196 bits in length. Table 9.4A lists all cell bit locations and definitions.

Table 9.4A. BOUNDARY SCAN CONTROL BITS

BIT	SYMBOL	PIN	TYPE	FUNCTION
0	DPOSI	99	I	Digital POS Factory Test Signal
1	DNEGI	98	I	Digital NEG Factory Test Signal
2	DCLKI	97	I	Digital CLK Factory Test Signal
3	DPOSO	96	O	Digital POS Factory Test Signal
4	DNEGO	95	O	Digital NEG Factory Test Signal
5	DCLKO	94	O	Digital CLK Factory Test Signal
6	TENA1	93	I	Factory Test Enable 1
7	TENA2	92	I	Factory Test Enable 2
8	MCLK	91	I	LIU Master Clock
9	FTCLK	89	I	Transmit Formatter Clock Input
10	FRCLK	87	O	Receive Framer Clock Output
11	FRD	85	O	Receive Framer Data Output
12	FRDEN	84	O	Receive Framer Data-Enable Output
13	FRSOF	83	O	Receive Framer Start-of-Frame Pulse
14	FRLOF	82	O	Receive Framer Loss-of-Frame Pulse
15	FRLOS	81	O	Receive Framer Loss-of-Signal Output
16	FRMECU	80	I	Receive Framer Manual Error-Counter Update
17	FTD	78	I	Transmit Formatter Data Input
18	FRO_ENA_N	—	Control Bit	Enable for the Framer Outputs
19	FTDEN	77	O	Transmit Formatter Data-Enable Output
20	FTSOF_ENA_N	—	Control Bit	Enable for the FTSOF
21	FTSOFO	76	O	Transmit Formatter Start-of-Frame Pulse
22	FTSOFI	76	I	Transmit Formatter Start-of-Frame Pulse
23	FTMEI	74	I	Transmit Formatter Manual Error Insert Pulse
24	CMS	73	I	CPU Bus Mode Select
25	CIM	72	I	CPU Bus Intel/Motorola Bus Select
26	CINT_ENA_N	—	Control Bit	CINT_N Enable
27	CINT_N	71	O	CPU Bus Interrupt
28	CWR_N	70	I	CPU Bus Write Enable
29	CRD_N	69	I	CPU Bus Read Enable
30	CCS_N	68	I	CPU Bus Chip Select
31	CDO[15]	67	O	CPU Bus Data Bit 15
32	CDI[15]	67	I	CPU Bus Data Bit 15
33	CDO[14]	65	O	CPU Bus Data Bit 14
34	CDI[14]	65	I	CPU Bus Data Bit 14
35	CDO[13]	64	O	CPU Bus Data Bit 13
36	CDI[13]	64	I	CPU Bus Data Bit 13
37	CDO[12]	63	O	CPU Bus Data Bit 12
38	CDI[12]	63	I	CPU Bus Data Bit 12
39	CDO[11]	62	O	CPU Bus Data Bit 11
40	CDI[11]	62	I	CPU Bus Data Bit 11
41	CDO[10]	61	O	CPU Bus Data Bit 10
42	CDI[10]	61	I	CPU Bus Data Bit 10
43	CDO[9]	59	O	CPU Bus Data Bit 9
44	CDI[9]	59	I	CPU Bus Data Bit 9
45	CDO[8]	58	O	CPU Bus Data Bit 8
46	CDI[8]	58	I	CPU Bus Data Bit 8
47	CDO[7]	57	O	CPU Bus Data Bit 7

BIT	SYMBOL	PIN	TYPE	FUNCTION
48	CDI[7]	57	I	CPU Bus Data Bit 7
49	CDO[6]	56	O	CPU Bus Data Bit 6
50	CDI[6]	56	I	CPU Bus Data Bit 6
51	CDO[5]	55	O	CPU Bus Data Bit 5
52	CDI[5]	55	I	CPU Bus Data Bit 5
53	CDO[4]	54	O	CPU Bus Data Bit 4
54	CDI[4]	54	I	CPU Bus Data Bit 4
55	CDO[3]	53	O	CPU Bus Data Bit 3
56	CDI[3]	53	I	CPU Bus Data Bit 3
57	CDO[2]	51	O	CPU Bus Data Bit 2
58	CDI[2]	51	I	CPU Bus Data Bit 2
59	CDO[1]	50	O	CPU Bus Data Bit 1
60	CDI[1]	50	I	CPU Bus Data Bit 1
61	CD_ENA_N	—	Control Bit	CPU Data Bus in Tri-State Operation
62	CDO[0]	49	O	CPU Bus Data Bit 0
63	CDI[0]	49	I	CPU Bus Data Bit 0
64	CA[7]	47	I	CPU Bus Address Bit 7
65	CA[6]	46	I	CPU Bus Address Bit 6
66	CA[5]	45	I	CPU Bus Address Bit 5
67	CA[4]	44	I	CPU Bus Address Bit 4
68	CA[3]	43	I	CPU Bus Address Bit 3
69	CA[2]	42	I	CPU Bus Address Bit 2
70	CA[1]	41	I	CPU Bus Address Bit 1
71	CA[0]	40	I	CPU Bus Address Bit 0
72	CALE	39	I	CPU Bus Address Latch Enable
73	HIZ_N	28	I	Tri-State Output Pins Enable
74	TEST_N	27	I	Factory Test Input
75	RST_N	26	I	Reset
76	LCLKI	17	I	LIU CLK Factory Test Signal
77	LNEGI	16	I	LIU NEG Factory Test Signal
78	LPOSI	15	I	LIU POS Factory Test Signal
79	LCLKO	8	O	LIU CLK Factory Test Signal
80	LNEGO	7	O	LIU NEG Factory Test Signal
81	TO_ENA_N	—	Control Bit	Enable for the Test Outputs
82	LPOSO	6	O	LIU POS Factory Test Signal

10. TEST REGISTERS

Register Name: **TEST1, TEST2, TEST3, TEST4**
Register Description: **Test Registers 1 to 4**
Register Address: **40 to 46**

Test Registers 1 through 4 are used to verify device operation during the DS3160 manufacturing process. These registers should never be written to during normal operation. A device reset forces the register contents to the correct operating values.

11. AC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin with Respect to V_{SS} (Except V_{DD})	-0.3V to +5.5V
Supply Voltage (V_{DD}) Range with Respect to V_{SS}	-0.3V to +3.63V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

*This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

Note: The typical values listed below are not production tested.

RECOMMENDED DC OPERATING CONDITION

(0°C to +70°C for DS3160)
(0°C to +85°C for DS3160C01)
(-40°C to +85°C for DS3160N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply (V_{DD})	V_{DD}	3.135		3.465	V	

DC CHARACTERISTICS

(V_{DD} = 3.135V to 3.465V, 0°C to +70°C for DS3160)

(V_{DD} = 3.135V to 3.465V, 0°C to +85°C for DS3160C01)
(V_{DD} = 3.135V to 3.465V, (-40°C to +85°C for DS3160N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current at V_{DD} = 3.465V	I_{DD}		150		mA	1
Lead Capacitance	C_{IO}		7		pF	
Input Leakage	I_{IL}	-10		+10	µA	2
Input Leakage (with Pullups)	I_{ILP}	-500		+500	µA	2
Output Leakage	I_{LO}	-10		+10	µA	3
Output Current (2.4V)	I_{OH}	-4.0			mA	
Output Current (0.4V)	I_{OL}	+1.0			mA	

NOTES:

1) FTCLK = FRCLK = 6.312MHz/other inputs at V_{DD} or grounded/other outputs left open-circuited.
2) $0V < V_{IN} < V_{DD}$.
3) Outputs in tri-state.

AC CHARACTERISTICS—FRAMER PORTS

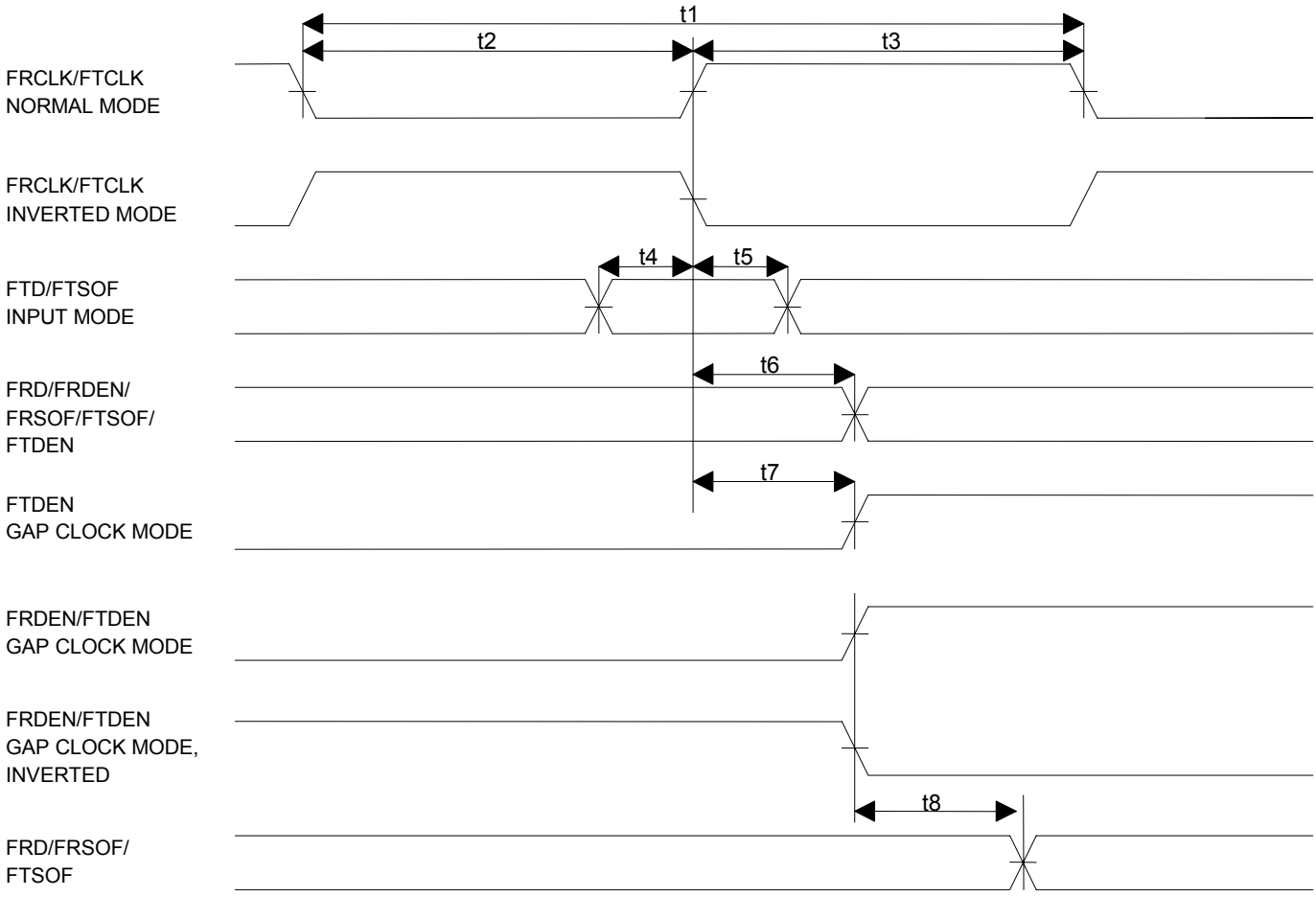
(V_{DD} = 3.135V to 3.465V, 0°C to +70°C for DS3160)
(V_{DD} = 3.135V to 3.465V, 0°C to +85°C for DS3160C01)
(V_{DD} = 3.135V to 3.465V, -40°C to +85°C for DS3160N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
FRCLK/FTCLK Clock Period	t1		158.43		ns	1
FTCLK Clock Low Time	t2	63			ns	
FTCLK Clock High Time	t3	63			ns	
FTD/FTSOF Setup Time to the Rising Edge or Falling Edge of FTCLK (Note 4)	t4	3			ns	2
FTD/FTSOF Hold Time from the Rising Edge or Falling Edge of FTCLK (Note 4)	t5	3			ns	2
Delay from the Rising Edge or Falling Edge of FRCLK/FTCLK to Data Valid on FRDEN/FRD/ FRSOF/FTDEN/FTSOF (Note 5)	t6	3		25	ns	3
Delay from the Rising Edge or Falling Edge of FTCLK to FTDEN (FTDEN in Gapped Clock Mode)	t7	0		23	ns	
Delay from the Rising Edge or Falling Edge of Gapped Clock to FRD, FRSOF, FTSOF	t8	2			ns	

NOTES:

1) FRCLK is a buffered version of the recovered LIU clock (RCLK) or FTCLK when in diagnostic loopback mode (DLB is enabled), and, as such, the duty cycle of FRCLK is determined by the source clock.
2) FTSOF is configured to be an input.
3) FTSOF is configured to be an output.
4) In normal mode, FTD (and FTSOF, if it is configured as an input) is sampled on the rising edge of FTCLK, and FRDEN, FRD, FRSOF, FTDEN (and FTSOF, if it is configured as an output) are updated on the rising edge of FRCLK or FTCLK.
5) In inverted mode, FTD (and FTSOF, if it is configured as an input) is sampled on the falling edge of FTCLK, and FRDEN, FRD, FRSOF, FTDEN (and FTSOF if it is configured as an output) are updated on the falling edge of FRCLK or FTCLK.

Figure 11A. FRAMER PORT AC TIMING DIAGRAM



AC CHARACTERISTICS—CPU BUS

(V_{DD} = 3.135V to 3.465V, 0°C to +70°C for DS3160)
(V_{DD} = 3.135V to 3.465V, 0°C to +85°C for DS3160C01)
(V_{DD} = 3.135V to 3.465V, -40°C to +85°C for DS3160N)

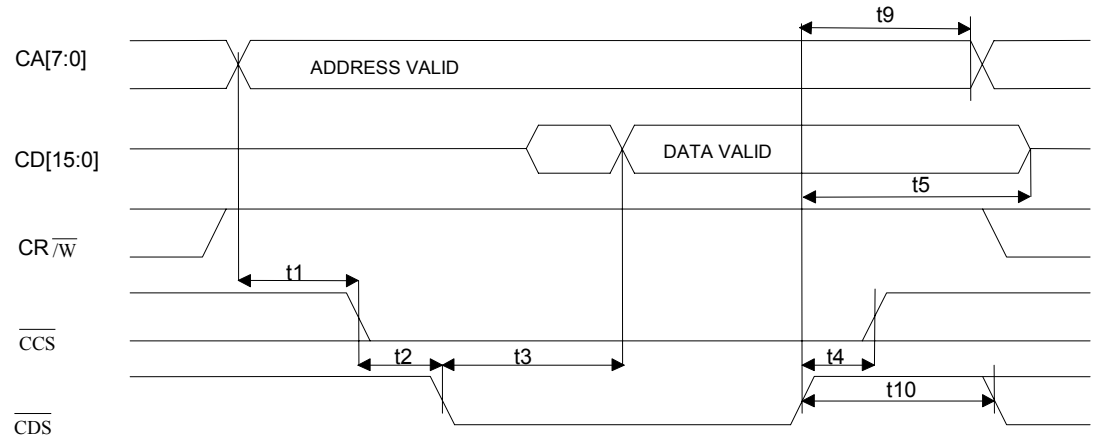
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Setup Time for CA[7:0] Valid to $\overline{CCS}$ Active	t1	0			ns	
Setup Time for $\overline{CCS}$ Active to Either $\overline{CRD}$, $\overline{CWR}$, or $\overline{CDS}$ Active	t2	0			ns	
Delay Time from Either $\overline{CRD}$ or $\overline{CDS}$ Active to CD[15:0] Valid	t3			65	ns	
Hold Time from Either $\overline{CRD}$, $\overline{CWR}$, or $\overline{CDS}$ Inactive to $\overline{CCS}$ Inactive	t4	0			ns	
Hold Time from $\overline{CCS}$ or $\overline{CRD}$ Inactive to CD[15:0] Tri-State	t5	2			ns	1
Wait Time from Either $\overline{CWR}$ or $\overline{CDS}$ Active to Latch CD[15:0]	t6	65			ns	
CD[15:0] Setup Time to Either $\overline{CWR}$ or $\overline{CDS}$ Inactive	t7	10			ns	
CD[15:0] Hold Time from Either $\overline{CWR}$ or $\overline{CDS}$ Inactive	t8	2			ns	
CA[7:0] Hold from Either $\overline{CRD}$, $\overline{CWR}$, or $\overline{CDS}$ Inactive	t9	5			ns	
$\overline{CRD}$, $\overline{CWR}$, or $\overline{CDS}$ Inactive Time	t10	75			ns	
Muxed Address Valid to CALE Falling	t11	10			ns	2
Muxed Address Hold Time	t12	10			ns	2
CALE Pulse Width	t13	30			ns	2
Setup Time for CALE High or Muxed Address Valid to $\overline{CCS}$ Active	t14	0			ns	2

NOTES:

1) Data on CD15:0 must be valid for the minimum time period.
2) In multiplexed bus applications (Figure 12E), CA[7:0] should be connected to CD[7:0] and the falling edge of CALE latches the address.
3) In nonmultiplexed bus applications (Figure 12D), CALE should be connected high.

Figure 11B. CPU BUS AC TIMING DIAGRAM (NONMULTIPLEXED)

Intel Read Cycle



Intel Write Cycle

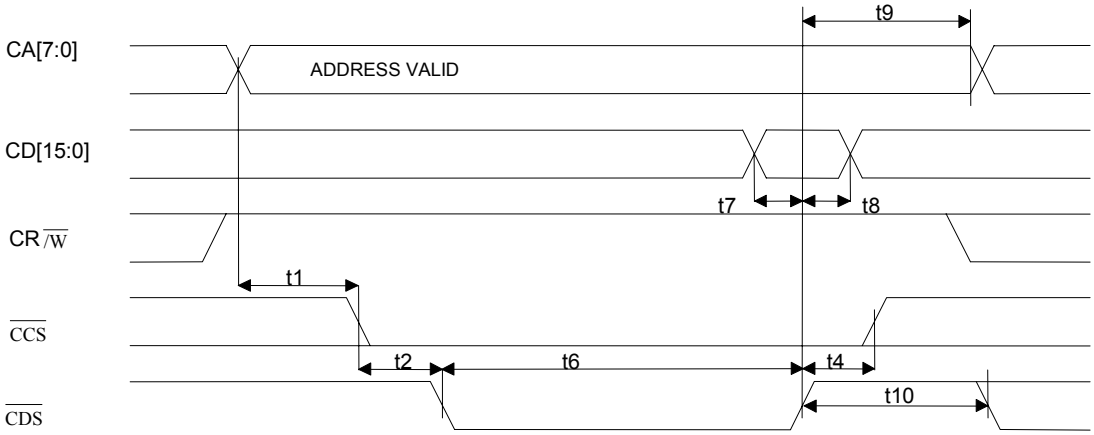
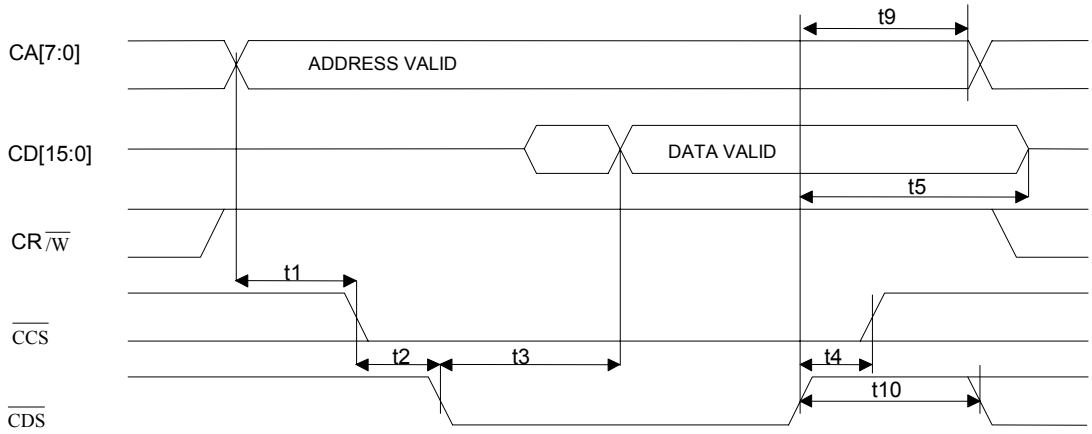


Figure 11B. CPU BUS AC TIMING DIAGRAM (NONMULTIPLEXED) (continued)

Motorola Read Cycle



Motorola Write Cycle

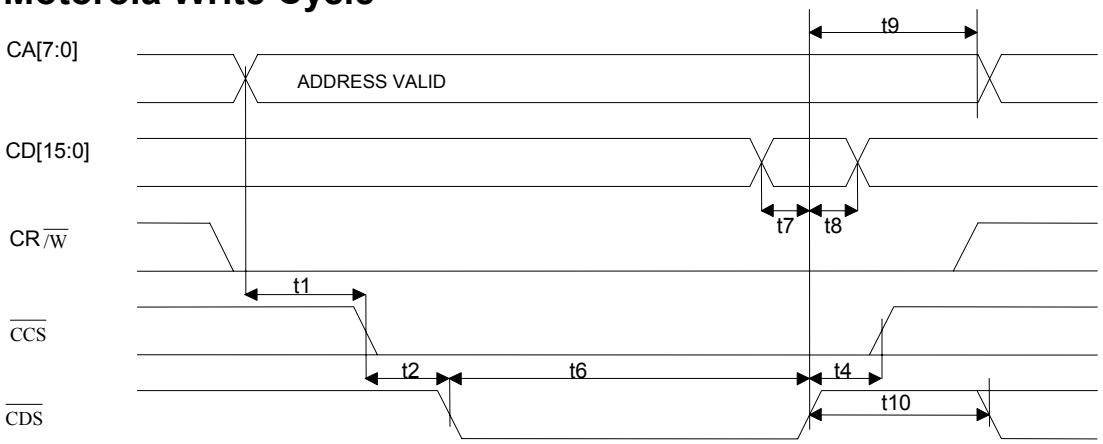
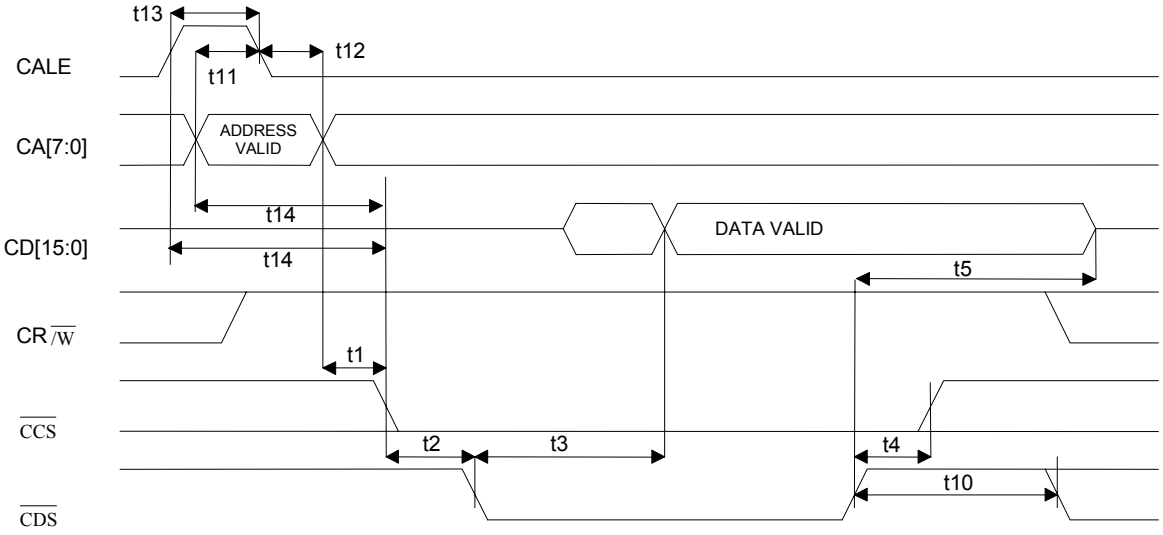


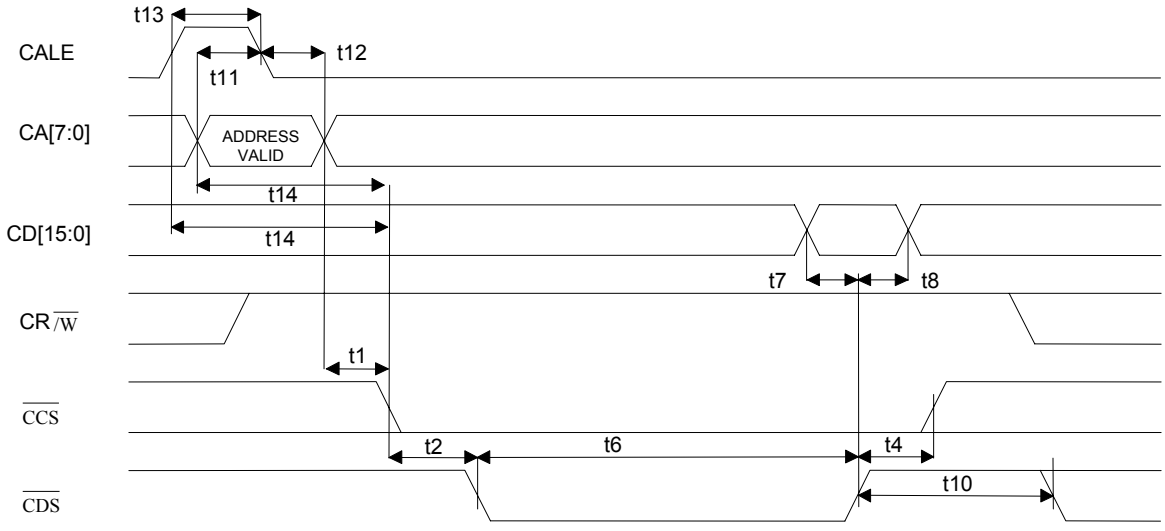
Figure 11C. CPU BUS AC TIMING DIAGRAM (MULTIPLEXED)

Intel Read Cycle



Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

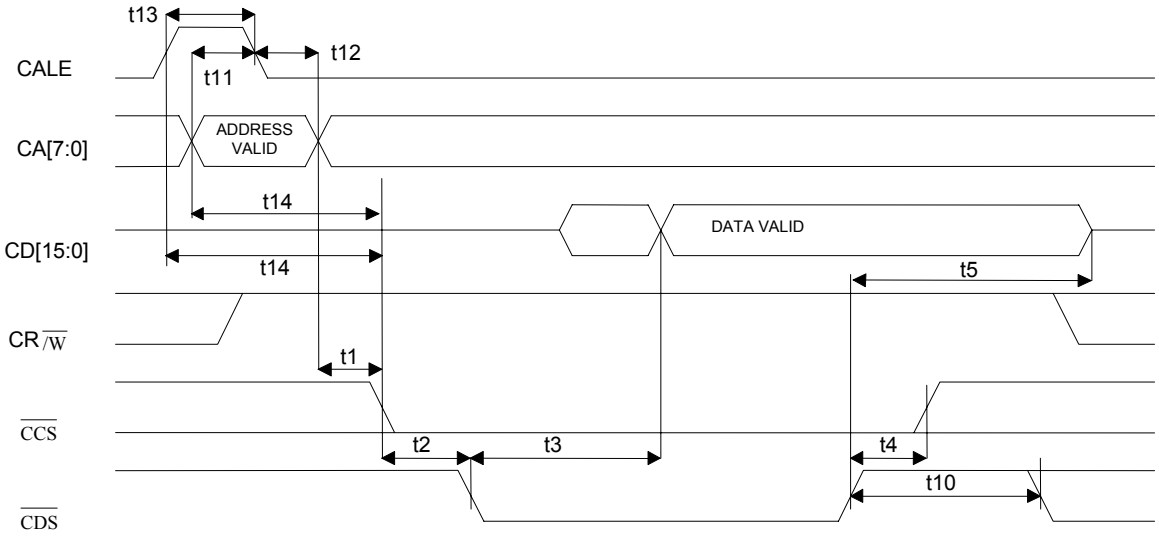
Intel Write Cycle



Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

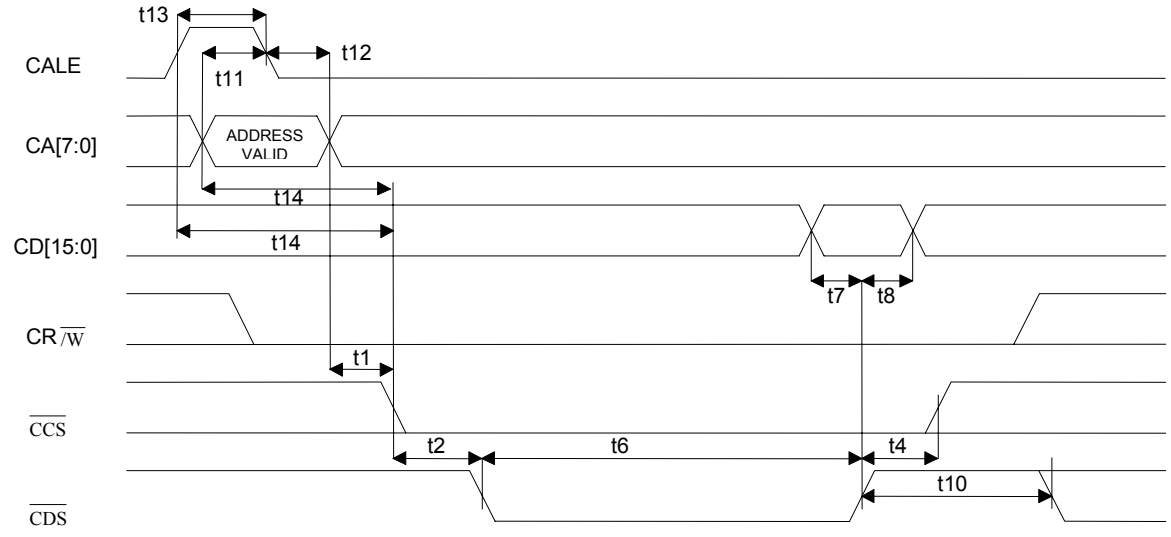
Figure 11C. CPU BUS AC TIMING DIAGRAM (MULTIPLEXED) (continued)

Motorola Read Cycle



Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

Motorola Write Cycle



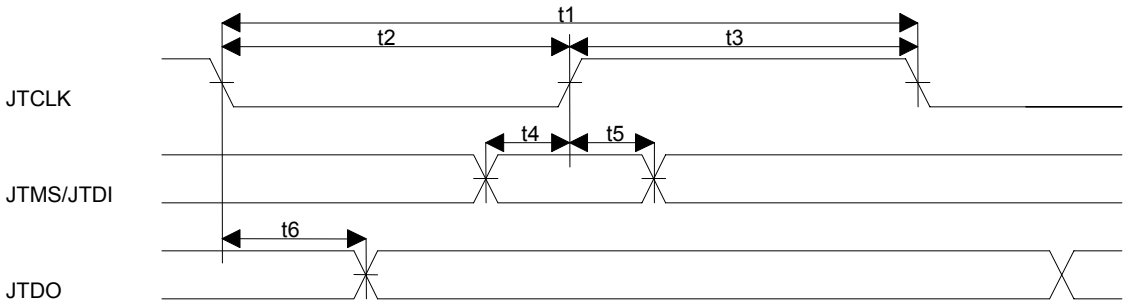
Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

AC CHARACTERISTICS—JTAG TEST PORT INTERFACE

(V_{DD} = 3.135V to 3.465V, 0°C to +70°C for DS3160)
(V_{DD} = 3.135V to 3.465V, 0°C to +85°C for DS3160C01)
(V_{DD} = 3.135V to 3.465V, -40°C to +85°C for DS3160N)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
JTCLK Clock Period	t1	1000			ns	
JTCLK Clock Low Time	t2	400			ns	
JTCLK Clock High Time	t3	400			ns	
JTMS/JTDI Setup Time to the Rising Edge of JTCLK	t4	50			ns	
JTMS/JTDI Hold Time from the Rising Edge of JTCLK	t5	50			ns	
Delay Time from the Falling Edge of JTCLK to Data Valid on JTDO	t6	2		50	ns	

Figure 11D. JTAG TEST PORT INTERFACE AC TIMING DIAGRAM

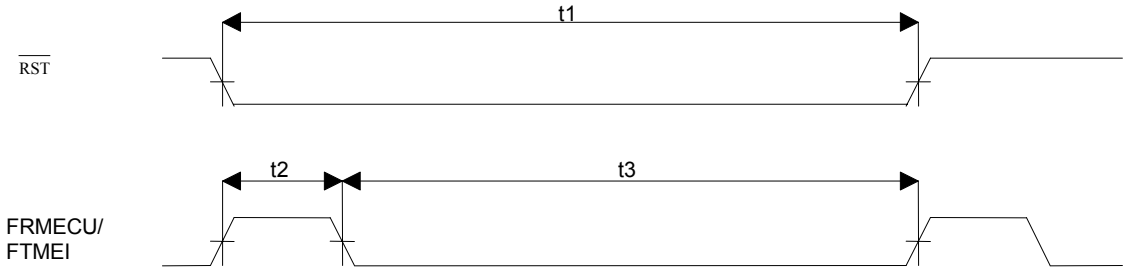


AC CHARACTERISTICS—RESET AND MANUAL ERROR COUNTER/ INSERT SIGNALS

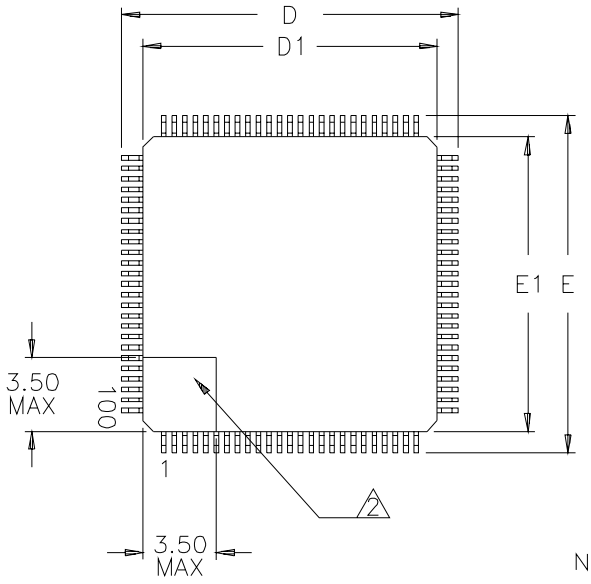
(V_{DD} = 3.135V to 3.465V, 0°C to +70°C for DS3160)
(V_{DD} = 3.135V to 3.465V, 0°C to +85°C for DS3160C01)
(V_{DD} = 3.135V to 3.465V, -40°C to +85°C for DS3160N)

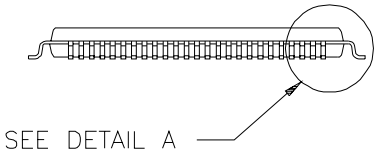
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{RST}$ Low Time	t1	1000			ns	
FRMECU/FTMEI High Time	t2	200			ns	
FRMECU/FTMEI Low Time	t3	200			ns	

Figure 11E. RESET AND MANUAL ERROR COUNTER/INSERT AC TIMING DIAGRAM



12. MECHANICAL DIMENSIONS

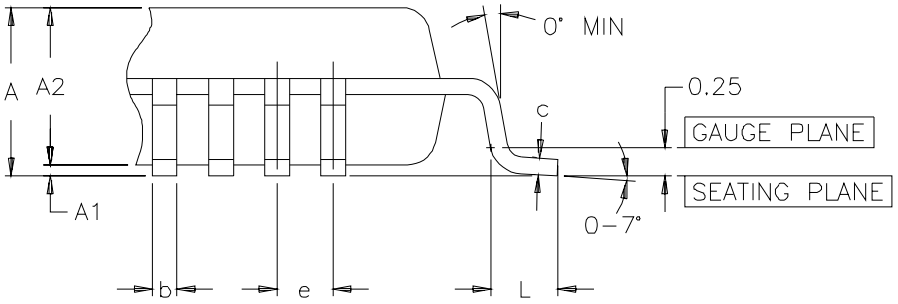




NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

DIM	MIN	MAX
A	–	1.60
A1	0.05	–
A2	1.35	1.45
b	0.17	0.27
c	0.09	0.20
D	15.80	16.20
D1	14.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75



DETAIL A

13. J2 FRAME FORMAT

The DS3160 supports the G.704 and NTT J2 frame format. Highlights of the J2 structure include the following:

- The J2 format is frame based.
- Each frame contains 96 bytes of user data, two reserved bytes, and five overhead bits for a total of 789 bits.
- The five overhead bits are designated as F-bits and are used for frame alignment, path CRC, and data link.
- The frame rate is 8000 per second or 125µs long.
- 789 bits per frame / 125µs per frame = 6.312Mbps line rate.
- The frames are grouped into four formatted multiframes.

Figure 13A. J2 FRAME STRUCTURE

Bit #	1–8	9–16	17–24	753–760	761–768	769–776	777–784	785	786	787	788	789
Frame 1	TS1	TS2	TS3	TS95	TS96	TS97	TS98	1	1	0	0	m
Frame 2	TS1	TS2	TS3	TS95	TS96	TS97	TS98	1	0	1	0	0
Frame 3	TS1	TS2	TS3	TS95	TS96	TS97	TS98	x1`	x2	x3	a	m
Frame 4	TS1	TS2	TS3	TS95	TS96	TS97	TS98	e1	e2	e3	e4	e5

FRAME COMPONENT	DEFINITION
TS1 . . . TS96	Byte interleaved user data
TS97, TS98	Reserved channels for signaling
Frame Alignment Signal	110010100 (See Figure 13A for location.)
m	4kHz data link
x1, x2, x3	Spare bits, set to 1 if not used
a	Remote LOF alarm bit, (1 = alarm, 0 = no alarm)
e1 . . . e5	CRC-5 check sequence. Starts with bit number 1 of frame 1 and ends at bit number 784 of frame 4 for a total of 3151 bits.

14. PROGRAMMING GUIDE AND OPERATIONAL NOTES

14.1 Power-Up/Reset Discussion

The DS3160 can be reset as a result of three actions:

- Detection of a power transition by the on-chip supply supervisor
- Through hardware by toggling the RST device pin
- Through software by setting the RST pin located in the MRID register

When a reset is issued, all of the internal registers are forced to their default states. A DS3160 status read immediately after a reset indicates the following:

- MSR:LOTC set and then immediately cleared if the clock is present.
- MSR:LIULOS set
- SR1:LOS set
- SR1:LOF set
- BERTECO:RLOS set
- HSR:TLWM set
- HSR:TEMPTY and REMPTY set

Also, because of the reset, FRD is forced to all 1's as a result of the LOS and the transmit, Rx monitor, and Tx monitor ports are tri-stated.

The recommended power-up sequence is (assuming the DS3160 has received a reset):

1) Wait 100ms after valid power.
2) Configure LIU, framer, and formatter.
3) Read status registers to clear transient history.
4) Read status registers for valid status.
5) Enable interrupts if used.
6) Optionally enable transmit, Rx monitor, and Tx monitor ports.

Device behavior notes after a power-up or a reset:

- Connecting to an active valid line
  - LOS and LOF are set
  - LOS clears
  - LOF clears
- Connecting to a line receiving AIS
  - LOS and LOF are set
  - LOS clears
  - LOF remains set
  - AIS becomes set
- Connecting to a line receiving RAI
  - LOS and LOF are set
  - LOS and LOF clear
  - RAI becomes set
- Connecting to a line receiving an unframed signal
  - LOS and LOF are set
  - LOS clear
  - LOF remains set
  - Connecting to a dead line
  - LOS and LOF are set
  - LOS and LOF remain set