

M/A-COM 6W C-Band High Power Amplifier

5.5 – 7.0 GHz

Preliminary Information

MAAPGM0025-DIE

Features

- ◆ 5.5 to 7.0 GHz Operation
- ◆ 6 Watt Saturated Output Power Level
- ◆ Variable Drain Voltage (4-10V) Operation
- ◆ Self-Aligned MSAG[®] MESFET Process

5.5-7.0 GHz GaAs MMIC HPA

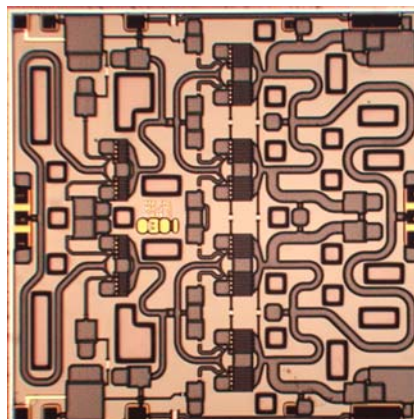
Primary Applications

- ◆ Satellite Communication
- ◆ Point-to-Point Radio (5.9-6.4 GHz)
- ◆ Point-to-Point Radio (6.525-6.875 GHz)

Description

The MAAPGM0025-Die is a 2-stage 6 W high power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested on wafer to ensure performance compliance. The part is fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG[®]) MESFET Process. This process features silicon nitride passivation and polyimide scratch protection.



Electrical Characteristics: $T_B = 40^\circ\text{C}^1$, $Z_0 = 50\Omega$, $V_{DD} = 8\text{V}$, $V_{GG} = -2\text{V}$, $P_{in} = 24\text{ dBm}$

Parameter	Symbol	Typical	Units
Bandwidth	f	5.5-7.0	GHz
Output Power	P_{OUT}	38	dBm
Power Added Efficiency	PAE	35	%
1-dB Compression Point	P_{1dB}	36	dBm
Small Signal Gain	G	17.5	dB
Input VSWR	VSWR	1.9 :1	
Gate Current	I_{GG}	< 10	mA
Output TOI	OTOI	43.3	dBm
Noise Figure	NF	5.25	dB
Drain Current	I_{DD}	< 2.5	A

1. T_B = MMIC Base Temperature

Maximum Operating Conditions ¹

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	29.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-2.0	V
Quiescent Drain Current (No RF)	I_{DQ}	3.04	A
Quiescent DC Power Dissipation (No RF)	P_{DISS}	20.1	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Voltage	V_{GG}	-2.4	-2.0	-1.6	V
Input Power	P_{IN}		24.0	27.0	dBm
Junction Temperature	T_J			150	°C
MMIC Base Temperature	T_B			Note 2	°C

2. Maximum MMIC Base Temperature = $150^{\circ}\text{C} - 4.0^{\circ}\text{C/W} * V_{DD} * I_{DQ}$

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply $V_{GG} = -2\text{ V}$, $V_{DD} = 0\text{ V}$.
2. Ramp V_{DD} to desired voltage, typically 8 V.
3. Adjust V_{GG} to set I_{DQ} , (approximately @ -2 V).
4. Set RF input.
5. Power down sequence in reverse. Turn gate voltage off last.



Specifications subject to change without notice.

Customer Service: Tel. (888)-563-3949

Email: macom_adbu_ics@tycoelectronics.com

- **North America:** Tel. (800) 366-2266
- **Asia/Pacific:** Tel. +81-44-844-8296, Fax +81-44-844-8298
- **Europe:** Tel. +44 (1344) 869 595, Fax+44 (1344) 300 020

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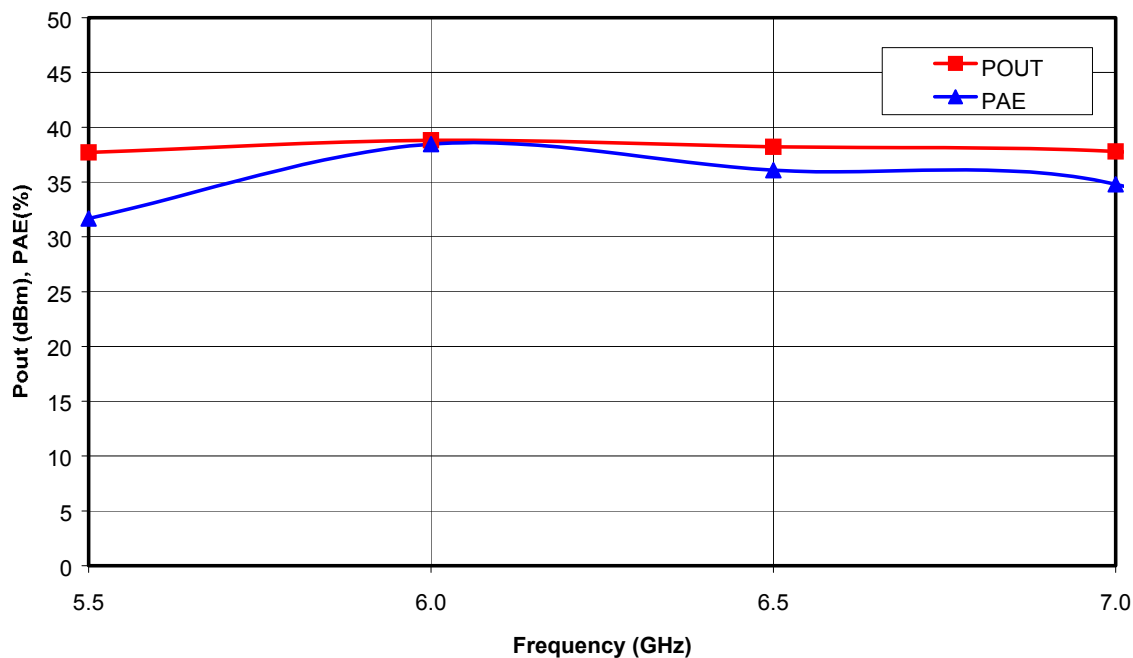


Figure 1. Output Power and Power Added Efficiency vs. Frequency at $V_{DD} = 8V$, $P_{in} = 24dBm$.

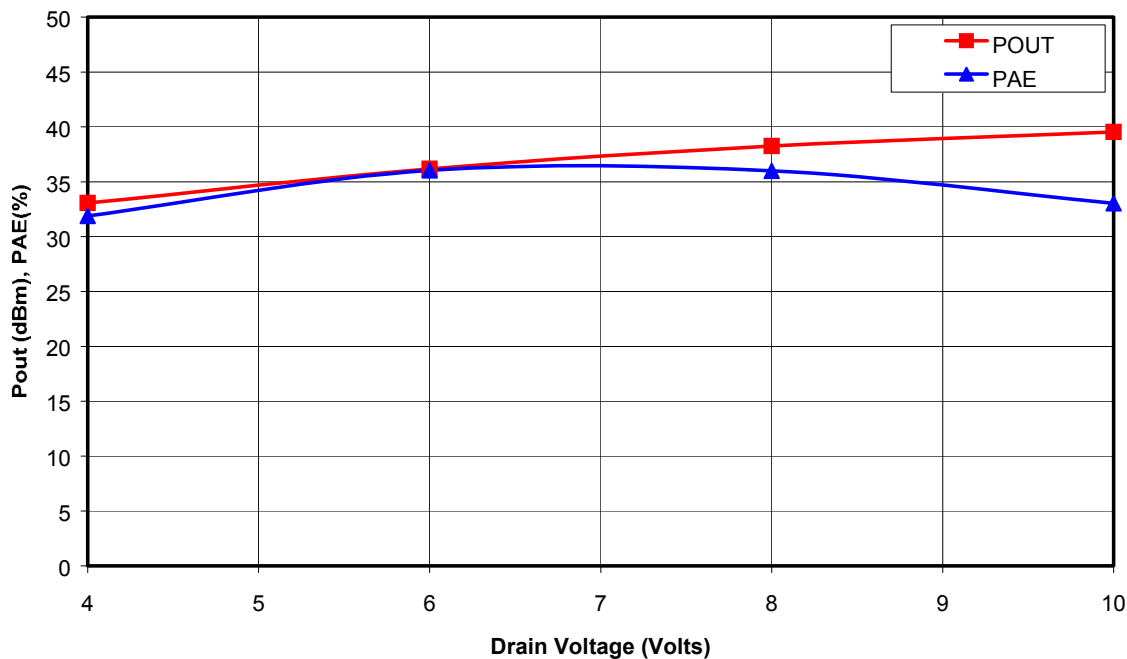


Figure 2. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at $f_o = 6.5 GHz$.

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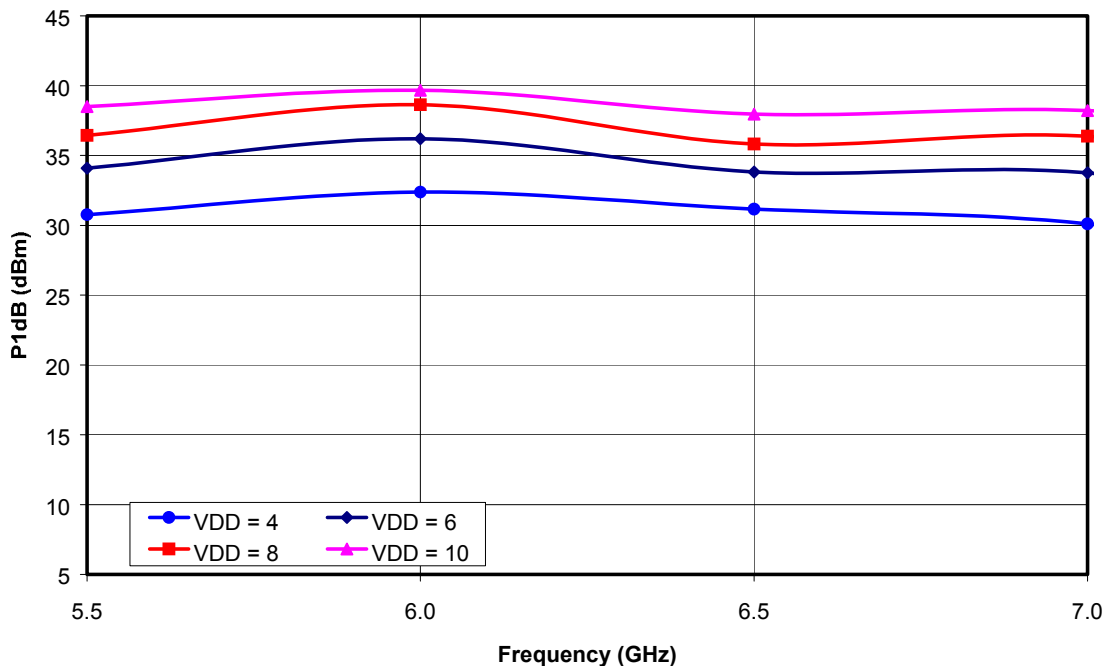


Figure 3. 1dB Compression Point vs. Drain Voltage

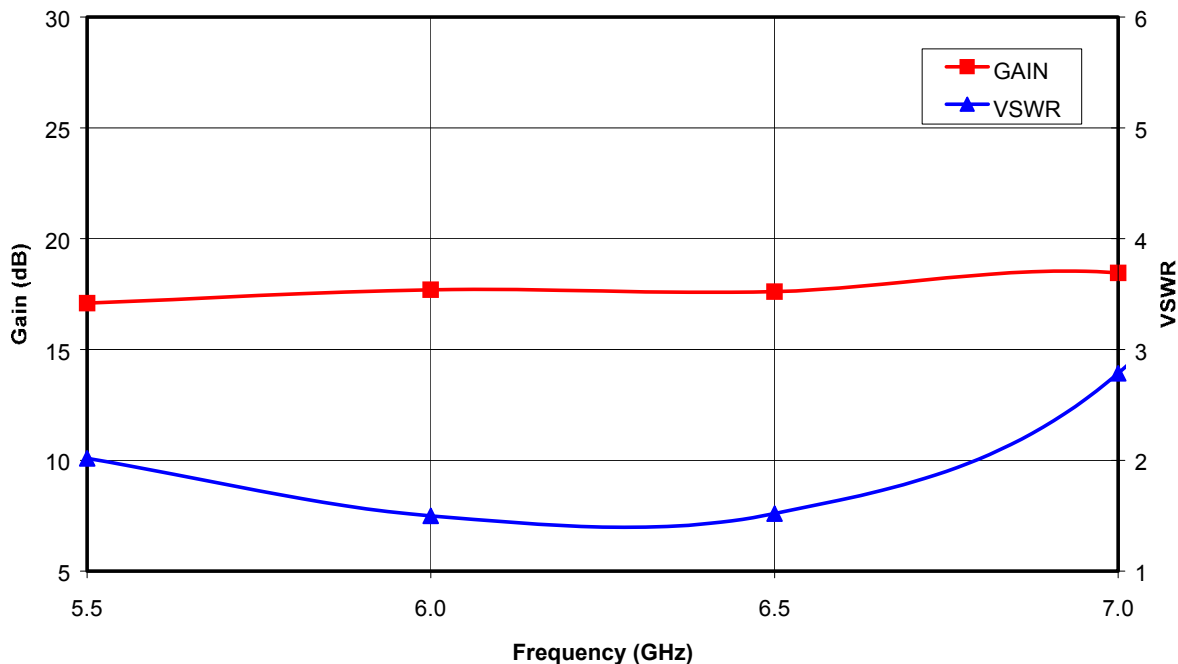


Figure 4. Small Signal Gain and VSWR vs. Frequency at VDD = 8V.

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Mechanical Information

Chip Size: 4.404 x 4.404 x 0.075 mm (174 x 174 x 3 mils)

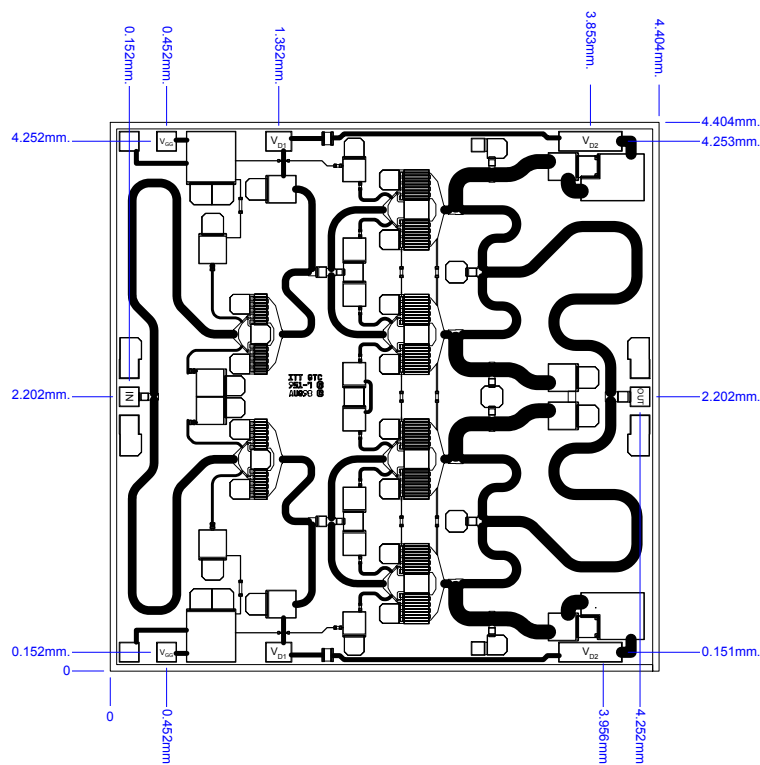


Figure 5. Die Layout

Bond Pad Dimensions

Pad	Size (μm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VD1	200 x 150	8 x 6
DC Drain Supply Voltage VD2	500 x 150	20 x 6
DC Gate Supply Voltage VGG	150 x 150	6 x 6

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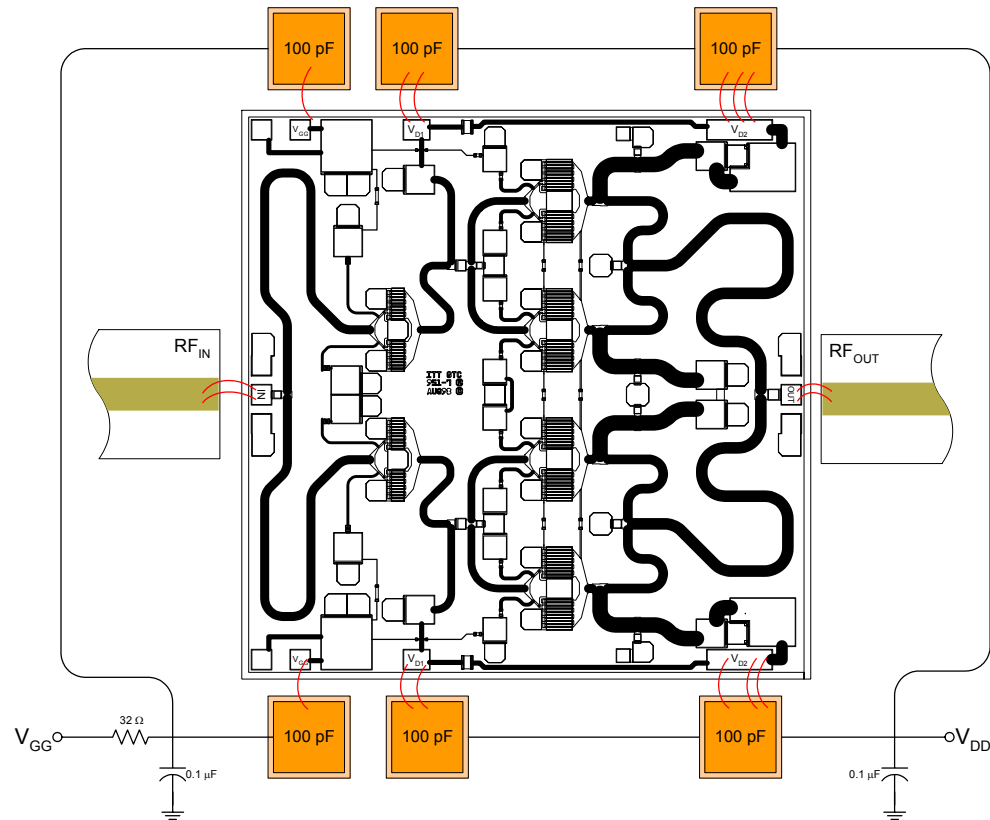


Figure 6. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization fixture for CW testing.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1-2 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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