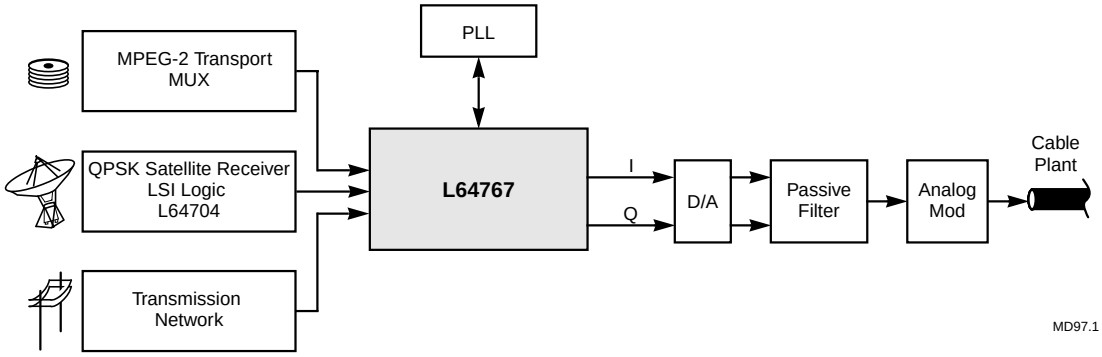
L64767
SMATV QAM Encoder
Datasheet

Introduction

LSI Logic's L64767 SMATV QAM Encoder is a highly-integrated device designed specifically for Satellite Master Antenna Television (SMATV) applications. The L64767 is ideally suited to any application that requires a low-power, highly integrated forward error correction (FEC) transmission encoder. Typical applications include rooftop SMATV systems, cable head-ends, and optical networks in fiber-deep networks.

Figure 1 shows a basic SMATV QAM system using the L64767. The device can process input from either an MPEG-2 transport encoder, a satellite receiver, or a transmission network.

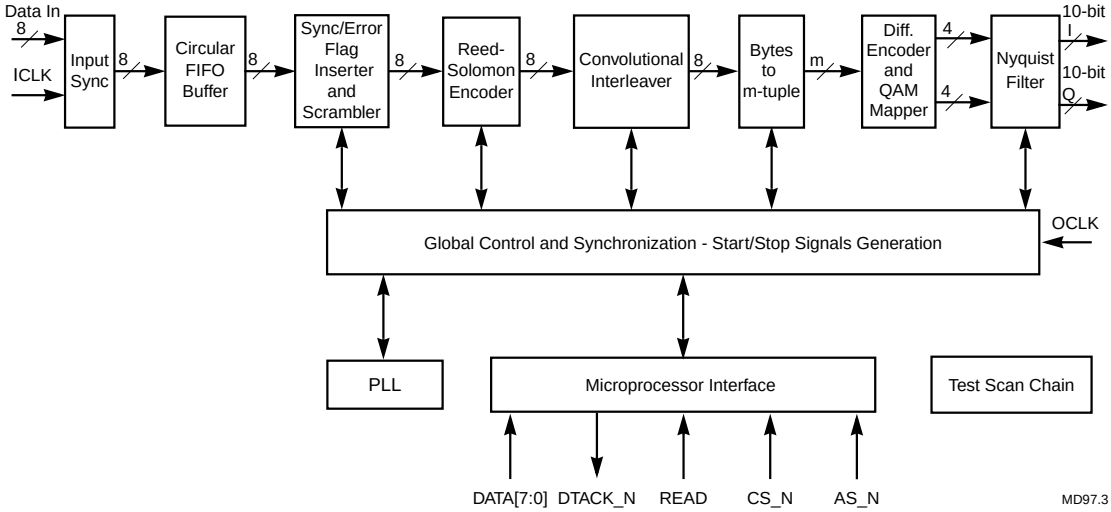
Figure 1. L64767 SMATV QAM System



The L64767 simplifies the design process for FEC and modulation encoding systems by providing built-in signal processing capabilities and a byte-parallel, power saving architecture. The L64767's ease of use will help system engineers create the next generation of time-to-volume sensitive digital products. In contrast, previous solutions for these systems forced system engineers to use many programmable and discrete devices on large circuit boards. These end products were expensive and power-intensive, both of which are unacceptable for today's SMATV applications.

The L64767 integrates CoreWare® processing elements that conform to the specifications described in the document *DTVB1190/DTVC37, Revision 3*. Figure 2 shows the L64767's major functional blocks.

Figure 2. L64767 Functional Blocks



The CoreWare processing elements of the L64767 comprise the data processing chain of the device and include:

- Input synchronizer
- Circular FIFO buffer
- Sync/error flag inserter and scrambler
- Reed-Solomon encoder
- Convolutional interleaver
- Bytes to m-tuple converter
- Differential encoder and QAM mapper
- Nyquist filter

In addition to the processing chain, the L64767 provides:

- Global control and synchronization components
- Microprocessor interface for configuring and monitoring internal registers
- Test scan chain

The L64767 can accept byte-parallel or bit-serial input and provides flexible input synchronization support. It can automatically search for a digital video broadcasting (DVB) or user-programmable 8-bit sync code. Alternatively, the L64767 can use an external frame start signal to indicate the beginning of a frame for input synchronization. By inserting the Reed-Solomon (RS) check words into the circular FIFO buffer, the device can also use an MPEG-2 input stream without gaps, or operate on packets with gaps for RS check words.

The length of sync words and sync blocks is user-programmable, and sync information can be reinserted as needed. The L64767 also provides an error indication bit for MPEG-2 transport packet errors. Using this bit, error flags from a preceding device can be properly inserted in the MPEG-2 transport stream.

The L64767 can process quadrature amplitude modulation (QAM) levels of 16, 32, 64, 128, and 256. The QAM level is user-programmable.

Features

- SMATV *DTVB1190/DTVC37, Revision 3* compliant
- Highly integrated, global synchronization and clock control
- 2- or 4-fold Nyquist filter oversampling
- Maskable interrupts for all error conditions
- Individual module bypass configuration modes
- IEEE 1149.1 JTAG interface for testing
- User-controllable input synchronization schemes
- Low-power (1 W), low-cost surface mount package
- Up to 7.8 Mbaud operation
- Up to 62 Mbits/second serial data input
- Up to 10 Mbytes/second parallel data input
- 16, 32, 64, 128, 256 QAM modes
- Reed-Solomon encoder
- Frame sync-byte insertion
- Convolutional data interleaving depth (B = 12)

Benefits

- Directly connects to LSI Logic's satellite receiver/FEC
- Allows low-cost external filters (4-fold oversampling mode)
- 85° C ambient operation without special cooling devices
- Entire device or individual SMATV CoreWare processing blocks available
- Easy interface to most input sources
- Continuous data-in, continuous data-out operation
- Input jitter handling and Reed-Solomon gap insertion by 128-word circular FIFO buffer

Functional Description

This section provides a brief description of the major blocks shown in Figure 2.

Input Synchronizer

As shown in Figure 2, only the input synchronizer is driven by the input clock. All other processing is done based on the OCLK. OCLK can be two or four times the symbol clock (SCLK) frequency based on the oversampling setting of the Nyquist filter.

ICLK is limited to a maximum of 62.5 MHz in serial input mode and 10 MHz in parallel input mode. The maximum symbol rate handled by the L64767 is 7.5 Mbaud. Therefore, OCLK is limited to 15 MHz in 2-fold oversampling mode and 30 MHz in 4-fold oversampling mode.

The input format for the L64767 is based on the data format specified in the MPEG-2 system layer standard in relation to the DVB transport framing structure. It requires a Reed-Solomon (204,188) protected transport packet to consist of 204 bytes, including the sync byte plus 187 data bytes and 16 redundancy bytes.

This basic format has been adopted by the V4/MOD-B task force for a multiprogram TV via satellite standard, and by the DVB group in Europe. In a scrambled DVB data stream, one out of every eight synchronization words is mod 2 complemented (inverted) in order to define the beginning of a scrambling sequence.

The descrambled stream contains no inverted sync word. This MPEG-2 frame format is the basic input format for the L64767 device. The device assumes that the inserted sync byte at the chip input can only have the normal value, not the inverted one. You can insert gaps for Reed-Solomon check bytes or make them available in the input stream.

To synchronize input, you can do one of the following:

- Send a frame start pulse at the FSTARTIN pin forcing the beginning of each Reed-Solomon code block. Whenever FSTARTIN is asserted, the L64767 reinserts the sync byte into the data stream and inverts the sync word every eight blocks, as defined by the DVB.

- Specify a unique sync byte to be inserted in the input stream in a specified sync length distance

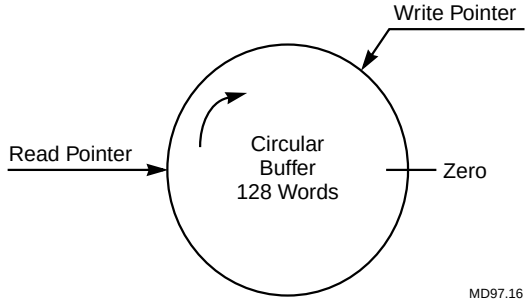
Synchronizing the L64767 with an input pulse will set byte and block boundaries with the pulse. The sync byte you define can be reinserted at the location of the pulse.

Circular FIFO Buffer

A dual-ported RAM implements the circular FIFO buffer in the L64767. The circular buffer has a write pointer driven by ICLK, and a read pointer driven by OCLK/4 (or OCLK/2 in 2-fold oversampling mode). Since there are no built-in mechanisms to prevent collisions of these pointers, you must configure the follow-up time and proper initial setup of the pointer distance through the phase-locked loop (PLL) module of the L64767. The circular FIFO buffer is illustrated in Figure 3.

You can ensure that the read pointer is directly opposite to the write pointer most of the time by properly programming delay values. This approach reduces the effect of PLL frequency swings that can occur during phases of an unstable input signal. You can also select smaller distances to reduce system delay.

Figure 3. Circular Read/Write FIFO Buffer



To initialize the circular FIFO buffer, download 0 to 127 cycles into the read address pointer to specify the distance between the read and write pointers. To do this, you can specify the FIFO delay value. When specifying this value, you must use Gray code numbers with even parity (an even number of 1s). Both the read and write pointers are Gray code counter-driven. The write pointer is initialized to zero when the read counter is loaded.

After initialization, both pointers run independently. The frequency relationship of OCLK to ICLK determines how the read and write pointers advance. The L64767 asserts its FIFOALARM pin whenever the two pointers are equal. This information is also available through a FIFO_ALARM_STORE bit.

Sync/Error Flag Inserter and Scrambler

By specifying the sync insertion mode, you can instruct the sync inserter to insert sync bytes into the data stream. Sync insertion minimizes bit errors in sync bytes (even if sync is already inserted in the stream). If sync bytes are contained in the bit stream and are used for synchronization of the device, regenerated sync bytes conceal single errors in the sync pattern.

When an uncorrectable error has occurred (ERRORIN signal is HIGH), the L64767 sets both the MPEG-2 transport_error_indicator bit in the packet (the most significant bit of the second byte in a packet) and ERF_STORE. You can use ERF_STORE to check if an error has occurred. You can also configure the L64767 to issue an interrupt for these errors or continue processing without an interrupt.

The scrambler module performs energy dispersion of the data stream. This module operates in parallel mode. For a complete description of the functional characteristics of this module refer to the standards document *DTVB1190/DTVC37, Revision 3*.

Reed-Solomon Encoder

Reed-Solomon (RS) codes aid in error correction by using redundant check symbols in its code words. RS error correction codes are systematic and operate on bytes rather than single-bit data streams. RS codes are expressed, by convention, as two numbers. The first indicates the total code word length (N). The second indicates the number of message bytes (K). The difference between these two numbers (N – K) is the number of check bytes.

Convolutional Interleaver

The interleaver rearranges the ordering of a sequence of symbols in a deterministic manner. Since the interleaver is convolutional, it requires less memory than the conventional RAM-intensive block type interleavers.

The interleaver is a (B, N) periodic interleaver with the following characteristics:

- The minimum separation at the interleaver output is B symbols for any two symbols that are separated by less than N symbols at the interleaver input.
- Any burst of b < B errors inserted by the channel results in single errors at the deinterleaver output.

Bytes to m-tuple Converter

The bytes to m-tuples converter organizes bytes into symbols (tuples) of m = 1, 2, 3, 4, 5, 6, 7, and 8 bits. To process the data stream, the L64767 feeds the converter packets of eight bytes together with a valid signal from the general control unit. The order of the conversion process starts with the MSB of the oldest byte first (see the document *DTVB1190/DTVC37, Revision 3* for details).

Differential Encoder and QAM Mapper

This block performs differential encoding and mapping for 16 to 256 QAM, as specified in the document *DTVB1190/DTVC37, Revision 3*.

Nyquist Filter

The Nyquist filter shapes signals for DVB compliance. This filter implements the square root raised cosine filtering function with roll off factor of 15%, as specified in *DTVB1190/DTVC37, Revision 3*. You can use other non-DVB filtering functions by downloading the appropriate filter coefficients.

The precision of the internal computations and the width of the output data bus are suitable up to 256 QAM. The filter interpolates the input data by a factor of two or four so that the filter output data rate is two or four times the filter input data rate. You specify the interpolation factor (oversampling) using a configuration register.

Global Control and Synchronization Module

The L64767's clocking scheme uses two independent clock signals (ICLK, OCLK) to control incoming data, internal data processing, and decoded output data. These clocks provide the timing for two circular FIFO buffers that read and write data. Data on the FIFO input is latched with respect to the valid rising edges of ICLK. Data on the FIFO output is read with respect to the valid rising edge of OCLK.

A FIFO control unit coordinates the operation of these two asynchronous ports and issues the appropriate control signals. For proper operation of the FIFO control unit, you must ensure that OCLK is frequency-locked to ICLK.

The global control circuitry of the L64767 governs the entire data path from an MPEG-2 input source, through the processing chain, and to the final output from the device. Global control ensures that the output data stream is continuous (no gaps between the symbols), assuming that the incoming data rate is constant. The output clock OCLK of the L64767 is externally derived from the input clock ICLK, and is kept in sync through a phase-locked loop (PLL) module locked to the appropriate ICLK versus OCLK ratio. Short term variations of frequency offset are handled by the 128-byte circular FIFO buffer. Other variations are controlled by the external PLL module.

You can check for overrun errors using the FIFO collision detection feature. This provides immediate output on a pin when a collision is detected and sends an interrupt-generating event on the microprocessor interface.

Microprocessor Interface

The L64767 has a bidirectional microprocessor interface that allows you to write to and read back from the 14 internal registers. During normal operation, the L64767 requires no interaction with the microprocessor. However, you must configure all registers after a reset operation to guarantee that the device will function properly.

The default operational mode of the L64767 is used for DVB-compliant operation at 64 QAM, and for four-fold oversampling. However, the chip supports modes of operation from 16 to 256 QAM.

The internal registers you configure through the microprocessor define the primary operational modes of the L64767. These modes and configurations include the following, among many others:

- Input synchronization mode (whether to lock synchronization to sync bytes or input pulses)
- Nyquist filter coefficients
- Delay value for proper FIFO initialization

The microprocessor interface is related to microcontrollers of the 68xxx family. The L64767 is not dedicated to supporting high-speed burst modes of DMA controllers with continuously asserted CS_N signal at the interface.

If the L64767 detects an error, the error is indicated on output pins of the L64767 and through the microprocessor interface. Error indications like the FIFOALARM signal are helpful for debugging and troubleshooting.

Test Unit

A built-in scan chain executes the functionality test. The pins SCAN_ENABLE, SCAN_MODE, and T_N are used for this purpose.

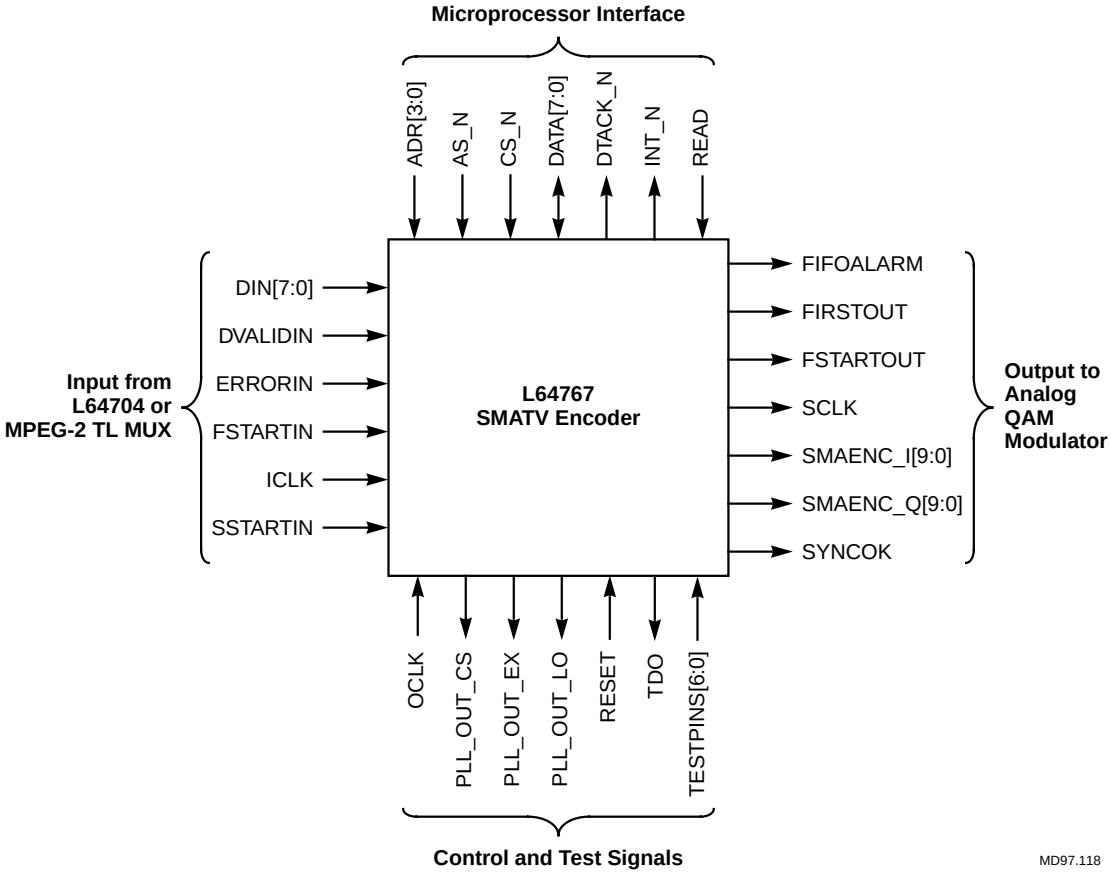
Signal Descriptions

This section describes the L64767's interface signals. As shown in Figure 4, these signals are grouped into the following categories:

- Input signals (for example, those from an LSI Logic L64704 for the MPEG-2 TL MUX)
- Output signals (for example, to an analog QAM modulator)
- Control signals (including test pins)
- Microprocessor interface signals

Within each category, the signals are described in alphabetical order by signal mnemonic.

Figure 4. L64767 Signals



Input Signals

This section describes the input signals to the L64767 from another device such as the LSI Logic L64704 for the MPEG-2 TL MUX.

DIN[7:0] **Parallel/Serial Data In** **Input**
This is a level-sensitive, 8-bit data bus for parallel or serial data input. Serial data is fed to DIN[0]. Data is sampled at the rising edge of ICLK.

DVALIDIN **Clock Enable Input** **Input**

This is an active HIGH, level-sensitive data signal. When HIGH, the L64767 accepts data from DIN[7:0] on a continuous basis. When LOW, the L64767 halts data input to the internal FIFO buffer and other data processing blocks. No new input from the DIN[7:0] pins is accepted.

ERRORIN **Error Detection Flag** **Input**

This is an active HIGH, level-sensitive data signal. When an uncorrectable error occurs, ERRORIN is HIGH. The L64767 checks the status of ERRORIN at the first bit of a frame. If an error has occurred, the ERRORIN status is copied to the MPEG-2 error indication bit if required.

FSTARTIN **External Sync Frame Start** **Input**

This is an active HIGH, level-sensitive data signal. Driving FSTARTIN to HIGH marks the beginning of an MPEG-2 transport packet. If the incoming bitstream contains no unique synchronization words, you must use this pin to indicate the frame start. Synchronization with FSTARTIN is forced into the chip and is not flywheel stabilized. If the sync insertion mode is programmed, the L64767 regenerates sync information and inserts it into the data stream as programmed by the microprocessor interface.

ICLK **Input Clock** **Input**

This is a positive, edge-triggered input clock. The L64767 samples inputs DIN[7:0], DVALIDIN, ERRORIN, FSTARTIN, and SSTARTIN on ICLK's rising edge. ICLK is either a byte clock or a bit clock, depending on the programming of SERIN (bit 7 of Register 0).

SSTARTIN **Sync Sequence Start** **Input**

This is an active HIGH signal that marks the beginning of a new, fully reset sequence. If the signal's falling edge is evaluated, all internal sequences (inverted sync, scrambler, interleaver, and differential encoder) are restarted with the next block start. If SSTARTIN is never asserted, all internal sequences run free after the reset. This pin has an internal pull-down resistor.

Output Signals

This section describes the output signals from the L64767 to another device such as an analog QAM modulator.

FIFOALARM **FIFO Collision Detected** **Output**
This alarm signal indicates the FIFO control has detected equal pointers for read and write access. The collision is probably caused by an unlocked external PLL-VCO circuitry. The signal is synchronized with SCLK-driven flip-flops for the output.

FIRSTOUT **First Block of a New Sequence Out** **Output**
This signal occurs together with FSTARTOUT and indicates the head of a sync block, which has just reset all internal sequences, as controlled by SSTARTIN. FIRSTOUT is the acceptance of an SSTARTIN falling edge delayed by all internal processing modules.

FSTARTOUT **Frame Start** **Output**
FSTARTOUT is driven HIGH during the first symbol in every sync frame. The width of FSTARTOUT reflects the number of bytes inserted by the gap parameter. A one-cycle width indicates no additionally inserted gaps. A width of 17 means 16 RS check bytes have been inserted. FSTARTOUT is applied only in synchronization word detection mode. If synchronization is forced by FSTARTIN pulses, FSTARTOUT is constantly LOW.

SCLK **Symbol Clock** **Output**
SCLK is a clock output signal that is synchronous to symbols and bytes processed internally.

SMAENC_I[9:0]
Symbol I Modulation **Output**
These signals provide 10-bit digital values at the digital filter output for D/A conversion and for analog modulation.

SMAENC_Q[9:0]
Symbol Q Modulation **Output**
These signals provide 10-bit digital values at the digital filter output for D/A conversion and for analog modulation.

SYNCOK **SYNC Detection/Phase Monitoring** **Output**
In internal sync mode, when this signal is HIGH, it indicates a correct lock to the input sync sequence, and the number of track steps required for synchronization is fulfilled. If synchronization is forced by FSTARTIN pulses, SYNCOK is constantly LOW.

Control Signals

This section describes the control signals for the L64767.

OCLK **Output Processing Clock** **Input**
This is a positive edge-triggered clock signal. The L64767 internally processes data (through the scrambler, interleaver, and Reed-Solomon encoder) based on a fraction of OCLK. Data outputs (I, Q, FSTARTOUT) are referenced to OCLK. OCLK is independent of ICLK.

PLL_OUT_CS **PLL Current Source** **Output**
This signal is a 4.5-mA charge pump output from the phase/frequency detector. The comparator is frequency- and phase-sensitive. This signal is normally 3-state Z level, and drives positive and negative current as required. Depending on the configuration, the current source can be inverted.

PLL_OUT_EX **PLL Phase Sensitive EXOR Comparator** **Output**
This signal is the output from the EXOR phase comparator.

PLL_OUT_LO **PLL Phase Sensitive Lock Detector** **Output**
This signal is the output from the PLL lock detector.

RESET **Reset** **Input**
This is a level-sensitive data signal. It resets all internal data paths. Reset timing is asynchronous to the device clocks and does not interfere with the active clock edges of ICLK and OCLK for reproducible output values. Reset affects all the configuration registers and filter coefficients, which must be downloaded again after reset.

Test Signals

The eight signals described below control functions such as chip-level, full scan tests, JTAG tests, and internal RAM tests. Five pins (TCK, TDI, TDO, TMS, and TRST) are used for JTAG tests. The other three pins are for SCAN_ENABLE, SCAN_MODE, and T_N (test output enable). Note that the L64767 is in normal functional mode when SCAN_ENABLE, SCAN_MODE, TCK, TDI, TMS, T_N, and TRST are left unconnected.

SCAN_ENABLE
Scan Enable **Input**
This is a level-sensitive data signal with a pull-down resistor. When HIGH, this signal enables scan chain shift. In default normal operation, SCAN_ENABLE is LOW.

SCAN_MODE **Scan Mode** **Input**
This is a level-sensitive signal with a pull-down resistor. When this signal is HIGH, the chip is switched to scan test mode. In default normal operation, SCAN_MODE is LOW.

TCK **Test Mode Clock** **Input**
When HIGH, this is a rising or falling edge signal for the JTAG test mode clock. In default normal operational mode, TCK is LOW.

TDI **Test Data Input** **Input**
When HIGH, this level-sensitive signal provides JTAG data input. In default normal operational mode, TDI is LOW.

TDO **Test Data** **Output**
This is the JTAG data output.

TMS **Test Mode Select** **Input**
When HIGH, this level-sensitive signal enables the JTAG test mode. In default normal operational mode, TMS is LOW.

T_N **Test Output Enable** **Input**
This is an active LOW signal with a pull-up resistor that disables the test mode when T_N is LOW. It switches all 3-stated buffers to high-impedance mode for test or device selection on a common bus. In default normal operation, T_N is HIGH.

TRST **JTAG Test Reset** **Input**
When HIGH, this level-sensitive data signal resets the JTAG unit. In default normal operational mode, TRST is LOW.

Microprocessor Interface Signals

This section describes the microprocessor interface signals of the L64767.

ADR[3:0] **Address for Internal Registers** **Input**
This is a level-sensitive, 4-bit address bus the L64767 uses along with the 8-bit data bus DATA[7:0], a read/write strobe (READ), a chip select strobe (CS_N), and an address strobe (AS_N) to read and write internal registers. The address lines are used to select among internal registers.

AS_N **Address Strobe** **Input**
This is an active LOW address strobe input signal. It latches the address on the ADR[3:0] bus on the falling edge.

CS_N **Chip Select** **Input**
This is an active LOW chip select strobe input signal. During a read cycle, CS_N must be LOW to access the on-chip data registers. The controller can latch the data from the L64767 with the rising edge of CS_N. During a write cycle, CS_N must go active LOW prior to data being valid from the controller to the L64767. After the data has met the minimum setup time, CS_N HIGH will strobe the data. There is a minimum write time to allow for internal synchronization.

DATA[7:0] **Data Bus [7:0]** **Bidirectional**
This is a level-sensitive data signal. The bidirectional data bus is used for input when writing data to the chip, and as output when the chip is read. When not being read or written, the data lines are 3-stated.

DTACK_N **Data Acknowledge** **Output**
This is an active LOW output signal indicating that the transaction on the data bus is completed.

INT_N	**Interrupt Request**	**Output**
	The L64767 drives INT_N LOW when the interrupt is enabled and an interrupt condition occurs. INT_N is an open drain output, requiring an external pull-up resistor for operation.	
READ	**Read/Write Strobe**	**Input**
	This level-sensitive data signal is an active LOW write strobe input signal. The microprocessor must drive this signal LOW to write to the L64767's registers, and must drive it HIGH to read from them.	

Specifications

This section presents the electrical, timing, pinout, and packaging specifications for the L64767.

Electrical Requirements

This section lists the DC electrical requirements for the L64767.

The tables in this section specify the electrical requirements for the L64767 encoder.

- Table 1 provides the L64767's absolute maximum electrical and temperature ratings.
- Table 2 provides the L64767's recommended operating conditions.
- Table 3 lists the L64767's DC characteristics.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Unit
V_{DD}	DC supply	-0.3 to +7	V
V_{IN}	Input voltage	-0.3 to V_{DD} +0.3	V
I_{IN}	DC input current	±10	mA
T_{STG}	Storage temperature range (plastic)	-40 to +125	°C

1. Referenced to V_{SS}.

Table 2. Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{DD}	DC supply	+4.75 to +5.25	V
T_A	Ambient temperature	0 to +85	°C

For values in Table 3, note that the L64767 is produced with LSI Logic's LCB300K HCMOS process, which is characterized by a 0.6-micron drawn gate-length (0.45-micron effective channel length). Values in the table are specified at V_{DD} = 5 V ± 5% at ambient temperature over the specified range.

The actual product characterization for the L64767 was not available at the time of this printing.

Table 3. DC Operating Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{IL}	Voltage input LOW, TTL		–	–	0.8	V
V_{IH}	Voltage input HIGH, TTL		2.0	–	–	V
V_{IL}	Voltage input LOW, CMOS				1.5	
V_{IH}	Voltage input HIGH, CMOS		3.5			
V_{OH}	Voltage output HIGH	I_{OH} = -4.0 mA	2.4	4.5	–	V
V_{OL}	Voltage output LOW	I_{OL} = 4.0 mA	–	0.1	0.4	V
I_{OZ}	Current 3-state leakage with pull-down	V_{DD} = Max, V_{OUT} = V_{SS} or V_{DD}	-10	±1	250	µA
I_{IN}	Current input leakage	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	-10	±1	10	µA
I_{IN}	Current input leakage with pull-up	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	-220	±1	10	µA
I_{IN}	Current input leakage with pull-down	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	-10	±1	250	µA
I_{DD}	Quiescent supply current	V_{IN} = V_{DD} or V_{SS}	–	–	2	mA
I_{CC}	Dynamic supply current	ICLK = 62.5 MHz, OCLK = 31.25 MHz, V_{DD} = Max	–	200	–	mA
P	Power dissipation				1	W

1. Specified at V_{DD} = 5 V ± 5% at ambient temperature over the specified range.

AC Timing

This section presents L64767 AC timing information, which was simulated using a 16 MHz microprocessor. The numbers in column 1 of Table 4 refer to the timing parameters shown in the timing diagrams that follow. All parameters in this table apply for T_A = 0 °C to 85 °C, V_{DD} = 4.75 V to 5.25 V, and an output load of 50 pF.

The actual product characterization for the L64767 was not available at the time of this printing.

Table 4. L64767 Timing Parameters

Parameter		Description	31/62 MHz		Unit
			Min	Max	
1	t_{CYCLE}	Clock Cycle OCLK	32	–	ns
2	t_{PWH}	Clock Pulse Width HIGH OCLK	15	–	ns
3	t_{PWL}	Clock Pulse Width LOW OCLK	15	–	ns
4	t_{I_CYCLE}	Clock Cycle ICLK	16	–	ns
5	t_{I_PWH}	Clock Pulse Width HIGH ICLK	7	–	ns
6	t_{I_PWL}	Clock Pulse Width LOW ICLK	7	–	ns
7	t_{I_S}	Input Setup Time to ICLK	6	–	ns
8	t_{I_H}	Input Hold to ICLK	1	–	ns
9	t_{OD}	Output Delay from OCLK	3	15	ns
10	t_{RWH}	Reset Pulse Width HIGH	50	–	ns
11	t_{WK}	Wake-up time after RESET, used for RAM initialization during microprocessor configuration access	1024 2244	– –	ICLK cycles with DVALIDIN = HIGH OCLK cycles
12	t_{SURCS}	READ Setup Before CS_N LOW	1	-	ns
13	t_{SUA}	ADR[3:0] Setup Before AS_N LOW	2	-	ns

(Sheet 1 of 2)

Table 4. (Cont.) L64767 Timing Parameters

Parameter		Description	31/62 MHz		Unit
			Min	Max	
14	t_{HLDA}	ADR[3:0] Hold After AS_N LOW	1	-	ns
15	t_{DCSDTL}	CS_N LOW to DTACK_N LOW	-	3 t_{CYCLE} + 15	ns
16	t_{HLDD}	Write Data Hold After CS_N HIGH	0	-	ns
17	t_{CYCLE_CS}	Minimum CS_N Width	2 t_{CYCLE}	-	ns
18	t_{HLDRCS}	READ Hold After CS_N HIGH	1	-	ns
19	t_{WRREC}	Write Recovery Time	2 t_{CYCLE}	-	ns
20	t_{DCSDTH}	CS_N HIGH to DTACK_N HIGH	-	2 t_{CYCLE} + 15	ns
21	t_{DELZL}	CS_N LOW to Data Driven	-	3 t_{CYCLE} + 20	ns
22	t_{DELD}	CS_N LOW to Data Valid	-	3 t_{CYCLE} + 20	ns
23	t_{DELLZ}	CS_N HIGH to Data 3-State	-	2 t_{CYCLE} + 20	ns
24	t_{SUD}	Data Setup Before CS_N Change	6	-	ns
25	t_{TDLY}	Delay from T_N	–	15	ns
(Sheet 2 of 2)					

Figure 5. L64767 Synchronous AC Timing

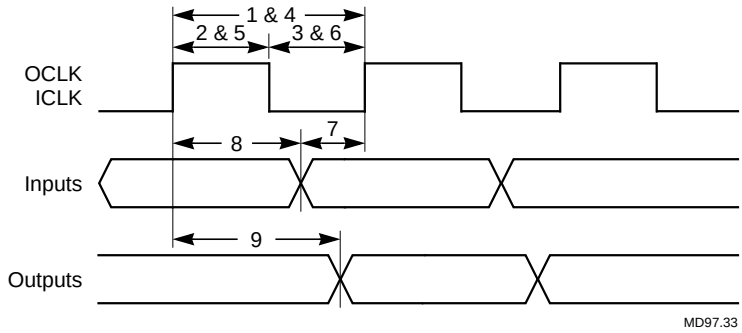


Figure 6. L64767 Read Cycle

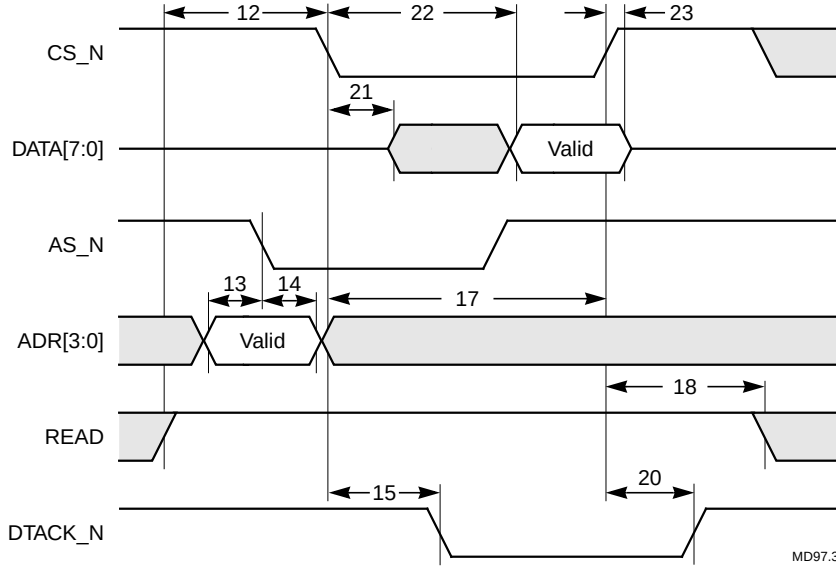


Figure 7. L64767 Write Cycle

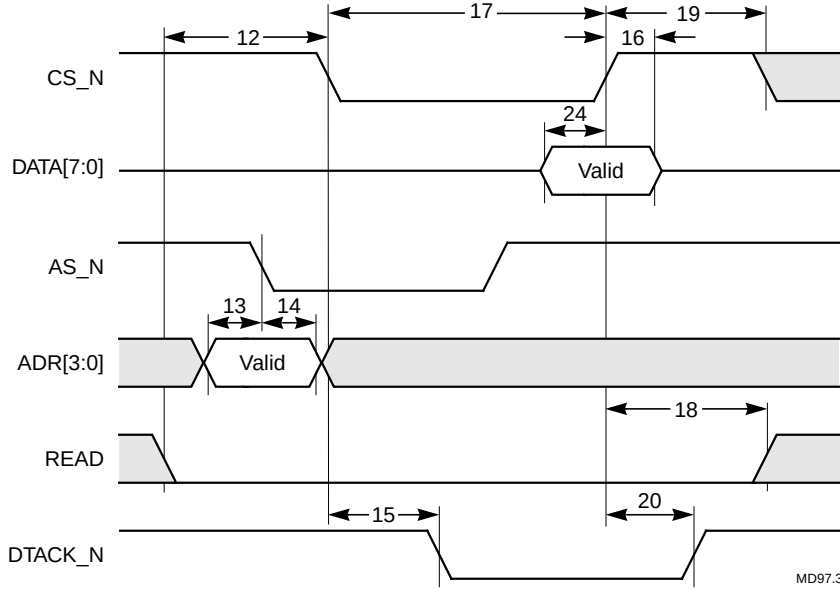


Figure 8. L64767 RESET Timing Diagram

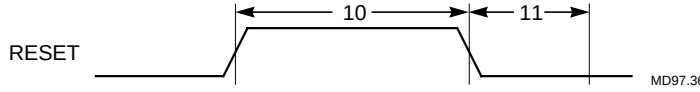
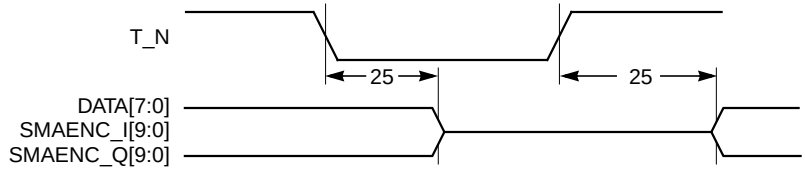


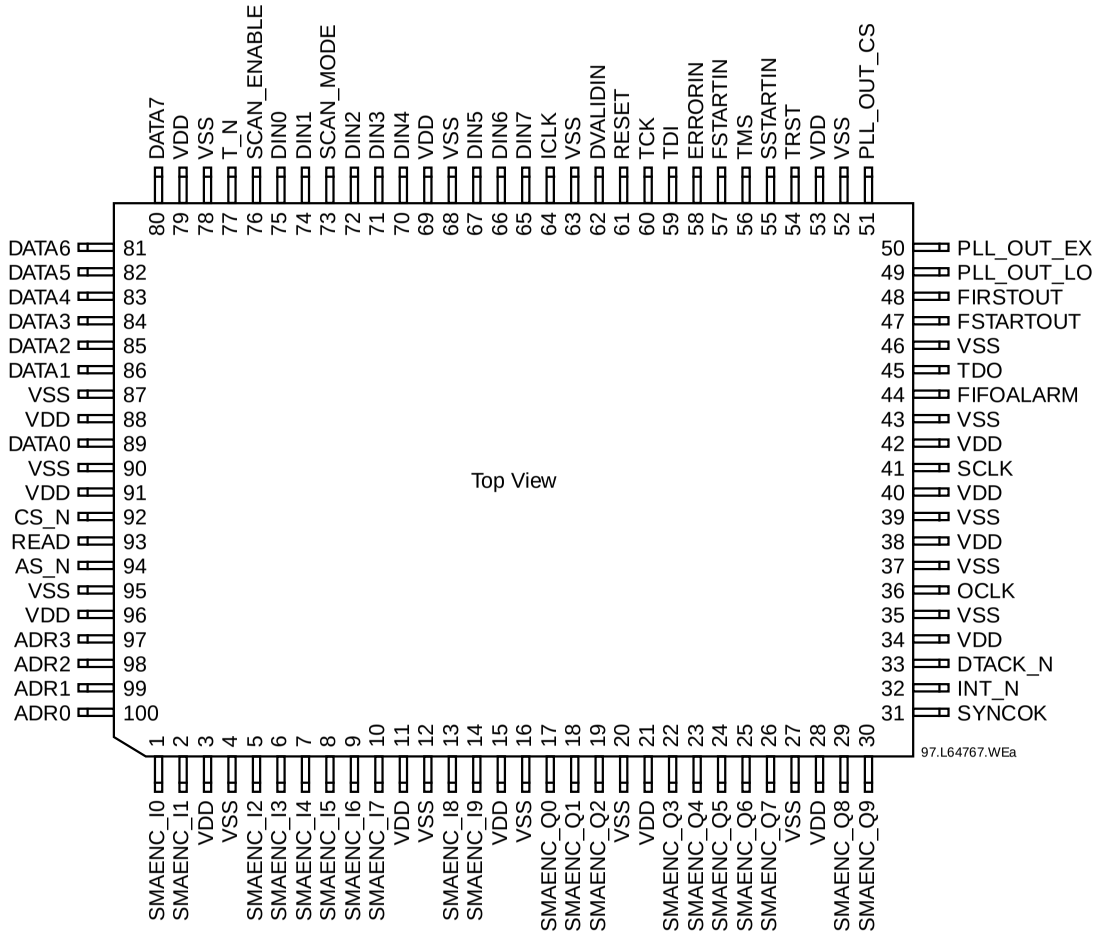
Figure 9. L64767 Bus 3-State Delay Timing



Pinout and Packaging

Figure 10 shows the signal pins of the L64767 SMATV encoder. It shows the location, pin number, and signal for each pin on the 100-pin MQUAD package. This pinout is followed by the mechanical dimensions of the L64767's package.

Figure 10. 100-Pin MQUAD Pinout



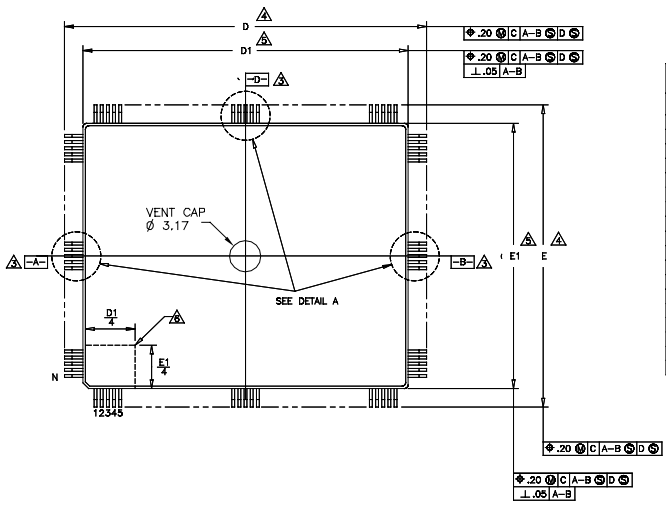
Mechanical Dimensions

Figure 11 provides packaging information for the 100-pin MQUAD (WE, RECTANGULAR) L64767 chip.

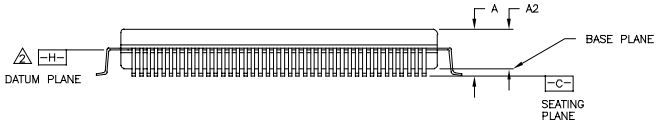
Figure 11. 100-Pin MQUAD Mechanical Drawing (Cavity Up)

For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code WE.

REVISIONS		
DESCRIPTION	DATE	REV.
SEE DOCUMENT CONTROL TITLE PAGE	1–22–97	1

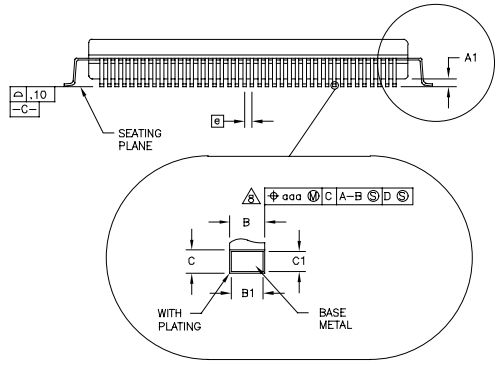


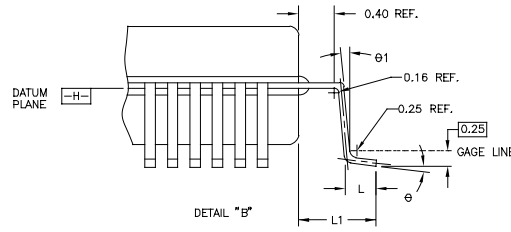
DIMENSIONS IN MM				NOTE
SYM	MIN	NOM	MAX	
A			3.40	
A1	0.25			
A2	2.50	2.80	3.05	
B	0.22	0.33	0.38	8,10
B1	0.22		0.33	
C	0.13		0.23	8,10
C1	0.15 +/– 0.03			
D	23.65	23.90	24.15	4
D1	19.70	20.00	20.10	5
e	0.65 BSC			
E	17.85	17.90	18.15	4
E1	13.74	14.00	14.10	5
L	0.73	0.88	1.03	
L1	1.95 REF.			
N	100			
θ	0		7	
θ1	0		7	
aaa			0.10	



LSI LOGIC CORPORATION		
48580 KATO ROAD FREMONT CA 94539		
TITLE: 100 LEAD MQUAD OUTLINE (CAVITY UP)		
CODE: WE	MD97.WE-1	
DWG NO. JZ01–000320–00	REV. 1	
SCALE NOT TO SCALE	SHEET 1 of 2	

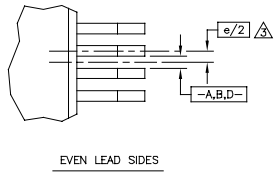
Figure 11 (Cont.) 100-Pin MQUAD Mechanical Drawing (Cavity Up)



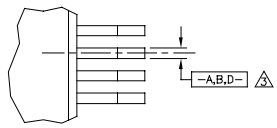


NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE –H– IS LOCATED AT THE SEAL PARTING LINE IS COINCIDENT WITH THE BOTTOM OF THE LEADS WHERE THE LEAD EXITS THE PACKAGE BODY
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
4. TO BE DETERMINED AT SEATING PLANE –C–.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE SEAL PROTRUSION ALLOWABLE PROTRUSION IS .25mm/.010" PER SIDE. DIMENSIONS D1 AND E1 DO NOT INCLUDE SEAL MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. CONTROLLING DIMENSION: MILLIMETER.
8. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .08mm/.003" TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACING BETWEEN ADJACENT LEADS TO BE 0.10 mm
9. MARKING AREA MUST BE FREE FROM PACKAGE SURFACE PROTRUSSION OR INTRUSION.
10. PLATING THICKNESS INCLUDED, PLATING THICKNESS TO BE 0.005mm MINIMUM, 0.020mm MAXIMUM.
11. VENT CAP PROTRUSION MUST NOT EXCEED 0.127 mm.



EVEN LEAD SIDES



ODD LEAD SIDES

DETAIL "A"

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LSI LOGIC CORPORATION 48580 KATO ROAD FREMONT CA 94539		
TITLE: 100 LEAD MQUAD OUTLINE (CAVITY UP)		
CODE: WE	MD97.WE-2	
DWG NO. JZ01–000320–00	REV. 1	
SCALE: NOT TO SCALE	SHEET 2 of 2	

L64767 Pin Descriptions

This section describes the signal pins of the L64767 SMATV encoder.

Table 5 summarizes the pins on the L64767. The table provides the signal types for both output and input pins, and the drive capacity for outputs. The summary is followed by Table 6, a pin list, which relates the signal on each pin to a pin number on the 100-pin MQUAD package.

Table 5. L64767 Pin Description Summary

Mnemonic	Description	Type	Drive (mA)	Active
DIN[7:0]	Parallel/Serial Data In	TTL Input	–	HIGH
DVALIDIN	Clock Enable Input	TTL Input	–	HIGH
ERRORIN	Error Detection Flag	TTL Input	–	HIGH
FSTARTIN	External Sync Frame Start	TTL Input	–	HIGH
ICLK	Input Clock	TTL Input	–	+
SSTARTIN	Sync Sequence Start	TTL Input with pull-down	–	HIGH
FIFOALARM	FIFO Collision Detected	Output	4	HIGH
FIRSTOUT	First Block of a New Sequence Out	Output	4	HIGH
FSTARTOUT	Frame Start	Output	4	HIGH
SCLK	Symbol Clock	Output	4	+
SMAENC_I[9:0]	Symbol I Modulation	3-State Output	4	HIGH
SMAENC_Q[9:0]	Symbol Q Modulation	3-State Output	4	HIGH
SYNCOK	Sync Detection/Phase Monitoring	Output	4	HIGH
OCLK	Output Processing Clock	TTL Input	–	+
PLL_OUT_CS	PLL Current Source	3-state Current Source	4	3-state
PLL_OUT_EX	PLL Phase Sensitive EXOR Comparator	Output	4	HIGH

(Sheet 1 of 2)

Table 5. (Cont.) L64767 Pin Description Summary

Mnemonic	Description	Type	Drive (mA)	Active
PLL_OUT_LO	PLL Phase Sensitive Lock Detector	Output	4	HIGH
RESET	Reset	TTL Input	–	HIGH
SCAN_ENABLE	Scan Enable	TTL Input with pull-down	–	HIGH
SCAN_MODE	Scan Mode	TTL Input with pull-down	–	HIGH
TCK	Test Mode Clock	TTL Input with pull-down	–	+
TDI	Test Data Input	TTL Input with pull-down	–	HIGH
TDO	Test Data	Output	4	HIGH
TMS	Test Mode Select	TTL Input with pull-down	–	HIGH
T_N	Test Output Enable	TTL Input with pull-up	–	LOW
TRST	JTAG Test Reset	TTL Input with pull-down	–	HIGH
ADR[3:0]	Address for Internal Registers	TTL Input	–	HIGH
AS_N	Address Strobe	TTL Input	–	LOW
CS_N	Chip Select	TTL Input	–	LOW
DATA[7:0]	Data Bus [7:0]	Bidirectional TTL I/O	–	HIGH
DTACK_N	Data Acknowledge	Output	4	LOW
INT_N	Interrupt Request	Open Drain, driving LOW	4	LOW
READ	Read/Write Strobe	TTL Input	–	HIGH

(Sheet 2 of 2)

Table 6. Pin List for the 100-pin MQUAD

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	SMAENC_I0	26	SMAENC_Q7	51	PLL_OUT_CS	76	SCAN_ENABLE
2	SMAENC_I1	27	VSS	52	VSS	77	T_N
3	VDD	28	VDD	53	VDD	78	VSS
4	VSS	29	SMAENC_Q8	54	TRST	79	VDD
5	SMAENC_I2	30	SMAENC_Q9	55	SSTARTIN	80	DATA7
6	SMAENC_I3	31	SYNCOK	56	TMS	81	DATA6
7	SMAENC_I4	32	INT_N	57	FSTARTIN	82	DATA5
8	SMAENC_I5	33	DTACK_N	58	ERRORIN	83	DATA4
9	SMAENC_I6	34	VDD	59	TDI	84	DATA3
10	SMAENC_I7	35	VSS	60	TCK	85	DATA2
11	VDD	36	OCLK	61	RESET	86	DATA1
12	VSS	37	VSS	62	DVALIDIN	87	VSS
13	SMAENC_I8	38	VDD	63	VSS	88	VDD
14	SMAENC_I9	39	VSS	64	ICLK	89	DATA0
15	VDD	40	VDD	65	DIN7	90	VSS
16	VSS	41	SCLK	66	DIN6	91	VDD
17	SMAENC_Q0	42	VDD	67	DIN5	92	CS_N
18	SMAENC_Q1	43	VSS	68	VSS	93	READ
19	SMAENC_Q2	44	FIFOALARM	69	VDD	94	AS_N
20	VSS	45	TDO	70	DIN4	95	VSS
21	VDD	46	VSS	71	DIN3	96	VDD
22	SMAENC_Q3	47	FSTARTOUT	72	DIN2	97	ADR3
23	SMAENC_Q4	48	FIRSTOUT	73	SCAN_MODE	98	ADR2
24	SMAENC_Q5	49	PLL_OUT_LO	74	DIN1	99	ADR1
25	SMAENC_Q6	50	PLL_OUT_EX	75	DIN0	100	ADR0

Notes

Notes

Notes

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