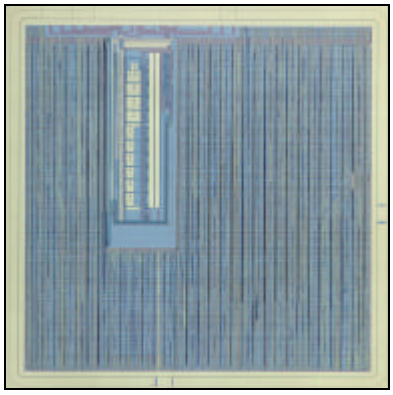
CW901101 10-Bit Pipelined ADC Core

CoreWare

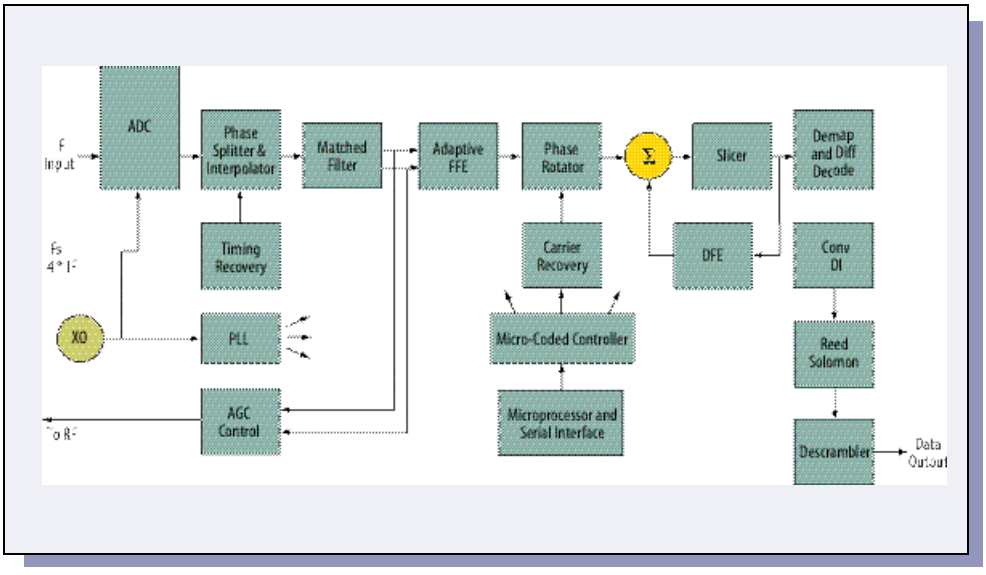
Overview

The CW901101 is a high-performance 10-bit 45MSPS analog-to-digital converter (ADC) core targeted for digital receivers of cable modems, digital set-top boxes or digital TVs (DTV). The core is compatible with LSI Logic's FlexStream® ASIC design environment to enable seamless integration of the mixed-signal core into complex ASICs. Proven in silicon, this core allows customers to reduce time to market while providing cost reductions by integrating the ADC on chip.



The CW901101 ADC Core

The complex, high frequency QAM IF signals received by digital receivers are generally downconverted or directconverted in the analog domain and then digitized using a high-speed ADC. They are then filtered and demodulated for further digital signal processing. Sampling techniques such as oversampling and undersampling are used to convert the analog QAM IF signals to a high resolution 10-bit parallel stream. Whether an application requires undersampling or oversampling, the ADC must deliver high levels of dynamic performance. The overall system performance will depend on the ADC's dynamic parameters including spurious-free dynamic range (SFDR), total harmonic distortion (THD) and signal-to-noise ratio (SNR) or signal-to-noise and distortion ratio (SINAD). The CW901101 core employs a pipelined architecture and meets the high signal integrity, bandwidth and sampling speeds necessary to digitize the incoming signals for 256-QAM or OFDM demodulation. Power consumption and core size have been optimized with performance to create an attractive solution for digital receivers.



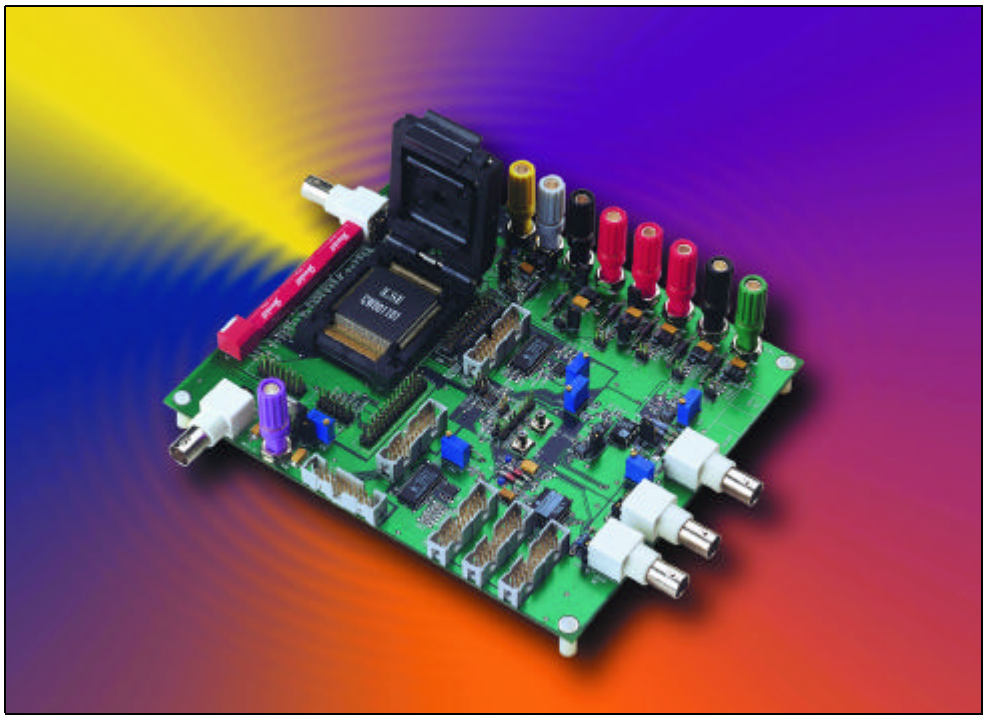
Cablestream™ QAM Receiver Block Diagram

LSI LOGIC

CW901101 10-Bit Pipelined ADC Core

Features

- 45MSPS - maximum sampling rate
- Input voltage range: 1 Vp-p, 2 Vp-p, or 3 Vp-p
- SNDR: 54dB minimum
- Maximum power dissipation: 150mW at 45MHz
- Analog voltage: 2.7 to 3.6 V
- Dual-mode digital voltage: 2.25 to 2.75 V or 1.62 to 1.98 V
- On-chip offset, gain and linearity calibration
- Two power-down modes
- On-chip digitally-trimmable bandgap reference



The CW901101 test board enables customers to evaluate the ADC performance for their target application prior to instantiating the core into the ASIC.

LSI Logic uses a dedicated mixed-signal design kit to provide a wide range of mixed-signal solutions for many applications. This design kit enables rapid re-use of mixed-signal cores as well as core verification from the transistor level up to system level. LSI Logic's wide portfolio of mixed-signal cores, including data converters, comparators, op amps, PLLs, high-speed transceivers, video DACs and audio DACs have been developed for easy instantiation into ASICs together with elements from LSI Logic's digital IP libraries, memories and I/Os.

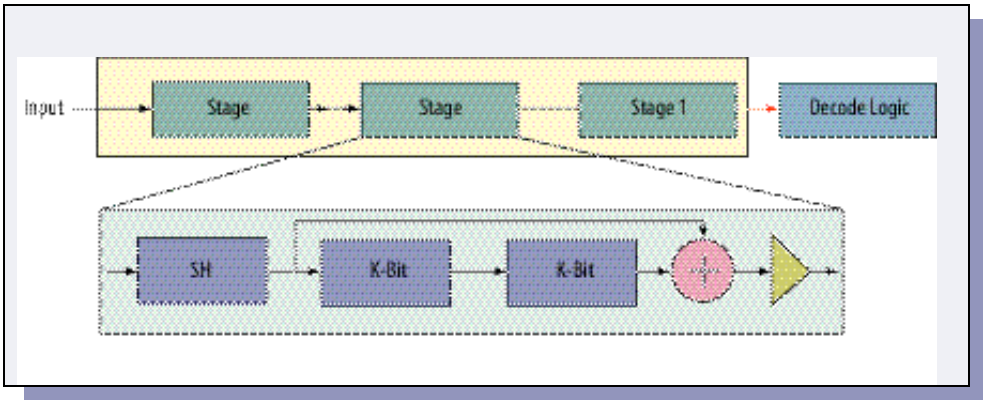
Together with the CW90110, LSI Logic offers a complete digital CoreWare® library of industry-standard building blocks including microprocessor and DSP cores, a range of leading-edge packaging options and a robust design methodology in 0.25-micron drawn G11™ process to meet customers' system-on-a-chip requirements.

CW901101 Description

The 10-bit CW901101 ADC core employs a pipelined architecture to maximize the achievable speed and resolution while maintaining a low-power and size-efficient solution. Following an initial 7.0 clock-cycle latency, a new 10-bit digital output is delivered once each clock cycle. Integral linearity is within ±1 least significant bit (LSB). The output format is 2's complement, ranging from 200 to 1FF.

The CW901101 can be configured to operate with a variety of system configurations. Both 2.5 V and 1.8 V digital core interfaces are supported, in addition to 3 pre-set and programmable input voltage ranges. For enhanced operation at lower conversion rates, two digitally-selectable input stages enable optimized dynamic performance at slower speeds, while programmable bias current levels allow for reduction of power consumption. Both single-ended and differential inputs are supported. A dual-mode power-down feature is available which enables either a complete power-down of the CW901101 or a 90% power-down with fast wake-up time.

The CW901101 can be independently digitally calibrated for linearity as well as gain and offset, depending upon the system sensitivity to these parameters. During calibration for linearity, two additional digital bits are produced which are then used to reduce numerical truncation errors. Digital programmability of the bandgap reference and full-span voltages allow the CW901101 to be calibrated for both absolute and relative gain and offset errors.



Pipelined ADC Architecture

Benefits

- Calibrates digitally to ensure converter linearity
- Programmable current reference for reduced power consumption in low-speed applications
- Optimized frontend for different sampling conversion rates
- Accepts both single-ended or differential-ended input signals

CW901101 10-Bit Pipelined ADC Core

Mixed-Signal ASIC Methodology

The 45MSPS 10-bit CW901101 ADC core is a member of LSI Logic's mixed-signal ASIC family. Designs proceed rapidly and with predictable results when using LSI Logic's design methodology and the companion CoreWare library of predefined, fully characterized functional blocks or cores.

The LSI Logic mixed-signal ASIC methodology enables a standard design flow to integrate analog circuit and digital logic elements on the same chip. It also enables ASIC sign-off with nonproprietary, third-party verification tools within the LSI Logic FlexStream design environment.

The application-ready mixed-signal cores include a complete set of design files:

- Verilog or VHDL analog behavioral model and digital structural model
- LSI Logic FlexStream database
- Static timing
- Synthesis models
- Netlist
- Topocell

LSI Logic uses test chips to verify core instantiation methodology, function and parametric performance. The test chips can serve as design lead vehicles when used on hardware evaluation boards for performance analysis. LSI Logic provides complete documentation and global customer design engineering support to ensure that all mixed-signal cores are easily instantiated into silicon and meet full manufacturability.

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