

MultiLynx™ CL2161 Universal HFC Interactive Cable Transceiver



OVERVIEW

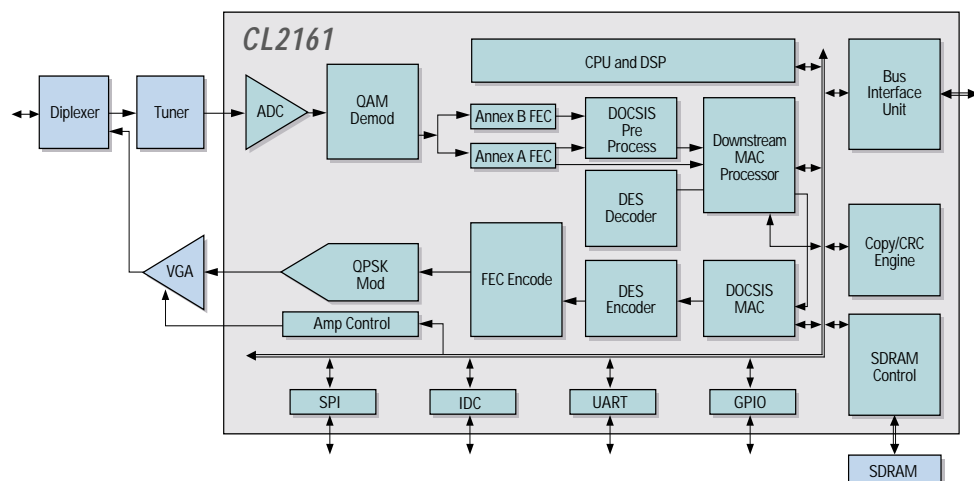
The MultiLynx™ CL2161 is a universal cable transceiver solution for advanced set-top boxes (STBs) and cable modems compliant with DVB In-Band, DOCSIS, and EuroDOCSIS standards. The CL2161 is built for STB and cable modem manufacturers requiring the maximum performance with the lowest system BOM cost. Its high level of integration provides manufacturers with a flexible, yet quick time-to-market solution.

The CL2161 is a complete and highly integrated solution combining a QAM demodulator for downstream reception, a QPSK/16-QAM modulator for upstream transmission, and a field-proven DOCSIS 1.0/1.1-compliant media access controller (MAC).

The downstream channel provides full 16-256 QAM demodulation and is compliant with ITU J.83 Annex A and B and integrates a 10 bit A/D converter. The upstream QPSK/16-QAM burst transmitter along with ITU J.112 Annex A-, B-compliant FEC encoding provides a robust and cost-effective solution for DOCSIS applications.

The hardware MAC (with packet parsing, filtering, and decryption), and the two internal processors – an 88 MHz mini-RISC and 117 MHz SPARC v8 processor, upon which the standard specific MAC software is executed – allow for flexible implementation of DVB In-Band, DOCSIS, or EuroDOCSIS standards.

The CL2161 has a full complement of low-speed peripheral interface devices including those commonly used on commercial tuners such as SPI, inter-device communications (IDC), UART, and GPIO interfaces.



High-Level Block Diagram of MultiLynx™ CL2161



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Multilynx™ CL2161 Universal HFC Interactive Cable Transceiver

The SPARC processor internal to the CL2161 includes a DSP instruction set necessary for IP telephony applications. When combined with a MPEG source encoder/decoder, this solution delivers video telephony technology to the consumer.

Forward Channel	
Standards Compliance	ITU-T J.83 Annex A and B, DOCSIS 1.0, DOCSIS 1.1
A/D Converter	Internal 10-bit
Symbol Rate	Variable from 1 – 7.2 Mbaud
QAM Constellations	16 - 256 QAM
IF Input Frequencies	36 MHz or 44 MHz IF inputs
Output	Optional transport stream output
Return Channel	
Standards Compliance	DOCSIS 1.0 and DOCSIS 1.1
D/A Converter	Internal 10-bit
RF Output	5 MHz to 65 MHz
Modulation	QPSK and 16 QAM
DOCSIS 1.0 Features	Advanced modem pre-equalization of transmit signal Internal CMTS clock synchronization: no VCXO
Additional Features	Analog and digital gain control
Processor and Control	
Internal Microprocessor	117 MHz SPARC V8 processor for Media Access Control software
Clock Generation	Onboard PLL running from a single external crystal
AGC Output	Supports many variable gain amplifier devices, including, but not limited to: Analog Devices AD8321, Lucent Technologies V4911, Anadigics ARA05050 and ARA 1400, Maxim MAX3501
Tuner Control	Implemented via SPI, IDC, or GPIO
Peripherals	
Interface Modules	Inter-Device Communications (IDC, Mastermode only) On-chip UART Serial Peripheral Interface (SPI) General Purpose I/O (GPIO)
MAC	
Standards Compliance	DOCSIS 1.0, DOCSIS 1.1, EuroDOCSIS, DVB In-Band
Host	
Master Mode	Coldfire, 68K, Async Flash
Slave Mode	PCI, Power PC, Coldfire (5206, 5307), 68K, SH3/4
Physical	
Input Voltage	3.3V + 5% (tolerates 5V inputs, except SDRAM), 1.8V
Packaging	208-pin PQFP
SPARC Operating Frequency	117 MHz or 88 MHz

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