LF3312
12-Mbit Frame Buffer / FIFO

Advance Information

Features

- 12,441,600-bit Frame Memory
- May be Organized Into the Following Configurations:
  - 1,555,200 x 8-bit (single channel)
  - 1,244,160 x 10-bit (single channel)
  - 1,036,800 x 12-bit (single channel)
  - 777,600 x 16-bit (single channel)
  - 622,080 x 20-bit (single channel)
  - 518,400 x 24-bit (single channel)
  - 777,600 x 8-bit (each of two parallel channels)
  - 622,080 x 10-bit (each of two parallel channels)
  - 518,400 x 12-bit (each of two parallel channels)
- Eight Operating Modes:
  - One-Channel Synchronous Shift Register (Single Clock Source)
  - One-Channel Framestore With Sequential Write and Random Access Read
  - One-Channel Framestore With Random Access Write and Sequential Read
  - One-Channel FIFO With Asynchronous I/O
  - Two-Channel Synchronous Shift Register (Single Clock Source)
  - FIFO + shift register; Channel B Synchronized to Channel A
  - Shift register + FIFO; Channel A Synchronized to Channel B
  - Two-Channel FIFO; Both Channels Sychronized to External Signal (a)

(a) power-up default mode

- Features in the Four Modes With Asynchronous FIFOs:
  - Near-Full/Empty Flags With Programmable Thresholds
- Features in the Six Purely Sequential (FIFO, shift register) Modes:
  - Up to 100 MHz Continuous Data Throughput Rate
- Features in the Two Random Access (non-FIFO) Modes:
  - Up to 100 MHz Data Rate
- LF3312s may be Connected in Parallel for HDTV, Multiframe SDTV, etc.
- Built-in ITUR-656 TRS detection and Synchronization
- User-Set/Resettable Read and Write Pointers
- Choice of Control Interfaces:
  - Two-wire Serial Microprocessor Interface
  - Parallel Microprocessor Interface
- Input Enable Control (Write Mask)
- Output Enable Control (Data Skipping)
- 169 ball BGA
- 1.8V Internal Core Power Supply
- 3.3V I/O Supply
- 5V-Tolerant I/O

Applications

- Field-Based or Frame-Based Comb Filtering
- Image or Data Sequence Capture
- Resynchronization of Data Streams
- Video Special Effects (Rotation, Zoom, Picture-in-Picture)
- Test Pattern Generation
- High Speed Data Buffering
- Motion Detection or Frame-to-Frame Correlation
- Closed Circuit or Security Camera Systems

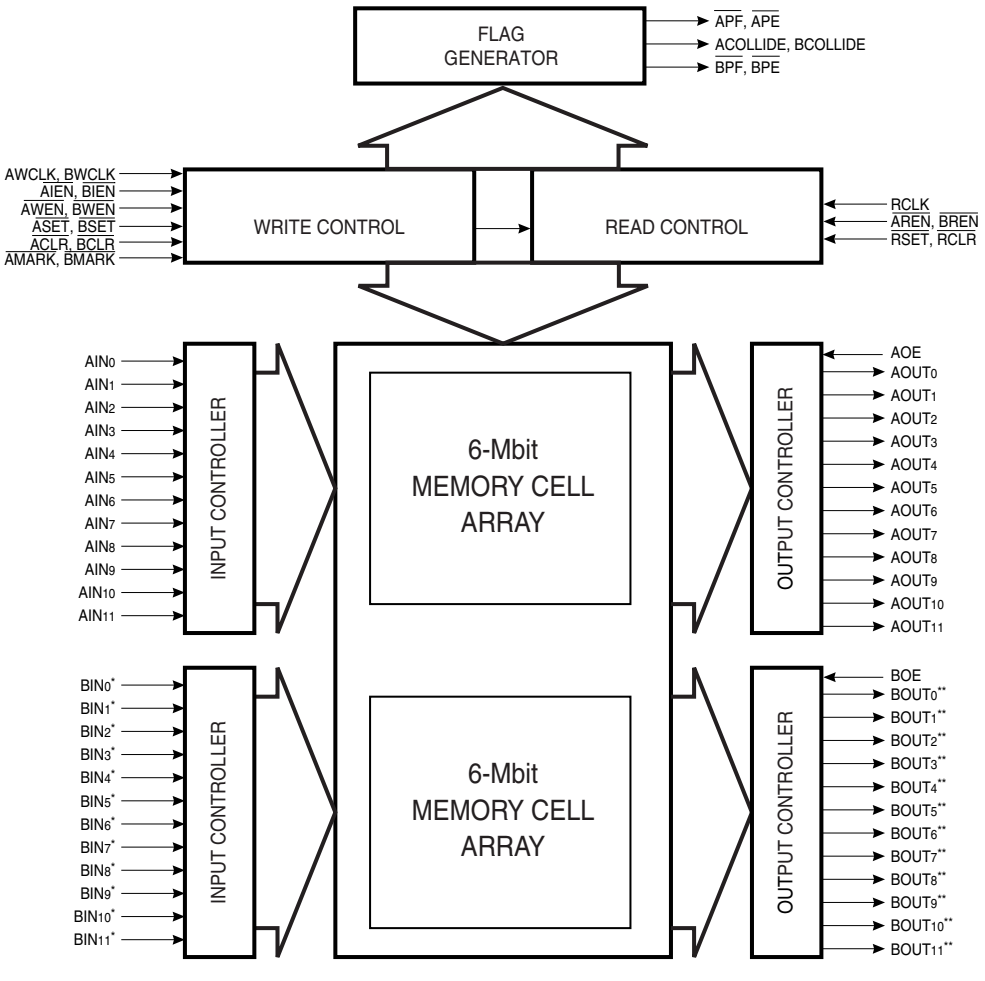
LF3312 Overview

The LF3312 is a 12,441,600-bit memory chip which can be configured by the user into either a two-data-port single-channel or a four-data-port dual-channel architecture. The input data ports may be clocked simultaneously or asynchronously with one another and with the output ports. Using the four 12-bit data ports provided, the user can operate the chip as one or two 8-, 10-, or 12-bit channels or as a single 16-, 20-, or 24-bit channel, without wasting any memory resources. Since reads are non-destructive, a given data value, once written into the memory core, may be read as many times as desired. A user requiring more storage can cascade up to sixteen LF3312s into a larger array. The device is controlled by sixteen instruction words of eight bits each, which may be programmed or verified via a standard I^2C 2-wire serial or parallel microprocessor interface.

The 3-bit OPMODE control selects one of the chip's eight distinct operating modes, each of which has versatile submode options:

- One-Channel FIFO With Asynchronous I/O
- Two-Channel FIFO; Both Channels Sychronized to External Signal
- One-Channel Synchronous Shift Register (Single Clock; User-set Latency)
- Two-Channel Synchronous Shift Register (Single Clock; User-set Latencies)
- One-Channel Framestore With Sequential Write and Random Access Read
- One-Channel Framestore With Random Access Write and Sequential Read
- Two-Channel FIFO; Channel A Synchronized to Channel B
- Two-Channel FIFO; Channel B Synchronized to Channel A

LF3312 Functional Block Diagram



* Doubles as lower portion of random address input
** Do bles as pper portion of random address inp t

Figure 1. Dual Channel FIFO Mode Functional Block Diagram

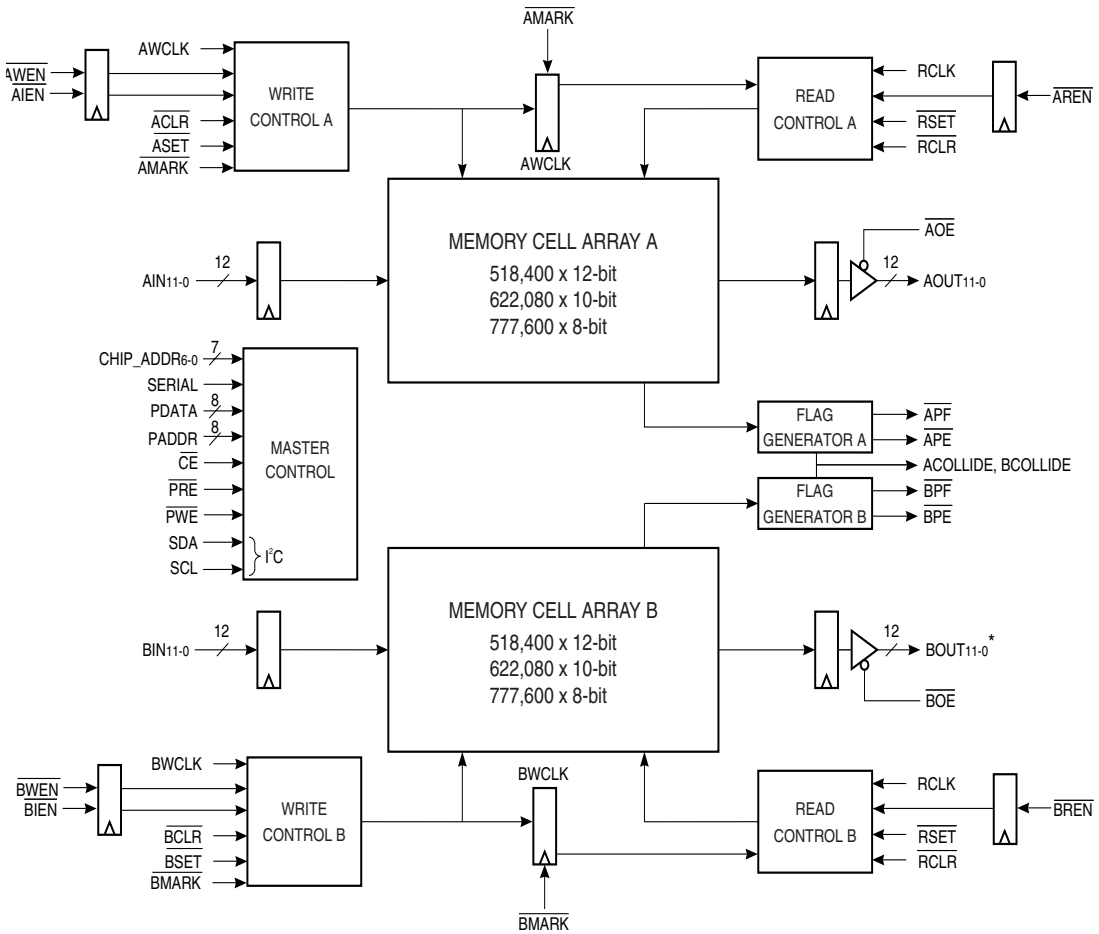


Figure 2. Single Channel FIFO Mode Functional Block Diagram

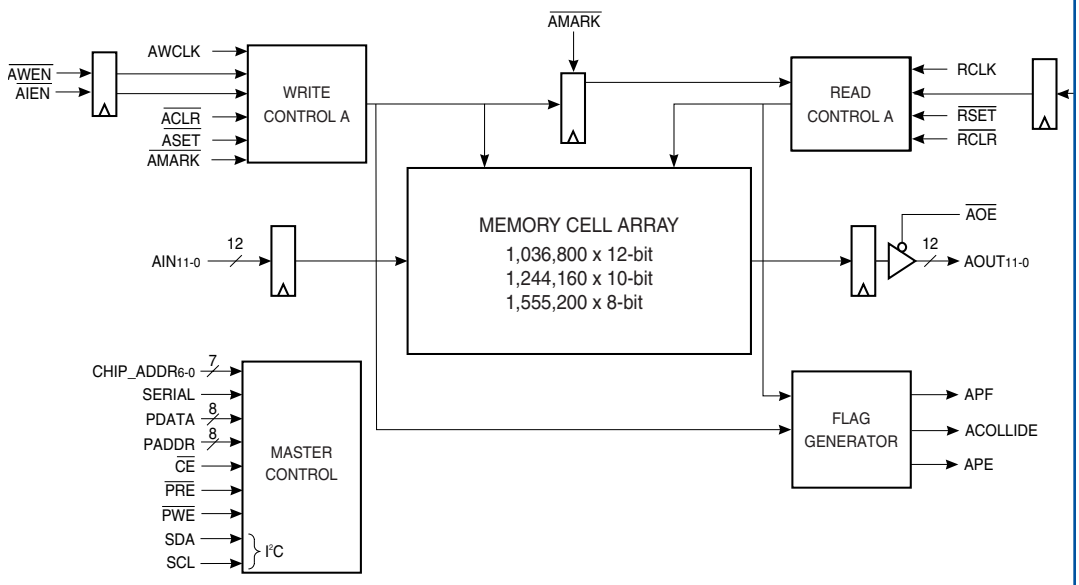
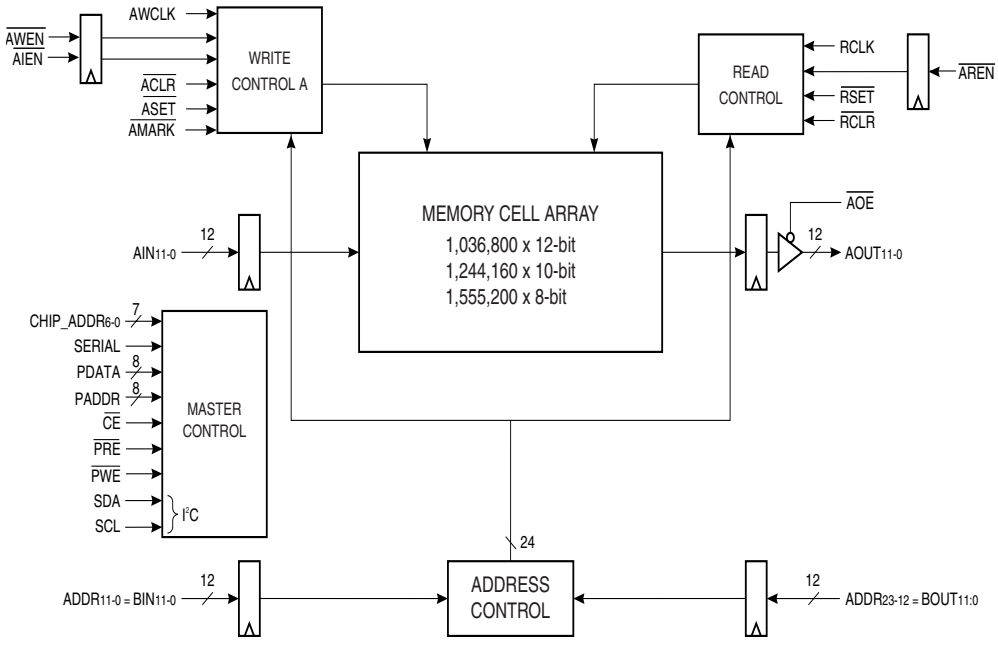


Figure 3. Random Access Mode Functional Block Diagram



Operating Modes

Asynchronous single-channel FIFO mode (OPMODE = 3)

In OPMODE 3, the LF3312 is configured as a single channel First-In-First-Out memory with a 12-Mbit core, with independant read and write clocks to allow for asynchronous operation. This mode is ideal for buffering or burst data applications.

As a single channel FIFO, the LF3312 must have AWCLK and BWCLK tied together as must be AWEN with BWEN, and AIEN with BIEN. In this mode the device can re-time a data stream according to a read sync signal (RSET or RCLR) and either ITU-R656 Timing Reference Signals (TRS) embedded within the incoming (video) data or the falling edge of a write sync signal applied to ACLR, ASET, or AMARK. The input (write) and output (read) clocks need not be synchronous with one another, although the memory core will eventually fill or empty if they differ in average frequency. After it "fills," the LF3312 will begin to lose prestored data by writing over it before it has been read. If the memory core "empties," the host will begin to read a stored data sequence for a second time. In either case, when the read and write addresses reach equality, the ACOLLIDE flag will go high, to alert the host. The almost-full and almost-empty flags provide advance warning of these conditions whenever user-selected "fullness" or "emptiness" thresholds, expressed in approximate eightieths of the memory core size, are exceeded. For example, if the 1/80 and 79/80 thresholds are enabled, flag APE will go HIGH whenever the read pointer lags behind the write pointer by less than 1/80 of the memory space, and flag APF will go HIGH whenever the read pointer leads the write pointer by this amount. (Calculations are performed modulo the total address space.) The data input and output are sequential and the timing between write and read sync signals dynamically determines the effective delay (depth) of the FIFO.

Dual-channel asynchronous FIFO mode (OPMODE = 7; power-on default)

OPMODE 7 operates identically to the single channel FIFO (OPMODE 3), with two independent chanels.

In dual-channel asynchronous FIFO mode, the device can accept two asynchronous data streams and automatically adjust the latency of each to bring it into alignment with an output sync signal applied to RSET or RCLR. Again, the user may reference input synchronization either to ACLR, ASET, BCLR, and BSET, to AMARK and BMARK, or to embedded TRS. The data read/output clock need not be synchronous with either of the two input clocks, which likewise need not be synchronous with one another. If memory core A or B "empties" or "fills" completely, ACOLLIDE and/or BCOLLIDE respectively, will be set accordingly if the write and read pointers collide.

The data Word that BMARK 'marks' (by going LOW during that xWCLK cycle) in the input data stream will be the first synchronized AOUT/BOUT data word. If N full frames of Channel A data have been loaded into AIN before the first Channel B data frame is loaded into BIN, the second frame of B channel data will be synchronized to the (N+1)th Channel A frame. (there will be N frames difference between Channel A and B).

Single-channel synchronous shift register mode (OPMODE = 0)

In OPMODE 0, the LF3312 becomes a single channel shift register with programmable total latency up to 2^{24}-8 clock cycles. Writes and reads occur simultaneously, hence synchronous operation.

In OPMODE 0, the user provides a single clock for both the input and output clocks and specifies a desired input-to-output data path latency, (ALAT) via the control interface. AWCLK, BWCLK, and RCLK must be tied together, as should AWEN, BWEN, AREN, and BREN. When activated, ALAT will begin to countdown, and once expired, will allow the inputs to begin to appear on the outputs. In OPMODE 0, ALAT countdown can be activated in two ways. The first occurs when the first enable is brought LOW after the LOAD signal has been set HIGH after MPU programming. The second is by bringing LOAD HIGH once MPU programming complete, after the enables have been brought LOW.

Operating Modes

Dual-channel synchronous shift register mode (OPMODE = 4)

The operation of dual-channel shift register mode is identical to single-channel operation, with the addition of a second independent channel. The latency for each channel is independent and set by the user.

The user must also supply a single clock to tie AWCLK, BWCLK, and RCLK together, and must load the respective desired constant latency for each channel, (ALAT, BLAT), via the microprocessor bus. ALAT and BLAT are activated in the same manner as in OPMODE 0, with the respective inputs being made available on the outputs once ALAT or BLAT expire. In this mode, $\overline{AWEN}$ and $\overline{AREN}$ must be tied together, as must be $\overline{BWEN}$ and $\overline{BREN}$.

Random access write mode (OPMODE = 2)

Random access write mode allows the user to write to any location in the memory by suppling the LF3312 with addresses via the BIN and BOUT data ports, while reads from memory are performed sequentially.

In OPMODE_2, $\overline{ASET}$ = 0, $\overline{BSET}$ = 1, $\overline{BCLR}$ = 0, AWCLK and BWCLK must be tied together as must $\overline{AWEN}$ and $\overline{BWEN}$. On each active write clock cycle (rising edge of AWCLK for which $\overline{AWEN}$ was LOW for the previous rising edge of AWCLK), the user directs the write pointer to any desired memory location, using what are otherwise the second channel data input and output ports. **In this application, BOUT[11:0] denotes the vertical component, and BIN[11:0], the horizontal component, of a Cartesian set.** Setting the control register ROW_LENGTH to the frame's row length internally defines the Cartesian coordinates. Or, if desired, the concatenation of BOUT[11:0] in front of BIN[11:0] represents a single 24-bit linear address. The user governs the mapping of (BOUT,BIN) to the internal memory space by setting the parameter ROW_LENGTH such that ADDRESS = BOUT * ROW_LENGTH + BIN. A ROW_LENGTH setting of 0 is interpreted as 4096, such that ADDRESS = a 24-bit concatenation of {BOUT,BIN} for this particular value. For a standard D1 video application with 1716 samples per line, the user would set ROW_LENGTH to 1716 decimal = 6B4 hex. Offset circuitry within the LF3312 permits the user to gang several chips in parallel and to use them collectively as a single large memory. Data are read out sequentially by rising edges of RCLK, under the control of $\overline{AREN}$ (read enable), $\overline{RSET}$ (read pointer force to constant), and $\overline{RCLR}$ (read pointer clear to 0). Holding $\overline{ASET}$ LOW keeps the chip continuously in random access write mode. Releasing $\overline{ASET}$ to its HIGH state causes the chip to continue to write sequentially from the last-loaded address, albeit still at the random access rate of up to 100MHz.

Random access read mode (OPMODE=1)

Random read gives the user the ability to read the contents of any memory location while writing sequentially into memory. Addressesing is accomplished through the BIN and BOUT data ports.

In OPMODE 1, $\overline{RSET}$ = 0, $\overline{BCLR}$ = 1, $\overline{BSET}$ = 0, MARK_SEL = 1, AWCLK and BWCLK must be tied together as well as $\overline{AWEN}$ and $\overline{BWEN}$. Similar to OPMODE = 2, the user controls this time the read pointer over ports BIN and BOUT. In this case, (single-address) writing is sequential and under the control of ACLR, $\overline{ASET}$, and $\overline{AWEN}$. As in random access write mode, BOUT[11:0] represents the upper bits or the vertical address, whereas BIN[11:0] represents the lower bits or the horizontal address. Releasing RSET HIGH causes the read address pointer to increment from its last randomly-assigned location.

Operating Modes

Dual-channel master/slave mode (OPMODE = 5)

OPMODE 5 is one of two master/slave synchronizing modes where two data streams are written into the LF3312 at independent rates and with independent TRS timing information. In this mode, both channels are synchronized together based on the sync data supplied to channel A or by the embedded TRS data within the A channel.

When in OPMODE 5, channel A operates as a fully synchronous master shift register, to which the data in asynchronous FIFO channel B is re-timed. The user drives AWCLK and RCLK from the incoming AIN data stream's sample clock, and BWCLK from the BIN data stream's clock. The user also specifies whether sync timing will be derived from TRS words embedded within the incoming data streams or from signals applied to ACLR and ASET or to AMARK and BMARK. AWEN, AREN and BREN must be tied together to maintain constant reference latency through channel A and to synchronize the outputs. When a MARK occurs, the signal MARK_ACTIVE_RSET when set high, allows the read pointer to be set to the registered value of the write pointer ALAT RCLK cycles later. If the user sets MARK_ACTIVE_RSET = 0, the LF3312 will ignore the internal read pointer set.

Dual-channel slave/master mode (OPMODE = 6)

OPMODE 6 is the reverse of OPMODE 5, with the difference being that the two streams are synchronized to the timing information applied to the B channel or embedded within the B channel as TRS data.

This OPMODE is identical to the previous, except that channel A is the slave FIFO and channel B is the master shift register, and RCLK needs to be tied to BWCLK, and BWEN needs to be tied to BREN and AREN. Similarly to mode 5, when a MARK occurs, the signal MARK_ACTIVE_RSET when set high, allows the read pointer to be set to the registered value of the write pointer BLAT number of RCLK cycles later. If the user sets MARK_ACTIVE_RSET = 0, the LF3312 will ignore the internal read pointer set.

Device Configuration

Programming the LF3312

The LF3312 has two MPU interfaces. The first is a standard two wire serial interface following the I²C protocol. The second is a parallel interface allowing the user to write a byte of data at a time to the configuration registers. When the user wishes to use the serial interface, the SERIAL pin must be set HIGH, while a LOW will chose the parallel interface.

Serial MPU Interface

When the SERIAL pin is HIGH, the serial interface is active. Up to 16 LF3312 devices can be connected to and programmed by the serial interface. The two wire interface is composed of an SCL clock pin and a bi-directional SDA data pin. When inactive, SDA and SCL are forced HIGH by external pull up resistors.

Data transmission is achieved over the SDA pin and must remain constant during the logical HIGH portion of the SCL clock pulse. The level of SDA, while SCL is HIGH, is interpreted as the appropriate bit value as will be shown later. Changing the data on SDA must only occur when SCL is low, because any changes to SDA while SCL is HIGH is interpreted as a start or stop request, which are shown in Figure 7 with an example data transfer in Figure 8.

The first operation to begin programming the LF3312 through the serial interface, is to send a start signal. When the interface is inactive, a HIGH to LOW transition must be sent on SDA while SCL is HIGH, notifying all connected devices (slaves) to expect a data transmission. When transferring data, the MSB of the eight bit sequence is the first bit to be transmitted to or from the master or slave. The first byte of data to be transmitted on SDA must consist of the 7-bit base address of the slave, along with an 8th READ/WRITE bit as the LSB, which describes the direction of the data transmission. The slave who's 7-bit value found on pins CHIP_ADDR6-, matches the 7-bit base address sent on SDA, will send an acknowledgement back to the master by bringing SDA LOW on the 9th SCL pulse.

During a write operation, if the slave does not send an acknowledgment back to the master device, SDA is left high which forces the master to generate a stop signal. In contrast, during a read operation, if there is no acknowledgement back from the master device, the LF3312 interprets this as if it were the end of the data transmission, and leaves SDA high, allowing the master to generate its stop signal.

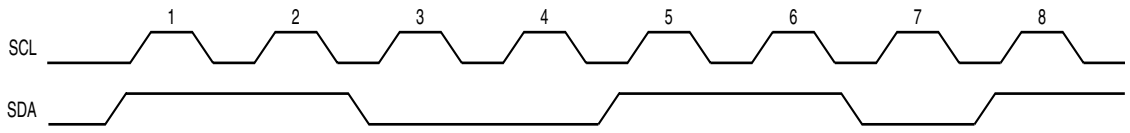
Figure 7 - I²C Start and Stop Signals

Device Configuration

There are four operations that can be performed between the master and the slave. They are: Write to consecutive registers, write to a single control register, read from consecutive registers and read from a single register. To write to consecutive control registers, a start signal and base address must be sent with the R/W bit as described above. After the acknowledgment back from the appropriate slave, the 8-bit address of the target control register must be written to the slave with the R/W bit LOW. The slave then acknowledges by setting SDA LOW. The data byte to be written into the register can now be transferred on SDA. The slave then acknowledges by setting SDA to be LOW on the next positive going pulse of SCL. The first control register address loaded into the LF3312 is considered as the beginning address for consecutive writes, and automatically increments to the next higher address space. Therefore after the acknowledgement, the data byte to configure register (first address + 1) can now be transferred from master to slave. At any point a stop signal can be given to end the data transfer. To write to a single control register, the same technique can be applied adding a stop signal after the first data write.

To read from consecutive control registers, the master must again give the start signal followed by a base address with the R/W bit = 0, as if the master wants to write to the slave. The appropriate slave then acknowledges. The master will then transfer the target register address to the slave and wait for an acknowledge. The master will then give a repeated start signal to the slave, along with the base address and R/W bit this time HIGH signifying a read and wait for an acknowledge. The user must write to the LF3312 to select the appropriate initial target register. Otherwise the starting position of the read is uncertain. Once the LF3312 acknowledges, the next byte of data on SDA is the contents of the addressed register sent from the device. If the master acknowledges, the LF3312 will send the next higher register's contents on the following byte of data. To read from only one register is the same procedure as for consecutive reading with a stop signal following the transfer of the register's contents.

Figure 8 - I²C Example of transferring 11001101 on SDA



Parallel MPU Interface

The parallel MPU interface can be used to write instructions to the control registers or to read them back for verification. When the SERIAL pin is LOW, the parallel interface becomes active. An external processor can write into an internal register by setting PADDR to the desired register address, selecting the chip using the $\overline{CE}$ pin, setting PDATA to the desired value and then pulsing $\overline{WE}$ LOW. The data will be written into the selected register when both $\overline{WE}$ and $\overline{CE}$ are LOW, and will be held when either signal goes HIGH. To read from a control register the processor must set PADDR to the desired address, select the chip with the $\overline{CE}$ pin, and then set $\overline{RE}$ LOW. The chip will then drive PDATA with the contents of the selected register. After the processor has read the value from PDATA, $\overline{RE}$ and $\overline{CE}$ should be set HIGH. The PDATA pins are turned off (High Impedance) whenever $\overline{CE}$ or $\overline{RE}$ are HIGH or when $\overline{WE}$ is LOW. The chip will only drive these pins when both $\overline{CE}$ and $\overline{RE}$ are LOW and $\overline{WE}$ is HIGH. One can also ground the $\overline{RE}$ pin and use the $\overline{WE}$ pin as a read/write direction control and use the $\overline{CE}$ pin as a control I/O strobe.

Device Configuration

Parallel Interface Cont'd

Figure 5 - Writing and Reading From a Control Register

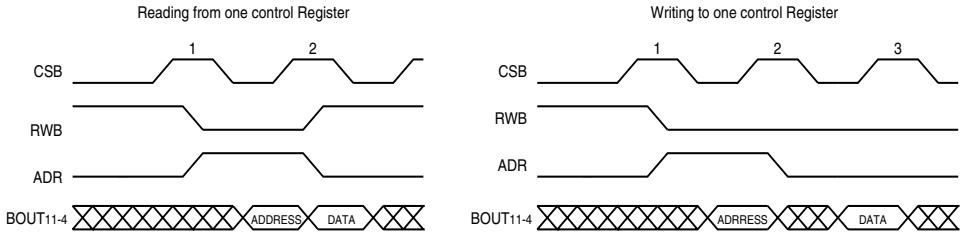
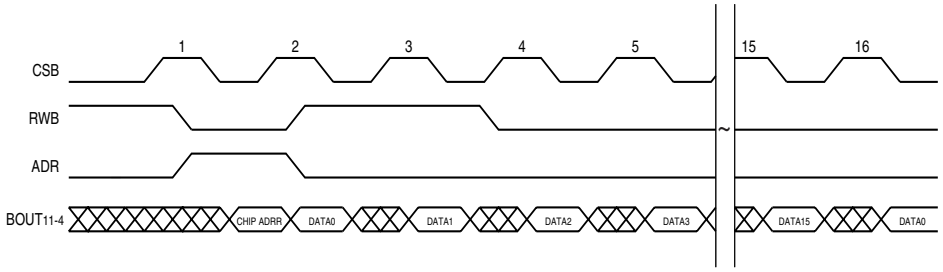


Figure 6 - Reading From Consecutive Control Registers



Detailed Signal Definition

Power

***VCC_{INT}* - Internal Core Power Supply**
+1.8V power supply. All pins must be connected.

***VCC_O* - Output Driver Power Supply**
+3.3V power supply. All pins must be connected.

Clocks

AWCLK - Write Clock A
Data present on AIN11-0 is written into the LF3312 on the rising edge of AWCLK when $\overline{\text{AWEN}}$ was LOW for the previous rising edge of AWCLK.

BWCLK - Write Clock B
In two-channel modes(OPMODES 4-7), data present on BIN11-0 is written into the LF3312 on the rising edge of BWCLK when $\overline{\text{BWEN}}$ is LOW. In one-channel modes(OPMODES 0-3), BWCLK must be tied to AWCLK.

RCLK
In single channel modes, data is read from the LF3312 and presented on the output port (AOUT11-0) after a rising edge of RCLK while $\overline{\text{AREN}}$ and $\overline{\text{AOE}}$ are LOW. In two-channel mode, data is also read from the LF3312 and presented on the output port (BOUT11-0) after a rising edge of RCLK while $\overline{\text{BREN}}$ and $\overline{\text{BOE}}$ are LOW.

Inputs

AIN11-0 - Data Input A
AIN11-0 is the 12-bit registered data input port. Bit 11 is the MSB in all modes. AIN1-0 are ignored in 10-bit mode and AIN3-0 are ignored in 8-bit mode. Any such unused inputs should either be tied to ground or driven to proper logic levels by external logic.

BIN11-0 - Data Input B
In dual-channel modes (OPMODES 4-7), BIN11-0 is the 12-bit registered data input port in all dual channel FIFO modes. Bit 11 is the MSB in all modes. BIN1-0 are ignored in 10-bit mode and BIN3-0 are ignored in 8-bit mode. Unused inputs should be tied off to ground or driven to proper logic levels by external logic. In random modes (OPMODES 1 & 2), BIN11-0 becomes the ADDR

CHIP_ADDR6-0 - Chip Address
CHIP_ADDR6-0 determines the LF3312's address on the two-wire microprocessor bus. Each LF3312 chip's 7-bit two-wire serial microprocessor interface address is equal to its CHIP_ADDR6-0.

SCL - Serial Clock Input
SCL is a standard two-wire serial microprocessor interface clock pin. With this chip, it functions as a dedicated input, since this part cannot be the master on an two-wire serial microprocessor interface.

ADDR23-0 - Random Read/Write Address
(OPMODES 1 and 2 ONLY) ADDR23-0 is a 24-bit memory address, which in OPMODE 2 becomes the random write address and the random read address when in OPMODE 1. AADR23-0 is input into the LF3312 via the BIN and BOUT data ports. BIN11-0 specifies the X-coordinate, ADDR11-0 and BOUT11-0 specifies the Y-coordinate, ADDR23-12 in linear mode, when the instruction register ROW_LENGTH is equal to 0(default). When ROW_LENGTH is equal to VALUE,

PADDR7-0 - Parallel Microprocessor Interface Address Port
PADDR7-0 is the 8-bit address port for the parallel microprocessor interface. When inactive becomes high impedance.

Detailed Signal Definition

Input/Output

PDATA7-0 - Parallel Microprocessor Interface Data Port
PDATA7-0 is the 8-bit data port for the parallel microprocessor interface. When inactive becomes high impedance.

SDA - Serial Data I/O
SDA is the standard bidirectional data pin of a two-wire serial microprocessor interface.

BOUT11-0 - Data Output B
In two-channel modes(OPMODES 4-7), BOUT11-0 is the 12-bit registered data output port. BOUT[11] is always the MSB. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when $\overline{BREN}$ is LOW. In OPMODES 1 and 2, BOUT11-0 becomes and input for the Y-coordinate of ADDR if ROW_LENGTH is equal to 0, or ADDR23-12 if ROW_LENGTH is some value other than zero. In OPMODES 0 or 3, BOUT11-0 represents ADDR23-12, when executing an RSET if and only if $\overline{AREN}$=0, MARKSEL=1, $\overline{BCLR}$=1. Again, if in OPMODES 0 or 3, BOUT11-0 represents ADDR23-12, when executing an ASET if and only if $\overline{AWEN}$=0, ACLR=1, $\overline{BSET}$=1. For more details on $\overline{RSET}$ and $\overline{ASET}$, please refer to their signal definitions.

Controls

$\overline{ACLR}$ - Channel A Write Pointer Clear
When $\overline{ACLR}$ is brought LOW, the next rising edge of AWCLK will bring the current value on AIN[11:0] into memory Channel A, address 0. Whenever $\overline{ACLR}$ is HIGH, the destination for AIN[11:0] will be controlled by $\overline{ASET}$. The user may program ACLR such that either its falling edge or its LOW state is active. If its LOW state is active, holding this pin LOW will hold the write address in its zero position continuously. This control takes effect only when $\overline{AWEN}$ is LOW.

$\overline{BCLR}$ - Channel B Write Pointer Clear / Channel A Write Random Select
In dual-channel modes (OPMODE = 4-7), this pin clears the Channel B Write Pointer, in the same manner that $\overline{ACLR}$ clears the Channel A Write Pointer, and the user may program it to be falling edge or LOW state active. In single-channel modes (OPMODE = 0-3), this pin and control MARKSEL govern the action of $\overline{RSET}$. In OPMODES 4-7, this control takes effect only when $\overline{BWEN}$ is LOW.

$\overline{ASET}$ - Channel A Write Pointer Set
This control is active only when $\overline{ACLR}$ is HIGH. Bringing $\overline{ASET}$ LOW will cause the next rising edge of AWCLK to bring the current value on AIN[11:0] into memory A, at the address specified by ALAT, or if OPMODE = 0-3 and $\overline{BSET}$ = 1, at the address whose Cartesian coordinates are present on BOUT and BIN. Whenever $\overline{ASET}$ and $\overline{ACLR}$ are HIGH, the next rising edge of AWCLK will bring the current AIN[11:0] data value into the next-higher address in sequence. $\overline{ASET}$ may be programmed to be either edge-triggered, in which case it affects the write pointer for only one clock cycle following a negedge, after which incrementing resumes, or level-triggered, in which case it affects the write pointer until it is brought HIGH. For continuous random access write operation, holding $\overline{ASET}$ LOW and programming it to be level-triggered will provide the needed continuous write pointer override. This control takes effect only when AWEN is LOW.

$\overline{BSET}$ - Channel B Write Pointer Set
In two-channel modes (OPMODE = 4-7), this pin's impact on the B write pointer is analogous to that of $\overline{ASET}$ on the A write pointer, and the user may program the pin's action to be either edge- or level-triggering. In one-channel modes, $\overline{BSET}$ determines whether $\overline{ASET}$ forces the write address pointer to ALAT (BSET = 0) or to BOUT,BIN ($\overline{BSET}$ = 1). In OPMODES 4-7, this control takes effect only when $\overline{BWEN}$ is LOW.

Detailed Signal Definition

$\overline{\text{AMARK}}$ - Channel A Write Address Pointer Mark
In single-channel mode, bringing this bit LOW will cause an internal register to store a copy the current value of the write address pointer, for subsequent use in synchronizing the corresponding read address pointer to the same location. Unlike ACLR and ASET, this control does not affect the write pointer value itself. The system must use AMARK instead of ACLR if the entire memory core can be filled between sequential falling edges of the sync reference signal. In contrast, the system must use ACLR or ASET to establish a definite relationship between the internal address and the data stream, as in random access read mode.

$\overline{\text{BMARK}}$ - Channel B Write Address Pointer Mark
(active only in dual channel modes, OPMODE = 4-7) Bringing this bit LOW will cause an internal register to store a copy the current value of the Channel B write address pointer, for use in synchronizing the corresponding read address pointer to the same location. This signal does not affect the value of the memory B write address pointer itself.

$\overline{\text{RSET}}$ - Read Address Pointer Set
In dual-channel modes (OPMODE = 4-7), if $\overline{\text{AREN}}$ is LOW, bringing $\overline{\text{RSET}}$ LOW will force read address pointer A to ALAT (if MARKSEL is HIGH) or to the value most recently captured from using AMARK (if MARKSEL is LOW). If BREN is LOW, bringing RSET LOW will force read address pointer B to BLAT (if MARKSEL is HIGH) or to the value most recently captured by BMARK (if MARKSEL is LOW). In single-channel modes (OPMODE = 0-3), if AREN is LOW, bringing RSET LOW will force the read address to the most recently marked value (MARKSEL LOW), to BLAT (MARKSEL HIGH and BCLR LOW), or to BOUT,BIN (MARKSEL is HIGH and BCLR is HIGH). This pin may be programmed to be either falling edge or level LOW active.

$\overline{\text{RCLR}}$ - Read Address Pointer Clear
Bringing RCLR LOW causes the next rising edge of RCLK to force the read address pointer (OPMODE 0-3) or pointers (OPMODE 4-7) to zero. This pin may be programmed to be active on its falling edge or in its LOW state. In single-channel mode, it can reset the read pointer only when AREN is LOW. In dual-channel mode, it can reset read pointer A only if AREN is LOW, and read pointer B only if BREN is LOW.

$\overline{\text{AWEN}}$ - Write Enable A
If $\overline{\text{AWEN}}$ is LOW, data on AIN11-0 is written to the device on the rising edge of AWCLK. When $\overline{\text{AWEN}}$ is HIGH, the device ignores data on AIN and holds the write pointer. The user must anticipate the use of $\overline{\text{AWEN}}$ by one cycle. Therefore when desiring not to write a sample, $\overline{\text{AWEN}}$ must be brought high the cycle before.

$\overline{\text{BWEN}}$ - Write Enable B
If $\overline{\text{BWEN}}$ is LOW, data on BIN11-0 is written to the device on the rising edge of BWCLK. When $\overline{\text{BWEN}}$ is HIGH, the device ignores data on BIN and holds the write pointer. The user must anticipate the use of $\overline{\text{BWEN}}$ by one cycle. Therefore when desiring not to write a sample, $\overline{\text{BWEN}}$ must be brought high the cycle before. In single channel modes (OPMODES 0-3), $\overline{\text{BWEN}}$ must be tied to $\overline{\text{AWEN}}$.

$\overline{\text{AIEN}}$ - Memory Write Enable A
$\overline{\text{AIEN}}$ is used to enable/disable writing into the memory core. A LOW on $\overline{\text{AIEN}}$ enables writing, while a HIGH on $\overline{\text{AIEN}}$ disables writing. The internal A write address pointer is incremented by $\overline{\text{AWEN}}$ regardless of the $\overline{\text{AIEN}}$ level. If disabling of $\overline{\text{AIEN}}$ is never desired, tie $\overline{\text{AIEN}}$ LOW.

$\overline{\text{BIEN}}$ - Memory Write Enable B
$\overline{\text{BIEN}}$ is used to enable/disable writing into the memory core. A LOW on $\overline{\text{BIEN}}$ enables writing, while a HIGH on $\overline{\text{BIEN}}$ disables writing. The internal A write address pointer is incremented by $\overline{\text{BWEN}}$ regardless of the $\overline{\text{BIEN}}$ level. If disabling of $\overline{\text{BIEN}}$ is never desired, tie $\overline{\text{BIEN}}$ LOW.

Detailed Signal Definition

$\overline{\text{AREN}}$ - Read Enable A
If $\overline{\text{AREN}}$ is LOW and the output port is enabled, data from Channel A is read and presented on AOUT11-0 after tD has elapsed from the rising edge of RCLK. If $\overline{\text{AREN}}$ goes HIGH, the last value loaded into Channel A output register will remain unchanged and the read pointer will be held. The user must anticipate the use of $\overline{\text{AREN}}$ by one cycle. Therefore when desiring not to read a sample, $\overline{\text{AREN}}$ must be brought high the cycle before.

$\overline{\text{BREN}}$ - Read Enable B
If $\overline{\text{BREN}}$ is LOW and the output port is enabled, data from Channel B is read and presented on BOUT11-0 after tD has elapsed from the rising edge of RCLK. If $\overline{\text{BREN}}$ goes HIGH, the last value loaded into Channel B output register will remain unchanged and the read pointer will be held. The user must anticipate the use of $\overline{\text{BREN}}$ by one cycle. Therefore when desiring not to read a sample, $\overline{\text{BREN}}$ must be brought high the cycle before.

SERIAL ***- Serial/Parallel Interface Selector***
When the user wishes to use the serial microprocessor to configure the LF3312, the SERIAL pin must be set HIGH, whereas if he or she wishes to use the parallel interface, SERIAL must be set LOW.

$\overline{\text{LOAD}}$ – Instruction Load
Bringing asynchronous control $\overline{\text{LOAD}}$ LOW updates the working instruction latches to match the current contents of the instruction preload latches. Holding it LOW causes the working latches to reflect all ongoing instruction preloads. Holding it HIGH permits the user to preset the instruction preload latches to any desired configuration without disturbing the work in progress.

$\overline{\text{RESET}}$ - Global Reset
Bringing asynchronous control $\overline{\text{RESET}}$ LOW forces all state machines and read and write pointers to 0 and holds them there until it is released HIGH. It also forces the control preload latch into a default single-channel FIFO state, if and only if $\overline{\text{LOAD}}$ is also LOW. To operate the chip in any other mode, the user may then preprogram the control registers via either the serial or the parallel microprocessor port. Bringing $\overline{\text{RESET}}$ LOW while holding $\overline{\text{LOAD}}$ HIGH will reset the state machines and pointers, but will not change either the preload or the working latches.

$\overline{\text{AOE}}$ - Output Enable A
When $\overline{\text{AOE}}$ is LOW, AOUT11-0 is enabled for output. When $\overline{\text{AOE}}$ is HIGH, AOUT11-0 is placed in a high-impedance state. In 10-bit modes, AOUT1-0 are unconditionally tristated. In 8-bit modes, AOUT3-0 are tristated. The flag outputs are not affected by $\overline{\text{AOE}}$.

$\overline{\text{BOE}}$ - Output Enable B
In any dual-channel mode, when $\overline{\text{BOE}}$ is LOW, BOUT11-0 is enabled for output. When $\overline{\text{BOE}}$ is HIGH, or in any single-channel mode, BOUT11-0 is placed in a high-impedance state. In 10-bit modes, BOUT1-0 are tristated. In 8-bit modes, BOUT3-0 are tristated. The flag outputs are not affected by $\overline{\text{BOE}}$.

$\overline{\text{CE}}$ - Chip Enable
When LOW, CE enables writing to the LF3312 with the parallel micrprocessor interface.

$\overline{\text{PWE}}$ - Parallel Microprocessor Interface Write Enable
When LOW, WE enables writing to the LF3312's Instruction Registers with the parallel micrprocessor interface.

$\overline{\text{PRE}}$ - Parallel Microprocessor Interface Read Enable
When LOW, RE enables reading from the LF3312's Instruction Registers with the parallel micrprocessor interface.

Detailed Signal Definition

Outputs

AOUT11-0 - Data Output A
AOUT11-0 is the 12-bit registered data output port. AOUT[11] is always the MSB. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when $\overline{\text{AREN}}$ is LOW.

BOUT11-0 - Data Output B
In OPMODES 4-7, BOUT11-0 is the 12-bit registered data output port. BOUT[11] is always the MSB. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when $\overline{\text{BREN}}$ is LOW. In OPMODES 0-3 refer to the input description of BOUT11-0.

APF - Programmable Almost Full Flag A
APF goes low when the write pointer is (Full - N) locations ahead of the read pointer. N is the value stored in the APF register and has no default value. APF is synchronized to the rising edge of AWCLK.

BPF - Programmable Almost Full Flag B
BPF goes low when the write pointer is (Full - N) locations ahead of the read pointer. N is the value stored in the BPF register and has no default value. BPF is synchronized to the rising edge of BWCLK.

APE - Programmable Almost Empty Flag A
APE goes HIGH when the write pointer is (N + 1) locations ahead of the read pointer. N is the value stored in the APE register and has no default value. APE is synchronized to the rising edge of RCLK.

BPE - Programmable Almost Empty Flag B
BPE goes HIGH when the write pointer is (N + 1) locations ahead of the read pointer. N is the value stored in the BPE register and has no default value. BPE is synchronized to the rising edge of RCLK.

ACOLLIDE - Memory Read/Write Pointer Collision Flag A
This flag goes high whenever the read and write addresses to the memory core (single-channel modes) or its “A” channel (dual-channel modes) coincide. By monitoring the partial full/empty flags, the user can ascertain the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full).

BCOLLIDE - Memory Read/Write Pointer Collision Flag B
In dual-channel modes, this flag goes high whenever the read and write addresses to the Channel B memory core coincide. By monitoring the partial full/empty flags, the user can ascertain the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full).

Instruction Register Map

The various 8-bit control registers may be pre-programmed with either the parallel microprocessor port (SERIAL=0), or through the serial microprocessor interface bus(SERIAL=1). Changes in pre-programming begin to affect the data path when LOAD is brought LOW. In each instance, the value in parens () is the default state following assertion of RESET while LOAD = 0.

Instruction Register 0 (dflt = 00000000)

3:0 = ROW_LENGTH[11:8]	(0000: 24-bit linear map; see reg 7)

Instruction Register 1 (dflt = 00000000)

7:0 = ROW_LENGTH[7:0]	(00000000: 24-bit linear map; see reg 6)

Instruction Register 2 (dflt = 00000000)

7:0 = ALATENCY[23:16]	(00000000: default = 0; see reg 9, a)

Instruction Register 3 (dflt = 00000000)

7:0 = ALATENCY[15:8]	(00000000: default = 0; see reg 8, a)

Instruction Register 4 (dflt = 00000000)

7:0 = ALATENCY[7:0]	(00000000: default = 0; see reg 8, 9)

Instruction Register 5 (dflt = 00000000)

7:0 = BLATENCY[23:16]	(00000000)

Instruction Register 6 (dflt = 00000000)

7:0 = BLATENCY[15:8]	(00000000)

Instruction Register 7 (dflt = 00000000)

7:0 = BLATENCY[7:0]	(00000000)

Instruction Register Map

Instruction Register 8 (dflt = 10_00_0_111)

7:6 = WIDTH[1:0]	(10: 10 bits)
5:4 = Reserved	(Make equal to 00)
3 = MARK_ACTIVE_RESET	(Make equal to 0)
2:0 = OPMODE	(111: Two-Channel Asynchronous FIFO)

Instruction Register 9 (dflt = 00_000_000)

7:6 = TRS_SYNC[1:0]	(00: ignore embedded TRS)
5 = B_FLD	(0: frame sync from TRS)
4 = A_FLD	(0: frame sync from TRS)
3 = MARK_SEL	(0: use marked address)
2:0 = FLAG_SET	(000: trigger empty, full on 1/80, 79/80)

Instruction Register a (dflt = 00000000)

7 = BSET_catch	(0: ignore BSET & TRS to force read pointer)
6 = ASET_catch	(0: ignore ASET & TRS to force read pointer)
5 = RSET_b_sel	(0: falling edge one shot RSET_b)
4 = RCLR_b_sel	(0: falling edge one shot RCLR_b)
3 = BSET_b_sel	(0: falling edge one shot BSET_b)
2 = BCLR_b_sel	(0: falling edge one shot BCLR_b)
1 = ASET_b_sel	(0: falling edge one shot ASET_b)

Instruction Register b (dflt = 00_00_00_00)

7:4 = BFLAG_CTL	(00: BPE, BPF are part-empty, -full)
3:0 = AFLAG_CTL	(00: APE, APF are part-empty, -full)

Instruction Register Map

Instruction Register c (dflt = 0000_0000)

7:4 = BASE_ADDR	(0000: lowest-address chip in a sequence)
3:0 = CASCADE	(0000: sequence comprises a single chip)

Instruction Register e (dflt = 00000000)

Instruction Register f (dflt = 00000000)

Instruction Register 10 (0)

Instruction Register Signals Defined

Register 0[3:0], Register 1[7:0] = ROW_LENGTH[11:0] - for Cartesian-to-linear address map in 1-chnl modes

This control governs the remapping of Cartesian coordinates arriving on BIN (horizontal component) and BOUT (vertical component) into a linear address, for use by the chip's internal address generator. Setting ROW_LENGTH to 0 causes the incoming address to be interpreted directly as a linear address (or equivalently, a Cartesian address with 4095 pixels per line), with the 12 bits of BOUT concatenated with the 12 bits of BIN.

Register 2[7:0], Register 3[7:0], Register 4[7:0] = ALATENCY[23:0] - Total wait latency, channel A

In single-channel synchronous shift register mode (OPMODE = 0), ALATENCY determines the effective shift register depth, i.e., such that the chip's input-to-out latency = TBD + (ALATENCY clock cycles). In dual-channel modes with synchronous A channel (OPMODE = 4, 5), these bits set the A channel delay only. For OPMODE = 0, 4, or 5, a falling edge on pin AMARK_b registers the current value of the write pointer and starts a countdown timer, which forces the read pointer to this registered value ALATENCY clock cycles later. The maximum delay that ALAT can be made equal to is 2^{24}-2 clock cycles.

In addition to this function, in all OPMODES, bringing ASET_b low forces the A (OPMODE 4-7) or single overall (OPMODE 0-3) memory write pointer to equal ALATENCY. Thus, when ALATENCY is used to establish a time delay, it is interpreted as an ordinary unsigned binary number. In contrast, when it is used to override an address pointer, ALATENCY[11:0] is equal to the 12-bit X-coordinate in a Cartesian plane, and ALATENCY[23:12] is considered the Y-coordinate. When ROW_LENGTH is 0, ALATENCY[23:0] is considered to be a linear address in the memory space. By changing the ROW_LENGTH, the X-coordinate can be from 0 to (ROW_LENGTH-1) to make up the Cartesian plane. For example, if ROW_LENGTH = 16, the X-coordinate or ALATENCY[11:0] can be from 0 to 15 in the Cartesian space.

Instruction Register Signals Defined

Register 5[7:0], Register 6[7:0], Register 7[7:0] = BLATENCY[23:0] - shift register depth for channel B

Valid only in two channel OPMODES 4 and 6. In these modes, BLATENCY impacts channel B exactly as ALATENCY did channel A in modes 4 and 5. Total Channel B data latency = TBD + (BLATENCY clock cycles).

Register 8[7:6] = WIDTH[1:0] - data word size at input/output ports

0x	8 bits	[11:4]	xOUT[3:0] tristated
10	10 bits	[11:2] (dflt)	xOUT[1:0] tristated
11	12 bits	[11:0]	

Register 8[5:4] = Reserved

Register 8[3] = MARK_ACTIVE_RSET

0	ignores the internal RSET that occurs following the MARK
1	obeys the internal RSET according to the MARK

Register 8[2:0] = OPMODE[2:0] - operating mode

000	1 chnl	synchronous shift register
001	1 chnl	random access read
010	1 chnl	random access write
011	1 chnl	asynchronous (slave) FIFO
100	2 chnl	synchronous shift register
101	2 chnl	FIFO, B slaved to A
110	2 chnl	FIFO, A slaved to B
111	2 chnl	asynchronous (slave) FIFO (dflt)

Instruction Register Signals Defined

Register 9[7:6] = TRS_SYNC[1:0] - response to embedded TRS EAV (a)

00	disable TRS sync detection (dflt)
01	F-bit of embedded TRS EAV marks current write pointer.
10	F-bit of embedded TRS EAV sets current write pointer to value set by BOUT/BIN (1-chnl.modes) or ALAT & BLAT (2-chnl. modes, respectively).
11	F-bit of embedded TRS EAV clears current write pointer. - If B_FLD = 0 (frame-based sync), action is on each B-channel EAV with F = 0 for which the preceding EAV had F = 1. - If B_FLD = 1 (field-based sync), action is on each B-chan EAV whose F differs from that of the preceding EAV. A_FLD affects the tA-channel operation in the same fashion.

Register 9[5] = B_FLD frame/field sync select, chnl B

0	use only falling F-bit in EAV; ignore rising (dflt)
1	use both rising and falling F-bit in EAV

Register 9[4] = A_FLD frame/field sync select, chnl A same logic as B_FLD

Register 9[3] MARK_SEL - This signal is used in combination with pin BCLR_b to determine to effect of bringing RSET_b low on the read pointer(s). When RSET_b goes to 0:

0	force read pointer(s) to marked address(es) (dflt)
1	force read pointer(s) as shown in following table:

OPMODE	*BCLR_b*	*Read Pointer Equals:*
0-3	1	remap address
0-3	0	BLAT
4-7	x	A=ALAT, B=BLAT

Instruction Register Signals Defined

Register 9[2:0] = FLAG_SET[2:0] - sets fractional "fullness" and "emptiness" thresholds in memory core.

Full flag goes HIGH when and only when the memory is at least "TH" full. Empty flag goes HIGH when and only when the memory is less than "TL" full.

000	TH = 79/80	TL = 1/80 (dflt)
001	TH = 78/80	TL = 2/80
010	TH = 77/80	TL = 3/80
011	TH = 76/80	TL = 4/80
100	TH = 75/80	TL = 5/80
101	TH = 74/80	TL = 6/80
110	TH = 73/80	TL = 7/80
111	TH = 72/80	TL = 8/80

Register a[7] = BSET_catch - (OPMODES 4-7 only)

0:	setting write pointer B does not mark its new value (dflt)
1:	setting write pointer B automatically marks its new value

Register a[6] = ASET_catch - (all OPMODES) logic same as above for BSET_catch

Register a[5:0] Control action.

Rb[5]	RSET_b_sel
Rb[4]	RCLR_b_sel
Rb[3]	BSET_b_sel
Rb[2]	BCLR_b_sel
Rb[1]	ASET_b_sel
Rb[0]	ACLR_b_sel
if 0:	Each falling edge on the corresponding control pin overrides a memory address counter for exactly one clock cycle, after which normal memory address incrementing immediately resumes. (dflt)
if 1:	The corresponding pin continuously overrides the memory address counter as long as it is held LOW. Memory address incrementing resumes when the pin is returned HIGH.

Instruction Register Signals Defined

Register b[7:4] = BFLAG_CTL[3:0] for pins BPE and BPF (See below for legend)

BFLAG_CTL	*BPE*	*BPF*	*BCOLLIDE*
0000	B empty	B full	BCOLLIDE
0001	RB=MB	RA=MA	BCOLLIDE
0010	BIN f	BIN v	BIN h
0011	BOUT f	BOUT v	BOUT h
0100	BIN f	BIN v	BCOLLIDE
0101	BOUT f	BOUT v	BCOLLIDE
0110	BIN f	BIN h	BCOLLIDE
0111	BOUT f	BOUT h	BCOLLIDE
1000	BIN v	BIN h	BCOLLIDE
1001	BOUT v	BOUT h	BCOLLIDE

AIN f, v, h are the TRS bits embedded in the incoming A channel TRS signals.
AOUT f, v, h are the TRS bits embedded in the emerging A channel TRS signals.
BIN f, v, h and *BOUT f, v, h* are the analogous B channel values.
RA(RB) is the read address pointer value for channel A(B).
MA(MB) is the memory address pointer value for channel A(B).

Rb[3:0] AFLAG_CTL[3:0] for pins APE and APF

AFLAG_CTL	*APE*	*APF*	*ACOLLIDE*
0000	A empty	A full	ACOLLIDE
0001	RB=MB	RA=MA	ACOLLIDE
0010	AIN f	AIN v	AIN h
0011	AOUT f	AOUT v	AOUT h
0100	AIN f	AIN v	ACOLLIDE
0101	AOUT f	AOUT v	ACOLLIDE
0110	AIN f	AIN h	ACOLLIDE
0111	AOUT f	AOUT h	ACOLLIDE
1000	AIN v	AIN h	ACOLLIDE
1001	AOUT v	AOUT h	ACOLLIDE

Register d[7:4] = BASE_ADDR[3:0] - position of chip in cascade series; 0000 = lowest; BASE_ADDR[3:0] must not exceed CASCADE[3:0]

Instruction Register Signals Defined

Register c[3:0] = CASCADE[3:0] - number of chips in a system with concatenated address spaces.

0000:	single chip operation; (dflt) sequential R, W memcore addresses, modulo 103,680
0001:	two chip cascade; sequential R, W addresses, modulo 207,360 ...
1111:	sixteen chip cascade; (a) sequential R, W addresses, modulo 1,658,880 (a) Note limits regarding the number of possible chips, related to WIDTH control: 0- 9 LF3312s: always accepted (WIDTH = xx) 10-12 LF3312s: only using 10 or 12 bit data (WIDTH = 1x) 13-15 LF3312s: only using 12 bit data (WIDTH = 11)

TSADR[4:0] test site address (active only if MPU pointer = 10000)

00	input FIFO read and write pointers [7:6] B write; [5:4] B read [3:2] A write; [1:0] A read
01	output FIFO read and write pointers same pattern as for input

Instruction Register Signals Defined

FIFOs - Addresses for testing purposes

02	input FIFO parse addresses [7:4] chan B; [3:0] chan A
03	output FIFO parse address [7:4] chan B; [3:0] chan A
04	FIFO read/write controls [7] in B write enable [6] in B read enable [5] in A write enable [4] in A read enable [3] out B write enable [2] out B read enable [1] out A write enable [0] out A read enable
05	front fifo full/empty flags [7] front FIFO B full [6] front FIFO B empty [5] front FIFO A full [4] front FIFO A empty
06	Memory A refresh addr[9:2]
07	{Memory A refresh addr[1:0], bank_adr[3:0], Memory A read/write control}
08	Memory B refresh addr[9:2]
09	{BMemory refresh addr[1:0], bank_adr[3:0], Memory B read/write control}
0a	Memory A read addr[9:2]
ob	Memory A read addr[1:0], Bank_adr[3:0]
oc	Memory B read addr[9:2]
od	Memory B read addr[1:0], Bank_adr[3:0]
oe	Memory A write addr[9:2] to FIFO
of	Memory A write addr[1:0], Bank_adr[3:0]
10	Memory B write addr[9:2] to FIFO
11	Memory B write addr[1:0], Bank_adr[3:0]

Instruction Register Signals Defined

TSBUS[7:0] Test site bus, if this address is set, the mpu interface reads out the contents of the data bus selected by TSADR

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC_{INT} , Internal supply voltage with respect to ground	–0.5V to + 2.0V
VCC_O, Output drivers supply voltage with respect to ground	–0.5V to + 4.0V
Signal applied to high impedance output	–0.5V to + 3.3V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Characteristic	Mode	Temperature Range	Supply Voltage
VCC_{INT}	Commerical	0°C to +70°C	1.7V ≤ Vcc ≤ 1.9V
VCC_O	Commerical	0°C to +70°C	3.00V ≤ Vcc ≤ 3.60V

Electrical Characteristics *Over Operating Conditions (Note 4)*

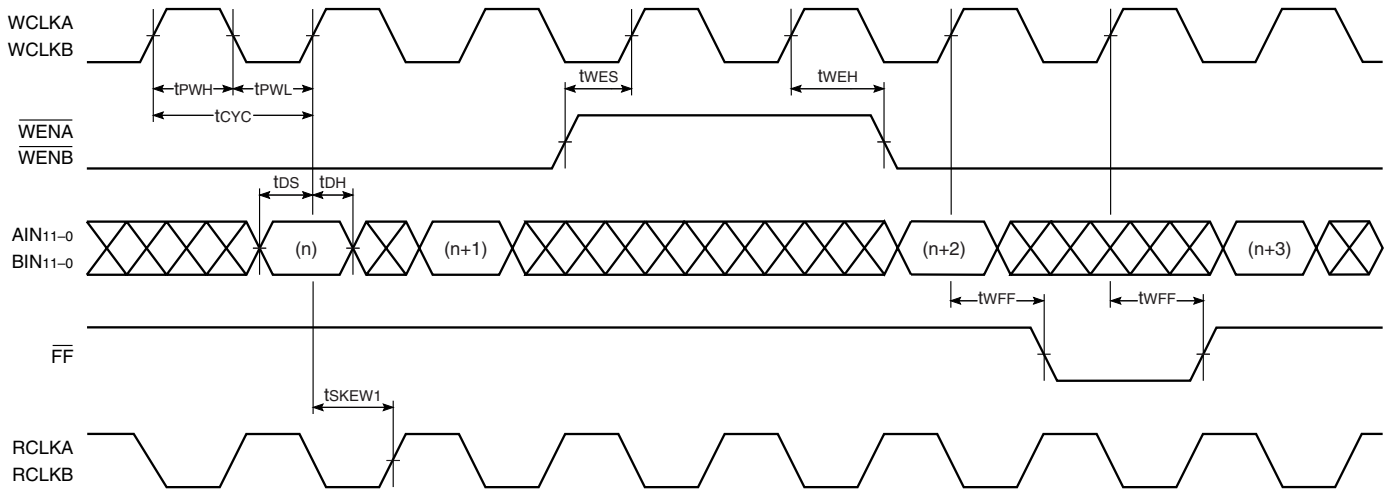
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4 mA				V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage				5.5	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{Ix}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Note 5,6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			7	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			7	pF

Switching Characteristics

Commercial Operating Range (0°C to +70°C) Notes 9, 10 (ns)

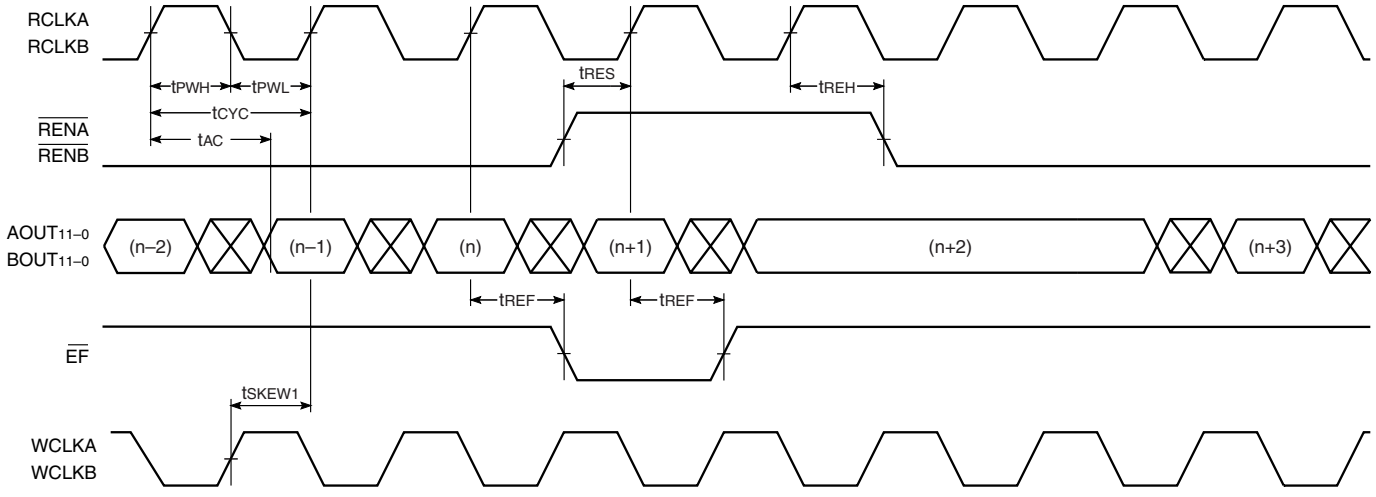
		LF3312QC10			
		10			
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	10			
t_{PWH}	Clock Pulse Width High	3			
t_{PWL}	Clock Pulse Width Low	3			
t_{DS}	Setup Time, All Inputs	4			
t_{DH}	Hold Time, All Inputs	0			
t_{WES}	Write Enable Setup Time	4			
t_{WEH}	Write Enable Hold Time	0			
t_{RES}	Read Enable Setup Time	4			
t_{REH}	Read Enable Hold Time	0			
t_{LDS}	Load Setup Time	4			
t_{LDH}	Load Hold Time	0			
t_{RS}	Read/Write Reset Setup Time	4			
t_{RH}	Read/Write Reset Hold Time	0			
t_{AC}	Access Time		6		
t_{WFF}	Write Clock to Full Flag		6		
t_{REF}	Read Clock to Empty Flag		6		
t_{PAF}	Write Clock to Programmable Almost-Full Flag		6		
t_{PAE}	Read Clock to Programmable Almost-Empty Flag		6		
t_{OHZ}	Output Enable to Output in Low Impedance		6		
t_{OLZ}	Output Enable to Output in High Impedance		6		
t_{SKEW1}	Skew Time Between Read and Write Clocks for $\overline{EF}$ and $\overline{FF}$		4		
t_{SKEW2}	Skew Time Between Read and Write Clocks for $\overline{PAEx}$ and $\overline{PAFx}$		4		

Write Cycle Timing



RWA = RWB = HIGH

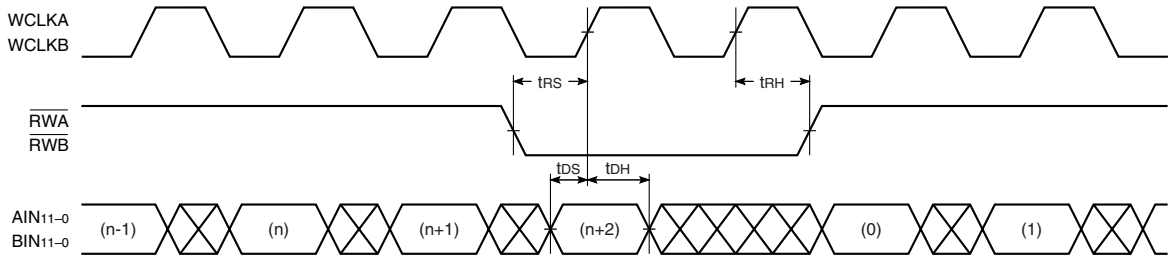
Read Cycle Timing



RRA = RRB = HIGH

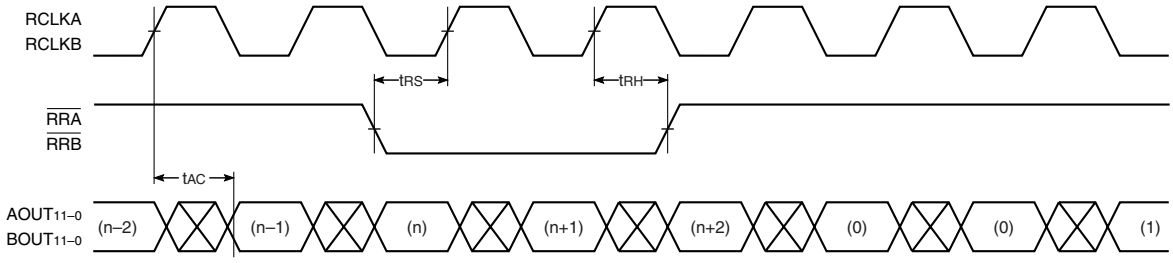
OEA = OEB = LOW

Write Reset Timing



$\overline{WENA}$ = $\overline{WENB}$ = LOW

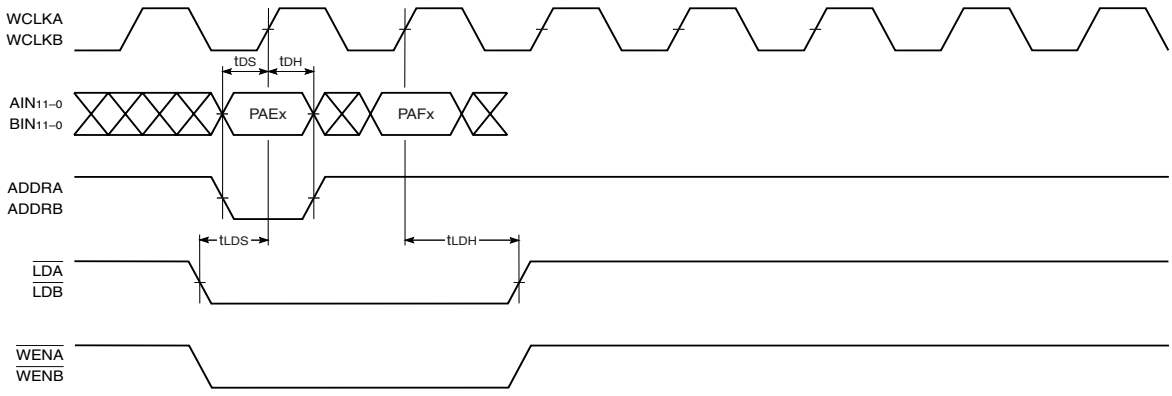
Read Reset Timing



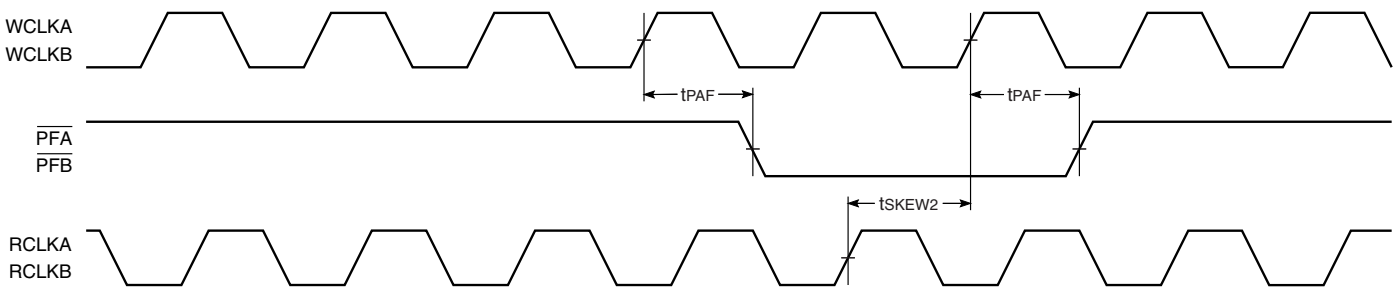
$\overline{RENA}$ = $\overline{RENB}$ = LOW

$\overline{OEA}$ = $\overline{OEB}$ = LOW

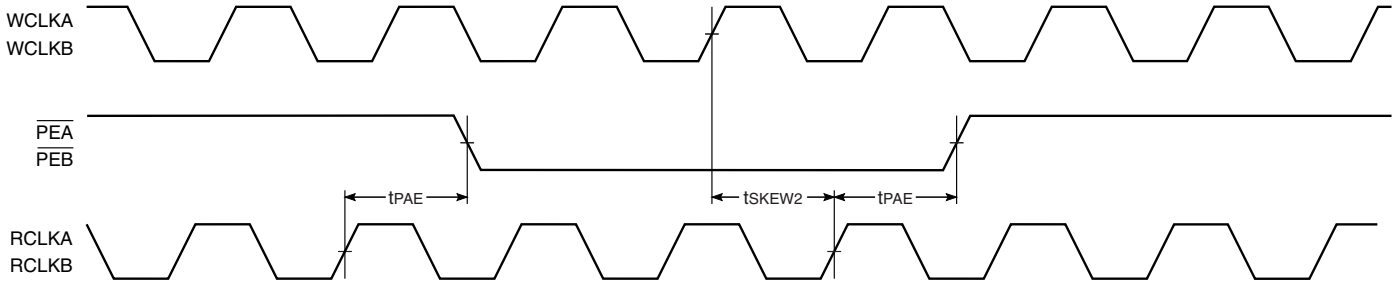
Programmable Flag Load Timing



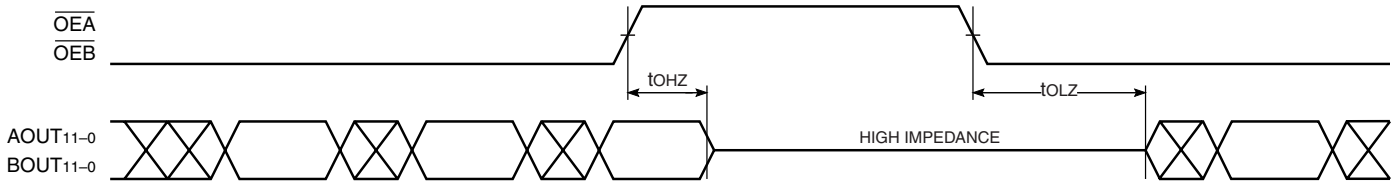
Programmable Almost Full Flag



Programmable Almost Empty Flag



Output Enable and Disable



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. The device can withstand operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels may be in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be approximated by:

$$\text{where} \quad \frac{NCV^2F}{2}$$

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with outputs changing every cycle and no load, at a 50 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, and no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{dis} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current change pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the device as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the device leads.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and **V**CC noise to maintain required input levels relative to the device ground pin.

Notes

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ena} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{dis} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{th}, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

Figure A. Output Loading Circuit

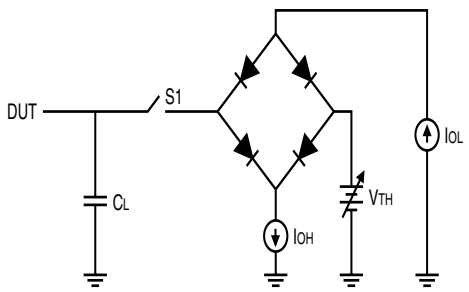
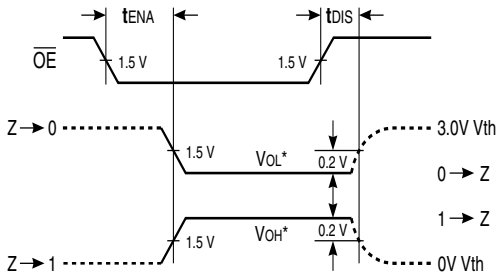


Figure B. Threshold Levels



VOL* Measured VOL with IOH = –10mA and IOL = 10mA
VOH* Measured VOH with IOH = –10mA and IOL = 10mA

Package and Ordering Information

169 Ball - Ball Grid Array (BGA)

0°C to 70°C--Commercial Screening	
Speed	LF3312QC10
10 ns	