LTC3723-1/LTC3723-2

Synchronous Push-Pull PWM Controllers

October 2003

FEATURES

- **High Efficiency Synchronous Push-Pull PWM**
- **1.5A Sink, 1A Source Output Drivers**
- **Adjustable Push-Pull Dead-Time and Synchronous Timing**
- **Adjustable System Undervoltage Lockout and Hysteresis**
- Adjustable Leading Edge Blanking
- Low Start-Up and Quiescent Currents
- Current Mode (LTC3723-1) and Voltage Mode (LTC3723-2) Operation
- Single Resistor Slope Compensation
- V_{CC} UVLO and 25mA Shunt Regulator
- Programmable Fixed Frequency Operation to 1MHz
- 50mA Synchronous Output Drivers
- Soft-Start, Cycle-by-Cycle Current Limiting and Hiccup Mode Short-Circuit Protection
- 5V, 15mA Low Dropout Regulator
- Available in 16-Pin SSOP Package

APPLICATIONS

- Telecommunications, Infrastructure Power Systems
- Distributed Power Architectures

DESCRIPTION

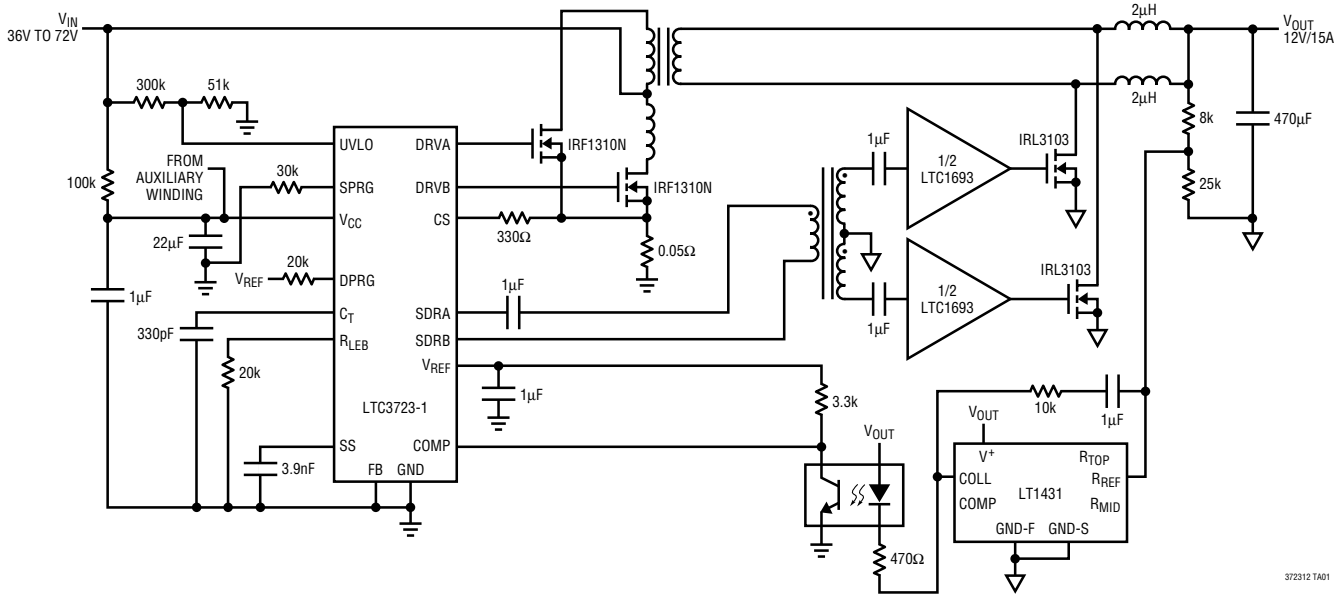
The LTC®3723-1/LTC3723-2 synchronous push-pull PWM controllers provide all of the control and protection functions necessary for compact and highly efficient, isolated power converters. High integration minimizes external component count, while preserving design flexibility.

The robust push-pull output stages switch at half the oscillator frequency. Dead-time is independently programmed with an external resistor. Synchronous rectifier timing is adjustable to optimize efficiency. A UVLO program input provides precise system turn-on and turn off voltages. The LTC3723-1 features peak current mode control with programmable slope compensation and leading edge blanking, while the LTC3723-2 employs voltage mode control with voltage feedforward capability.

The LTC3723-1/LTC3723-2 feature extremely low operating and start-up currents. Both devices provide reliable short-circuit and overtemperature protection. The LTC3723-1/LTC3723-2 are offered in a 16-pin SSOP package.

TYPICAL APPLICATION

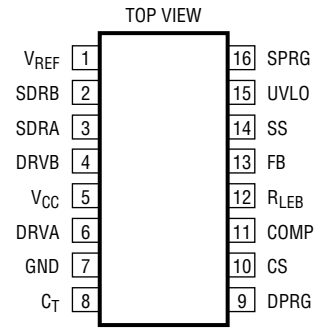
Isolated 36V to 72V DC to 12V/15A Push-Pull Converter



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to GND (Low Impedance Source) .....–0.3V to 10V
(Chip Self-Regulates at 10.3V)
UVLO to GND ..... –0.3V to V_{CC}
All Other Pins to GND
(Low Impedance Source) .....–0.3V to 5.5V
V_{CC} (Current Fed) 40mA
V_{REF} Output Current ..... Self-Regulated
Operating Temperature (Notes 5,6)
LTC3723E ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10sec)..... 300°C

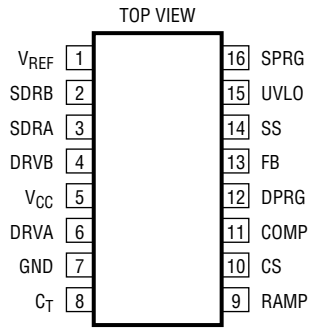
PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC3723EGN-1
GN PART MARKING
37231



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC3723EGN-2
GN PART MARKING
37232

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 9.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{CCUV}	V_{CC} Undervoltage Lockout	Measured on V_{CC}			10.25	10.7	V
V_{CCHY}	V_{CC} UVLO Hysteresis	Measured on V_{CC}		3.8	4.2		V
I_{CCST}	Start-Up Current	V_{CC} = V_{UVLO} – 0.3V	●		145	230	µA
I_{CCRN}	Operating Current	No Load on Outputs			3	6	mA
V_{SHUNT}	Shunt Regulator Voltage	Current into V_{CC} = 10mA			10.3	10.8	V
R_{SHUNT}	Shunt Resistance	Current into V_{CC} = 10mA to 17mA			1.4	3.5	Ω
SUVLO	System UVLO Threshold	Measured on UVLO Pin, 10mA into V_{CC}		4.8	5.0	5.2	V
SHYST	System UVLO Hysteresis Current	Current Flows Out of UVLO Pin, 10mA into V_{CC}		8.5	10	11.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 9.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Pulse Width Modulator							
ROS	Ramp Offset Voltage	Measured on COMP, RAMP = 0V			0.65		V
I_{RMP}	Ramp Discharge Current	RAMP = 1V, COMP = 0V, C_T = 4V, 3723-1 Only			50		mA
I_{SLP}	Slope Compensation Current	Measured on CS, C_T = 1V, 3723-1 Only C_T = 2.25V			30 68		µA µA
DCMAX	Maximum Duty Cycle	COMP = 4.5V	●	47	48.2	50	%
DCMIN	Minimum Duty Cycle	COMP = 0V	●		0		%
DTADJ	Dead-Time				130		ns
Oscillator							
OSCI	Initial Accuracy	T_A = 25°C, C_T = 270pF		220	250	280	kHz
OSCT	V_{CC} Variation	V_{CC} = 6.5V to 9.5V, Overtemperature	●	–3		3	%
OSCV	C_T Ramp Amplitude	Measured on C_T			2.35		V
Error Amplifier							
V_{FB}	FB Input Voltage	COMP = 2.5V, (Note 3)		1.172	1.2	1.22	V
FB_I	FB Input Range	Measured on FB, (Note 4)		–0.3		2.5	V
AVOL	Open-Loop Gain	COMP = 1V to 3V, (Note 3)		70	90		dB
I_{IB}	Input Bias Current	COMP = 2.5V, (Note 3)			5	50	nA
V_{OH}	Output High	Load on COMP = –100µA		4.7	4.92		V
V_{OL}	Output Low	Load on COMP = 100µA			0.27	0.5	V
I_{SOURCE}	Output Source Current	COMP = 2.5V		400	700		µA
I_{SINK}	Output Sink Current	COMP = 2.5V		2	5		mA
Reference							
V_{REF}	Initial Accuracy	T_A = 25°C, Measured on V_{REF}		4.925	5.00	5.075	V
REFLD	Load Regulation	Load on V_{REF} = 100µA to 5mA			2	15	mV
REFLN	Line Regulation	V_{CC} = 6.5V to 9.5V			1	10	mV
REFTV	Total Variation	Line, Load and Temperature	●	4.900	5.000	5.100	V
REFSC	Short-Circuit Current	V_{REF} Shorted to GND		18	30	45	mA
Push-Pull Outputs							
DRVH(x)	Output High Voltage	$I_{OUT(x)}$ = –100mA		9	9.2		V
DRVL(x)	Output Low Voltage	$I_{OUT(x)}$ = 100mA			0.17	0.25	V
RDH(x)	Pull-Up Resistance	$I_{OUT(x)}$ = –10mA to –100mA			2.9	4	Ω
RDL(x)	Pull-Down Resistance	$I_{OUT(x)}$ = –10mA to –100mA			1.7	2.5	Ω
TDR(x)	Rise-Time	$C_{OUT(x)}$ = 1nF			10		ns
TDF(x)	Fall-Time	$C_{OUT(x)}$ = 1nF			10		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 9.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Outputs						
OUTH(x)	Output High Voltage	$I_{OUT(x)}$ = –30mA	9.0	9.2		V
OUTL(x)	Output Low Voltage	$I_{OUT(x)}$ = 30mA		0.44	0.6	V
RHI(x)	Pull-Up Resistance	$I_{OUT(x)}$ = –10mA to -30mA		11	15	Ω
RLO(x)	Pull-Down Resistance	$I_{OUT(x)}$ = –10mA to -30mA		15	20	Ω
TR(x)	Rise-Time	$C_{OUT(x)}$ = 50pF		10		ns
TF(x)	Fall-Time	$C_{OUT(x)}$ = 50pF		10		ns
Current Limit and Shutdown						
CLPP	Pulse by Pulse Current Limit Threshold	Measured on CS	280	300	320	mV
CLSD	Shutdown Current Limit Threshold	Measured on CS	475	600	725	mV
CLDEL	Current Limit Delay to Output	100mV Overdrive on CS, (Note 2)		80		ns
SSI	Soft-Start Current	SS = 2.5V	10	13	16	µA
SSR	Soft-Start Reset Threshold	Measured on SS	0.7	0.4	0.1	V
FLT	Fault Reset Threshold	Measured on SS	4.5	4.2	3.5	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Includes leading edge blanking delay, R_{LEB} = 20k, not tested in production.

Note 3: FB is driven by a servo loop amplifier to control V_{COMP} for these tests.

Note 4: Set FB to –0.3V, 2.5V and insure that COMP does not phase invert.

Note 5: The LTC3723E–1/LTC3723E-2 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

PIN DESCRIPTIONS (LTC3723-1/LTC3723-2)

V_{REF} (Pin 1/Pin 1): Output of the 5.0V Reference. V_{REF} is capable of supplying up to 18mA to external circuitry. V_{REF} should be decoupled to GND with a 1µF ceramic capacitor.

SDRB (Pin 2/Pin 2): 50mA Driver for Synchronous Rectifier associated with DRVB.

SDRA (Pin 3/Pin 3): 50mA Driver for Synchronous Rectifier associated with DRVA.

DRVB (Pin 4/Pin 4): High Speed 1.5A Sink, 1A Source Totem Pole MOSFET Driver. Connect to gate of external push-pull MOSFET with as short a PCB trace as practical to preserve drive signal integrity. A low value resistor connected between DRVA and the MOSFET gate is optional and will improve the gate drive signal quality if the PCB trace from the driver to the MOSFET cannot be made short.

V_{CC} (Pin 5/Pin 5): Supply Voltage Input to the LTC3723-1/LTC3723-2 and 10.25V Shunt Regulator. The chip is enabled after V_{CC} has risen high enough to allow the V_{CC} shunt regulator to conduct current and the UVLO comparator threshold is exceeded. Once the V_{CC} shunt regulator has turned on, V_{CC} can drop to as low as 6V (typical) and maintain operation. Bypass V_{CC} to GND with a high quality 1µF or larger ceramic capacitor to supply the transient currents caused by the high speed switching and capacitive loads presented by the on chip totem pole drivers.

PIN DESCRIPTIONS (LTC3723-1/LTC3723-2)

DRVA (Pin 6/Pin 6): High Speed 1.5A Sink, 1A Source Totem Pole MOSFET Driver. Connect to gate of external push-pull MOSFET with as short a PCB trace as practical to preserve drive signal integrity. A low value resistor connected between DRVA and the MOSFET gate is optional and will improve the gate drive signal quality if the PCB trace from the driver to the MOSFET cannot be made short.

GND (Pin 7/Pin 7): All circuits in the LTC3723 are referenced to GND. Use of a ground plane is highly recommended. V_{IN} and V_{REF} bypass capacitors must be terminated with a star configuration as close to GND as practical for best performance.

C_T (Pin 8/Pin 8): Timing Capacitor for the Oscillator. Use a ±5% or better low ESR ceramic capacitor for best results. C_T ramp amplitude is 2.35V peak-to-peak (typical).

DPRG (Pin 9/Pin 12): Programming Input for Push-Pull Dead-Time. Connect a resistor between DPRG and V_{REF} to program the dead-time. The dead-time is approximately equal to ($1.30 \cdot 10^{-12} \cdot$ RDPRG). The nominal voltage on DPRG is 2V.

RAMP (N/A/Pin 9): Input to PWM Comparator for LTC3723-2 Only (Voltage Mode Controller). The voltage on RAMP is internally level shifted by 650mV.

CS (Pin 10/Pin 10): Input to Pulse-by-Pulse and Overload Current Limit Comparators, Output of Slope Compensation Circuitry. The pulse-by-pulse comparator has a nominal 300mV threshold, while the overload comparator has a nominal 600mV threshold. An internal switch discharges CS to GND after every timing period. Slope compensation current flows out of CS during the PWM period. An external resistor connected from CS to the external current sense resistor programs the amount of slope compensation.

COMP (Pin 11/Pin 11): Error Amplifier Output, Inverting Input to Phase Modulator.

R_{LEB} (Pin 12/N/A): Timing Resistor for Leading Edge Blanking. Use a 10k to 100k resistor connected between R_{LEB} and GND to program from 40ns to 310ns of leading edge blanking of the current sense signal on CS for the LTC3723-1. A ±1% tolerance resistor is recommended. The LTC3723-2 has a fixed blanking time of approximately 80ns. The nominal voltage on R_{LEB} is 2V. If leading edge blanking is not required, tie R_{LEB} to V_{REF} to disable.

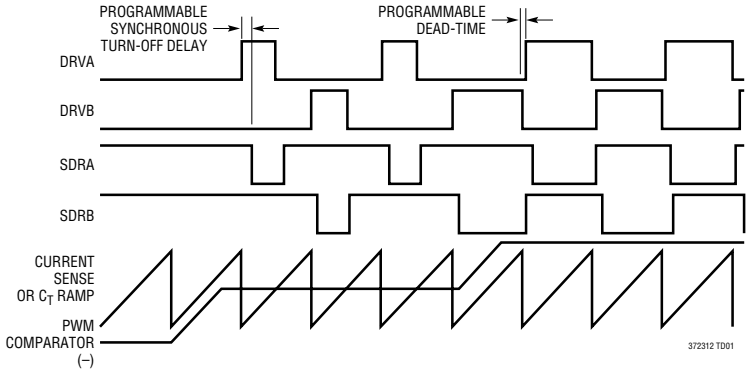
FB (Pin 13/Pin 13): Error Amplifier Inverting Input. This is the voltage feedback input for the LTC3723. The nominal regulation voltage at FB is 1.2V.

SS (Pin 14/Pin 14): Soft-Start/Restart Delay Circuitry Timing Capacitor. A capacitor from SS to GND provides a controlled ramp of the current command (LTC3723-1) or duty cycle (LTC3723-2). During overload conditions, SS is discharged to ground initiating a soft-start cycle. SS charging current is approximately 13μA. SS will charge up to approximately 5V in normal operation. During a constant overload current fault, SS will oscillate at a low frequency between approximately 0.5V and 4V.

UVLO (Pin 15/Pin 15): Input to Program System Turn-On and Turn-Off Voltages. The nominal threshold of the UVLO comparator is 5.0V. UVLO is connected to the main DC system feed through a resistor divider. When the UVLO threshold is exceeded, the LTC3723-1/LTC3723-2 commences a soft-start cycle and a 10μA (nominal) current is fed out of UVLO to program the desired amount of system hysteresis. The hysteresis level can be adjusted by changing the resistance of the divider. UVLO can also be used to terminate all switching by pulling UVLO down to less than 4V. An open drain or collector switch can perform this function without changing the system turn on or turn off voltages.

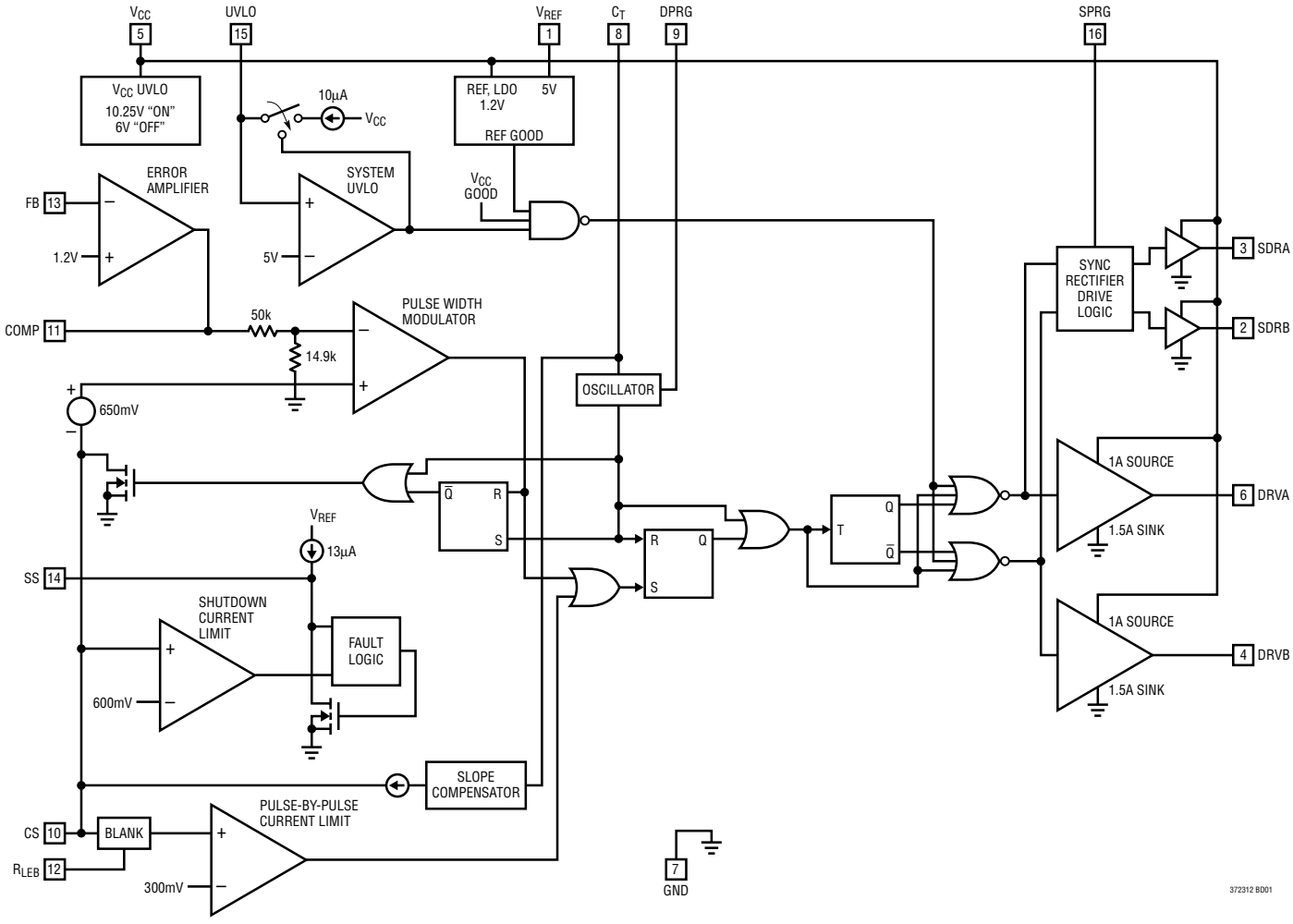
SPRG (Pin 16/Pin 16): A resistor is connected between SPRG and GND to set the turn off delay for the synchronous rectifier driver outputs. The nominal voltage on SPRG is 2V.

TIMING DIAGRAM



BLOCK DIAGRAMS

LTC3723-1 Block Diagram



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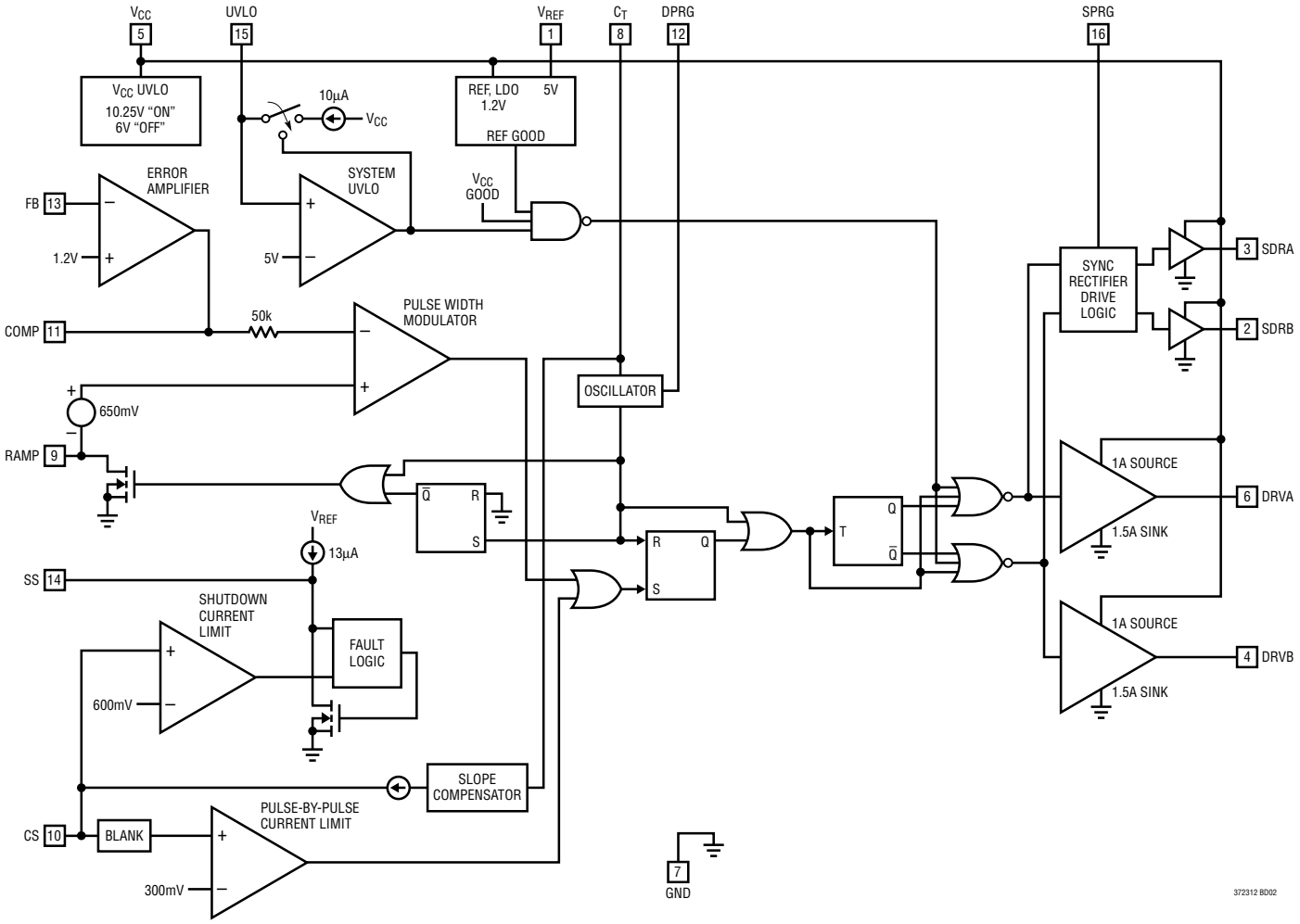
BLOCK DIAGRAMS

LTC3723-2 Block Diagram



OPERATION

Please refer to the detailed Block Diagrams for this discussion. The LTC3723-1 and LTC3723-2 are synchronous PWM push-pull controllers. The LTC3723-1 operates with peak pulse-by-pulse current mode control while the LTC3723-2 offers voltage mode control operation. They are best suited for moderate to high power isolated power systems where small size and high efficiency are required. The push-pull topology delivers excellent transformer utilization and requires only two low side power MOSFET switches. Both controllers generate 180° out of phase 0% to <50% duty cycle drive signals on DRVA and DRVB. The external MOSFETs are driven directly by these powerful on-chip drivers. The external MOSFETs typically control opposite primary windings of a centertapped power transformer. The centertap primary winding is connected to the input DC feed. The secondary of the transformer can be configured in different synchronous or nonsynchronous configurations depending on the application needs.

The duty ratio is controlled by the voltage on COMP. A switching cycle commences with the falling edge of the internal oscillator clock pulse. The LTC3723-1 attenuates the voltage on COMP and compares it to the current sense signal to terminate the switching cycle. The LTC3723-2 compares the voltage on COMP to a timing ramp to terminate the cycle. The LTC3723-2's C_T waveform can be used for this purpose or separate R-C components can be connected to RAMP to generate the timing ramp. If the voltage on CS exceeds 300mV, the present cycle is terminated. If the voltage on CS exceeds 600mV, all switching stops and a soft-start sequence is initiated.

The LTC3723-1 / LTC3723-2 also provide drive signals for secondary side synchronous rectifier MOSFETs. Synchronous rectification improves converter efficiency, especially as the output voltages drop. Independent turn-off control of the synchronous rectifiers is provided via SPRG in order to optimize the benefit of the synchronous rectifiers. A resistor from SPRG to GND sets the desired turn off delay.

A host of other features including an error amplifier, system UVLO programming, adjustable leading edge blanking, slope compensation and programmable dead-time provide flexibility for a variety of applications.

Programming Driver Dead-Time

The LTC3723-1/LTC3723-2 controllers include a feature to program the minimum time between the output signals on DRVA and DRVB commonly referred to as the driver dead-time. This function will come into play if the controller is commanded for maximum duty cycle. The dead-time is set with an external resistor connected between DPRG and V_{REF} (see Figure 1). The nominal regulated voltage on DPRG is 2V. The external resistor programs a current which flows into DPRG. The dead-time can be adjusted from 90ns to 300ns with this resistor. The dead-time can also be modulated based on an external current source that feeds current into DPRG. Care must be taken to limit the current fed into DPRG to 350µA or less.

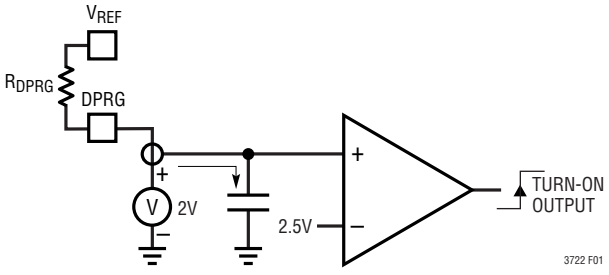


Figure 1. Delay Timeout Circuitry

OPERATION

Powering the LTC3723-1/LTC3723-2

The LTC3723-1/LTC3723-2 utilize an integrated V_{CC} shunt regulator to serve the dual purposes of limiting the voltage applied to V_{CC} as well as signaling that the chip's bias voltage is sufficient to begin switching operation (under voltage lockout). With its typical 10.2V turn-on voltage and 4.2V UVLO hysteresis, the LTC3723-1/LTC3723-2 is tolerant of loosely regulated input sources such as an auxiliary transformer winding. The V_{CC} shunt is capable of sinking up to 40mA of externally applied current. The UVLO turn-on and turn-off thresholds are derived from an internally trimmed reference making them extremely accurate. In addition, the LTC3723-1/LTC3723-2 exhibits very low (145µA typ) start-up current that allows the use of 1/8W to 1/4W trickle charge start-up resistors.

The trickle charge resistor should be selected as follows:

$R_{START(MAX)} = V_{IN(MIN)} – 10.7V/250µA$

Adding a small safety margin and choosing standard values yields:

APPLICATION	V_{IN} RANGE	R_{START}
DC/DC	36V to 72V	100k
Off-Line	85V to 270V_{RMS}	430k
PFC Preregulator	390V_{DC}	1.4M

V_{CC} should be bypassed with a 0.1µF to 1µF multilayer ceramic capacitor to decouple the fast transient currents demanded by the output drivers and a bulk tantalum or electrolytic capacitor to hold up the V_{CC} supply before the bootstrap winding, or an auxiliary regulator circuit takes over.

$C_{HOLDUP} = (I_{CC} + I_{DRIVE}) • t_{DELAY}/3.8V$
(minimum UVLO hysteresis)

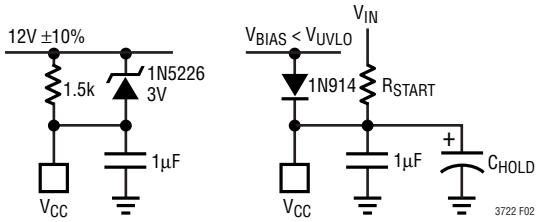


Figure 2. Bias Configurations

Regulated bias supplies as low as 7V can be utilized to provide bias to the LTC3723-1/LTC3723-2. Refer to Figure 2 for various bias supply configurations.

Programming Undervoltage Lockout

The LTC3723-1/LTC3723-2 provides undervoltage lockout (UVLO) control for the input DC voltage feed to the power converter in addition to the V_{CC} UVLO function described in the preceding section. Input DC feed UVLO is provided with the UVLO pin. A comparator on UVLO compares a divided down input DC feed voltage to the 5V precision reference. When the 5V level is exceeded on UVLO, the SS pin is released and output switching commences. At the same time a 10µA current is enabled which flows out of UVLO into the voltage divider connected to UVLO. The amount of DC feed hysteresis provided by this current is: 10µA • R_{TOP}, (Figure 3). The system UVLO threshold is: 5V • {(R_{TOP} + R_{BOTTOM})/R_{BOTTOM}}. If the voltage applied to UVLO is present and greater than 5V prior to the V_{CC} UVLO circuitry activation, then the internal UVLO logic will prevent output switching until the following three conditions are met: (1) V_{CC} UVLO is enabled, (2) V_{REF} is in regulation and (3) UVLO pin is greater than 5V.

UVLO can also be used to enable and disable the power converter. An open drain transistor connected to UVLO as shown in Figure 3 provides this capability.

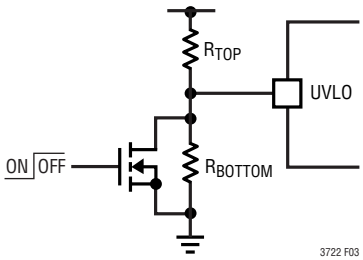


Figure 3. System UVLO Setup

OPERATION

Off-Line Bias Supply Generation

If a regulated bias supply is not available to provide V_{CC} voltage to the LTC3723-1/LTC3723-2 and supporting circuitry, one must be generated. Since the power requirement is small, approximately 1W, and the regulation is not critical, a simple open-loop method is usually the easiest and lowest cost approach. One method that works well is to add a winding to the main power transformer, and post regulate the resultant square wave with an L-C filter (see Figure 4a). The advantage of this approach is that it maintains decent regulation as the supply voltage varies, and it does not require full safety isolation from the input winding of the transformer. Some manufacturers include a primary winding for this purpose in their standard product offerings as well. A different approach is to add a winding to the output inductor and peak detect and filter the square wave signal (see Figure 4b). The polarity of this winding is designed so that the positive voltage square wave is produced while the output inductor is freewheeling. An advantage of this technique over the previous is that it does not require a separate filter inductor and since the voltage is derived from the well-regulated output voltage, it is also well controlled. One disadvantage is that this winding will require the same safety isolation that is required for the main transformer. Another disadvantage is that a much larger V_{CC} filter capacitor is needed, since it does not generate a voltage as the output is first starting up, or during short-circuit conditions.

Programming the LTC3723-1/LTC3723-2 Oscillator

The high accuracy LTC3723-1/LTC3723-2 oscillator circuit provides flexibility to program the switching frequency and slope compensation required for current mode control (LTC3723-1). The oscillator circuit produces a 2.35V peak-to-peak amplitude ramp waveform on C_T. Typical maximum duty cycles of 49% are possible. The oscillator is capable of operation up to 1MHz by the following equation:

$$C_T = 1/(14.8k \bullet F_{OSC})$$

Note that this is the frequency seen on C_T. The output drivers switch at 1/2 of this frequency. Also note that higher switching frequency and added driver dead-time via DPRG will reduce the maximum duty cycle.

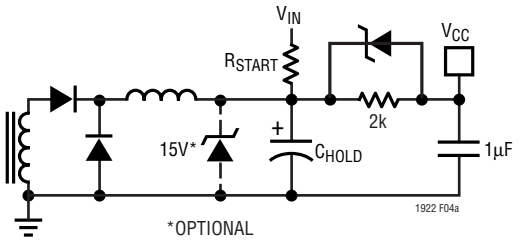


Figure 4a. Auxiliary Winding Bias Supply

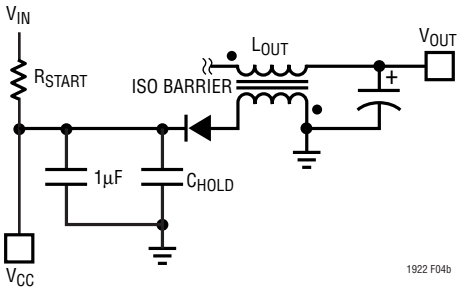


Figure 4b. Output Inductor Bias Supply

OPERATION

The LTC3723-1 derives a compensating slope current from the oscillator ramp waveform and sources this current out of CS. This function is disabled in the LTC3723-2. The desired level of slope compensation is selected with an external resistor connected between CS and the external current sense resistor, (Figure 5).

Current Sensing and Overcurrent Protection

Current sensing provides feedback for the current mode control loop and protection from overload conditions. The LTC3723-1/LTC3723-2 are compatible with either resistive sensing or current transformer methods. Internally connected to the LTC3723-1/LTC3723-2 CS pin are two comparators that provide pulse-by-pulse and overcurrent shutdown functions respectively, (Figure 6).

The pulse-by-pulse comparator has a 300mV nominal threshold. If the 300mV threshold is exceeded, the PWM cycle is terminated. The overcurrent comparator is set approximately 2x higher than the pulse-by-pulse level. If the current signal exceeds this level, the PWM cycle is terminated, the soft-start capacitor is quickly discharged and a soft-start cycle is initiated. If the overcurrent condition persists, the LTC3723-1/LTC3723-2 halts PWM operation and waits for the soft-start capacitor to charge up to approximately 4V before a retry is allowed. The soft-start capacitor is charged by an internal 13μA current source. If the fault condition has not cleared when soft-start reaches 4V, the soft-start pin is again discharged and a new cycle is initiated. This is referred to as hiccup mode operation. In normal operation and under most abnormal conditions, the pulse-by-pulse comparator is fast enough to prevent hiccup mode operation. In severe cases, however, with high input voltage, very low $R_{DS(ON)}$ MOSFETs and a shorted output, or with saturating magnetics, the overcurrent comparator provides a means of protecting the power converter.

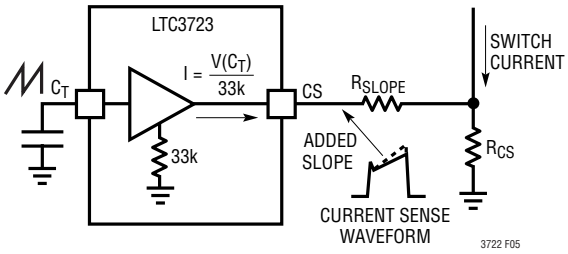


Figure 5. Slope Compensation Circuitry

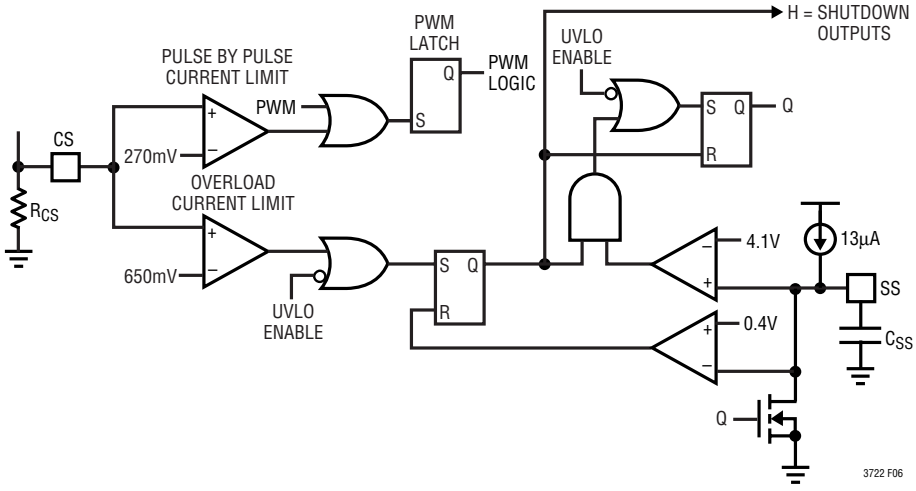


Figure 6. Current Sense/Fault Circuitry Detail

OPERATION

Leading Edge Blanking

The LTC3723-1/LTC3723-2 provides programmable leading edge blanking to prevent nuisance tripping of the current sense circuitry. Leading edge blanking relieves the filtering requirements for the CS pin, greatly improving the response to real overcurrent conditions. It also allows the use of a ground referenced current sense resistor or transformer(s), further simplifying the design. With a single 10k to 100k resistor from R_{LEB} to GND, blanking times of approximately 40ns to 320ns are programmed. If not required, connecting R_{LEB} to V_{REF} can disable leading edge blanking. Keep in mind that the use of leading edge blanking will slightly reduce the linear control range for the pulse width modulator.

High Current Drivers

The LTC3723-1/LTC3723-2 high current, high speed drivers provide direct drive of external power N-channel MOSFET switches. The drivers swing from rail to rail. Due to the high pulsed current nature of these drivers (1.5A sink, 1A source), care must be taken with the board layout to obtain advertised performance. Bypass V_{CC} with a 1µF minimum, low ESR, ESL ceramic capacitor. Connect this capacitor with minimal length PCB leads to both V_{CC} and GND. A ground plane is highly recommended. The driver output pins (DRVA, DRVB) connect to the gates of the external MOSFET switches. The PCB traces making these connections should also be as short as possible to minimize overshoot and undershoot of the drive signal.

Synchronous Rectification

The LTC3723-1/LTC3723-2 produces the precise timing signals necessary to control secondary side synchronous rectifier MOSFETs on SDRA and SDRB. Synchronous rectifiers are used in place of Schottky or silicon diodes on the secondary side to improve converter efficiency. As MOSFET $R_{DS(ON)}$ levels continue to drop, significant efficiency improvements can be realized with synchronous rectification, provided that the MOSFET switch timing is optimized. Synchronous rectification also provides bipolar output current capability, that is, the ability to sink as well as source current.

Programming the Synchronous Rectifier Turn-Off Delay

The LTC3723-1/LTC3723-2 controllers include a feature to program the turn-off edge of the secondary side synchronous rectifier MOSFETs relative to the beginning of a new primary side power delivery pulse. This feature provides optimized timing for the synchronous MOSFETs which improves efficiency. At higher load currents it becomes more advantageous to delay the turn-off of the synchronous rectifiers until the transformer core has been reset to begin the new power pulse. This allows for secondary freewheeling current to flow through the synchronous MOSFET channel instead of its body diode.

The turn-off delay is programmed with a resistor from SPRG to GND, (Figure 7). The nominal regulated voltage on SPRG is 2V. The external resistor programs a current which flows out of SPRG. The delay can be adjusted from approximately 20ns to 200ns, with resistor values of 10k to 200k. Do not leave SPRG floating. The amount of delay can also be modulated based on an external current source that sinks current out of SPRG. Care must be taken to limit the current out of SPRG to 350µA or less.

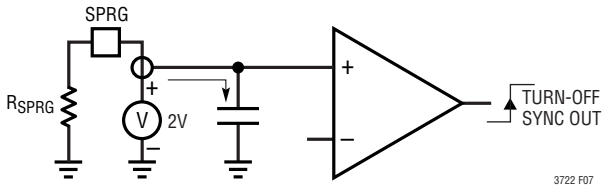


Figure 7. Synchronous Delay Circuitry

TYPICAL APPLICATION

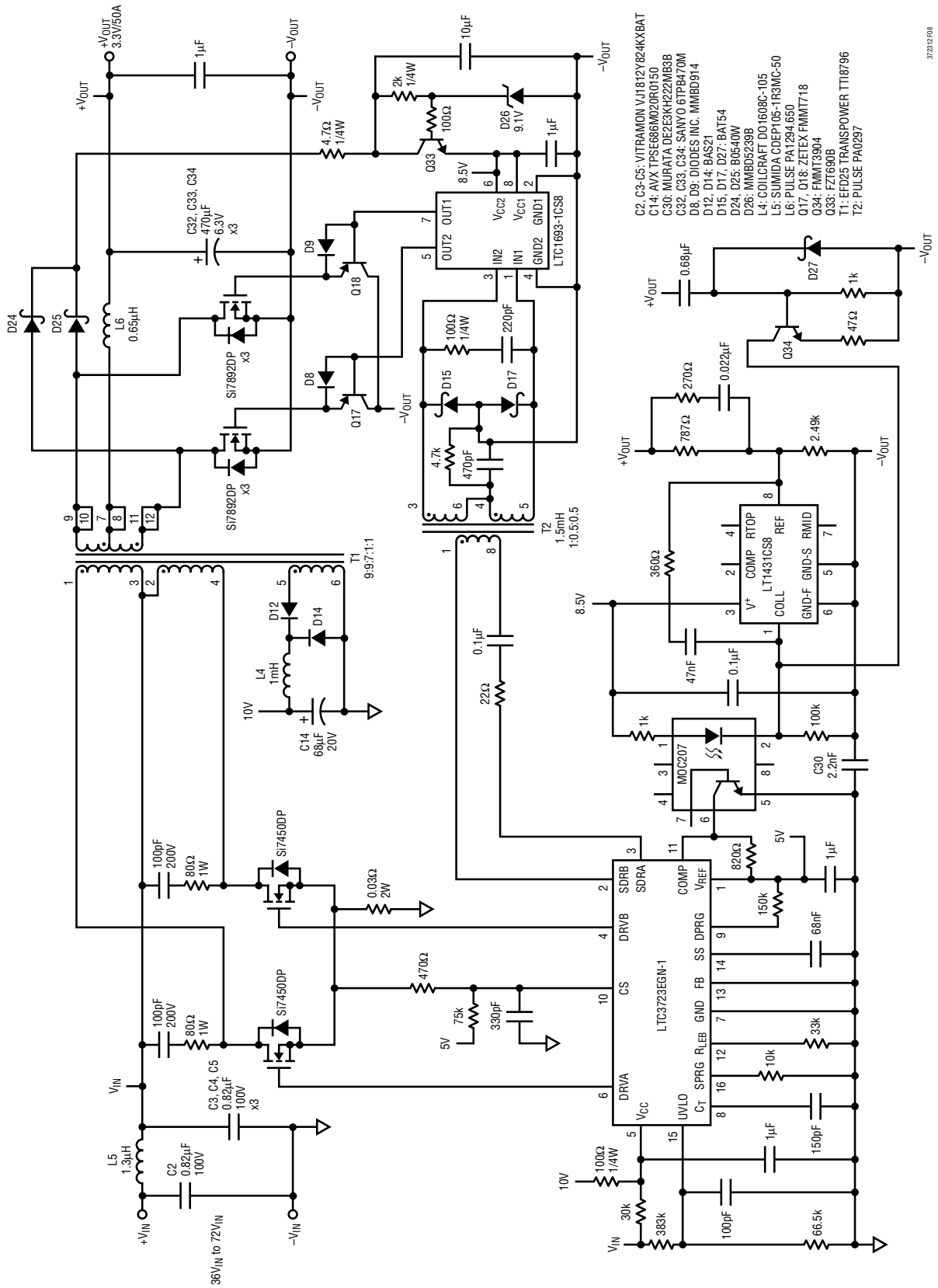


Figure 8. LTC3723-1 165W, 36V_{IN} to 72V_{IN} to 3.3V/50A Isolated Push-Pull Converter

TYPICAL APPLICATION

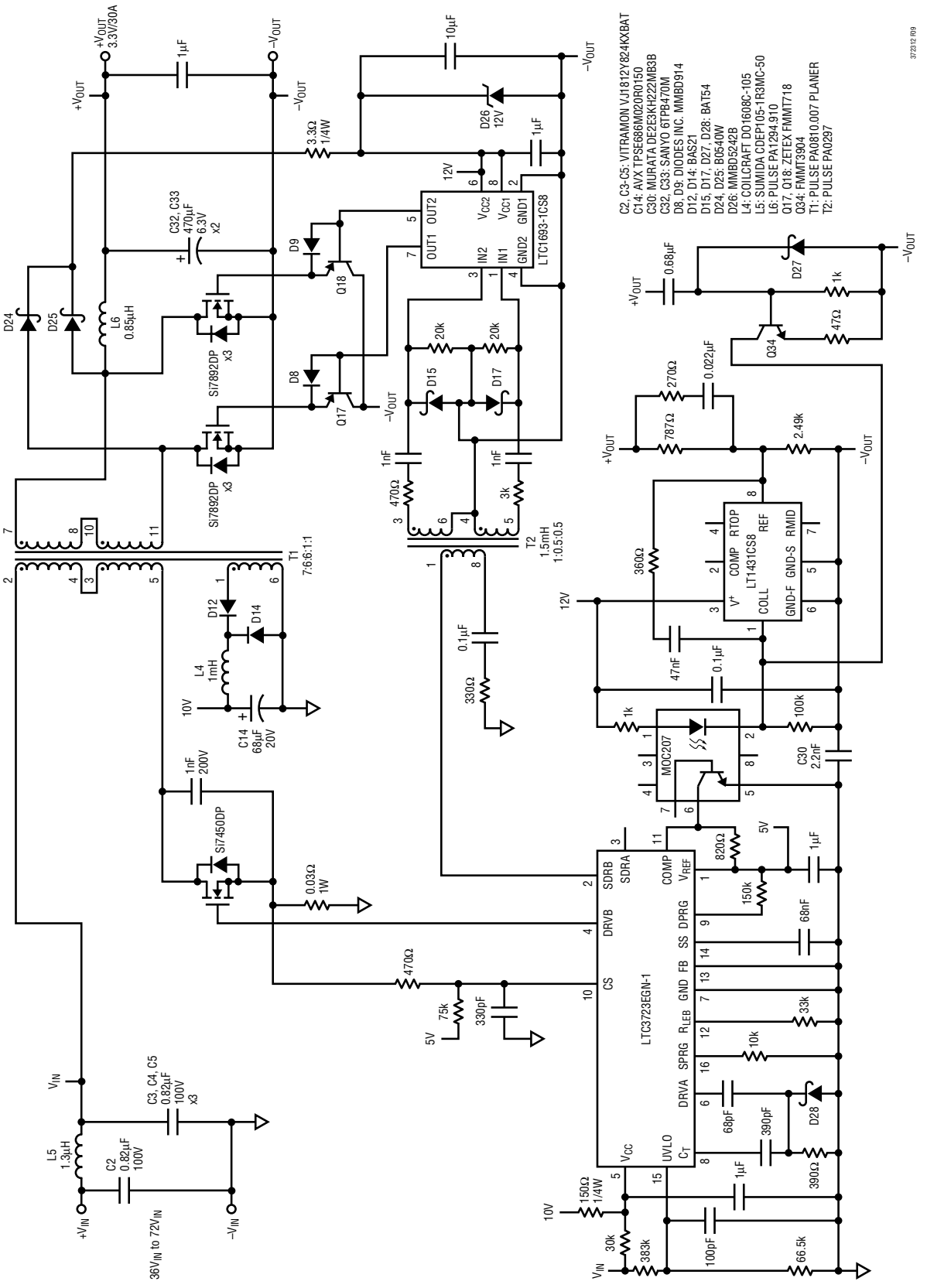
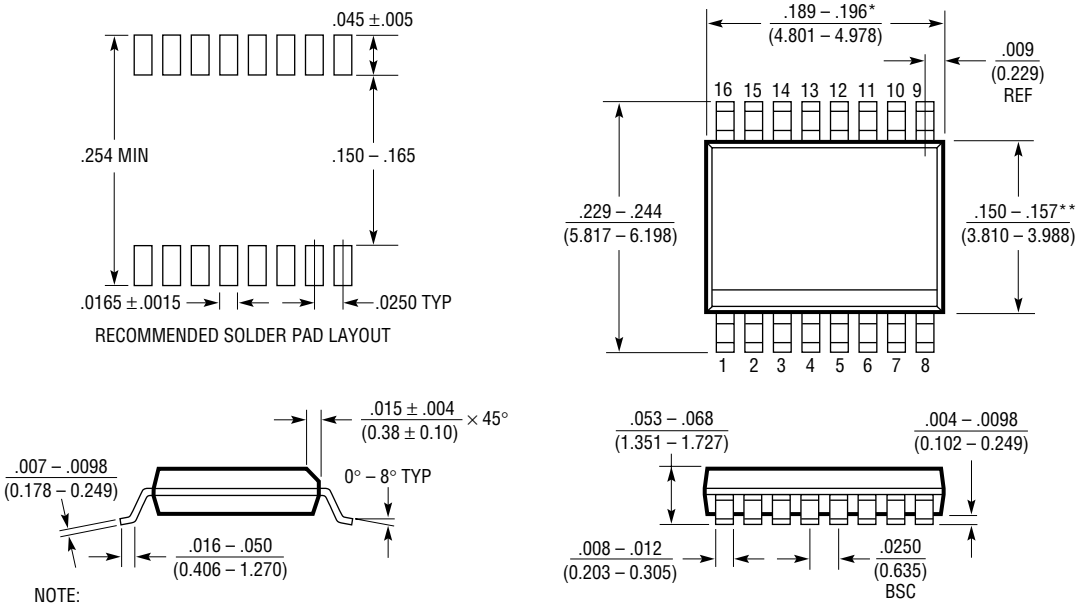


Figure 9. LTC3723-1 100W, 36V_{IN} to 72V_{IN} to 3.3V/30A Isolated Forward Converter

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1431	Reference and Opto-Driver	Drives Opto-Coupler
LT1681/LT3781	Synchronous Forward Controllers	High Efficiency 2-Switch Forward Control
LTC1693-1	Dual MOSFET Gate Drivers	High Speed MOSFET Gate Drivers
LTC3722-1/LTC3722-2	Dual Mode Phase Modulated Full-Bridge Controllers	ZVS Full-Bridge Controllers
LT3804	Secondary Side Dual Output Controller with Opto Driver	Regulates Two Secondary Outputs; Optocoupler Feedback Driver and Second Output Synchronous Driver Controller

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LT/TP 1003 1K • PRINTED IN USA