

A.HE83134 Introduction

HE83134 is a member of Jess Tech HE8000 series 8-bit CMOS micro-controller. This IC can share the LCD pin and I/O pin (From 640-dot of LCD driver + 12 Bit I/O Port ... 320-dot of LCD driver + 32 Bit I/O Port), the combination of the above is selected by Mask Option. It built-in one internal Op-Amp allows interfacing with light, speech, temperature and humidity sensor for control application. It built-in one 7-bit D/A converter and one PWM output module to provide a speech output interfaces. Use the built-in 256K ROM can store around 80 seconds of speech data. In addition, it can be connected with external SRAM or Flash RAM for recording function.

The HE83134 provides a very simple and effective instruction set, each instruction byte occupies only 1.5 clock cycle time, therefore, and it is suitable to apply in the high performance systems.

B.HE83134 Features

- Operating Voltage: 2.4V – 5.2V
- Operation frequency Range: DC ~ 8MHz @ 5.0V
DC ~ 4MHz @ 2.4V
- ROM size: 256K Bytes
- RAM size: 256 Bytes
- Dual Clock: Normal(Fast) clock: 32.768K ~ 8MHz
Slow clock: 32.768KHz
- Operating Mode: DUAL , FAST , SLOW , IDLE , SLEEP
- Built-in WATCH DOG TIMER
- 12~32 bi-directional I/O pins, PUSH-PULL or OPEN DRAIN output selected by mask option
- Built-in an internal Op-Amp
- 640~320 LCD driver (A , B TYPE)
- Built-in one 7-bit D/A Converter
- Built-in a PWM output circuit
- Provides two internal and two external interrupt
- Provides three 16-bit timer
- Instruction Set : 32 Instructions, 4 types of Addressing Mode, 2 individual Pointer for ROM (18-bit) and RAM (8-bit) table access.

C.HE83134 Application

- Interface to Light, Sound, Temperature and Humidity sensor for controlling application.
- Suitable in LCD games, education toys, data bank, translator and some mid-to-high end electronic products.
- Interface with external SRAM or Flash RAM for recording function.

D. Pin Assignment

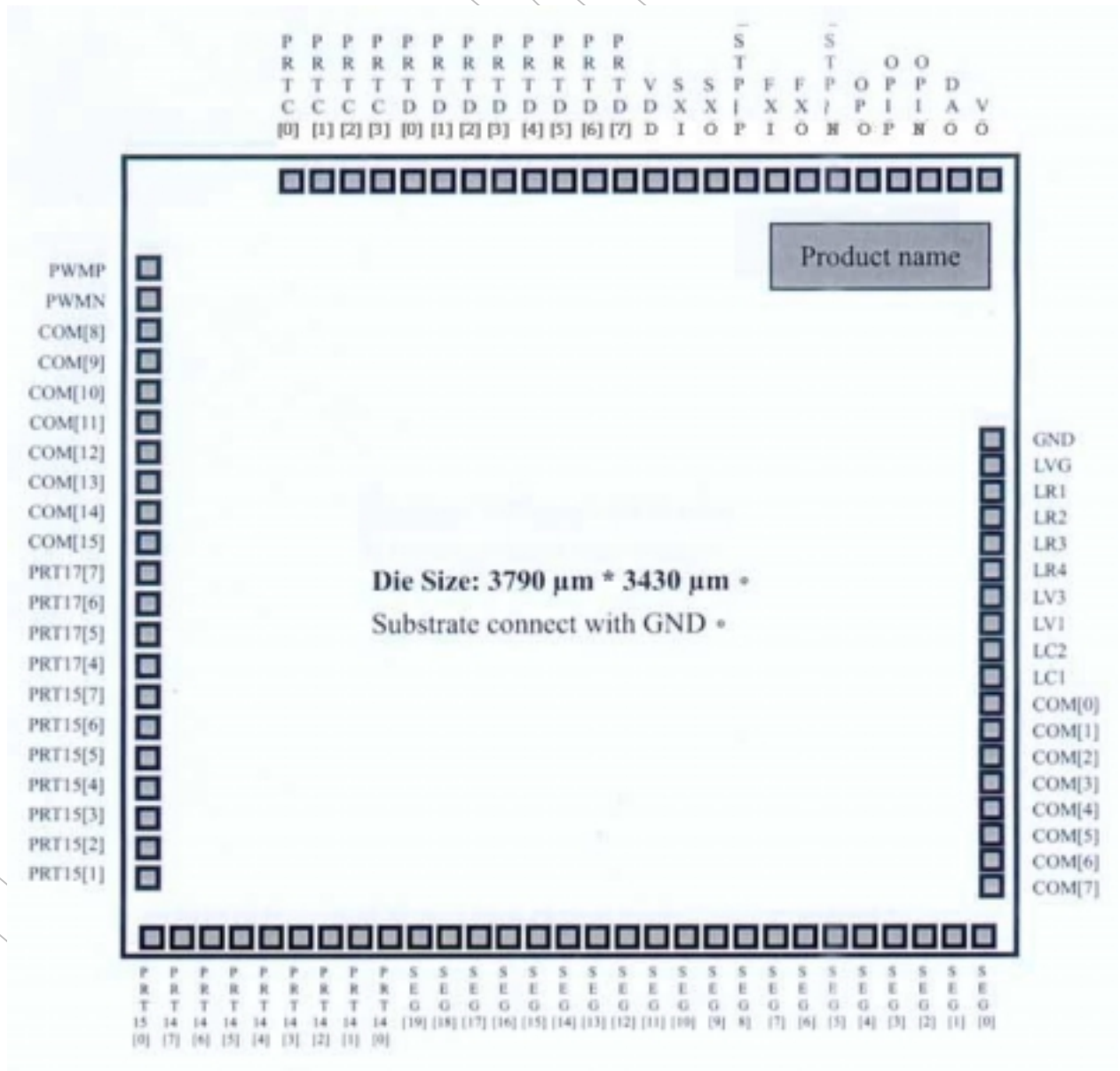
Pin	Pin Name	I/O	Function	Description
77 76	FXI, FXO	B, O	External Fast Clock pin. To connect the Crystal or R, C oscillation to generate 32.768KHz ~ 8MHz system clock.	Mask Option settings : MO_FCK/SCKN=00 : Slow Clock only 01 : Illegal 10 : Dual Clock 11 : Fast Clock only
80 79	SXI, SXO	I, O	External Slow Clock pin . To connect the 32.768KHz oscillator to generate the stable frequency for Slow Mode, and provide IC LCD display, Timer clock source.	MO_FOSCE=0 : Internal fast oscillation 1 : External fast oscillation MO_FXTAL=0 : R,C oscillation for Fast Clock 1 : Crystal oscillation for Fast Clock MO_SXTAL=0 : R,C oscillation for 32.768K Clock 1 : X'tal oscillation for 32.768K Clock Program the value of OP1 and OP2 to change the operating modes (Normal, Slow, Idle and Sleep). In Dual Clock mode , the system runs in Fast Clock, only the Timer 1 use the 32.768K clock source.
75	RSTP_N	I	System reset signal	Pull this pin to low level to reset the system. Besides, Select the Mask Option (MO_PORE=1) to enable the IC internal Power-on Reset function. In addition, the MO_WDTE is used for Watch Dog Timer setting : MO_WDTE =0 : Disable Watch Dog Timer =1 : Enable Watch Dog Timer
78	TSTP_P	I	Test Pin.	Please bond this pin and add a test point on PCB for debugging. Leave this pin floating is OK.
90.. 92 1	PRTC[3:0]	B	Port C bi-directional I/O pin (4 pins)	Mask Option MO_CPP[3:0] to preset the output type: MO_CPP=1 : Push-pull output ; = 0 : Open-drain output. When assigned the port to input pin, send a '1' and read the result to get the input value.
82.. 89	PRTD[7:0]	B	Port D bi-directional I/O pin, (8 pins). PRTD[7:2] is also a Wake-up pin and PRTD[7:6] is used for interrupt input pin.	Mask Option MO_DPP[7:0] to preset the output type: MO_DPP=1 : Push-pull output ; 0 : Open-drain output. When assigned the port to input pin, send a '1' and read the result to get the input value.
12.. 15	PRT17[7:4]/ SEG[39:36]	B/ O	Port 17 bi-directional I/O pin, (4 pins), or it can be shared to LCD segment Segment[39:36] °	Use Mask Option MO_LIO17[7:0] to select the pins are I/O or LCD segment: MO_LIO17[7:0]= 0; I/O Pin = 1; When the pins are assignment to I/O pin, select the MASK Option MO_17PP[7:4] for output type MO_14PP=0 : Open-drain output =1 : Push-pull output,
16.. 23	PRT15[7:0]/ SEG[35:28]	B/ O	Port 15 bi-directional I/O pin, (8 pins), or it can be shared to LCD segment Segment[35:28] °	Mask Option MO_LIO15[7:0] to select the pins are I/O or LCD segment.: MO_LIO15[7:0]= 0; I/O Pin = 1; When the pins are assignment to I/O pin, select the MASK Option MO_15PP[7:0] for output type MO_15PP[7:0] =0 : Open-drain output =1 : Push-pull output,

24.. 31	PRT14[7:0]/ SEG[27:20]	B/ O	Port 14 bi-directional I/O pin, (8 pins), or it can be shared to LCD segment Segment[27:20] °	Mask Option MO_LIO14[7:0] to select the pins are I/O or LCD segment: MO_LIO14[7:0]=0 ; I/O pin=1 ; When the pins are assignment to I/O pin, select the MASK Option MO_14PP[7:0] for output type MO_14PP=1 : Open-drain output 0 : Push-pull output
11..4, 52.. 59	COM[15:0]	O	LCD COMMon Output	Fill data from 80H, refer LCD and RAM map.
32.. 51	SEG[19:0]	O	LCD SEGment Output	
61	LC2	B	Charge Pump Switch 1	When LV3=VDD, Charge Pump for LCD is turn off. The 0.1uF capacitor must be removed to avoid current consumption.
60	LC1	B	Charge Pump Switch 2	
63	LV3	B	Charge Pump V3	Refer to application circuit.
62	LV1	B	Charge Pump V1	
64.. 67	LR[4..1]	B	LCD Resister level 4 ~ 0	Refer to application circuit.
68	LVG	I	LCD Virtual Ground	Refer to application circuit.
2	PWMP	O	PWM +ve O/P pin, can directly drive Speaker or Buzzer for voice output.	Preset the Bit2 of VOC register: PWM =1 ; turn on PWM.
3	PWMN	O	PWM -ve O/P pin, can directly drive Speaker or Buzzer for voice output.	Preset the Bit2 of VOC register: PWM =1 ; turn on PWM.
70	VO	O	D/A voice output	Preset the Bit-1 of VOC register: DA=1 ; turn on VO.
71	DAO	O	D/A Output, for OP-Amp use	Preset the Bit-0 of VOC register: OP=1 ; turn on DAO.
72	OPIN	I	OPAMP Inverting I/P pin	Preset the bit0 of VOC register: OP=1 ; turn on OP Individual built-in OP-Amp
73	OPIP	I	OPAMP Non-inverting I/P pin.	
74	OPO	O	OPAMP O/P pin	
81	VDD	P	Positive Power Input	Adding 0.1mF capacitor as by-pass capacitor is between VDD and GND is necessary
69	GND	P	Power Ground Input	

E.LCD RAM Map

Page 0	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]
COM0	80H	90H	A0H	B0H	C0H
COM1	81H	91H	A1H	B1H	C1H
COM2	82H	92H	A2H	B2H	C2H
:	:	:	:	:	:
:	:	:	:	:	:
COM13	8DH	9DH	ADH	BDH	CDH
COM14	8EH	9EH	AEH	BEH	CEH
COM15	8FH	9FH	AFH	BFH	CFH

F. Pin Diagram



G. Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRTC[0]	-1011.00	1635.10	47	SEG[4]	1025.00	-1636.50
2	PWMP	-1820.20	1287.70	48	SEG[3]	1140.50	-1636.50
3	PWMN	-1820.20	1124.30	49	SEG[2]	1256.00	-1636.50
4	COM[8]	-1820.20	985.20	50	SEG[1]	1371.50	-1636.50
5	COM[9]	-1820.20	869.80	51	SEG[0]	1487.00	-1636.50
6	COM[10]	-1820.20	754.20	52	COM[7]	1818.30	-1535.20
7	COM[11]	-1820.20	638.80	53	COM[6]	1818.30	-1419.80
8	COM[12]	-1820.20	523.20	54	COM[5]	1818.30	-1304.20
9	COM[13]	-1820.20	407.80	55	COM[4]	1818.30	-1188.80
10	COM[14]	-1820.20	292.20	56	COM[3]	1818.30	-1073.20
11	COM[15]	-1820.20	176.80	57	COM[2]	1818.30	-957.80
12	PRT17[7]	-1820.20	61.20	58	COM[1]	1818.30	-842.20
13	PRT17[6]	-1820.20	-54.20	59	COM[0]	1818.30	-726.80
14	PRT17[5]	-1820.20	-169.80	60	LC1	1818.30	-611.20
15	PRT17[4]	-1820.20	-285.20	61	LC2	1818.30	-495.80
16	PRT15[7]	-1820.20	-400.80	62	LV1	1818.30	-380.20
17	PRT15[6]	-1820.20	-516.20	63	LV3	1818.30	-264.80
18	PRT15[5]	-1820.20	-631.80	64	LR4	1818.30	-149.20
19	PRT15[4]	-1820.20	-747.20	65	LR3	1818.30	-33.80
20	PRT15[3]	-1820.20	-862.80	66	LR2	1818.30	81.80
21	PRT15[2]	-1820.20	-978.20	67	LR1	1818.30	197.20
22	PRT15[1]	-1820.20	-1093.80	68	LVG	1818.30	312.80
23	PRT15[0]	-1747.00	-1636.50	69	GND	1818.30	428.20
24	PRT14[7]	-1631.50	-1636.50	70	VO	1699.90	1634.40
25	PRT14[6]	-1516.00	-1636.50	71	DAO	1548.10	1634.40
26	PRT14[5]	-1400.50	-1636.50	72	OPIN	1414.50	1635.10
27	PRT14[4]	-1285.00	-1636.50	73	OPIP	1299.00	1635.10
28	PRT14[3]	-1169.50	-1636.50	74	OPO	1183.50	1635.10
29	PRT14[2]	-1054.00	-1636.50	75	RSTP_N	1068.00	1635.10
30	PRT14[1]	-938.50	-1636.50	76	FXO	952.50	1635.10
31	PRT14[0]	-823.00	-1636.50	77	FXI	837.00	1635.10
32	SEG[19]	-707.50	-1636.50	78	TSTP_P	721.50	1635.10
33	SEG[18]	-592.00	-1636.50	79	SXO	606.00	1635.10
34	SEG[17]	-476.60	-1636.50	80	SXI	490.40	1635.10
35	SEG[16]	-361.10	-1636.50	81	VDD	374.90	1635.10
36	SEG[15]	-245.60	-1636.50	82	PRTD[7]	259.40	1635.10
37	SEG[14]	-130.10	-1636.50	83	PRTD[6]	143.90	1635.10
38	SEG[13]	-14.60	-1636.50	84	PRTD[5]	28.40	1635.10
39	SEG[12]	101.00	-1636.50	85	PRTD[4]	-87.10	1635.10
40	SEG[11]	216.40	-1636.50	86	PRTD[3]	-202.60	1635.10
41	SEG[10]	331.90	-1636.50	87	PRTD[2]	-318.10	1635.10
42	SEG[9]	447.40	-1636.50	88	PRTD[1]	-433.60	1635.10
43	SEG[8]	563.00	-1636.50	89	PRTD[0]	-549.10	1635.10
44	SEG[7]	678.50	-1636.50	90	PRTC[3]	-664.60	1635.10
45	SEG[6]	794.00	-1636.50	91	PRTC[2]	-780.10	1635.10
46	SEG[5]	909.50	-1636.50	92	PRTC[1]	-895.60	1635.10

H. Electrical Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ $V_{dd}+0.5V$	
Output Voltage	V_o	-0.5V ~ $V_{dd}+0.5V$	
Operating Temperature	T_{op}	0°C ~ 70°C	
Storage Temperature	T_{st}	-50°C ~ 100°C	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.2V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1 V_{dd}	
Operating Frequency	F_{max}	8MHz	$V_{dd}=5.0V$
		4MHz	$V_{dd}=2.4V$
Operating Temperature	T_{op}	0°C ~ 70°C	
Storage Temperature	T_{st}	-50°C ~ 100°C	

Test condition:TEMP=25°C, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		10	20	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		6	10	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable, LCD option=300Kohm Voltage-doubler OFF		12	20	μA
			LCD Enable, LCD option=30Kohm, Voltage-doubler ON		100	120	
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{oHPW}	PWM Output Drive Current	PWMP, PWMN*2	$V_{DD}=3V; V_{oh}=2V$	12	15		mA
I_{oLPW}	PWM Output Sink Current	PWMP, PWMN*2	$V_{DD}=3V; V_{oL}=1V$	33	40		mA
I_{oVO}	DAC Output Current	VO, DAO	$V_{DD}=3V; VO=0\sim 2V, Data=7F$	2.5	3		mA
V_{IH}	Input High Voltage	I/O pins		0.8			V
				V_{DD}			
V_{IL}	Input Low Voltage	I/O pins				0.2	V
						V_{DD}	
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold= $2/3V_{DD}$ (input from low to high) Threshold= $1/3V_{DD}$ (input from high to low)		1/3		V
					V_{DD}		
I_{oH}	Output Drive Current	I/O pull-high*1	$V_{oL}=2.0V$	50			μA
I_{oL1}	Output Sink Current	I/O pull-low*1	$V_{oL}=0.4V$	1.0			mA
I_{IL1}	Input Low Current	RSTP_N	$V_{IL}=GND$, pull high Internally		20		μA
I_{IL2}	Input Low Current	I/O	$V_{IL}=GND$, if pull high Internally by user		100		μA

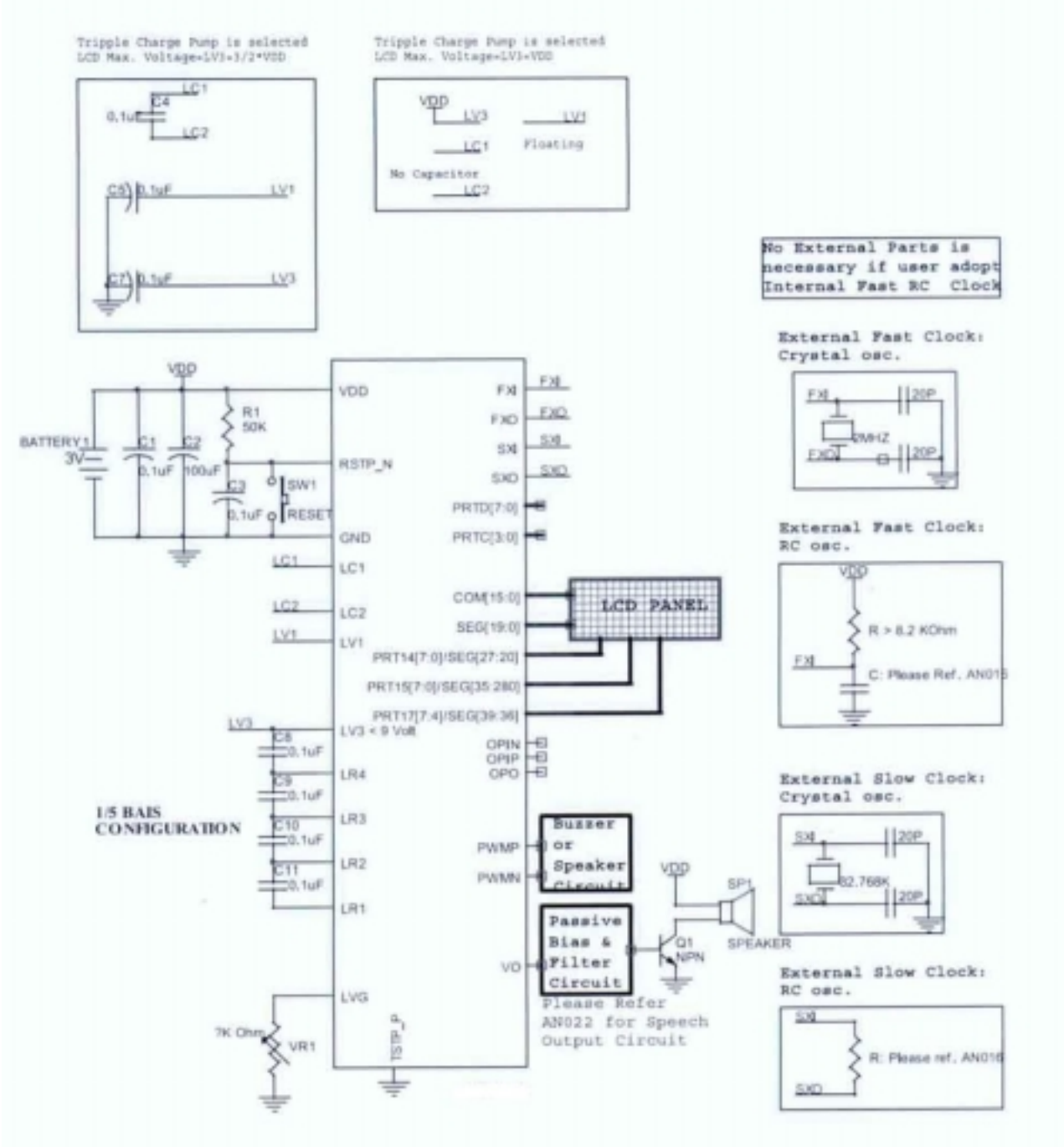
Note: *1: Drive Current Spec. for Push-Pull I/O port only

Sink Current Spec. for both Push-Pull and Open-Drain I/O port.

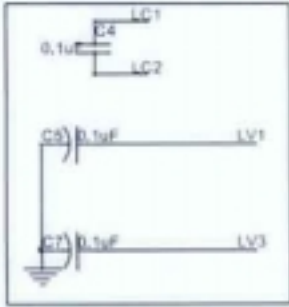
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current

to get the total amount of current. ($I_{oHPWM} \cdot I_{oLPWM} * N$; N=0,1,2,3,4,5)

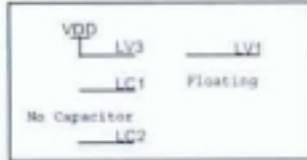
I. Application Circuit



Tripple Charge Pump is selected
 LCD Max. Voltage=LV1+1/2*VDD

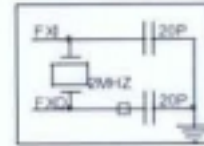


Tripple Charge Pump is selected
 LCD Max. Voltage=LV1+VDD

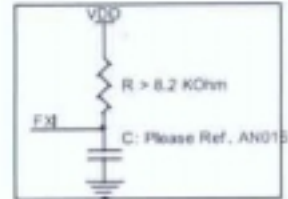


No External Parts is necessary if user adopt Internal Fast RC Clock

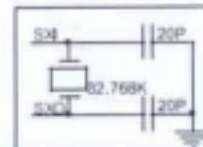
External Fast Clock: Crystal osc.



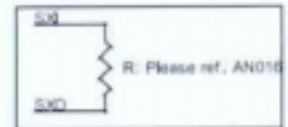
External Fast Clock: RC osc.



External Slow Clock: Crystal osc.



External Slow Clock: RC osc.

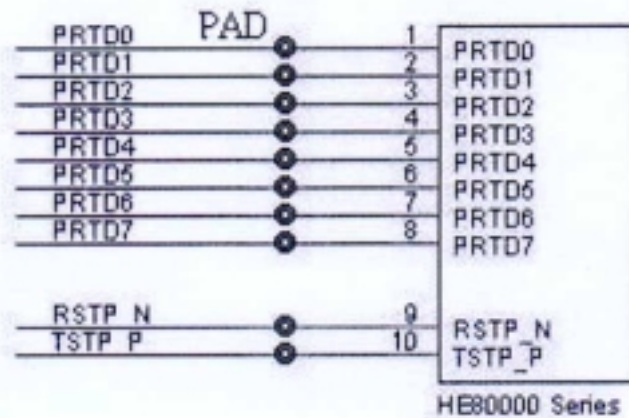


J. Important Note

For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.

LCD driving circuit must be turn off before IC goes into sleep mode

Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then JESS can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole.)



LV3 must small than 9.0 Volt. Otherwise IC may breakdown.

SUPPLEMENTARY SPECIFICATION: HE82/83/89 PWM application

Description:

For HE83/89 PWM application, the following points must be bare in mind.

1. The PWM output can direct drive buzzer.
2. For direct drive speaker, it must use 32Ω or above speaker.
3. For speaker application, it must add capacitors between IC's VDD ground and its PWM output, see below figure.

Note: the $1\mu\text{F}$ capacitor must be connected near IC's

