International
IOR Rectifier

PRELIMINARY

IRPT4052

POWIRTRAIN™

Integrated Power Stage for 7.5 hp Motor Drives

- *7.5 hp (5.5kW) power output*

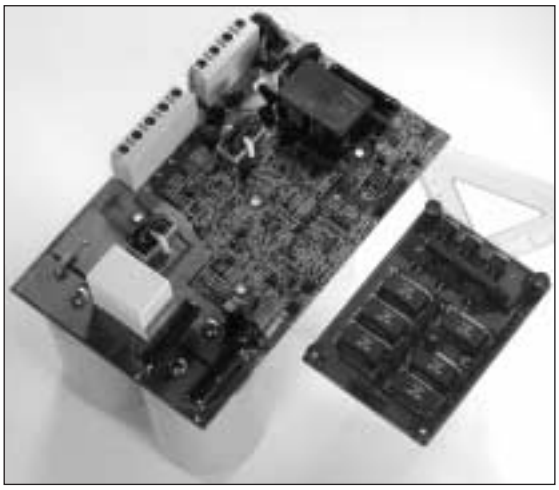
  Industrial rating at 150% overload for 1 minute
- *380 - 480V AC input, 50/60Hz*
- *Available as complete system or sub-system assemblies*

Power Assembly

- *3-phase rectifier bridge*
- *3-phase short circuit rated, ultrafast IGBT inverter*
- *HEXFRED™ UltraFast™ soft recovery free-wheeling diode*
- *NTC temperature sensor*
- *Pin-to-base plate isolation 2500V rms*
- *Easy-to-mount package*
- *Case temperature range -25 C to 125 C operational*

Driver-Plus Board

- *Capacitor filter with precharge current limit*
- *Isolated gate drive circuits*
- *On-board local power supply for gate driver and capacitor precharge control*
- *MOV surge suppression at input*
- *Isolated inverter current feedback*
- *Short circuit, earth/ground fault, over-temperature protection*
- *Input and output terminals; optional external brake*
- *Control interface connector*



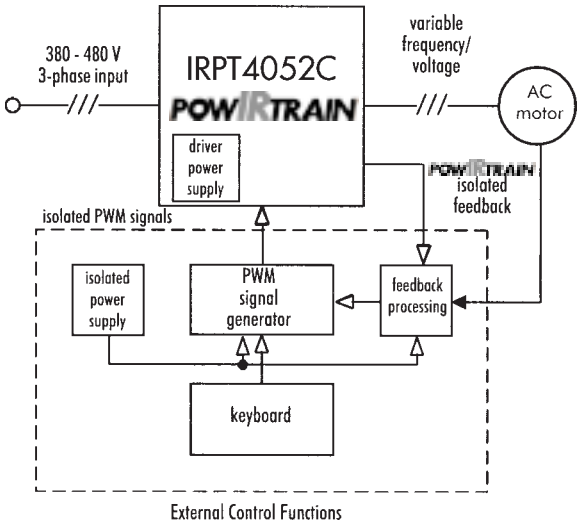


Figure 1. The IRPT4052C POWIRTRAIN within a motor control system

System Description

The IRPT4052C POWIRTRAIN provides the complete power conversion function for a 7.5hp (5.5kW) variable voltage, variable frequency, AC motor controller. The POWIRTRAIN combines a power assembly IRPT4052A with a Driver-*Plus* Board IRPT4052D. Figure 1 shows the block diagram of the POWIRTRAIN within an AC motor control system.

The power assembly contains a 3-phase input bridge rectifier, 3-phase IGBT inverter and a thermistor mounted on an Insulated Metal Substrate (IMS) power board. It is designed for easy mounting to a heat sink.

The Driver-Plus Board contains DC link capacitors, capacitor pre-charge function, isolated IGBT gate drive circuits, shutdown protection, isolated trip and current feedback signals, and local power supply. It interfaces to the power assembly via soldered connector pins. Terminal blocks are provided on the Driver-*Plus* Board for all end-user external connections to the POWIRTRAIN.

Output power is Pulse-Width Modulated (PWM), 3-phase, variable-frequency, variable voltage controlled by externally generated user provided PWM controller for inverter IGBT switching. The PWM input signals and feedback signals are optically isolated from the power circuit.

The IRPT4052C offers several benefits to the drive manufacturer as listed below:

- It eliminates component selection, design layout, interconnection, gate drive, local power supply, thermal sensing, current sensing, and protection.
- It provides committed power semiconductor losses and junction temperatures.
- Gate drive and protection circuits are designed to closely match the operating characteristics of the power semiconductors. This allows power losses to be minimized and power rating to be maximized to a greater extent than is possible by designing with individual components.
- Optimized layout for performance and efficiency is provided.
- Low inductance system reduces noise and snubber requirements.

  [POWIRTRAIN specifications and ratings are given for system input and output voltage and current, power losses and heat sink requirements over a range of operating conditions. POWIRTRAIN system ratings are verified by IR in final testing.]

Power Assembly

The IRPT4052A power assembly consists of input rectifiers, NTC thermistor, output inverter and connectors mounted on an Insulated Metal Substrate (IMS) substrate. The input side employs surface mount 1600V rated SMD-220 rectifier diodes and the inverter section employs surface mount SMD-10, 1200V IGBT Co-pack switches. The NTC thermistor mounted near the inverter provides temperature sensing capability. The lead spacing on the power assembly meets UL840 pollution level 2 requirements.

The power circuit and layout are carefully designed to minimize inductance in the power path, to reduce noise during inverter operation and to improve the inverter efficiency. The power level interfaces to the Driver-*Plus* Board through solder pins, minimizing assembly and alignment. The power assembly is designed to be mounted to a heat sink with five screw mount positions, one in each corner and a fifth near the center, in order to insure good thermal contact between the IMS and the heat sink.

Figure 2. IRPT4052A Power Assembly

The IRPT4052D Driver-*Plus* Board

The Driver-*Plus* Board, shown in figure 3, is the interface between the controller and the power stage. It contains the IGBT gate drivers, sensing and protection circuitry, feedback and local power supply. It also houses the DC link capacitors, relay and relay control circuit used for implementing the capacitor precharge function. Figure 4 provides detailed functional block diagrams of the IRPT4052D.

The **gate drive circuits** deliver on/off gate drive signals to the IGBTs' gates, corresponding with input PWM control signals IN1 through IN6. The PWM gate normally allows the input PWM control signal to pass to the input opto-isolators of the gate drive circuits. The conduction periods of the inverter switches essentially mimic those demanded by the PWM input signals.

During power-up and power-down, or in the event of overcurrent (OI) or overtemperture (OT), the **latch** inhibits the PWM gate, deactivating the gate drive circuits and shutting off the inverter.

The **relay control circuit** delivers an on/off signal via an opto-isolator to the relay driver which controls the relay (K1). The relay contact is open during power-up, inserting the resistor R in series with the DC bus capcitor and limiting the capacitor charging current. In normal operation, the relay contact is closed. If the AC line voltage falls below 300V or if one input phase is lost, or if the DC line voltage falls to less than 82% of the peak line voltage, the relay contact opens.

The **UV circuit** senses the voltage of the local power supply, and sends a signal via an opto-isolator to the latch in the event of undervoltage. The UV circuit normally activates the latch only during power-up and power-down, preventing the IGBTs from being turned on when the local power supply voltage is too low for proper IGBT switching.

The **current signal processing circuit** receives inputs from current transformers connected in series with the input lines and the DC bus capacitor. The output of the current signal processing circuit, IFB, is essentially an isolated replica of the inverter input current. An isolated current feedback signal, I_{FB}, is provided as an output of the IRPT4052A. If the inverter current exceeds the trip level of 45A, I_{FB} also activates the latch.

The **thermistor** activates the latch if the temperature of the IMS substrate exceeds a set level. The 15V isolated power supply used to power the IRPT4052 should be the same as the one for the PWM generation, otherwise the protection functions will be disabled.

The **switching power supply** delivers a nominal 18V DC output, referenced to the negative DC bus, N. This feeds the gate drive, relay control and under voltage (UV) circuits, which are optically isolated from the control input section, and therefore require their own local power source.

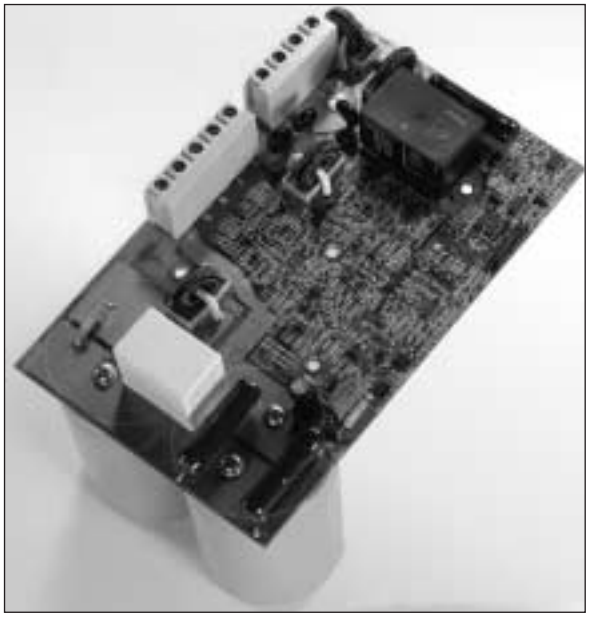


Figure 3. IRPT4052D Driver-*Plus* Board

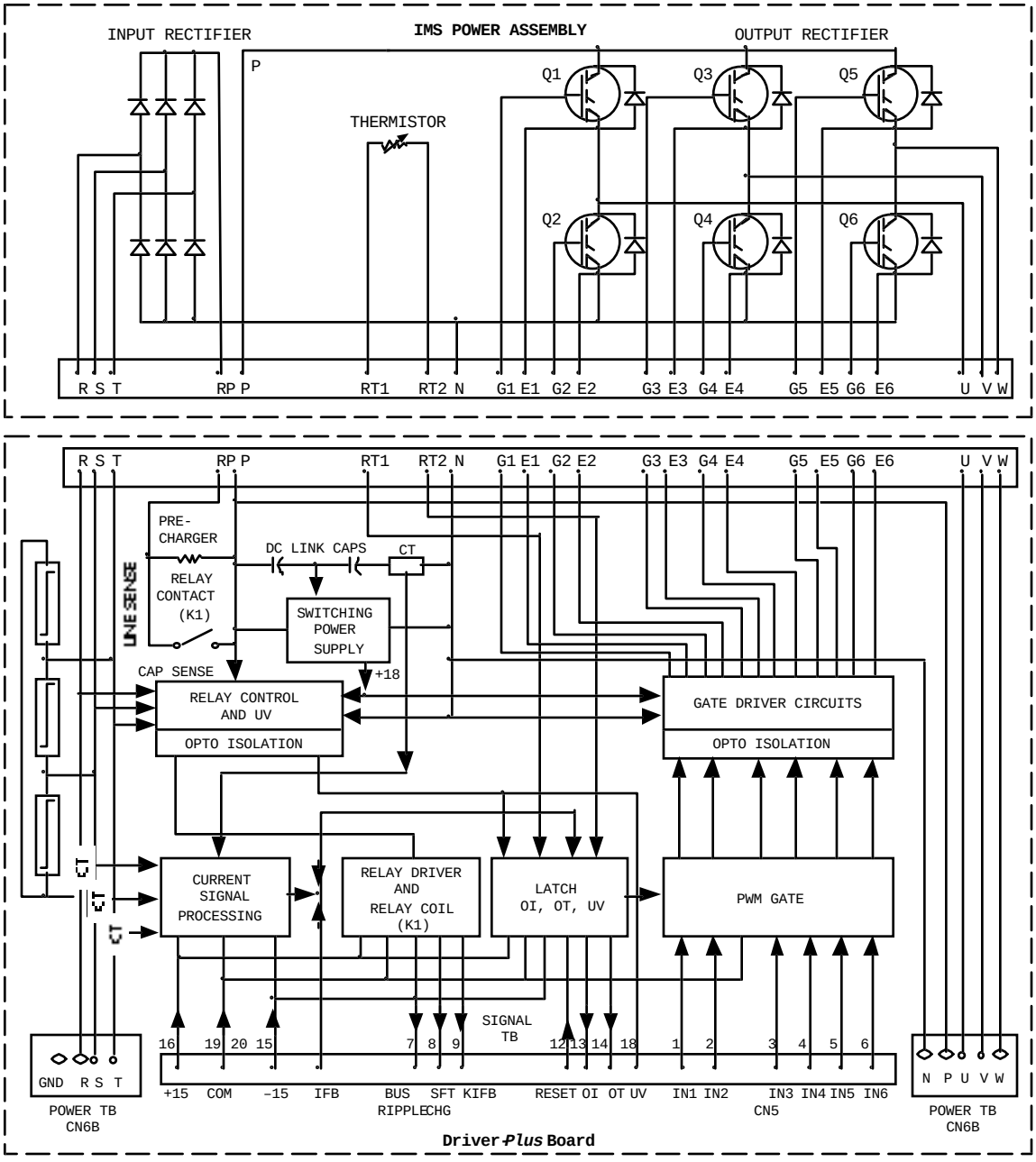


Figure 4. IRPT4052C Basic Architecture

Specifications

PARAMETERS	VALUES	CONDITIONS
Input Power		
Voltage	380V, -15%, 480V +10%, 3-phase	
Frequency	50 - 60Hz	
Input current	20A rms	T_A = 40°C, R_{thSA} = 0.148°C/W
	300 A peak	10ms half-cycle, non-repetitive surge
Output Power		
Voltage	0 - 480V rms	defined by external PWM control
Nominal motor hp (kW)	7.5hp (5.5 kW) nominal full load power 150% overload for 1 minute	V_{in} = 440VAC PWM frequency = 4kHz, f_e = 60Hz, T_A = 40°C, R_{thSA} = 0.148°C/W
Nominal motor current	12.5A rms nominal full load current 18.75A rms 150% overload for 1 minute	
DC Link		
DC link voltage	850V maximum	
Control Inputs		
Control power	15V ±5%, 200mA positive supply 15V ±5%, 10mA negative supply	
PWM input signals IN1 - IN6	15V, 10mA, ±10% (max rise/fall time 150nsec)	input signals uninhibited internally
Input resistance IN1 - IN6	720 ohms ±5%	input signals inhibited internally
Pulse deadtime	2.5 μsec, minimum	
Minimum input pulse duration	1.0 μsec	
Maximum pulse duration for each upper IGBT	20ms	
RESET	15V active high, CMOS input (min duration 1μsec)	
SFT CHG	2 mA pull-down to energize relay (overrides internal control)	
Protection		
Output current trip level	45A peak, ±10%	
Overtemperature trip level	100°C, ±5%	
Ground current trip level	40A peak, ±10%	
Short circuit shutdown time	1.5 μsec typical	output terminals shorted
Feedback Signals		
Current feedback signal, IFB	100mV/A ±10% max. DC offset 200mV	
Overcurrent trip signal, OI	active high, 15V CMOS	
Overtemp trip signal, OT	active high, 15V CMOS	
BUS RIPPLE	15V high 4.7k pull-up, <0.5V low at 1.0mA; high-to-low transition at V_{bus} = 82% peak of line voltage	
UV	15V high, 10k pull-up, during UV <0.5 low at 1mA with no UV	
Relay coil feedback, K1FB	15V high when relay coil energized; low when relay coil de-energized	
Capacitor Precharge		
DC bus capacitor precharge time	400msecs max	measured from input line closure; line voltage > 300V
Module		
Isolation voltage	2500V rms	pin-to-baseplate, 60Hz, 1 min.
Operating case temperature	-25°C to 125°C	95% RH max. (non-condensing)
Mounting torque	5 Nm	M5 screw type
System Environment		
Ambient operating temp. range	0 to 40°C	95% RH max. (non-condensing)
Storage temp.range	-25°C to 60°C	

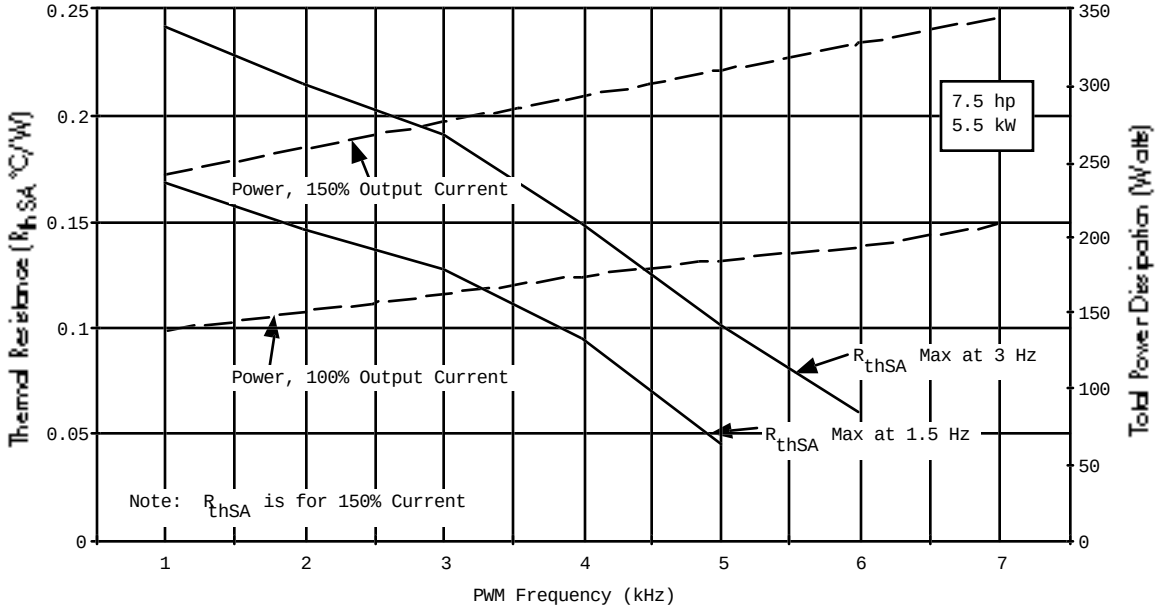


Figure 5a. 7.5hp/12.5A output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency (Induction Motor Load)

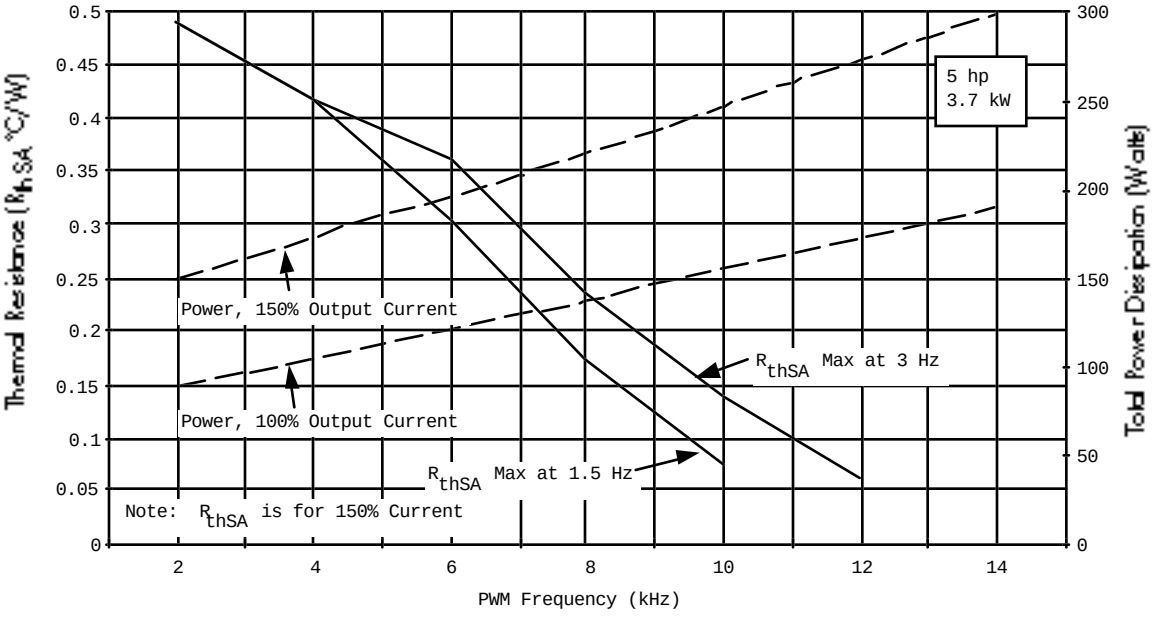


Figure 5b. 5hp/8.25A output Heat Sink Thermal Resistance and Power Dissipation vs. PWM Frequency (Induction Motor Load)

Operating Conditions: V_{in} = 440V_{rms} MI = 1.15, PF-0.8, T_A = 40°C, Z_{thSA} limits temperature rise (ÐT_c) during 1 minute overload to 10°C

Mounting, Hookup and Application Instructions

Mounting

Unless supplied connected, first connect the IRPT4052D and the IRPT4052A power assembly.

1. Remove all particles and grit from the heat sink and power substrate.
2. Spread a .004" to .005" layer of silicone grease on the heat sink, covering the entire area that the power substrate will occupy. Recommended heat sink flatness is .001 inch/inch and Total Indicator Readout (TIR) of .005" below substrate.
3. Place the power substrate onto the heat sink with the mounting holes aligned and press it firmly into the silicone grease.
4. Place the 5 M5 mounting screws through the PCB and power substrate and into the heat sink and tighten with fingers.

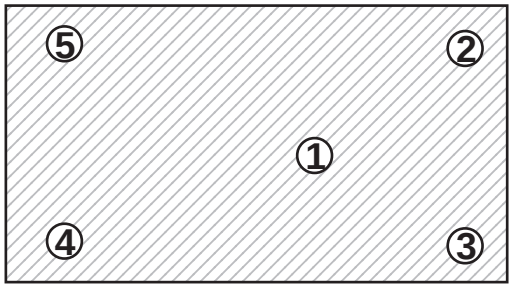


Figure 6. Power Assembly Mounting Screw Sequence

5. Tighten the screws to 2 Nm torque, according to the sequence shown in figure 6.
6. Re-tighten the screws to 4-5 Nm using the same sequence as in step 5.

Control Connections

All input and output connections are made via a female connector to CN6.

Power Connections

3-phase input connections are made to terminals R, S and T. Inverter output terminal connections are made to terminals U, V and W. Positive and negative DC bus connections are brought out to terminals P (positive) and N (negative). An external braking circuit can be connected across terminals P and N.

Logic Sequence During Power-Up

When 3-phase input power is first switched on, PWM inputs to the IRPT4052 must be inhibited until all the following logic conditions are met:

1. external 15V supply is established
2. UV feedback signal is low, indicating local power supply for gate drive circuits is established
3. K1FB signal is high, indicating capacitor precharge relay is energized.

When these conditions are simultaneously met, a 15V RESET pulse should be applied to the RESET input.
PWM input signals can now be released to the IRPT4052. The first PWM input signals to each of the lower IGBT inputs (IN2, IN4, IN6) should have at least 50µs duration, to allow the bootstrap capacitors to charge.

Logic Sequence During Power-Down

The following sequence is recommended for normal power down:

1. reduce motor speed to zero by PWM control
2. inhibit PWM inputs
3. disconnect main power

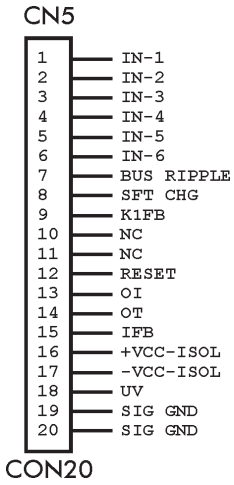


Figure 7a. Control Signal Connector

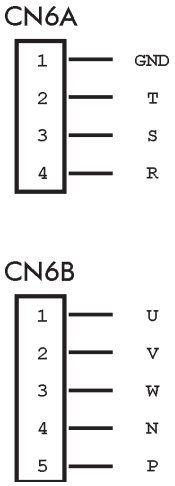
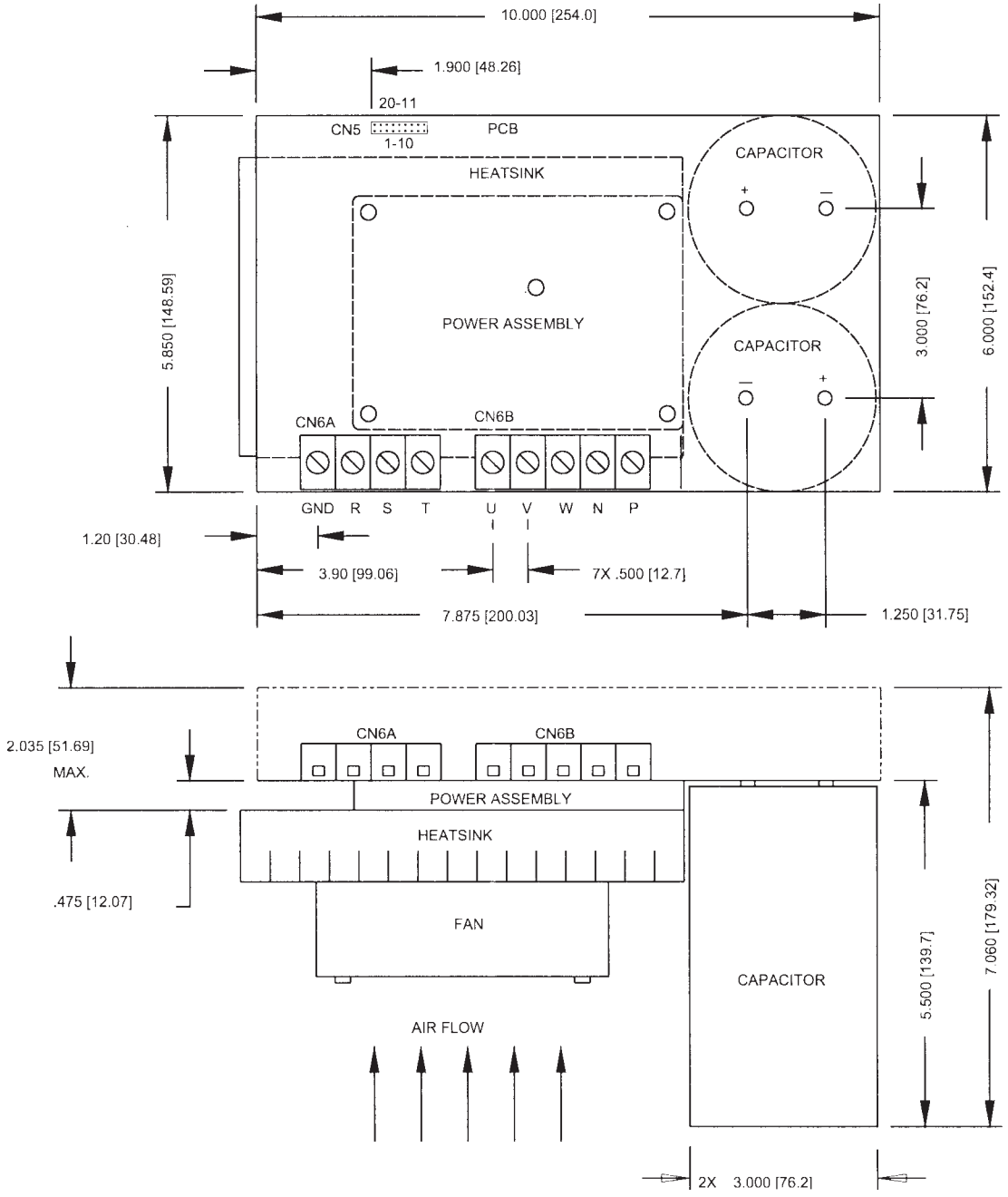


Figure 7b. Input and Output Terminal Blocks

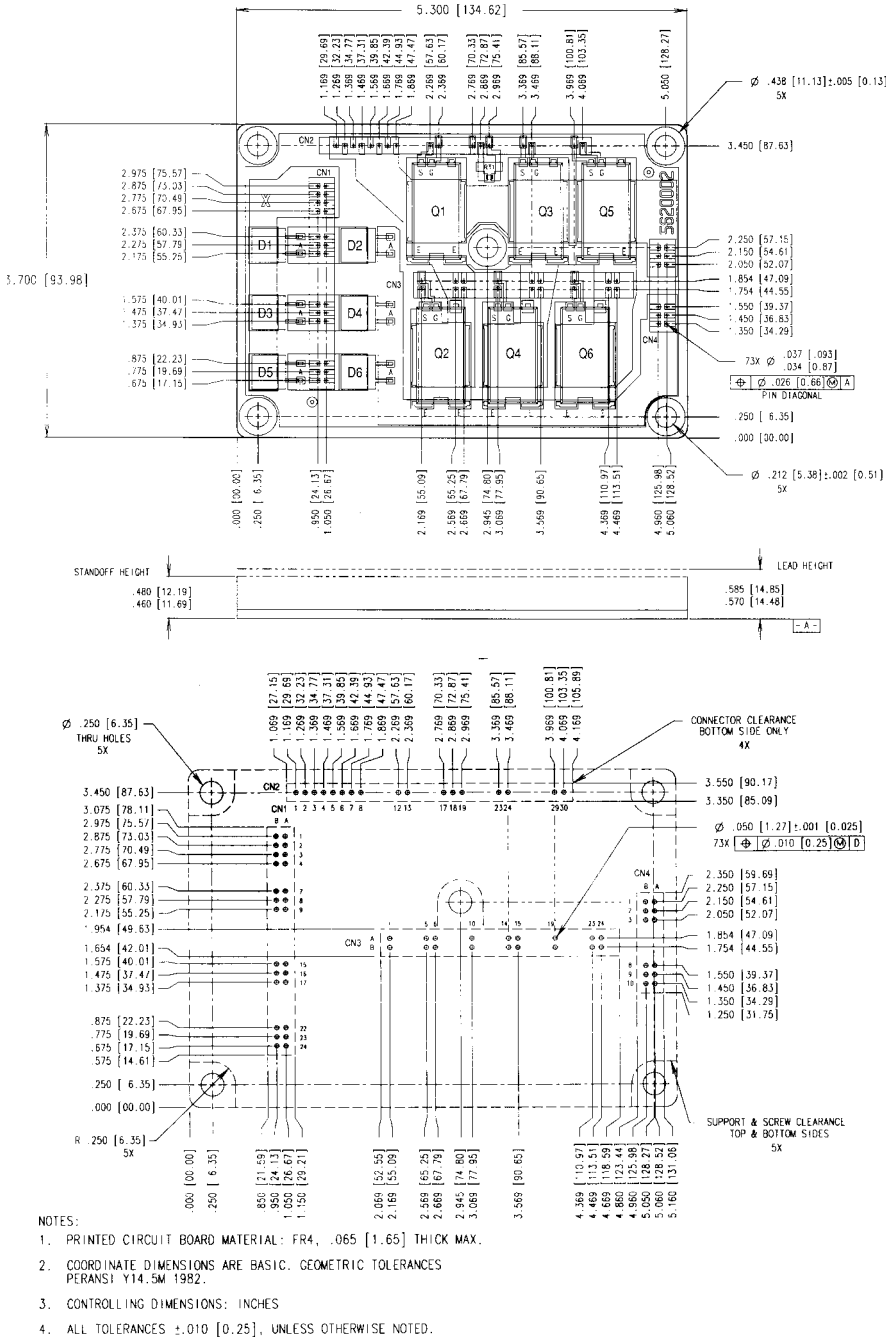
IRPT4052D Mechnical Specifications

NOTE: Dimensions are in inches (millimeters)



IRPT4052A Mechnical Specifications

NOTE: Dimensions are in inches (millimeters)



NOTES:

1. PRINTED CIRCUIT BOARD MATERIAL: FR4, .065 [1.65] THICK MAX.
2. COORDINATE DIMENSIONS ARE BASIC. GEOMETRIC TOLERANCES PERANSI Y14.5M 1982.
3. CONTROLLING DIMENSIONS: INCHES
4. ALL TOLERANCES ±.010 [0.25], UNLESS OTHERWISE NOTED.

Figure 8. Driver-*Plus* Board Hole Position and Sizes for Power Assembly

Part Number Identification and Ordering Instructions

IRPT4052A Power Assembly

IMS assembly incorporating 1600V SMD-220 input rectifiers, 1200V short circuit rated ultra-fast IGBT inverter with ultra-fast freewheeling diodes in SMD10 packages, along with a temperature sensing NTC thermistor.

IRPT4052C Complete POWIRTRAIN

Power Assembly (IRPT4052A) and Driver-*Plus* Board (IRPT4052D) pre-assembled and tested to meet all system specifications.

IRPT4052D Driver-*Plus* Board

Printed circuit board assembled with DC link capacitors, relay in-rush circuit, high power terminal blocks, surge suppression MOVs, IGBT gate drivers, protection circuitry and low power supply. The PCB is functionally tested with standard power assembly to meet all system specifications.

IRPT4052E Design Kit

Complete POWIRTRAIN (IRPT4052C) with full set of design documentation including schematic diagram, bill of material, mechanical layout, schematic file, Gerber files and design tips.

Functional Information

Capacitor Precharge

When the input line voltage is first switched on, the charging current of the DC bus capacitors is limited by a 100 Ohm pre-charge resistor. When the bus capacitor has charged to approximately 85% of the peak line voltage, the capacitor pre-charge control circuit energizes the relay K1, bypassing the 100ý pre-charge resistor, so long as the line voltage exceeds 300V rms and all three input phase voltages are present.

The relay feedback signal, K1FB is the voltage across the relay coil. This is 15V high when the relay is energized, and low when the relay is de-energized. At start-up, the input PWM signals should be inhibited externally until K1FB becomes high, since if the inverter is operated before the pre-charge resistor is bypassed, this resistor will be overloaded. The relay will drop out during operation if the DC bus voltage falls to less than 82% of the peak line voltage; if one or more input line voltages is lost; or if the input voltage falls below 300V. K1FB then becomes low and the PWM input signals should be inhibited externally to avoid overloading the pre-charge resistor.

The BUS RIPPLE feedback signal is high when the relay is de-energized, and low when it is energized. If one of the input phases is lost, the relay drops out and the BUS RIPPLE signal oscillates from high to low at line frequency.

The relay can be energized, if required, during single-phase operation by pulling down the SFT CHG terminal via an external open-collector transistor. The pull-down current is 2mA.

Discharging the Bus Capacitors

When the input power is switched off, the “top” bus capacitor is discharged by a 10k resistor.

The “lower” bus capacitor is discharged by a 10k resistor until its voltage reaches approximately 80V. Thereafter, discharge of the “lower” capacitor is via a 110k resistor.

Bootstrap Supplies for the Gate Drive Circuits

The gate drive circuits for the upper IGBTs are powered from floating bootstrap capacitors. Each bootstrap capacitor is charged via the corresponding lower IGBT when this is switched on. Prior to initial application of the PWM input signals at start-up, the bootstrap capacitors are uncharged. Thus, an upper IGBT will not be turned on until after the corresponding lower IGBT has first been turned on to charge the bootstrap capacitor for the upper IGBT. The minimum initial conduction period of each lower IGBT at start-up should be about 50µsec, to allow sufficient time for initial charging of the bootstrap capacitors. In normal operation, the bootstrap capacitor maintains adequate gate drive voltage for a period of 20 milliseconds. The maximum duration of the PWM input pulses (1N1, 1N3 and 1N5) should not exceed this period.

PWM Input Signals

PWM input signals must be 15V positive logic. They must source 10mA into the opto-isolators of the IGBT gate driver circuits. When inhibited by the internal PWM gate during power up, power down and fault conditions, each PWM input signal becomes loaded by a 720 Ohm resistor. Maximum rise and fall times of the PWM input signals should be 150 nsecs. Minimum dead time between outgoing and incoming PWM signals to the IGBTs in a given inverter leg should be 2.5µsecs. This is necessary to avoid inverter shoot-through. The minimum duration of any PWM input pulse should be 1µsec. Typical propagation delay between the PWM input and drive output at the gate of the IGBT is 300ns.

Undervoltage (Local Power Supply)

The undervoltage circuit monitors the voltage of the local gate driver power supply and sends a high input signal during undervoltage which sets the latch and inhibits the PWM input signals. This signal, brought out on pin 18 of CN5, is high during undervoltage. After it has gone low during power-up, a 15V RESET signal must be applied to reset the latch and allow the PWM input signals to pass to the gate drive circuits.

Overcurrent Trip

Peak line-to-line fault current in excess of a nominal value of 45A and peak line-to-ground current in excess of 40A sets the latch and internally inhibits the IGBT gate drive. The overcurrent feedback signal, OI, simultaneously goes high. Reaction time to a bolted short circuit is typically about 1µsec.

Overtemperature Trip

If the temperature of the IMS substrate exceeds a nominal value of 100°C, the overtemperature circuit sets the latch and internally inhibits the PWM input signals. The overtemperature feedback signal, OT, simultaneously goes high.

Latch Reset

The LED1 lights up when any of the fault signals (UV, OI, OT) set the latch, indicating a fault condition. When the RESET signal is applied to the latch, the LED1 goes OFF if the fault that is setting the latch clears.

The internal PWM inhibit condition is cleared by applying a 15V signal to the RESET terminal for a minimum period of 1 microsecond

Heat Sink Requirements

Figures 5a through 5d (pp. 6-7) show the thermal resistance of the heat sink required for various output power levels and PWM switching frequencies. Maximum total losses of the unit are also shown.

This data is based on the following key operating conditions:

- The maximum continuous combined losses of the rectifier and inverter occur at full pulse-width modulation. These maximum losses set the maximum continuous operating temperature of the heat sink.
- The maximum combined losses of the rectifier and inverter at full pulse-width modulation under overload set the incremental temperature rise of the heat sink during overload.
- The minimum output frequency at which full overload current is to be delivered sets the peak IGBT junction temperatures.

At low frequency IGBT junction temperature tends to follow the instantaneous fluctuations of the output current. Thus, peak junction temperature rise increases as output frequency decreases.

Voltage Rise During Braking

The motor will feed energy back to the DC link during electrical braking, forcing the DC bus voltage to rise above the level defined by the input line voltage.

Deceleration of the motor must be controlled by appropriate PWM control to keep the DC bus voltage within the rated maximum value. For high inertial loads or for very fast deceleration rates, this can be achieved by connecting an external dissipative circuit, which keeps the bus voltage within the rated value across the P and N. ❑

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