

ACS521MS

Radiation Hardened 8-Bit Magnitude Comparator

January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96709 and Intersil' QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose>300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10⁻¹⁰ Errors/Bit/Day
- SEU LET Threshold >100 MEV-cm²/mg
- Dose Rate Survivability.....>10¹² RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range 4.5V to 5.5V
- Input Logic Levels
 - VIL = 30% of VCC Max
 - VIH = 70% of VCC Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay 15ns (Max), 10ns (Typ)

Description

The Intersil ACS521MS is a Radiation Hardened 8 bit magnitude comparator device. It provides a low output YB when Word A equals word B and input GB is low. All other input states cause a high output.

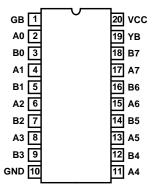
The ACS521MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

The ACS521MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

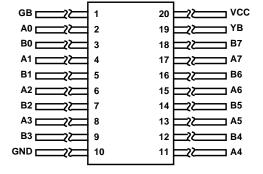
20 PIN CERAMIC DUAL-IN-LINE MIL-STD-1835 DESIGNATOR CDIP2-T20, **LEAD FINISH C**

TOP VIEW



20 PIN CERAMIC FLATPACK MIL-STD-1835 DESIGNATOR CDFP4-F20, **LEAD FINISH C**

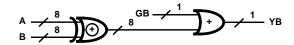
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9670901VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9670901VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACS521D/Sample	25°C	Sample	20 Lead SBDIP
ACS521K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACS521HMSR	25°C	Die	Die

Functional Diagram



TRUTH TABLE

	OUTPUT		
GB	Α	В	YB
0	Α =	L	
0	Α -	Н	
1	Х	Х	Н

NOTE: L = Low, H = High, X = Don't Care

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site http://www.intersil.com

Die Characteristics

DIE DIMENSIONS:

102mils x 102mils 2,600mm x 2,600mm

METALLIZATION:

Type: AlSi

Metal 1 Thickness: 7.125kÅ ±1.125kÅ

Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO₂

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

 $<2.0 \times 10^5 \text{ A/cm}^2$

BOND PAD SIZE:

> 4.3mils x 4.3mils > 110 μ m x 110 μ m

Metallization Mask Layout

