



Intel® IXP2400 Network Processor

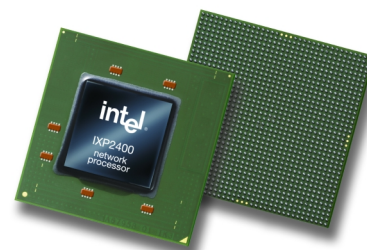
For OC-48/2.5 Gbps network access and edge applications

Product Highlights

- Eight fully programmable multi-threaded microengines for packet forwarding and traffic management on a single chip, supporting 5.4 giga-operations per second
- Introduces Hyper Task Chaining processing technology that enables deep packet inspection via software pipelining at 2.5 Gbps
- Integrated high-performance, low-power 32-bit Intel® XScale™ core for processing complex algorithms, route table maintenance, and system-level management functions
- Deep packet inspection: 14 million enqueue/dequeue packet operations per second, supporting packet processing of minimum 40-byte Packet over Sonet (PoS) packets
- Standards-based interfaces for easy integration
- Comprehensive development environment, including Software Development Kit, containing software tools, libraries and APIs and hardware development platform for rapid product development and prototyping
- Broad range of complementary technology from third-party software, silicon and board vendors for rapid time-to-market
- Low power consumption and small package size reduce system cost
- Intel® Internet Exchange Architecture (Intel® IXA) technology enables customers to reuse investments in Intel® network processors and software

Product Overview

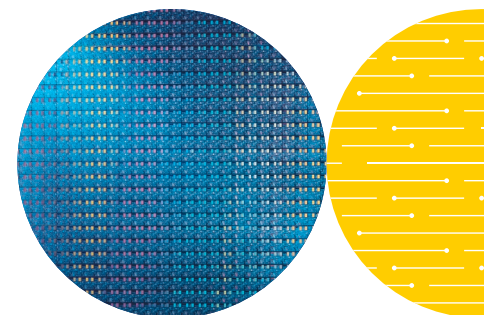
Equipment designed for network access and edge applications requires high levels of processing performance to support value-added network services at OC-48/2.5 Gbps line rates. While rapidly adding these new services, network equipment vendors must continue to minimize development time and cost. To support these requirements and to extend time-in-market, network processors must combine performance with highly flexible control of processing resources. In addition, implementation of standards-based interfaces for easy component integration and the ability to leverage software investments by reusing code can dramatically speed time-to-market and lower development costs.



The Intel® IXP2400 network processor is a member of Intel's second-generation network processor family. It is designed for a wide range of access and edge applications including multi-service switches, routers, broadband access devices, and wireless infrastructure systems. Based on the first-generation Intel® IXP1200 network processor, the IXP2400 is a fully programmable network processor that implements a high-performance parallel processing architecture on a single chip for processing complex algorithms, deep packet inspection, traffic management, and forwarding at wire speed. Its store-and-forward architecture combines a high-performance Intel XScale core with eight 32-bit independent multi-threaded microengines that cumulatively provide more than 5.4 giga-operations per second. The microengines provide the processing power to perform tasks that traditionally required expensive high-speed ASICs.

Intel's second-generation network processors are the first implementation of Intel's Hyper Task Chaining technology. This unique network processing approach allows a single stream packet/cell processing problem to be decomposed into multiple, sequential tasks that can be easily linked together. The hardware design uses fast and flexible sharing of data and event signals among threads and microengines to manage data-dependent operations among multiple parallel processing stages with low latency.

Intel in
Communications



Through this combination of flexible software pipelining and fast inter-process communication, Hyper Task Chaining delivers rich processing capability at OC-48/2.5 Gbps line rates.

The IXP2400 network processor delivers this enhanced performance with the programmability designed to speed the deployment of intelligent network services. A centerpiece of Intel IXA, Intel's second-generation network processor architecture scales to successive generations of networking products and is supported by a common set of development tools, libraries, and example designs. In combination, they provide the foundation for a comprehensive development environment that can dramatically accelerate time-to-market, while enabling customers to reuse their investments in software.

Application Flexibility

The ability of the IXP2400 network processor to support OC-48/2.5 Gbps line rates makes it ideal for a wide variety of high-performance applications such as Wide Area Networking (WAN) multi-service switches, DSLAMs (DSL access multiplexers), CMTS

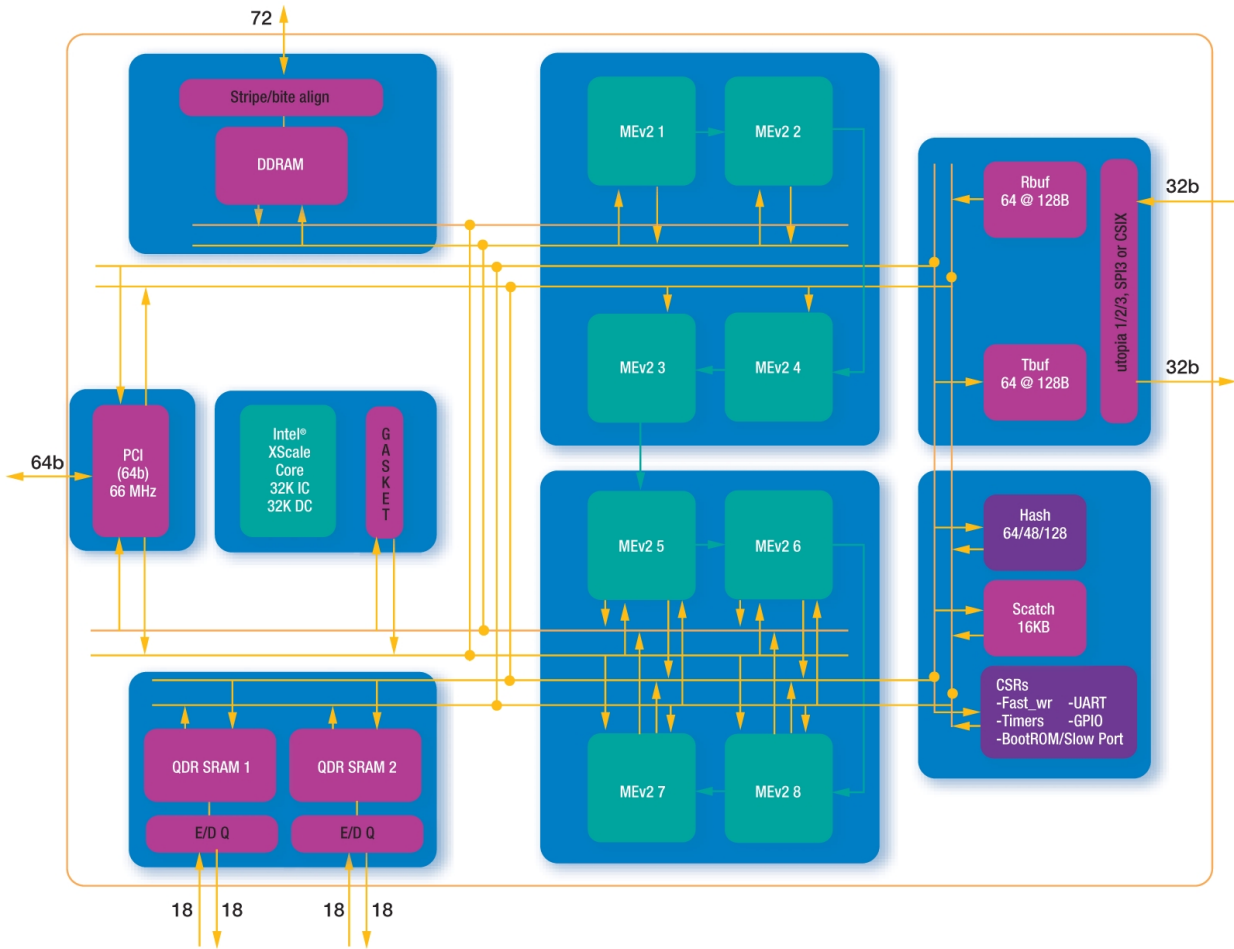
(cable modem termination system) equipment, 2.5G and 3G wireless infrastructure base station controllers and gateways, and Layer 4–7 switches including content-based load balancers, and firewalls. The programmability of the IXP2400 also makes it well suited for VoIP gateways, multi-service access platforms, high-end routers, remote access concentrators, and Virtual Private Network (VPN) gateways. Usage models for the IXP2400 in the target market segments listed above are as follows:

- Aggregation, ATM SARing, traffic shaping, policing, forwarding, and protocol conversion in DSLAM equipment
- Aggregation, forwarding, and protocol conversion in CMTS equipment
- ATM SARing, encryption, and forwarding in base station controllers/radio network controllers
- GTP Tunneling and IPv6 forwarding in wireless infrastructure
- ATM SARing, traffic shaping, policing, protocol conversion, and aggregation for multi-service switches
- Content-aware load balancing, forwarding, and policing

Features

Benefits

Eight integrated programmable microengines with 4K instruction program stores	Enhanced second-generation flexible multi-threaded RISC processors that can be programmed to deliver intelligent transmit and receive processing, with robust software development environment for rapid product development
Integrated Intel® XScale™ core <ul style="list-style-type: none"> —32 Kbyte—Instruction cache —32 Kbyte—Data cache —2 Kbyte—Mini-data cache 	Embedded 32-bit RISC core for high-performance processing of complex algorithms, route table maintenance, and system-level management functions. Lowers system cost and saves board space
Two unidirectional 32-bit media interfaces (Rx and Tx) programmable to be SPI-3, UTOPIA 1/2/3 or CSIX-L1. Each path is configured for 4x8 bit, 2x16 bit, 1x32 bit or combinations of 8 and 16 bit data paths	Supports industry-standard cell and packet interfaces to media and fabric devices delivering 4 Gbps performance rates that can support OC-48 plus fabric encapsulation overhead or 4xGbE; simplifies design and interface to custom ASIC devices
One industry-standard DDR DRAM interface	Memory subsystem supports the network processor store-and-forward processing model
Two industry-standard QDR SRAM interface	Memory subsystem for look-up tables and access lists, or coprocessors (such as CAM/TCAM, IPsec devices). NPF standardized interface for coprocessors
PCI 2.2 64-bit/66 MHz I/O interface	Supports industry-standard connection to system host processors
Asynchronous control interface supports 8-, 16-, 32-bit slow port devices	Provides control interface for connecting to maintenance port of PHY devices and flash memory
Hardware support for memory access queuing	Simplifies application development and reduces system cost
JTAG support	Improves hardware debug ability
Software Development Kit Hardware Development Platform	Improves time-to-market via robust hardware and software development tools
Additional integrated hardware features: <ul style="list-style-type: none"> —Hardware Hash Unit (48, 64, and 128 bit) —16-Kbyte Scratchpad Memory —Serial UART port for debug —Eight general-purpose I/O pins —Four 32-bit timers 	Simplifies development, reduces development cost, and saves board space



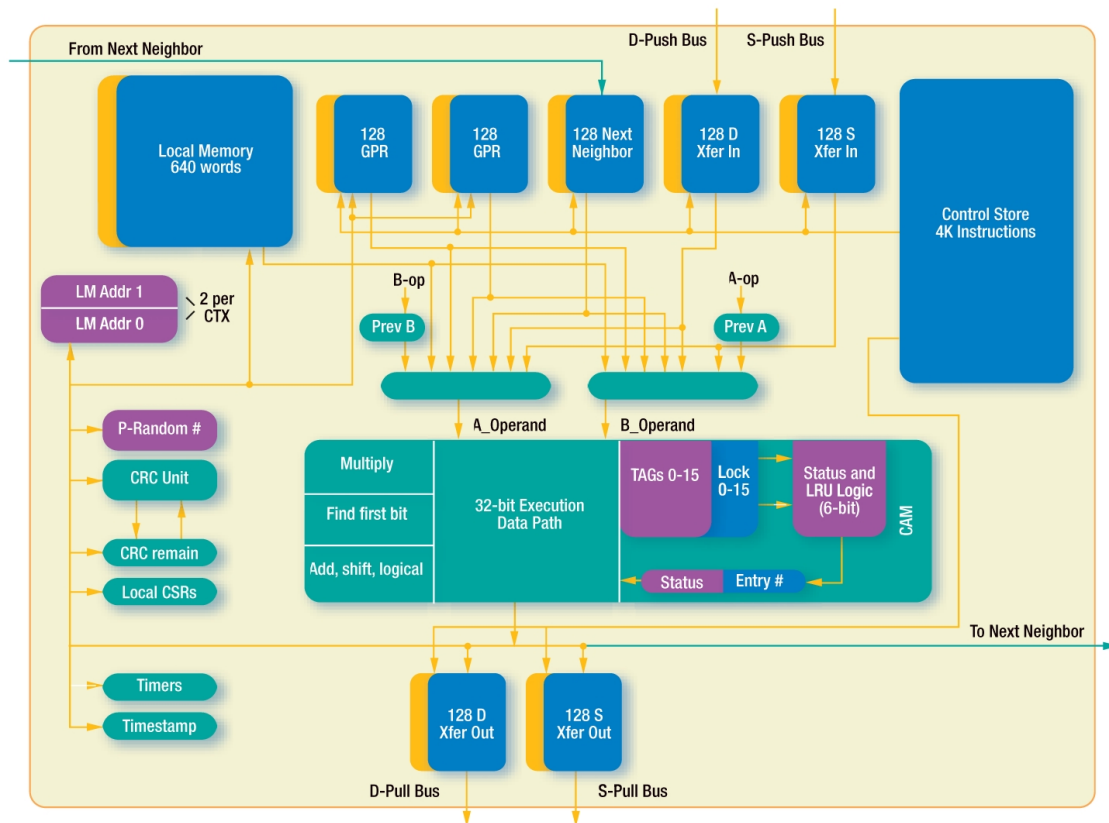
Intel® IXP2400 Network Processor Block Diagram

Hyper Task Chaining

Hyper Task Chaining implements several significant innovations to ensure low latency communication among processes. These mechanisms include Next Neighbor registers that enable individual microengines to rapidly pass data and state information to adjacent microengines. Reflector Mode pathways ensure that data and global event signals can be shared with multiple microengines, using 32-bit unidirectional buses that connect the IXP2400 network processor's internal processing and memory resources. A third enhancement, Ring Buffer registers, provides a highly efficient mechanism for flexibly linking tasks among multiple software pipelines. Ring buffers allow developers to establish "producer-consumer" relationships among microengines, efficiently propagating results along the pipeline in FIFO order. To minimize latency associated with external memory references, register structures are complemented by 16 entries of Content Addressable Memory (CAM) associated with each microengine. Configured as a distributed cache, the CAM enables multiple threads and microengines to manipulate related data simultaneously while maintaining data coherency.

Second-generation Hardware Enhancements

In addition to Hyper Task Chaining, the Intel IXP2400 also implements additional, hardware-assisted features to increase performance and simplify development. These enhancements provide flexible, easy-to-use mechanisms to support a variety of complex packet/cell processing requirements, freeing developers to focus upon implementing their own unique features. In addition to local memory to improve processing performance, the IXP2400 includes built-in resources for tasks such as ATM Segmentation and Reassembly; pseudo-random number generation for table lookups; time stamps to support flow metering; and a multiply function for complex algorithm calculations such as Quality of Service. In addition, the network processor automates packet manipulation for byte alignment to improve developer productivity and streamline code flows.



Microengine

Development Environment

Intel provides a comprehensive development environment that enables customers to rapidly develop applications for the Intel IXP2400 network processor and migrate existing applications from the Intel IXP1200 network processor family. The development environment includes the Intel® Internet Exchange Architecture Software Development Kit (Intel® IXA SDK) 3.0 complemented by a hardware development platform with supporting software and tools.

The Intel IXA SDK 3.0 enables hardware and software engineering to proceed in parallel. The SDK provides the software team with an easy-to-use graphical simulation environment for developing, debugging, and optimizing a network application at the same time that the hardware team is working on design and prototyping the device. By using the development tools, network building blocks and the Intel® IXA Portability Framework in the SDK, the design team can achieve an unparalleled time-to-market advantage.

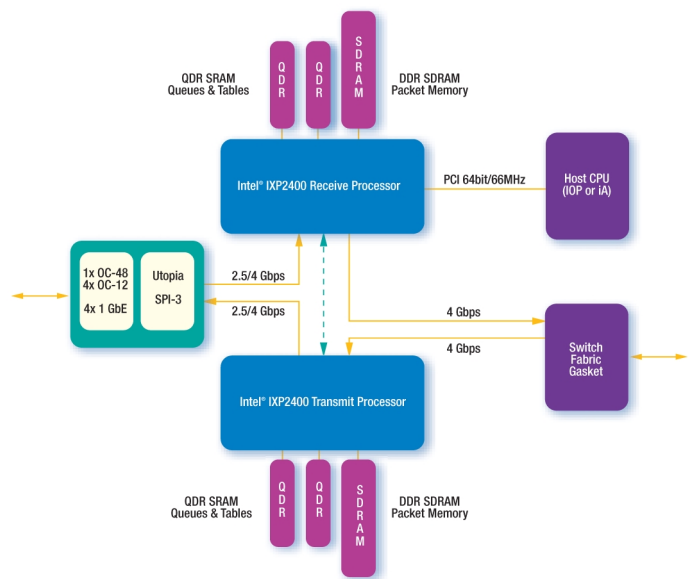
Intel IXA SDK 3.0 preserves investments in software for the IXP1200 network processor by maintaining the familiar best-in-class Developer's Workbench programming environment and extending it to support the IXP2400 and IXP2800 network processors. Developers who use the Intel® IXA SDK portable macro library, Intel® Microengine C compiler and the Intel® Microengine C Networking Library and the programming framework with the IXP1200 will be able to retarget their code for the IXP2400 and IXP2800 by using the same or similar facilities in SDK 3.0. The Microengine Development Environment (Workbench/Transactor) provides an integrated development environment (IDE) for advanced, graphical, cycle-accurate simulation, profiling, and debugging. It enables faster prototyping, intuitive optimization, and

fast time-to-market development of networking applications for the highly parallel, multi-threaded second-generation microengine architecture. The Transactor can be used to solve concurrency issues by simulating packets going into and out of the network processor, and it enables detailed visualization of processes and events within the network processor.

The Transactor identifies opportunities for code optimization by capturing history and statistics that show cycle-by-cycle interactions among the threads and memory units. The Transactor also includes a scripting engine for setting test configurations and creating test cases. Simulation tools include queue, memory, and thread histories which show memory and processor utilization, memory reference latencies, and queue depths.

The SDK provides high-level tools, embedded operating system support, the Intel IXA Software Portability Framework, software building blocks/libraries, and reference applications to enable customers to evaluate, demonstrate, tune performance, and develop applications for the network processor to meet product requirements.

The hardware development platform is comprised of an industry-standard form factor chassis, Intel IXP2400 base board, and a choice of modular media cards for maximum design flexibility. Complementary silicon and coprocessors will also be available from Intel or third parties. These components will be designed to work together to provide the flexibility, scalability, and performance levels required to meet the demands of tomorrow's high-performance networks.



Multiple LAN/WAN configurations with the IXP2400 network processor

This diagram highlights a number of different LAN and WAN design configurations that can be implemented with the Intel® IXP2400 network processor.

Description

Specification

Microengine operating frequency	600 MHz, 400 MHz 32-bit data path
Microengine program control stores	4K instructions (4K x 40 bit)
Receive interface (UTOPIA, SPI-3 or CSIX)	Completely independent from Tx path 32 data signals, two clocks, control and parity signals 3.3V LVTTTL signaling (single edge) w/global synch clocking Configurable for UTOPIA (1/2/3); SPI-3 (POS-PHY 2/3) or CSIX-L1B UT and SPI-3 modes enable combination of 16-bit and 8-bit channels 25–133 MHz operation
Transmit interface (UTOPIA, SPI-3 or CSIX)	Completely independent from Rx path 32 data signals, two clocks, control and parity signals 3.3V LVTTTL signaling (single edge) w/global synch clocking Configurable for UTOPIA (1/2/3); SPI-3 (POS-PHY 2/3) or CSIX-L1B UT and SPI-3 modes enable combination of 16-bit and 8-bit channels 25–133 MHz operation
Intel® XScale™ core operating frequency	600 MHz, 400 MHz
PCI interface	64-bit/66 MHz PCI 2.2 compliant
SRAM interface (QDR) Two Channels	Supports both QDR I and QDR II. Peak bandwidth of 1.6 Gbps per channel at frequency of 200 MHz (800 Mbytes/sec read, 800 Mbytes/sec write); up to 16 Mbytes per channel; parity protected
DDR DRAM One Channel	Peak bandwidth of 2.4 Gbytes (19.2 Gbps) per channel at frequency of 150 MHz and 100 MHz; up to 2 Gbytes memory; ECC protected; 64-bit wide interface
Operating temperature @ 600 MHz	0° to +70° C, -40° to +85° C ambient
Operating temperature @ 400-MHz Frequency	0° to +70° C, -40° to +85° C ambient
Power supply	Vdd=1.3V±5% (600 MHz), Vdd=1.1V±5% (400 MHz) Vdd1=1.5V±5% (QDR) Vdd2=2.5V±5% (DDR) Vdd3=3.3V±5% (Media, PCI)
Power dissipation	~13 Watts typical, ~16 Watts max @ 600 MHz operation ~9 Watts typical, ~12 Watts max @ 400 MHz operation
Package	1356 Ball FCBGA 37.5 mm x 37.5 mm
Solder ball pitch	1 mm

Intel® Internet Exchange Architecture (Intel® IXA)

Intel IXA is a packet processing architecture that provides a foundation for software portability across multiple generations of network processors. Intel IXA is based on programmable microengines, Intel XScale technology and the Intel IXA portability framework. Additional information on Intel IXA and the Intel network processor product line is available at the addresses listed below.

Intel Advantage

Intel is a leading supplier of communications building blocks, adding value at many levels of integration. Through continuous innovations and advancements in connectivity and processing in the network, Intel is delivering, along with its customers and developer community, a wide choice of solutions that enable faster time-to-market, longer time-in-market, and increased revenue opportunity.

Intel Access

Communications Processing Web page

<http://www.intel.com/go/commsprocessing>

Intel® Network Processors Web page

<http://developer.intel.com/design/network/products/npfamily/>

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