Data Sheet, DS 1, March 2001

Q-SMINT®O
2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** (**O**rdinary)
PEF 80912/80913 Version 1.3

Wired Communications

Infineon technologies

Never stop thinking.

Edition March 2001

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Q-SMINT®O
2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(O**rdinary)
PEF 80912/80913 Version 1.3

Wired
Communications

Never stop thinking.

Revision History: **March 2001** DS 1

Previous Version: Preliminary Data Sheet 10.00

Page	Subjects (major changes since last revision)
All	Editorial changes, addition of notes for clarification etc.
Table 1, **Chapter 1.3**	introduced new version 80913 with extended performance of the U-interface
Chapter 2.4.5.1	S-transceiver NT state machine: added note : 'By setting the Test Mode pins TM0-2 to '010' / '011': Continuous Pulses / Single Pulses, the S-transceiver starts sending the corresponding test signal, but no state transition is invoked.'
Chapter 2.4.5.1	C/I commands: removed 'unconditional command' from description C/I-command 'DR'
Figure 16	Corrected figure: 'Complete Activation Initiated by Exchange': info4 is sent by the NT (not byTE)
Chapter 4.1	Absolute Maximum Ratings: Maximum Voltage on VDD: 4.2V (before: 4.6V)
Chapter 4.1	Refined references for ESD requirements:' ...(CDM), EIA/JESD22-A114B (HBM) ---'
Chapter 4.2	Input/output leakage current set to 10µA (before: 1µA)
Table 19	U-transceiver characteristics: enhanced S/N+D for 80913 and threshold level for 80912 and 80913 distinguished
Chapter 4.6.3	Parameters of the UVD/POR Circuit: defined reduced range of hysteresis: min. 30mV/max. 90mV relaxed upper limit of Detection Threshold to 2.92V (before: 2.9V) defined max. rising VDD for power-on
Chapter 6.3	External circuitry for T-SMINT updated

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

Table of Contents **Page**

Table of Contents **Page**

List of Figures

List of Tables

Page

1 Overview

The **PEF 80912 / 80913** (Q-SMINT®O) offers all NT1 features known from the PEB / PEF 8091 [11] and can hence replace the latter in all NT1 applications.

Table 1 summarizes the 2nd generation NT products.

Table 1 NT Products of the 2nd Generation

	PEF80912	PEF80913	PEF81912	PEF81913	PEF82912	PEF82913
	Q-SMINT®O		Q-SMINT®IX		Q-SMINT®I	
Package	P-MQFP-44		P-MQFP-64 P-TQFP-64		P-MQFP-64 P-TQFP-64	
Register access	no		U+S+HDLC+ IOM®-2		U+S+ IOM®-2	
Access via	n.a.		parallel (or SCI or IOM®-2)		parallel (or SCI or IOM®-2)	
MCLK, watchdog timer, SDS, BCL, D-channel arbitration, IOM®-2 access and manipulation etc. provided	no		yes		yes	
HDLC controller	no		yes		no	
NT1 mode available	yes (only)		no		no	
Extended U-Performance 20kft	no	yes	no	yes	no	yes

1.1 References

[1] TS 102 080, Transmission and Multiplexing ; ISDN basic rate access; Digital transmission system on metallic local lines, ETSI, November 1998

[2] T1.601-1998 (Revision of ANSI T1.601-1992), ISDN-Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification), ANSI, 1998

[3] ST/LAA/ELR/DNP/822, CNET, France

[4] RC7355E, 2B1Q Generic Physical Layer Specification, British Telecommunications plc., 1997

[5] FZA TS 0095/01:1997-10, Technische Spezifikationen für Netzabschlußgeräte für den ISDN Basisanschluß (NT-BA), Post & Telekom Austria, 1997

[6] pr ETS 300 012 Draft, ISDN; Basic User Network Interface (UNI), ETSI, November 1996

[7] T1.605-1991, ISDN-Basic Access Interface for S and T Reference Points (Layer 1 Specification), ANSI, 1991

[8] I.430, ISDN User-Network Interfaces: Layer 1 Recommendations, ITU, November 1988

[9] IEC-Q, ISDN Echocancellation Circuit, PEB 2091 V4.3, User's Manual 02.95, Siemens AG, 1995

[10] SBCX, S/T Bus Interface Circuit Extended, PEB 2081 V3.4, User's Manual 11.96, Siemens AG, 1996

[11] NTC-Q, Network Termination Controller (2B1Q), PEB / PEF 8091 V1.1, Data Sheet 10.97, Siemens AG, 1997

[12] INTC-Q, Intelligent Network Termination Controller (2B1Q), PEB / PEF 8191 V1.1, Data Sheet 10.97, Siemens AG, 1997

[13] IOM®-2 Interface Reference Guide, Siemens AG, 03.91

[14] SCOUT-S(X), Siemens Codec with S/T-Transceiver, PSB 2138x V1.3, Preliminary Data Sheet 8.99, Infineon Technologies, 1999

[15] PITA, PCI Interface for Telephony/Data Applications V0.3, SICAN GmbH, September 1997

[16] Dual Channel SLICOFI-2, HV-SLIC; DUSLIC; PEB3265, 4265, 4266; Data Sheet DS2, Infineon Technologies, July 2000.

2B1Q Second Gen. Modular ISDN NT (Ordinary) Q-SMINT®O

PEF 80912/80913

Version 1.3

1.2 Features PEF 80912

P-MQFT-44

Features known from the PEB / PEF 8091

- Single chip solution including U- and S-transceiver
- Perfectly suited for the NT1 in the ISDN
- Fully automatic activation and deactivation
- U-interface (2B1Q) conform to ETSI [1], ANSI [2] and CNET [3]:
  - Meets all transmission requirements on all ETSI, ANSI and CNET loops with margin
  - Conform to British Telecom's RC7355E [4]
  - Compliant with ETSI 10 ms micro interruptions
  - MLT input and decode logic (ANSI [2])
- S/T-interface conform to ETSI [6], ANSI [7] and ITU [8]
  - Supports point-to-point and bus configurations
  - Meets and exceeds all transmission requirements
- Pin programmable CSO-bit
- Optional IOM®-2 interface eases chip testing and evaluation
- Activation status LED supported

Type	Package
PEF 80912/80913	P-MQFT-44

New Features

- Reduced number of external components for external U-hybrid required
- Optional use of up to 2x20Ω resistors on the line side of the transformer (e.g. PTCs)
- Pin Uref and the according external capacitor removed
- Improved ESD (2 kV instead of <850 V)
- Inputs accept 3.3 V and 5 V
- I/O (open drain) accepts pull-up to 3.3 V[1)]
- Pin compatible with T-SMINT®O (2nd Generation)
- LED indicates Loopback 2 (LBBD)
- Power-on reset and Undervoltage Detection with no external components
- Lowest power consumption due to
  - Low power CMOS technology (0.35µ)
  - Newly optimized low power libraries
  - High output swing on U- and S-line interface leads to minimized power consumption
  - Single 3.3 Volt power supply
- 200 mW (NTC-Q: 285 mW) power consumption with random data over ETSI Loop 2.
- 15 mW typical power consumption in power down (NTC-Q: 28 mW)

1.3 Features PEF 80913

The Q-SMINT®O PEF 80913 provides all features of the PEF 80912. Additionally, a significantly enhanced performance of the U-interface as compared to ETSI [1], ANSI [2] and CNET [3] requirements is guaranteed:
Transparent transmission on 20kft AWG26 with a BER < 10^{-7} (without noise).

1) Pull-ups to 5 V must be avoided. A so-called 'hot-electron-effect' would lead to long term degradation.

1.4 Not Supported are ...

- Integrated U-hybrid
- 'NT-Star' with star point on the IOM®-2 bus (already not supported in NTC-Q).
- The oscillator architecture was changed with respect to the NTC-Q to reduce power consumption. As a consequence, the Q-SMINT®O always needs a crystal and pin XIN can not be connected to an external clock as it was possible for IEC-Q and NTC-Q. This does not limit the use of the Q-SMINT®O in NTs since all NT designs use crystals anyway.

1.5 Pin Configuration

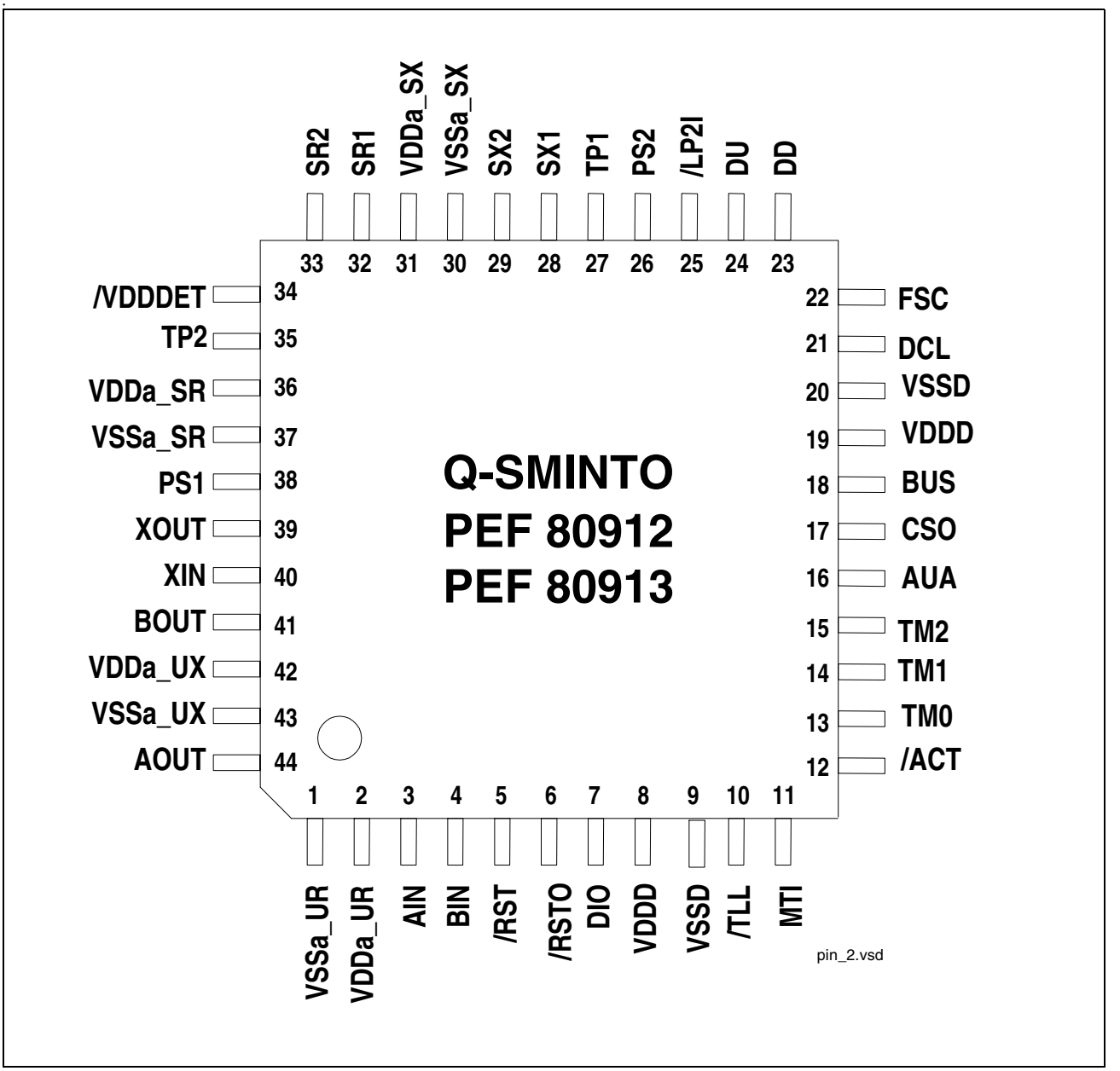


Figure 1 Pin Configuration

1.6 Block Diagram

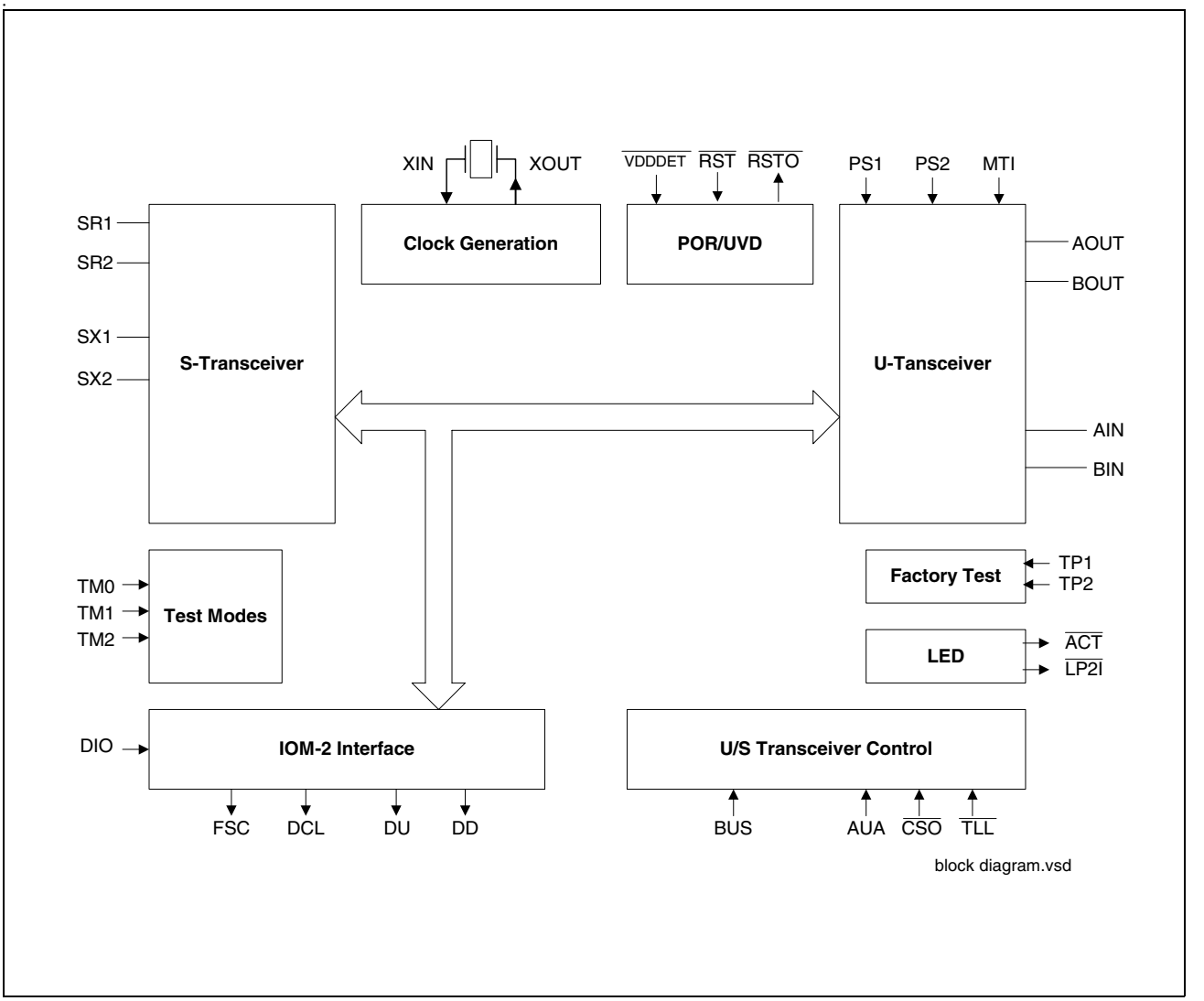


Figure 2 Block Diagram

1.7 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

Pin		Symbol	Type	Function
2		VDDa_UR	–	Supply voltage for U-Receiver (3.3 V ± 5 %)
1		VSSa_UR	–	Analog ground (0 V) U-Receiver
42		VDDa_UX	–	Supply voltage for U-Transmitter (3.3 V ± 5 %)
43		VSSa_UX	–	Analog ground (0 V) U-Transmitter
36		VDDa_SR	–	Supply voltage for S-Receiver (3.3 V ± 5 %)
37		VSSa_SR	–	Analog ground (0 V) S-Receiver
31		VDDa_SX	–	Supply voltage for S-Transmitter (3.3 V ± 5 %)
30		VSSa_SX	–	Analog ground (0 V) S-Transmitter
19		VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
20		VSSD	–	Ground (0 V) digital circuits
8		VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
9		VSSD	–	Ground (0 V) digital circuits
22		FSC	O	**Frame Sync:** 8-kHz frame synchronization signal
21		DCL	O	**Data Clock:** IOM®-2 interface clock signal (double clock): 512 kHz
25		$\overline{\text{LP2I}}$	O	**Loopback 2 indication:** Can directly drive a LED (4 mA). 0: LBBD received, Loopback 2 closed 1: Loopback 2 not closed.
23		DD	O	**Data Downstream:** Data on the IOM®-2 interface
24		DU	O	**Data Upstream:** Data on the IOM®-2 interface

Table 2 Pin Definitions and Functions (cont'd)

Pin		Symbol	Type	Function
7		DIO	I	**Disable IOM®-2:** 1: FSC, DCL, DU and DD high Z 0: FSC, DCL, DU and DD push-pull
16		AUA	I	**Auto U Activation:** 1: U-transceiver attempts one automatic activation after reset. Tie to '0' in applications that do not require auto-start after reset.
17		CSO	I	**Cold Start Only:** '1' selects CSO-bit to '0'. (normal) '0' selects CSO-bit to '1'. (special cases) The pin only controls the CSO-bit in the U-frame. The U-transceiver itself is always a warm-start transceiver according to ANSI and ETSI.
18		BUS	I (PU)	**Bus mode on S-interface:** 1: passive S-bus (fixed timing) 0: point-to-point / extended passive S-bus (adaptive timing)
5		$\overline{\text{RST}}$	I	**Reset:** Low active reset input. Schmitt-Trigger input with hysteresis of typical 360 mV. Tie to '1' if not used.
6		$\overline{\text{RSTO}}$	OD	**Reset Output:** Low active reset output.
10		$\overline{\text{TLL}}$	I	**Triple-Last-Look** Select validation algorithm for received M4 bit towards state machine: '0': CRC & TLL '1': CRC
13		TM0	I	**Test Mode 0** Selects test pattern (see **Page 11**).
14		TM1	I	**Test Mode 1** Selects test pattern (see **Page 11**).
15		TM2	I	**Test Mode 2** Selects test pattern (see **Page 11**).

Table 2 Pin Definitions and Functions (cont'd)

Pin		Symbol	Type	Function
28		SX1	O	**S-Bus Transmitter Output (**positive**)**
29		SX2	O	**S-Bus Transmitter Output (**negative**)**
32		SR1	I	**S-Bus Receiver Input**
33		SR2	I	**S-Bus Receiver Input**
40		XIN	I	**Crystal 1:** Connected to a 15.36 MHz crystal
39		XOUT	O	**Crystal 2:** Connected to a 15.36 MHz crystal
44		AOUT	O	**Differential U-interface Output**
41		BOUT	O	**Differential U-interface Output**
3		AIN	I	**Differential U-interface Input**
4		BIN	I	**Differential U-interface Input**
34		$\overline{\text{VDDDET}}$	I	**VDD Detection:** This pin selects if the V_{DD} detection is active ('0') and reset pulses are generated on pin $\overline{\text{RSTO}}$ or whether it is deactivated ('1') and an external reset has to be applied on pin $\overline{\text{RST}}$.
11		MTI	I	**Metallic Termination Input.** Input to evaluate Metallic Termination pulses. Tie to '1' if not used.
38		PS1	I	**Power Status (primary).** The pin status is passed to the overhead bit 'PS1' in the U frame to indicate the status of the primary power supply ('1' = ok).
26		PS2	I	**Power Status (secondary).** The pin status is passed to the overhead bit 'PS2' in the U frame to indicate the status of the secondary power supply ('1' = ok).

Table 2 Pin Definitions and Functions (cont'd)

Pin		Symbol	Type	Function
12		$\overline{\text{ACT}}$	O	**Activation LED.** Indicates the activation status of U- and S-transceiver. Can directly drive a LED (4 mA).
27		TP1	I	**Test Pin 1.** Used for factory device test. Tie to V_{SS}
35		TP2	I	**Test Pin 2.** Used for factory device test. Tie to V_{SS}

PU: Internal pull-up resistor (typ. 100 µA)

I: Input

O: Output (Push-Pull)

OD: Output (Open Drain)

1.7.1 Specific Pins

LED Pins $\overline{\text{ACT}}$, $\overline{\text{LP2I}}$

A LED can be connected to pin **$\overline{\text{ACT}}$** to display four different states (off, slow flashing, fast flashing, on). It displays the activation status of the U- and S-transceiver according to **Table 3**.

with:

Table 3 ACT States

Pin $\overline{\text{ACT}}$	LED	U_Deactivated	U_Activated	S_Activated
V_{DD}	off	1	x	x
8Hz	8Hz	0	0	x
1Hz	1Hz	0	1	0
GND	on	0	1	1

U_Deactivated: 'Deactivated State' as defined in **Chapter 2.3.5.5**.

U_Activated: 'Synchronized 1', 'Synchronized 2', 'Wait for ACT', 'Transparent', 'Error S/T', 'Pend. Deact. S/T', 'Pend. Deact. U' as defined in **Chapter 2.3.5.5**.

S-Activated: 'Activated State' as defined in **Chapter 2.4.5**.

Note: Optionally, pin $\overline{ACT}$ can drive a second LED with inverse polarity (connect this additional LED to 3.3 V only).

Another LED can be connected to pin **$\overline{LP2I}$** to indicate an active Loopback 2 according to **Table 4**.

Table 4 LP2I States

Pin $\overline{LP2I}$	LED	EOC-Command LBBD
V_{DD}	off	received no EOC-LBBD or received RTN after an LBBD command.
GND	on	EOC-command LBBD (50) has been received. Complete analog loop is being closed on the S-interface.

Test Modes

Different test patterns on the U- and S-interface can be generated via pins TM0-2 according to **Table 5**.

Table 5 Test Modes

TM0	TM1	TM2	U-transceiver	S-transceiver
0	0	0	Reserved for future use. Normal operation in this version.	
0	0	1		
0	1	0	Normal operation	96 kHz[1] Continuous Pulses
0	1	1		2 kHz[2] Single Pulses
1	0	0	Data Through[3]	Normal operation
1	0	1	Send Single Pulses[4]	
1	1	0	Quiet Mode[5]	
1	1	1	normal operation	

1) The S-transceiver transmits pulses with alternating polarity at a rate of 192 kHz resulting in a 96 kHz envelope.

2) The S-transceiver transmits pulses with alternating polarity at a rate of 4 kHz resulting in a 2 kHz envelope.

3) Forces the U-transceiver into the state 'Transparent' where it transmits signal SN3T.

4) Forces the U-transceiver to go into state 'Test' and to send single pulses. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs.

5) The U-transceiver is hardware reset.

1.8 System Integration

The Q-SMINT®O provides NT1 functionality without a microcontroller being necessary. Special selections can be done via pin strapping (CSO, $\overline{TLL}$, BUS, etc.). The device has no µP interface.

The IOM®-2 Interface serves only for monitoring and debugging purposes. It can be regarded as a window to the internal IOM®-2.

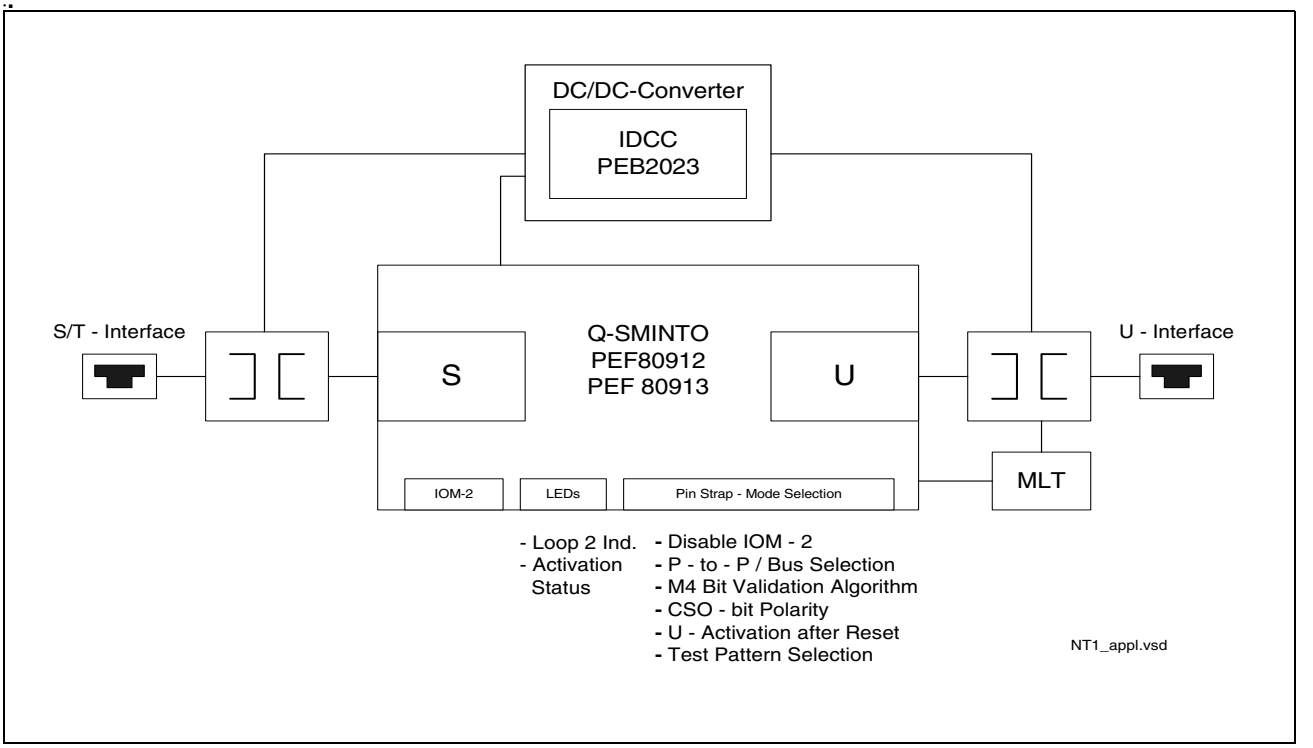


Figure 3 Application Example Q-SMINT®O: Standard NT1

2 Functional Description

2.1 Reset Generation

External Reset Input

At the $\overline{RST}$ input an external reset can be applied forcing the Q-SMINT®O in the reset state. This external reset signal is additionally fed to the $\overline{RSTO}$ output.

Reset Ouput

If $\overline{VDDDET}$ is active, then the deactivation of a reset output on $\overline{RSTO}$ is delayed by t_{DEACT} (see **Table 22**).

Reset Generation

The Q-SMINT®O has an on-chip reset generator based on a Power-On Reset (POR) and Under Voltage Detection (UVD) circuit (see **Table 22**). The POR/UVD requires no external components.

The POR/UVD circuit can be disabled via pin $\overline{VDDDET}$.

The requirements on V_{DD} ramp-up during power-on reset are described in **Chapter 4.6.3**.

Clocks and Data Lines During Reset

During reset the data clock (DCL) and the frame synchronization (FSC) keep running.

During reset DD and DU are high; with the exception of:

- The output C/I code from the U-Transceiver on DD is 'DR' = 0000
- The output C/I code from the S-Transceiver on DU is 'TIM' = 0000.

2.2 IOM®-2 Interface

The IOM®-2 interface always operates in NT mode according to the IOM®-2 Reference Guide [13].

2.2.1 IOM®-2 Functional Description

The IOM®-2 interface consists of four lines: FSC, DCL, DD, DU. The rising edge of FSC indicates the start of an IOM®-2 frame. The DCL clock signal synchronizes the data transfer on both data lines DU and DD. The DCL is twice the bit rate. The bits are shifted out with the rising edge of the first DCL clock cycle.

Note: It is not possible to write any data via IOM®-2 into the Q-SMINT®O.

The IOM®-2 interface can be enabled/disabled with pin DIO.

The FSC signal is an 8 kHz frame sync signal. The number of PCM timeslots on the transmit line is determined by the frequency of the DCL clock, with the 512 kHz clock 1 channel consisting of 4 timeslots is available.

IOM®-2 Frame Structure of the Q-SMINT®O

The frame structure on the IOM®-2 data ports (DU,DD) of the Q-SMINT®O with a DCL clock of 512 kHz is shown in **Figure 4**.

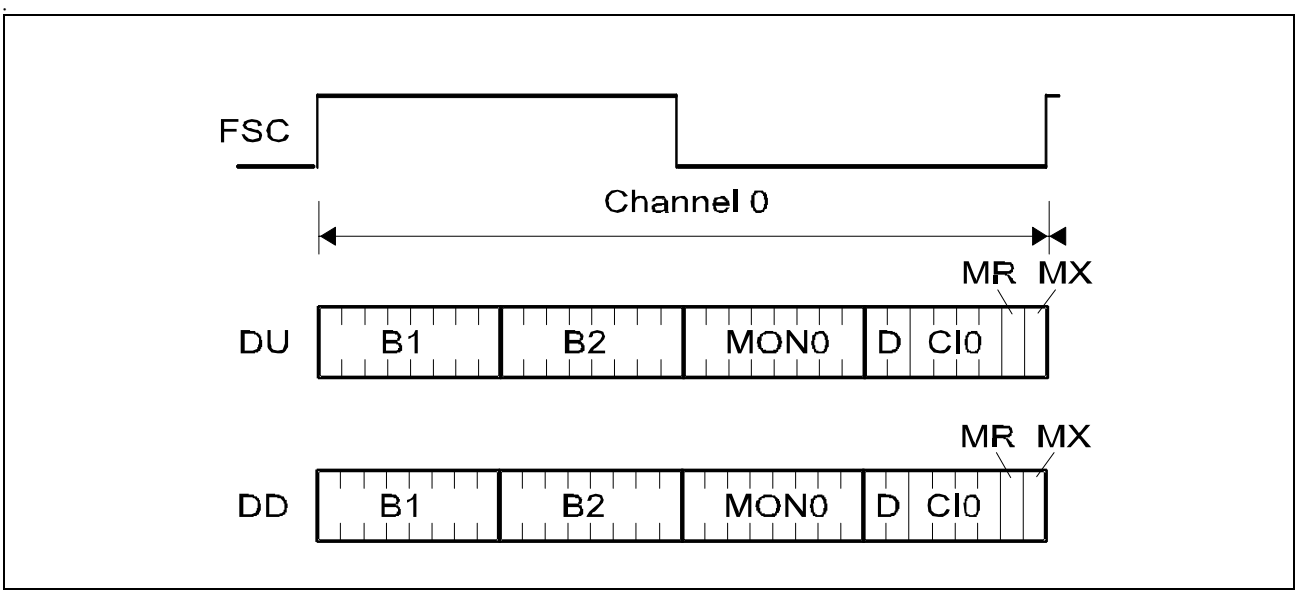


Figure 4 IOM®-2 Frame Structure of the Q-SMINT®O

The frame is composed of one channel:

Channel 0 contains 144-kbit/s of user and signaling data (2B + D), a MONITOR programming channel (not available in Q-SMINT®O) and a command/indication channel (CI0) for control of e.g. the U-transceiver.

2.3 U-Transceiver

The state machine of the U-Transceiver is based on the NT state machine in the PEB / PEF 8091 documentation [11].

Basic configurations are selected via pin strapping.

2.3.1 2B1Q Frame Structure

Transmission on the U_{2B1Q}-interface is performed at a rate of 80 kbaud. The code used is reducing two bits to one quaternary symbol (2B1Q).

Data is grouped together into U-superframes of 12 ms each. Each superframe consists of eight basic frames which begin with a synchronization word and contain 222 bits of information. The first basic frame of a superframe starts with an inverted synchword (ISW) compared to the other basic frames (SW). The structure of one U-superframe is illustrated in **Figure 5** and **Figure 6**.

ISW	1. Basic Frame	SW	2. Basic Frame	. . .	SW	8. Basic Frame
<---12 ms--->						

Figure 5 U-Superframe Structure

(I) SW (Inverted) Synch Word 18 Bit (9 Quat)	12 × 2B + D User Data 216 Bits (108 Quat)	M1 – M6 Maintenance Data 6 Bits (3 Quat)
<---1,5 ms--->		

Figure 6 U-Basic Frame Structure

Out of the 222 information bits 216 contain 2B + D data from 12 IOM®-frames, the remaining 6 bits are used to transmit maintenance information. Thus 48 maintenance bits are available per U-superframe. They are used to transmit two EOC-messages (24 bit), 12 Maintenance (overhead) bits and one checksum (12 bit).

Table 6 U-Superframe Format

		Fram-ing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118 s	118 m	119 s	119 m	120 s	120 m
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOC a1	EOC a2	EOC a3	ACT/ ACT	1	1
	2	SW	2B + D	EOC dm	EOC i1	EOC i2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOC i3	EOC i4	EOC i5	SCO/ PS2	CRC1	CRC2
	4	SW	2B + D	EOC i6	EOC i7	EOC i8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOC a1	EOC a2	EOC a3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOC dm	EOC i1	EOC i2	1	CRC7	CRC8
	7	SW	2B + D	EOC i3	EOC i4	EOC i5	UOA / SAI	CRC9	CRC 10
	8	SW	2B + D	EOC i6	EOC i7	EOC i8	AIB / NIB	CRC 11	CRC 12
2,3…									
						LT- to NT dir. >	/	< NT- to LT dir.	

– ISW Inverted Synchronization Word (quad): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quad): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel
  a = address bit
  d/m = data / message bit
  i = information (data / message)
– ACT Activation bit
  ACT = (1) –> Layer 2 ready for communication

–	DEA	Deactivation bit	DEA = (0) –> LT informs NT that it will turn off
–	CSO	Cold Start Only	CSO = (1) –> NT-activation with cold start only
–	UOA	U-Only Activation	UOA = (0) –> U-only activated
–	SAI	S-Activity Indicator	SAI = (0) –> S-interface is deactivated
–	FEBE	Far-end Block Error	FEBE = (0) –> Far-end block error occurred
–	PS1	Power Status Primary Source	PS1 = (1) –> Primary power supply ok
–	PS2	Power Status Secondary Source	PS2 = (1) –> Secondary power supply ok
–	NTM	NT-Test Mode	NTM = (0) –> NT busy in test mode
–	AIB	Alarm Indication Bit	AIB = (0) –> Interruption (according to ANSI)
–	NIB	Network Indication Bit	NIB = (1) –> no function (reserved for network use)
–	SCO	Start on Command only bit	
–	1	(currently not defined by ANSI/ETSI)	

can be accessed by the system interface for proprietary use

The principle signal flow is depicted in **Figure 7** and **Figure 8**. The data is first grouped in bits that are covered by the CRC and bits that are not. After the CRC generation the bits are arranged in the proper sequence according to the 2B1Q frame format, encoded and finally transmitted.

In receive direction the data is first decoded, descrambled, deframed and handed over for further processing.

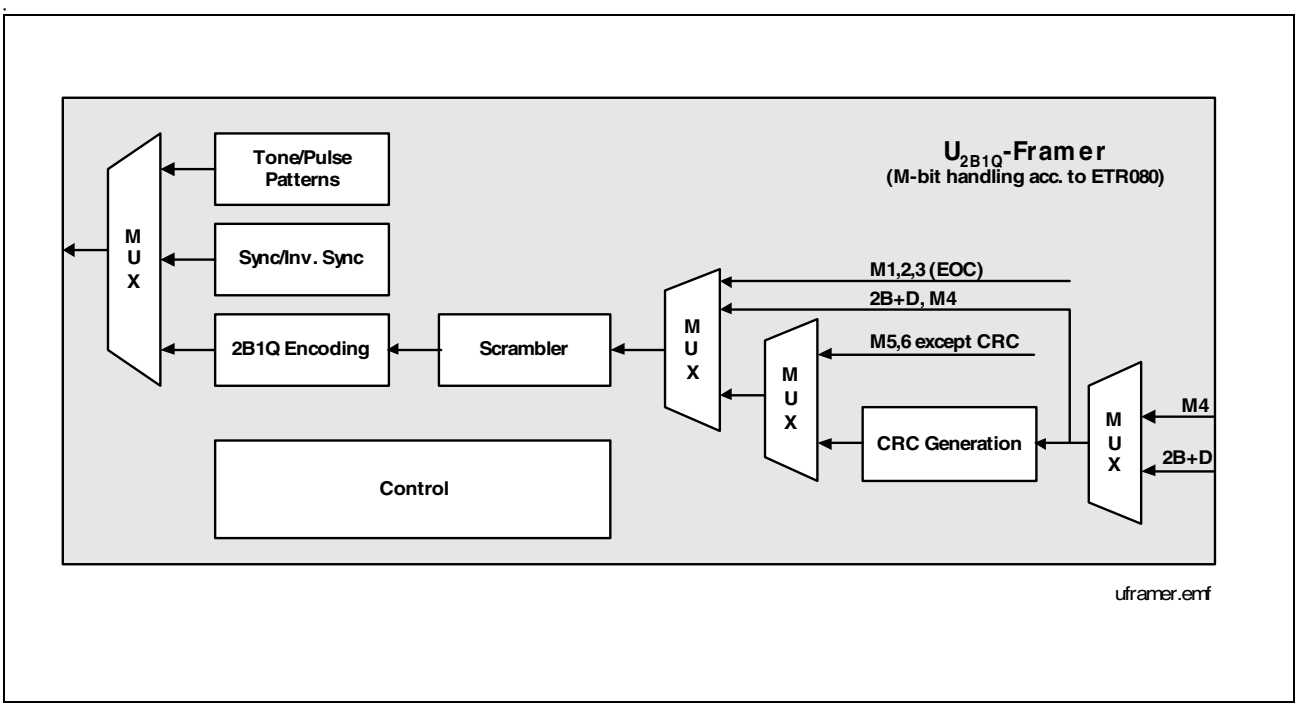


Figure 7 U_{2B1Q} Framer - Data Flow Scheme

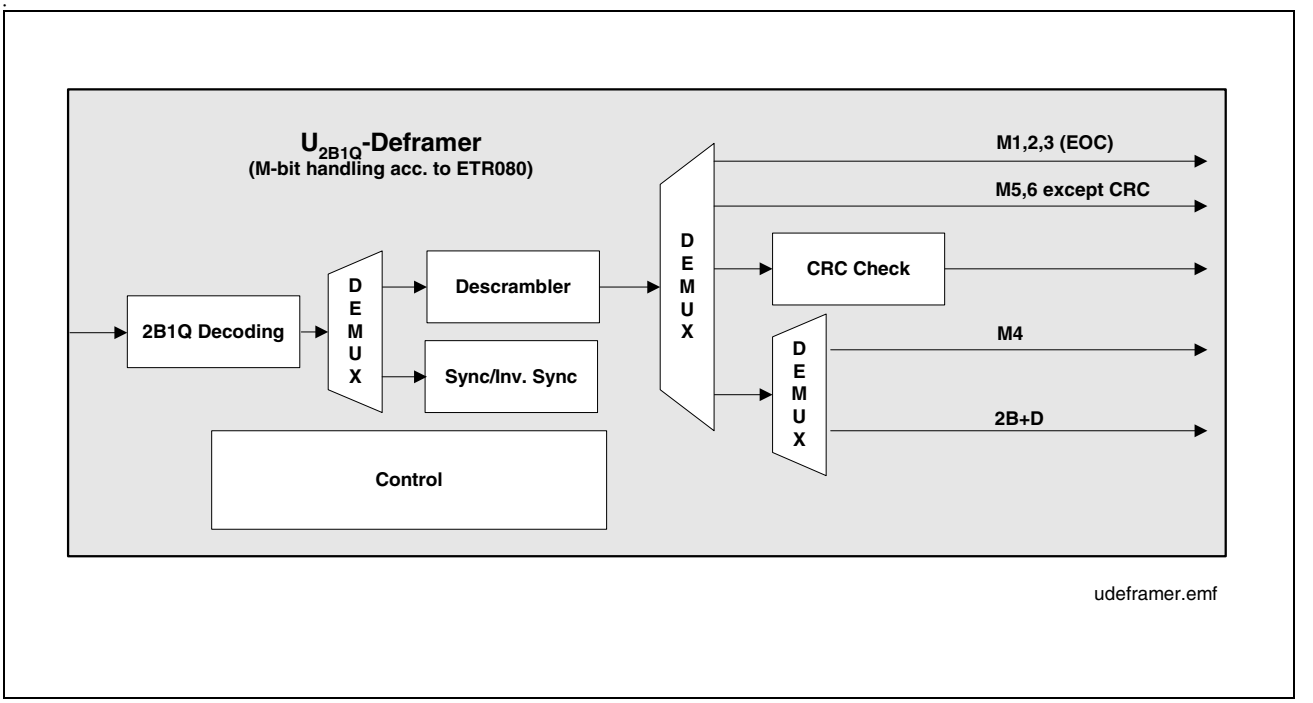


Figure 8 U_{2B1Q} Deframer - Data Flow Scheme

2.3.2 Cyclic Redundancy Check / FEBE bit

An error monitoring function is implemented covering the 2B + D and M4 data transmission of a U-superframe by a Cyclic Redundancy Check (CRC).

The computed polynomial is:

$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The check digits (CRC bits CRC1, CRC2, …, CRC12) generated are transmitted in the U-superframe. The receiver will compute the CRC of the received 2B + D and M4 data and compare it with the received CRC-bits generated by the transmitter.

A CRC-error will be indicated to both sides of the U-interface, as a NEBE (Near-end Block Error) on the side where the error is detected, as a FEBE (Far-end Block Error) on the remote side. The FEBE-bit will be placed in the next available U-superframe transmitted to the originator.

2.3.3 Scrambling/ Descrambling

The scrambling algorithm ensures that no sequences of permanent binary 0s or 1s are transmitted. The scrambling / descrambling process is controlled fully by the Q-SMINT®O. Hence, no influence can be taken by the user.

2.3.4 C/I Codes

The operational status of the U-transceiver is controlled by the Control/Indicate channel (C/I-channel).

Table 7 presents all defined C/I codes.

An indication is issued permanently by the U-transceiver on DD until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify every state individually.

Table 7 U - Transceiver C/I Codes

Code	IN	OUT
0000	TIM	DR
0001	RES	–
0010	–	–
0011	–	–
0100	EI1	EI1
0101	SSP	–
0110	DT	–
0111	–	PU
1000	AR	AR
1001	–	–
1010	ARL	ARL
1011	–	–
1100	AI	AI
1101	–	–
1110	–	AIL
1111	DI	DC

AI: Activation Indication

AIL: Activation Indication Loop

AR: Activation Request

ARL: Activation Request Local Loop

DC: Deactivation Confirmation

DI: Deactivation Indication

DR: Deactivation Request

DT: Data Through test mode

EI1: Error Indication 1

PU: Power-Up

RES: Reset

SSP: Send Single Pulses test mode

TIM: Timing request

2.3.5 State Machine for Line Activation / Deactivation

2.3.5.1 Notation

The state machines control the sequence of signals at the U-interface that are generated during the start-up procedure. The informations contained in the following state diagrams are:

– State name
– U-signal transmitted
– Overhead bits transmitted
– C/I-code transmitted
– Transition criteria
– Timers

Figure 9 shows how to interpret the state diagrams.

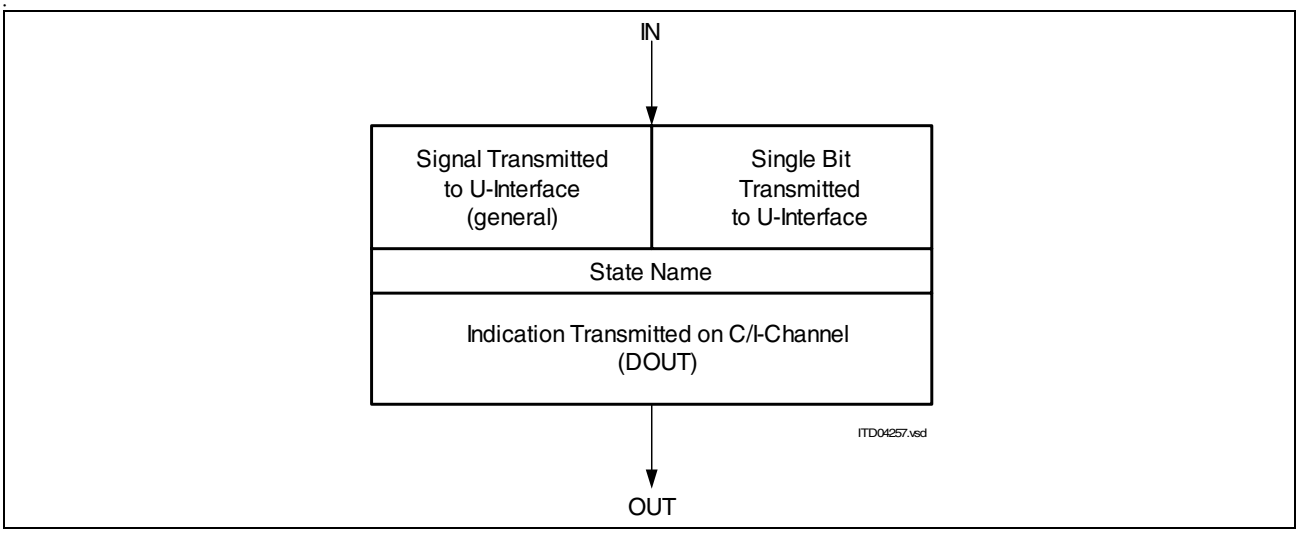


Figure 9 Explanation of State Diagram Notation

Combinations of transition criteria are possible. Logical “AND” is indicated by “&” (TN & DC), logical “OR” is written “or” and for a negation “/” is used. The start of a timer is indicated with “TxS” (“x” being equivalent to the timer number). Timers are always started when entering the new state. The action resulting after a timer has expired is indicated by the path labelled “TxE”.

2.3.5.2 Standard NT State Machine (IEC-Q / NTC-Q Compatible)

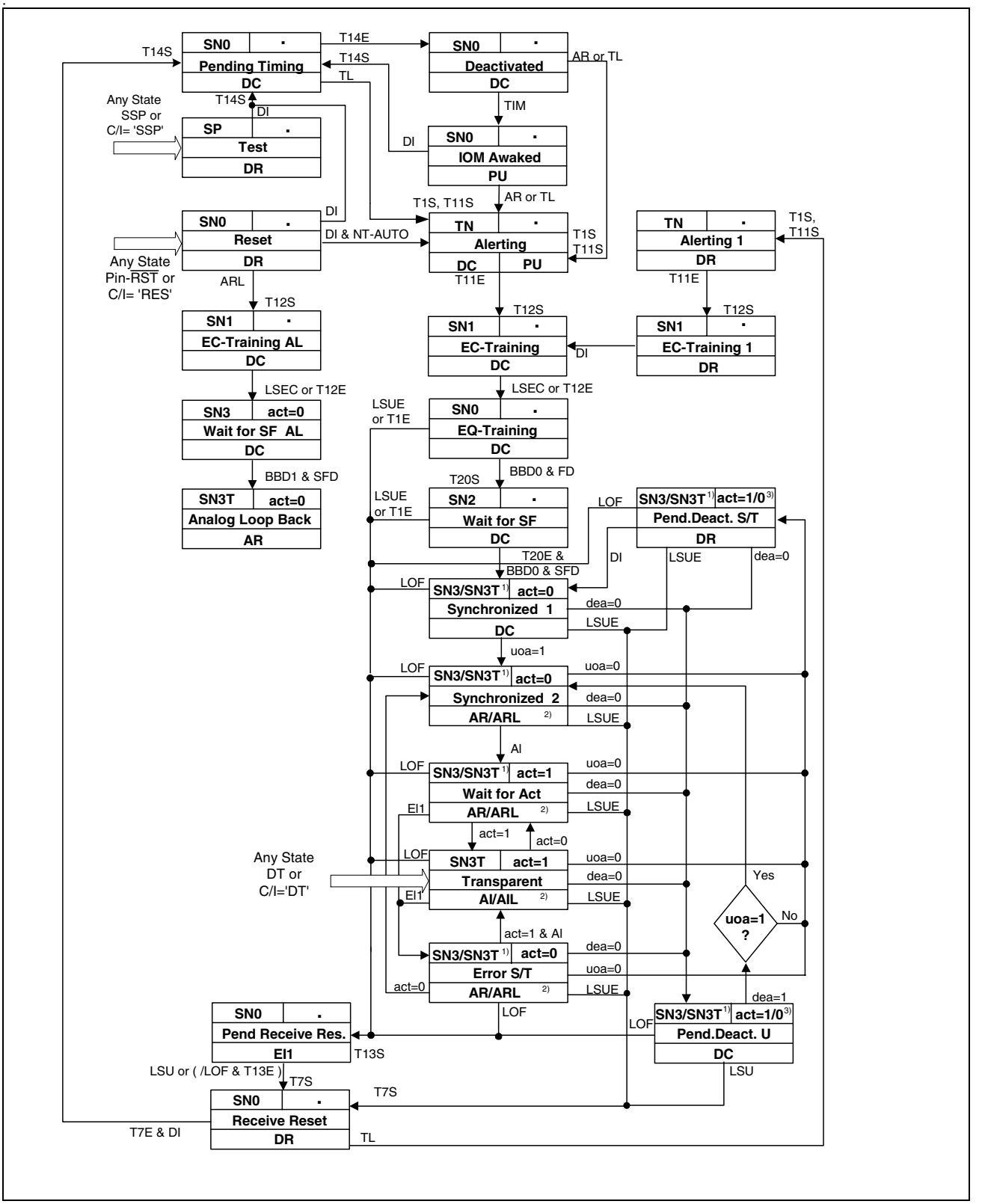


Figure 10 Standard NT State Machine (IEC-Q / NTC-Q Compatible) (Footnotes: see "Dependence of Outputs" on Page 26)

*Note: The test modes 'Data Through' (DT), 'Send Single Pulses' (SSP) and 'Quiet Mode' (QM) can be generated via pins TM0-2 according to **Table 5**.*
*If the Metallic Loop Termination is used, then the U-transceiver is forced into the states 'Reset' and 'Transparent' by valid pulse streams on pin MTI according to **Table 13**.*

2.3.5.3 Inputs to the U-Transceiver:

C/I-Commands:

AI — Activation Indication
The downstream device issues this indication to announce that its layer-1 is available. The U-transceiver informs the LT side by setting the "ACT" bit to "1".

AR — Activation Request
The U-transceiver is requested to start the activation process by sending the wake-up signal TN.

ARL — Activation Request Local Loop-back
The U-transceiver is requested to operate an analog loop-back (close to the U-interface) and to begin the start-up sequence by sending SN1 (without starting timer T1). This command may be issued only after the U-transceiver has been HW- or SW-reset. This eases that the EC- and EQ-coefficient updating algorithms converge correctly. The ARL-command has to be issued continuously as long as the loop-back is required.

DI — Deactivation Indication
This indication is used during a deactivation procedure to inform the U-transceiver that it may enter the deactivated (power-down) state.

DT — Data Through
This unconditional command is used for test purposes only and forces the U-transceiver into the "Transparent" state.

EI1 — Error Indication 1
The downstream device indicates an error condition (loss of frame alignment or loss of incoming signal). The U-transceiver informs the LT-side by setting the ACT-bit to "0" thus indicating that transparency has been lost.

RES — Reset
Unconditional command which resets the U-transceiver.

SSP — Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface.

TIM — Timing
The U-transceiver is requested to enter state 'IOM®-2 Awaked'.

U-Interface Events:

ACT = 0/1 ACT-bit received from LT-side.
- ACT = 1 requests the U-transceiver to transmit transparently in both directions. In the case of loop-backs, however, transparency in both directions of transmission is established when the receiver is synchronized.
- ACT = 0 indicates that layer-2 functionality is not available.

DEA = 0/1 DEA-bit received from the LT-side
- DEA = 0 informs the U-transceiver that a deactivation procedure has been started by the LT-side.
- DEA = 1 reflects the case when DEA = 0 was detected by faults due to e.g. transmission errors and allows the U-transceiver to recover from this situation.

UOA = 0/1 UOA-bit received from network side
- UOA = 0 informs the U-transceiver that only the U-interface is to be activated. The S/T-interface must be deactivated.
- UOA = 1 requests the S/T-interface (if present) to activate.

Timers

The start of timers is indicated by TxS, the expiry by TxE. **Table 8** shows which timers are used:

Table 8 Timers Used

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T7	40	Hold time	Receive reset
T11	9	TN-transmission	Alerting
T12	5500	Supervisor EC-converge	EC-training
T13	15000	Frame synchronization	Pend. receive reset
T14	0.5	Hold time	Pend. timing
T20	10	Hold time	Wait for SF

2.3.5.4 Outputs of the U-Transceiver:

The following signals and indications are issued on IOM®-2 (C/I-indications) and on the U-interface (predefined U-signals):

C/I-Indications

AI — Activation Indication
The U-transceiver has established transparency of transmission. The downstream device is requested to establish layer-1 functionality.

AIL — Activation Indication Loopback
The U-transceiver has established transparency of transmission. The downstream device is requested to establish a loopback #2.

AR — Activation Request
The downstream device is requested to start the activation procedure.

ARL — Activation Request Loop-back
The U-transceiver has detected a loop-back 2 command in the EOC-channel and has established transparency of transmission in the direction IOM®-2 to U-interface. The downstream device is requested to start the activation procedure and to establish a loopback #2.

DC — Deactivation Confirmation
Idle code on the IOM®-2-interface.

DR — Deactivation Request
The U-transceiver has detected a deactivation request command from the LT-side for a complete deactivation or a S/T only deactivation. The downstream device is requested to start the deactivation procedure.

EI1 — Error Indication 1
The U-transceiver has entered a failure condition caused by loss of framing on the U-interface or expiry of timer T1.

Signals on U-Interface

The signals SNx, TN and SP transmitted on the U-interface are defined in **Table 9**.

Table 9 U-Interface Signals

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
TN [1)]	± 3	± 3	± 3	± 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal

Table 9 U-Interface Signals(cont'd)

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
SN3T	present	present	normal	normal
Test Mode				
SP[2)]	test signal	test signal	test signal	test signal

Note: [1)]Alternating ± 3 symbols at 10 kHz.

Note: [2)]A series of single pulses spaced at intervals of 1.5 ms; alternating +/-3.

Input Signals of the State Machine and related U-Signals

The table below summarizes the input signals that control the NT state machine and that are extracted from the U-interface signal sequences.

LOF	**Loss of framing** This condition is fulfilled if framing is lost for 573 ms.
LSEC	**Loss of signal behind echo canceller** Internal Signal which indicates that the echo canceller has converged
LSU	**Loss of Signal on U-Interface** This signal indicates that a loss of signal level for a duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the NT waits for a response (no signal level) from the LT-side.
LSUE	**Loss of Signal on U-Interface - Error condition** After a loss of signal has been noticed, a 588 ms timer is started. When it has elapsed , the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the NT is not prepared to lose signal level i.e. the LT has stopped transmission because of loss of framing, an unsuccessful activation, or the transmission line is interrupted.
FD	**Frame Detected**
SFD	**Super Frame Detected**

BBD0 / BBD1	**BBD0/1 Detected** These signals are set if either ’1' (BBD1) or ’0' (BBD0) were detected in 4 subsequent basic frames. It is used as a criterion that the receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD0 corresponds to the received signal SL2 in case of a normal activation, BBD1 corresponds to the internally received signal SN3 in case of analog loop back.
TL	**Awake tone detected** The U-transceiver is requested to start an activation procedure.

Signals on IOM®-2

The Data (B+B+D) is set to all ’1’s in all states besides the states listed in **Table 10**.

Table 10 States with Operational Data on IOM®-2

Synchronized1
Synchronized2
Wait for ACT
Transparent
Error S/T
Pend. Deac. S/T
Pend. Deac. U
Analog Loop Back

Dependence of Outputs

- Outputs denoted with [1] in **Figure 10**:
  Signal output on U_{k0} depends on the received EOC command and on the history of the state machine according to **Table 11**:

Table 11 Signal Output on U_{k0}

EOC Command	History of the State Machine	Signal output on U_{k0}
received ’LBBD’	no influence	SN3T
received no ’LBBD’ or ’RTN’ after an ’LBBD’	state ’Transparent’ has not been reached previously during this activation procedure	SN3
	state ’Transparent’ has been reached previously during this activation procedure	SN3T

- Outputs denoted with [2] in **Figure 10**:
  C/I-code output depends on received EOC-command 'LBBD' according to **Table 12**:

Table 12 C/I-Code Output

EOC Command	Synchronized 2	Wait for Act	Transparent	Error S/T
received no 'LBBD' or 'RTN' after an 'LBBD'	AR	AR	AI	AR
received 'LBBD'	ARL	ARL	AIL	ARL

- Outputs denoted with [3] in **Figure 10**:
  In States 'Pend. Deact. S/T' and 'Pend. Deact. U' the ACT-bit output depends on its value in the previous state.
- The value of the issued SAI-bit depends on the received C/I-code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity of the downstream device.
- If state Alerting is entered from state Deactivated, then C/I-code 'PU' is issued, else C/I-code 'DC' is issued.

2.3.5.5 Description of the NT-States

The following states are used:

Alerting

The wake-up signal TN is transmitted for a period of T11 either in response to a received wake-up signal TL or to start an activation procedure on the LT-side.

Alerting 1

"Alerting 1" state is entered when a wake-up tone was received in the "Receive Reset" state and the deactivation procedure on the NT-side was not yet finished. The transmission of wake-up tone TN is started.

Analog Loop-Back

Transparency is achieved in both directions of transmission. This state can be left by making use of any unconditional command.

Deactivated

Only in state Deactivated the device may enter the power-down mode.

EC Training

The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled.

EC-Training 1

The “EC-Training 1” state is entered if transmission of signal SN1 has to be started and the deactivation procedure on the NT-side is not yet finished.

EC-Training AL

The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled.

EQ-Training

The receiver waits for signal SL1 or SL2 to be able to update the AGC, to recover the timing phase, to detect the synch-word (SW), and to update the EQ-coefficients.

Error S/T

The downstream device is in an error condition (EI1). The LT-side is informed by setting the ACT-bit to “0” (loss of transparency on the NT-side).

IOM®-2-Awaked

The U-transceiver is deactivated, but may not enter the power-down mode.

Pending Deactivation of S/T

The U-transceiver has received the UOA-bit at zero after a complete activation of the S/T-interface. The U-transceiver requests the downstream device to deactivate by issuing DR.

Pending Deactivation of U-Interface

The U-transceiver waits for the receive signal level to be turned off (LSU) to start the deactivation procedure.

Pending Receive Reset

The “Pending Receive Reset” state is entered upon detection of loss of framing on the U-interface or expiry of timer T1. This failure condition is signalled to the LT-side by turning off the transmit level (SN0). The U-transceiver then waits for a response (no signal level LSU) from the LT-side.

Pending Timing

In the NT-mode the pending timing state assures that the C/I-channel code DC is issued four times before entering the ’Deactivated’ state.

Receive Reset

In state ’Receive Reset’ a reset of the Uk0-receiver is performed, except in case that state ’Receive Reset’ was entered from state ’Pend. Deact. U’. Timer T7 assures that no activation procedure is started from the NT-side for a minimum period of time of T7. This gives the LT a chance to activate the NT.

Reset

In state ’Reset’ a software-reset is performed.

Synchronized 1

State ’Synchronized 1’ is the fully active state of the U-transceiver, while the downstream device is deactivated.

Synchronized 2

In this state the U-transceiver has received UOA = 1. This is a request to activate the downstream device.

Test

The test signal SSP is issued as long as TM2-0 = ’101’ . For further details see **Table 9**.

Transparent

This state is entered upon the detection of ACT = 1 received from the LT-side and corresponds to the fully active state.

Wait for ACT

Upon the receipt of AI, the NT waits for a response (ACT = 1) from the LT-side.

Wait for SF

The signal SN2 is sent on the U-interface and the receiver waits for detection of the superframe.

Wait for SF AL

This state is entered in the case of an analog loop-back and allows the receiver to update the AGC, to recover the timing phase, and to update the EQ-coefficients.

2.3.6 Metallic Loop Termination

For North American applications a maintenance controller according to ANSI T1.601 section 6.5 is implemented. The maintenance pulse stream from the U-interface Metallic Loop Termination circuit (MLT) is fed to pin MTI, usually via an optocoupler. It is digitally filtered for 20 ms and decoded independently on the polarity by the maintenance controller according to **Table 13**. Therefore, the maintenance controller is capable of detecting the DC and AC signaling format. The Q-SMINT®O automatically sets the U-transceiver in the proper state and issues an interrupt. The state selected by the MLT is indicated via two bits.

The Q-SMINT®O reacts on a valid pulse stream independently of the current U-transceiver state. This includes the power-down state.

A test mode is valid for 75 seconds. If during the 75 seconds a valid pulse sequence is detected the 75 s timer starts again. After expiry of the 75 s timer the MLT maintenance controller goes back to normal operation.

Table 13 ANSI Maintenance Controller States

Number of counted pulses	ANSI maintenance controller state	U-transceiver State Machine
<= 5	ignored	no impact
6	Quiet Mode	transition to state 'Reset' start timer 75s
7	ignored	no impact
8	Insertion Loss Measurement	transition to state 'Transparent' start timer 75s
9	ignored	no impact
10	normal operation	transition to state 'Reset'
>= 11	ignored	no impact

Figure 11 shows examples for pulse streams with inverse polarity selecting Quiet Mode.

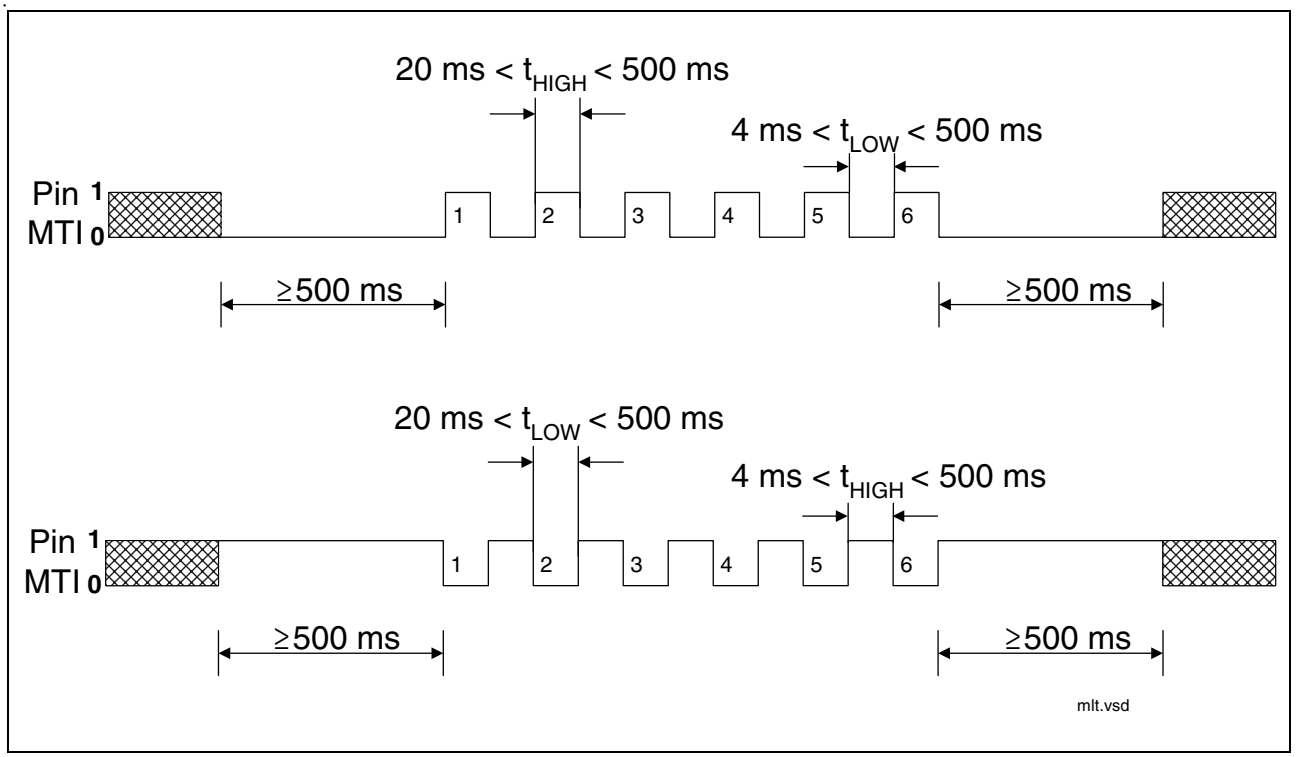


Figure 11 Pulse Streams Selecting Quiet Mode

2.4 S-Transceiver

The S-Transceiver offers the NT state machine described in the User's Manual V3.4 [10].

The S-transceiver basic configurations are performed via pin strapping.

2.4.1 Line Coding, Frame Structure

Line Coding

The following figure illustrates the line code. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with two exceptions:
For the required frame structure a code violation is indicated by two consecutive pulses of the same polarity. These two pulses can be adjacent or separated by binary ONEs.
In bus configurations a binary ZERO always overwrites a binary ONE.

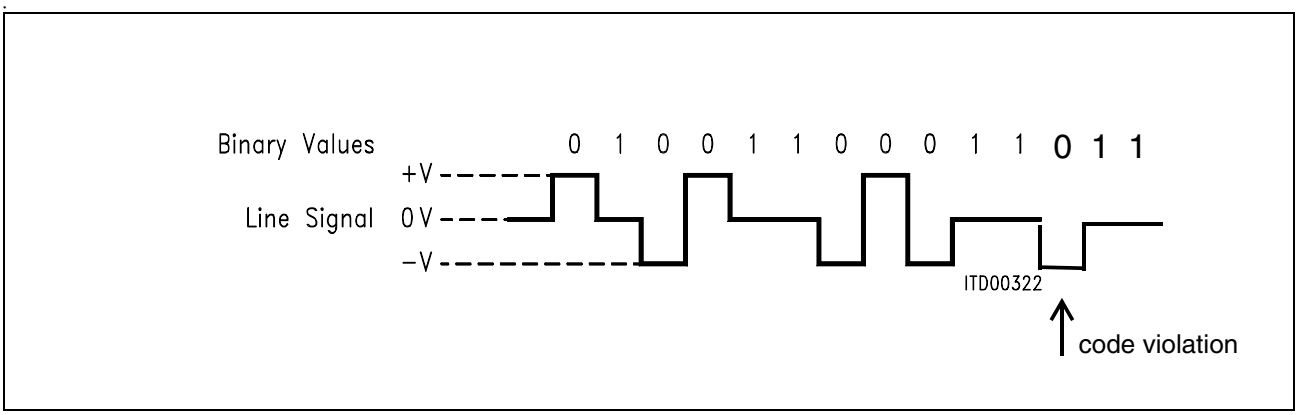


Figure 12 S/T -Interface Line Code

Frame Structure

Each S/T frame consists of 48 bits at a nominal bit rate of 192 kbit/s. For user data (B1+B2+D) the frame structure applies to a data rate of 144 kbit/s (see **Figure 12**).
In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

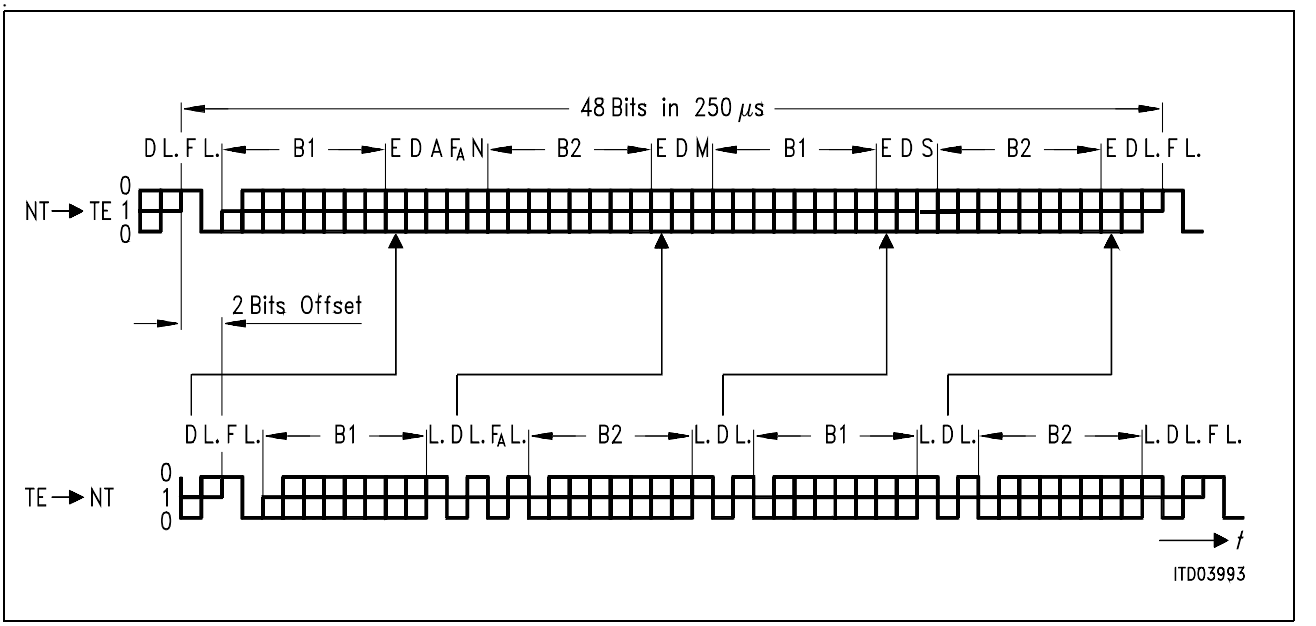


Figure 13 Frame Structure at Reference Points S and T (ITU I.430)

– F	Framing Bit	F = (0b) → identifies new frame (always positive pulse, always code violation)
– L.	D.C. Balancing Bit	L. = (0b) → number of binary ZEROs sent after the last L. bit was odd
– D	D-Channel Data Bit	Signaling data specified by user
– E	D-Channel Echo Bit	E = D → received E-bit is equal to transmitted D-bit
– F_A	Auxiliary Framing Bit	See section 6.3 in ITU I.430
– N		N = $\overline{F_A}$
– B1	B1-Channel Data Bit	User data
– B2	B2-Channel Data Bit	User data
– A	Activation Bit	A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
– S	S-Channel Data Bit	S_1 channel data (see note below)
– M	Multiframing Bit	M = (1b) → Start of new multi-frame

Note: The ITU I.430 standard specifies S1 - S5 for optional use.

2.4.2 S/Q Channels, Multiframing

The S/Q channels are not supported.

2.4.3 Data Transfer between IOM®-2 and S_0

In the state G3 (Activated) the B1, B2 and D bits are transferred transparently from the S/T to the IOM®-2 interface and vice versa. In all other states ’1’s are transmitted to the IOM®-2 interface.

2.4.4 Loopback 2

C/I commands ARL and AIL close the analog loop as close to the S-interface as possible. ETSI refers to this loop under ’loopback 2’. ETSI requires, that B1, B2 and D channels have the same propagation delay when being looped back.

The D-channel Echo bit is set to bin. 0 during an analog loopback (i.e. loopback 2). The loop is transparent.

Note: After C/I-code AIL has been recognized by the S-transceiver, zeros are looped back in the B and D-channels (DU) for four frames.

2.4.5 State Machine

The state diagram notation is given in **Figure 14**.

The information contained in the state diagrams are:

– state name
– Signal received from the line interface (INFO)
– Signal transmitted to the line interface (INFO)
– C/I code received (commands)
– C/I code transmitted (indications)
– transition criteria

The transition criteria are grouped into:

– C/I commands
– Signals received from the line interface (INFOs)
– Reset

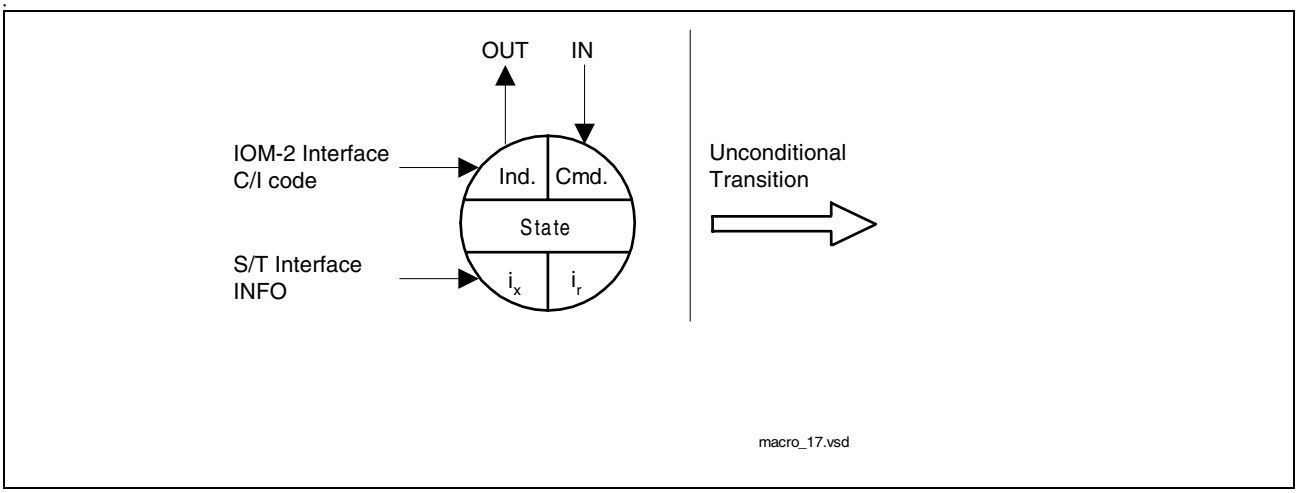


Figure 14 State Diagram Notation

As can be seen from the transition criteria, combinations of multiple conditions are possible as well. A “∗” stands for a logical AND combination. And a “+” indicates a logical OR combination.

Test Signals

- 2 kHz Single Pulses (TM1)

  One pulse with a width of one bit period per frame with alternating polarity.
- 96 kHz Continuous Pulses (TM2)

  Continuous pulses with a pulse width of one bit period.

Note: The test signals TM1 and TM2 can be generated via pins TM0-2 according to ***Table 5****.*

Reset States

After an active signal on the reset pin $\overline{\text{RST}}$ the S-transceiver state machine is in the reset state.

C/I Codes in Reset State

In the reset state the C/I code 0000 (TIM) is issued. This state is entered after a hardware reset ($\overline{\text{RST}}$).

C/I Codes in Deactivated State

If the S-transceiver is in state ‘Deactivated‘ and receives $\overline{\text{i0}}$, the C/I code 0000 (TIM) is issued until expiration of the 8 ms timer. Otherwise, the C/I code 1111 (DI) is issued.

Receive Infos on S/T

I0	INFO 0 detected
$\overline{I0}$	Level detected (signal different to I0)
I3	INFO 3 detected
$\overline{I3}$	Any INFO other than INFO 3

Transmit Infos on S/T

I0	INFO 0
I2	INFO 2
I4	INFO 4
It	Send Single Pulses (TM1). Send Continuous Pulses (TM2).

2.4.5.1 State Machine NT Mode

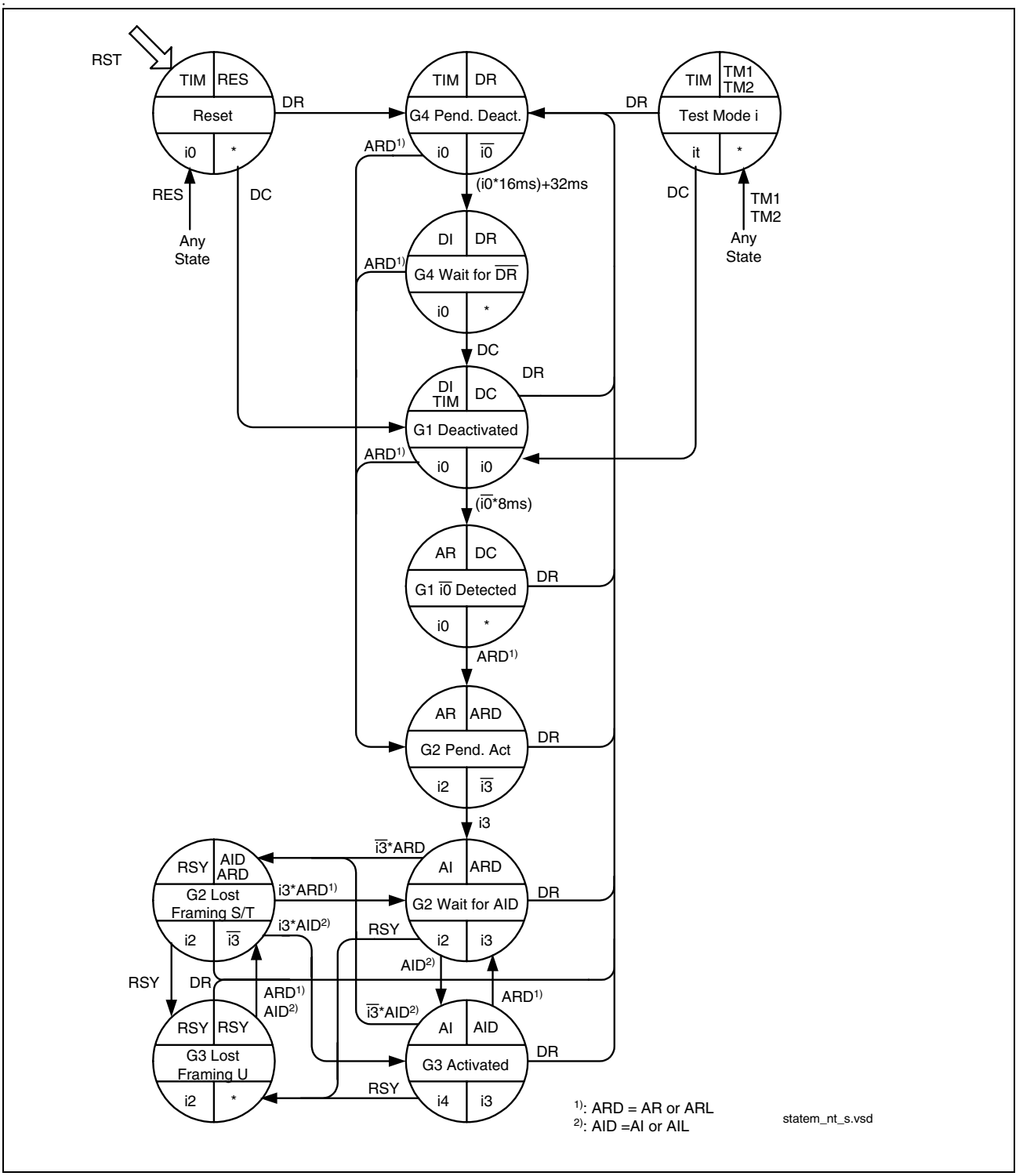


Figure 15 State Machine NT Mode

Note: By setting the Test Mode pins TM0-2 to ’010’ / ’011’: Continuous Pulses / Single Pulses, the S-transceiver starts sending the corresponding test signal, but no state transition is invoked.

G1 Deactivated

The S-transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. Activation is possible from the S/T interface and from the IOM®-2 interface.

G1 $\overline{\text{I0}}$ Detected

An $\overline{\text{INFO 0}}$ is detected on the S/T-interface, translated to an “Activation Request” indication in the C/I channel. The S-transceiver is waiting for an AR command, which normally indicates that the transmission line upstream is synchronized.

G2 Pending Activation

As a result of the ARD command, an INFO 2 is sent on the S/T-interface. INFO 3 is not yet received. In case of ARL command, loop 2 is closed.

G2 wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the S-transceiver waits for a “switch-through” command AID from the device upstream.

G3 Activated

INFO 4 is sent on the S/T-interface as a result of the “switch through” command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

G2 Lost Framing S/T

This state is reached when the transceiver has lost synchronism in the state G3 activated.

G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the transmission line, the S-transceiver transmits INFO 2.

G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state “G4 wait for DR”) is issued by the transceiver when:

either INFO0 is received for a duration of 16 ms

or an internal timer of 32 ms expires.

G4 wait for $\overline{DR}$

Final state after a deactivation request. The S-transceiver remains in this state until DC is issued.

Unconditional States

Test Mode TM1

Send Single Pulses

Test Mode TM2

Send Continuous Pulses

C/I Commands

Command	Abbr.	Code	Remark
Deactivation Request	DR	0000	Deactivation Request. Initiates a complete deactivation by transmitting INFO 0.
Reset	RES	0001	Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command.
Send Single Pulses	TM1	0010	Send Single Pulses.
Send Continuous Pulses	TM2	0011	Send Continuous Pulses.
Receiver not Synchronous	RSY	0100	Receiver is not synchronous
Activation Request	AR	1000	Activation Request. This command is used to start an activation.
Activation Request Loop	ARL	1010	Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface.
Activation Indication	AI	1100	Activation Indication. Synchronous receiver, i.e. activation completed.

Command	Abbr.	Code	Remark
Activation Indication Loop	AIL	1110	Activation Indication Loop
Deactivation Confirmation	DC	1111	Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

Indication	Abbr.	Code	Remark
Timing	TIM	0000	Interim indication during deactivation procedure.
Receiver not Synchronous	RSY	0100	Receiver is not synchronous.
Activation Request	AR	1000	$\overline{\text{INFO 0}}$ received from terminal. Activation proceeds.
Illegal Code Ciolation	CVR	1011	Illegal code violation received. This function has to be enabled in S_CONF0.EN_ICV.
Activation Indication	AI	1100	Synchronous receiver, i.e. activation completed.
Deactivation Indication	DI	1111	Timer (32 ms) expired or INFO 0 received for a duration of 16 ms after deactivation request.

3 Operational Description

3.1 Layer 1 Activation/Deactivation

3.1.1 Complete Activation Initiated by Exchange

Figure 16 depicts the procedure if activation has been initiated by the exchange side (LT).

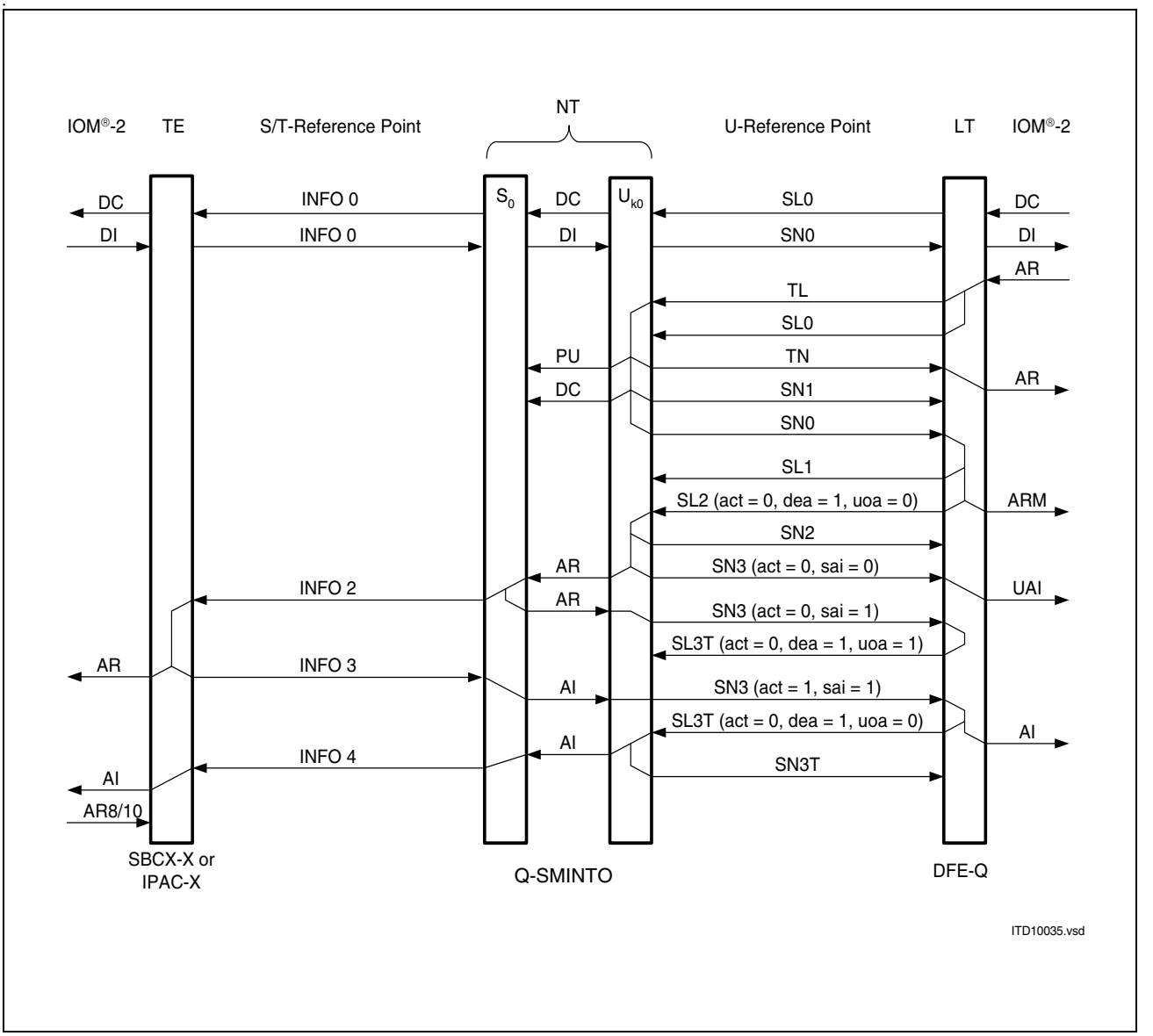


Figure 16 Complete Activation Initiated by Exchange

3.1.2 Complete Activation Initiated by TE

Figure 17 depicts the procedure if activation has been initiated by the terminal side (TE).

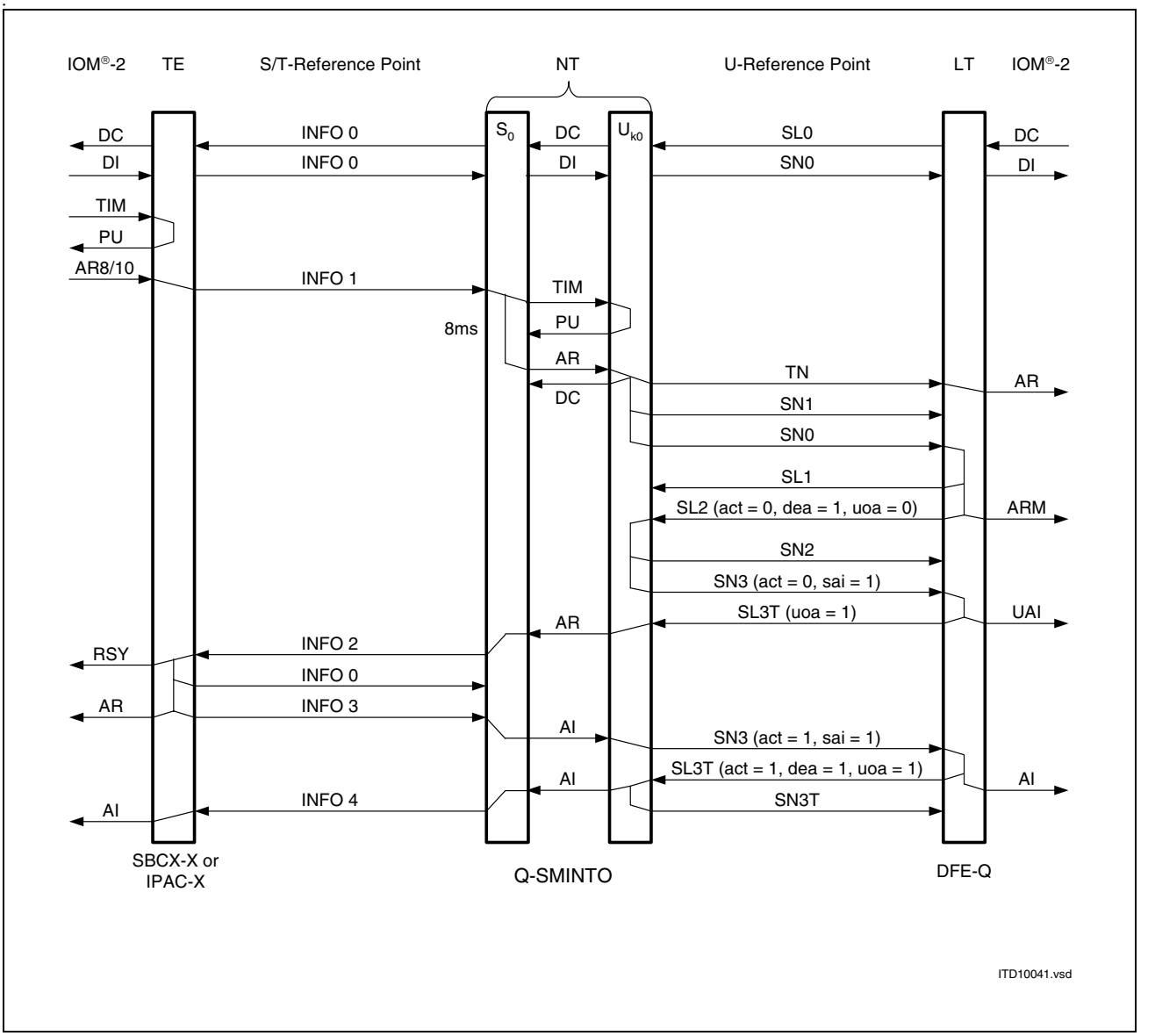


Figure 17 Complete Activation Initiated by TE

3.1.3 Complete Deactivation

Figure 18 depicts the procedure if deactivation has been initiated. Deactivation of layer 1 is always initiated by the exchange.

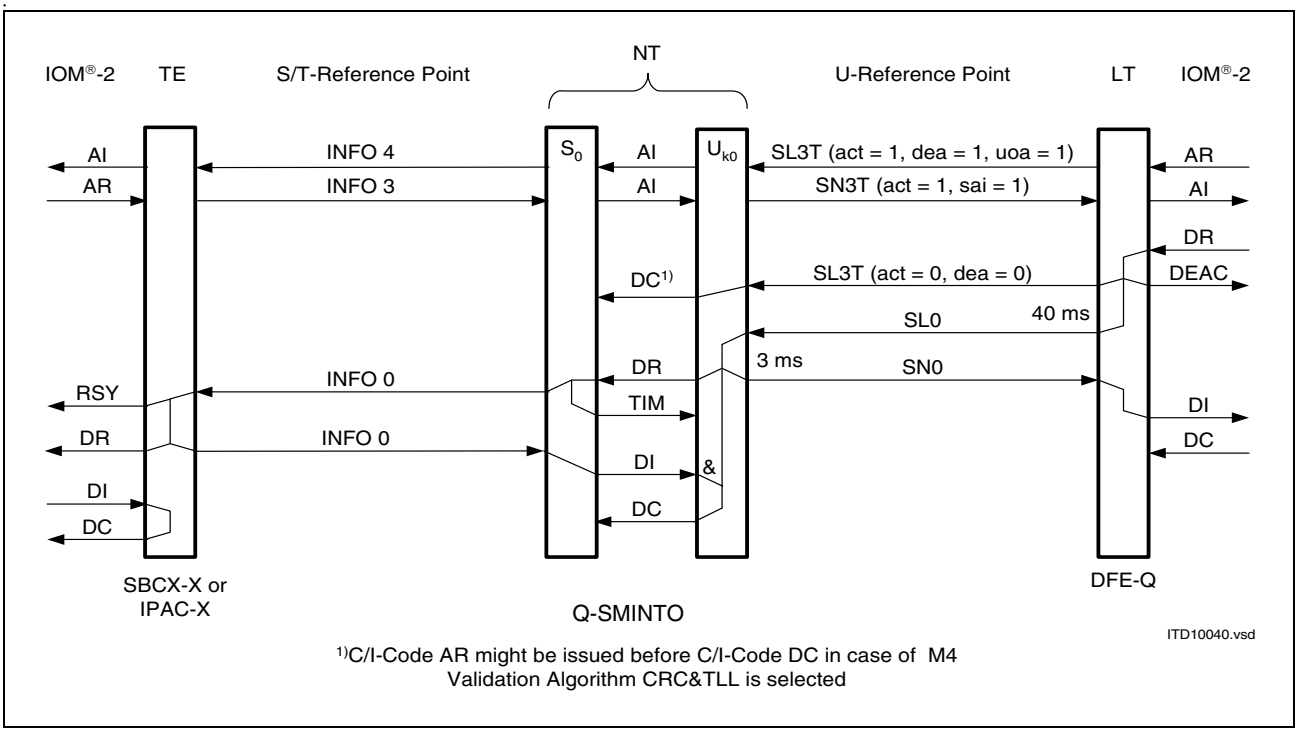


Figure 18 Complete Deactivation Initiated by Exchange

3.1.4 Partial Activation

Figure 19 depicts the procedure if partial activation has been initiated by the exchange.

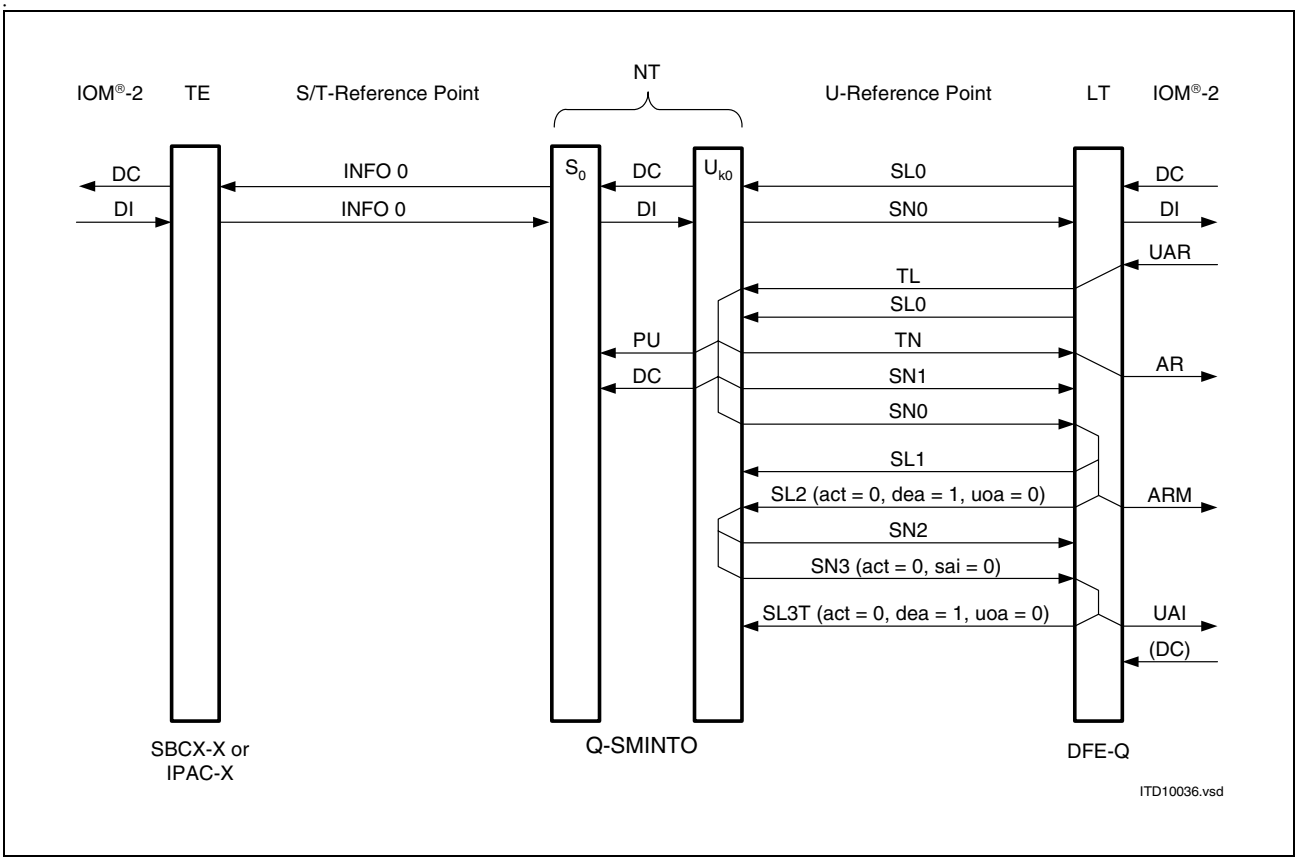


Figure 19 Partial Activation

3.1.5 Activation from Exchange with U Active

Figure 20 depicts the procedure if activation has been initiated by the exchange with U already being active.

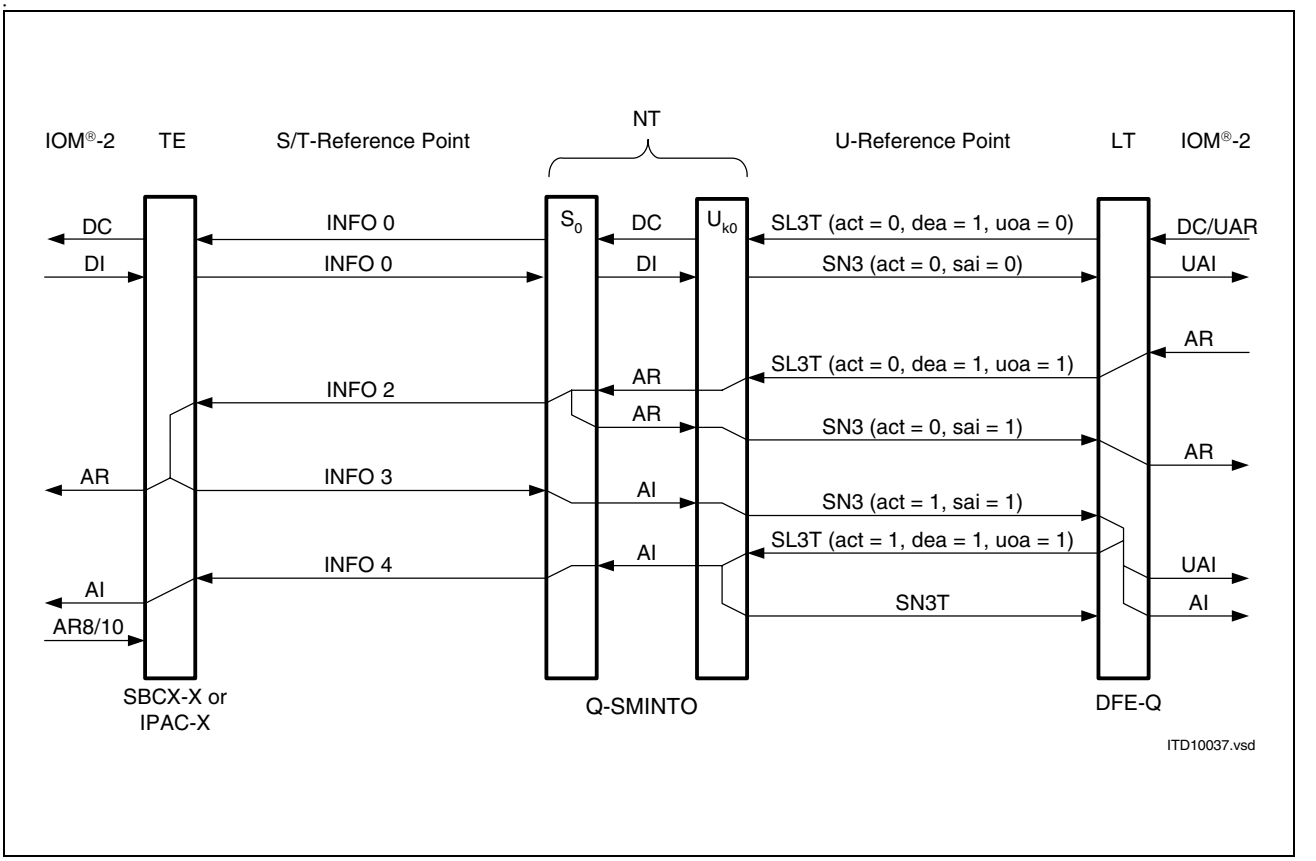


Figure 20 Activation from LT with U Active

3.1.6 Activation from TE with U Active

Figure 21 depicts the procedure if activation has been initiated by the TE with U already being active.

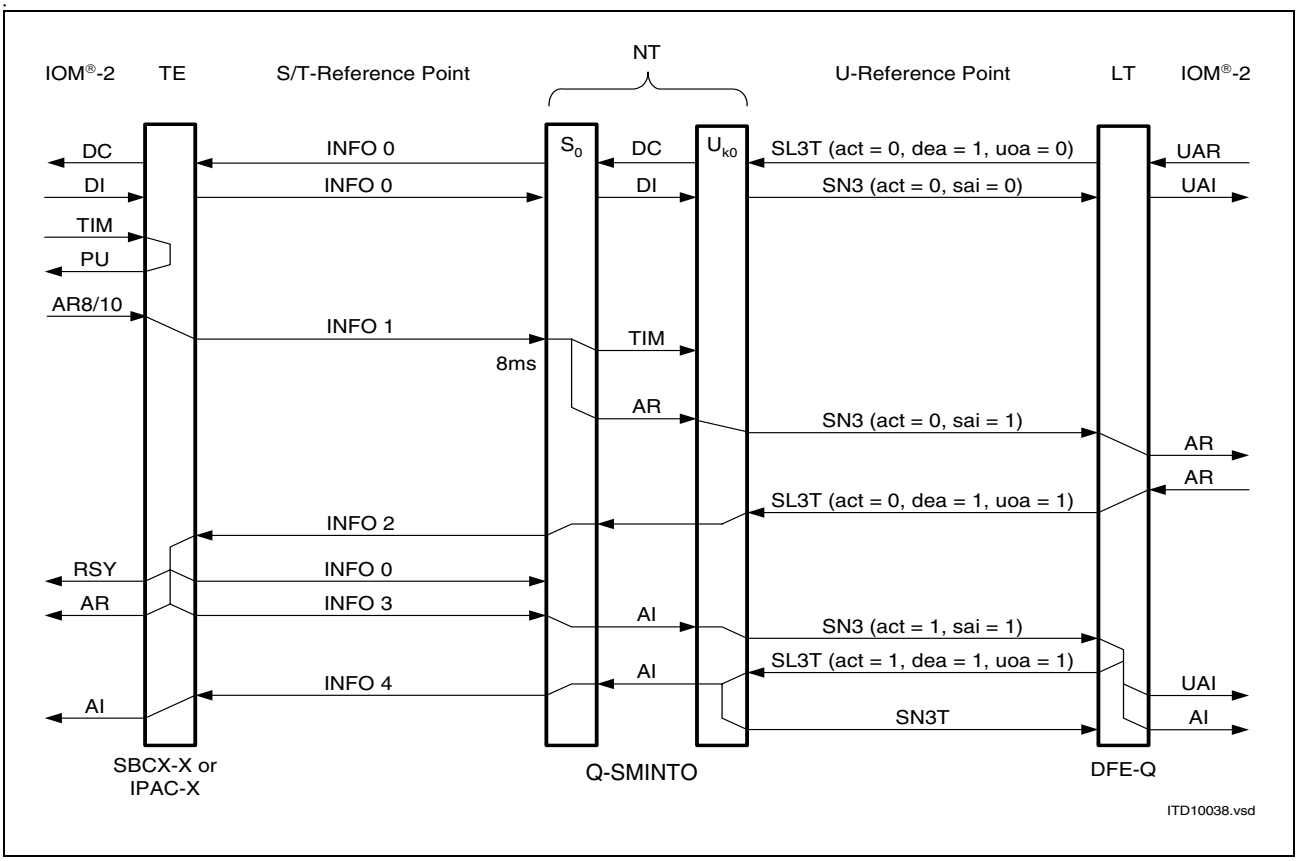


Figure 21 Activation from TE with U Active

3.1.7 Partial Deactivation with U Active

Figure 22 depicts the procedure if partial deactivation has been initiated by the exchange; i.e. U remains active.

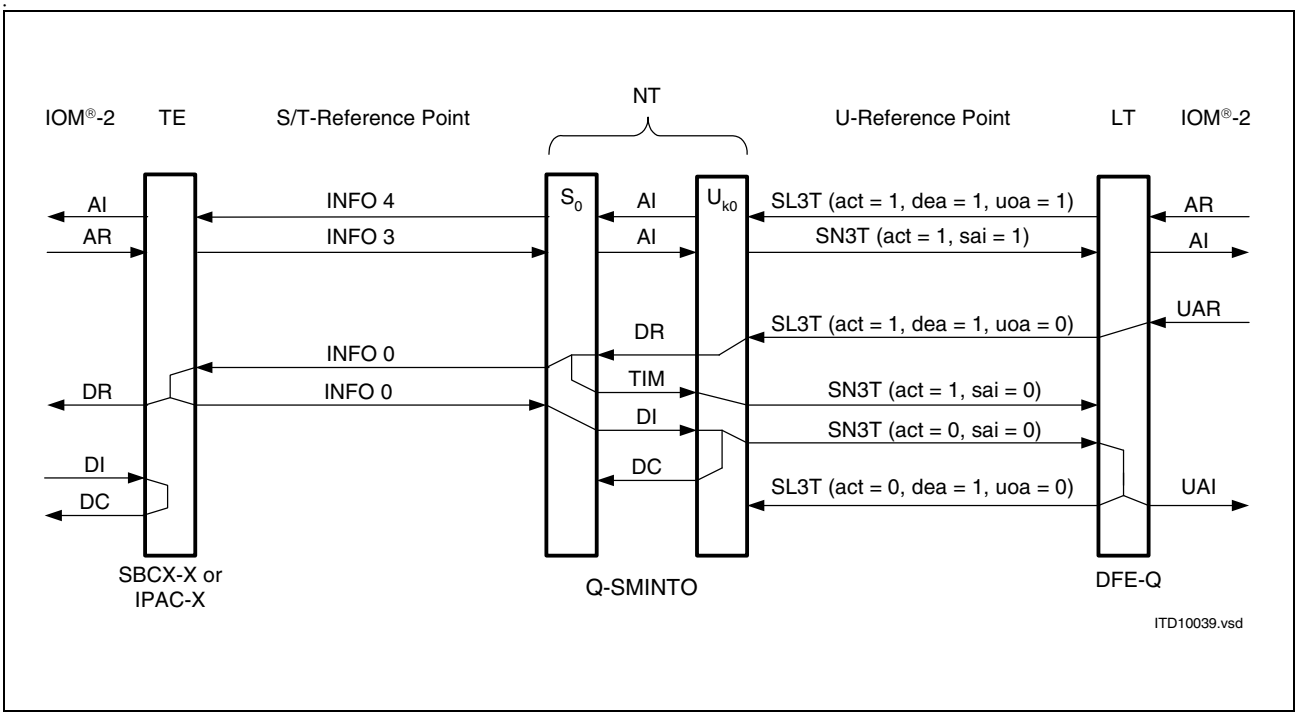


Figure 22 Partial Deactivation with U Active

3.1.8 Loop 2

Figure 23 depicts the procedure if loop 2 is closed and opened.

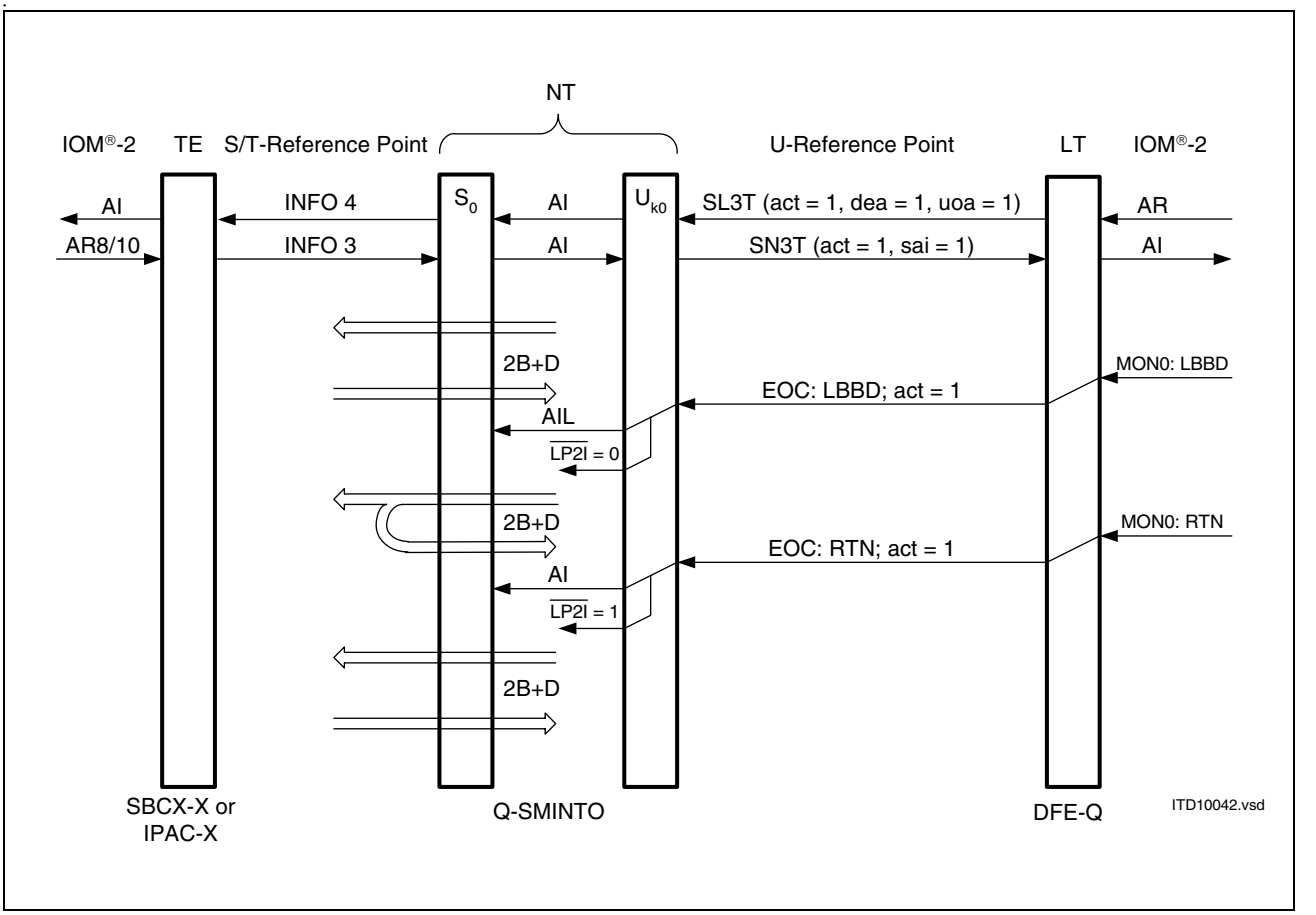


Figure 23 Loop 2

Note: Closing / resolving loop 2 may provoke the S-transceiver to resynchronize. In this case, the following C/I-codes are exchanged immediately upon receipt of AIL / AI, respectively: DU: 'RSY', DD: 'ARL', DU: 'AI', DD: 'AIL' / 'AI'.

3.2 Layer 1 Loopbacks

Test loopbacks are specified by the national PTTs in order to facilitate the location of defect systems. Four different loopbacks are defined. The position of each loopback is illustrated in **Figure 24**.

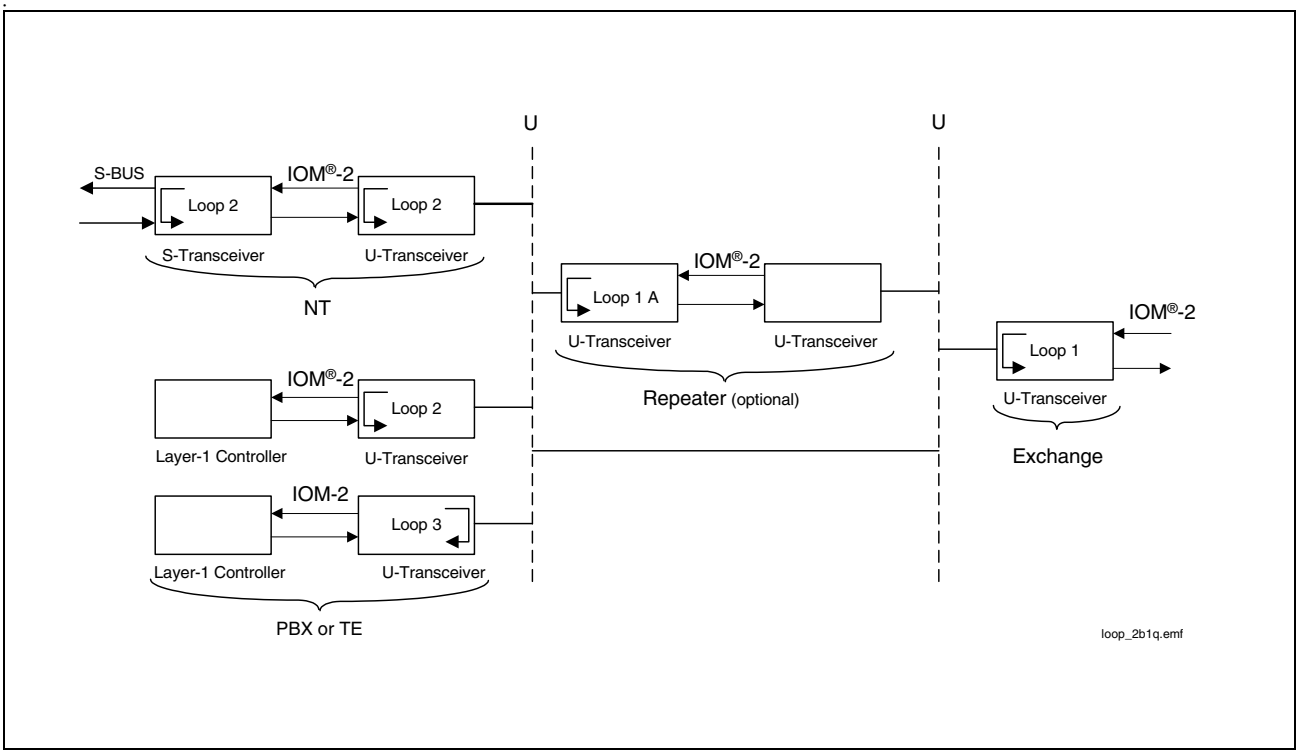


Figure 24 Test Loopbacks

Loopbacks #1, #1A and #2 are controlled by the exchange. Loopback #3 is controlled locally on the remote side. All four loopback types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner. Only the data looped back internally is processed; signals on the receive pins are ignored. The propagation delay of actually looped B and D channels data must be identical in all loopbacks.

3.2.1 Loopback No.2

For loopback #2 several alternatives exist. Both the type of loopback and the location may vary. The following loopback types belong to the loopback-#2 category:

- complete loopback (B1,B2,D), in a downstream device
- B1-channel loopback, always performed in the U-transceiver
- B2-channel loopback, always performed in the U-transceiver

All loop variations performed by the U-transceiver are closed as near to the internal IOM®-2 interface as possible.

Normally loopback #2 is controlled by the exchange. The maintenance channel is used for this purpose. All loopback functions are latched. This allows channel B1 and channel B2 to be looped back simultaneously.

3.2.1.1 Complete Loopback

When receiving the request for a complete loopback, the U transceiver passes it on to the downstream device, e.g. the S-bus transceiver. This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent”

3.2.1.2 Loopback No.2 - Single Channel Loopbacks

Single channel loopbacks are always performed directly in the U-Transceiver. No difference between the B1-channel and the B2-channel loopback control procedure exists.

3.3 External Circuitry

3.3.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.

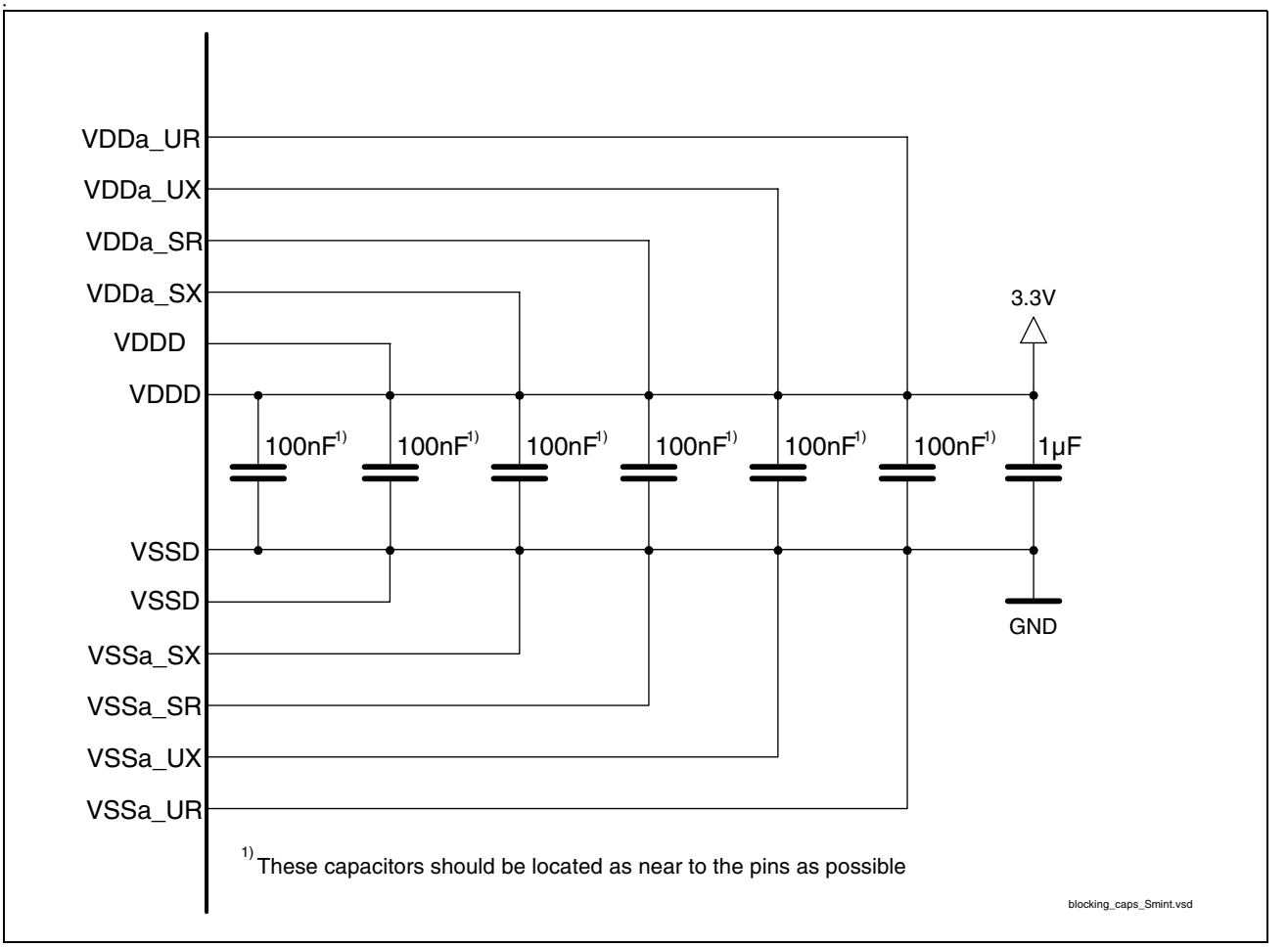


Figure 25 Power Supply Blocking

3.3.2 U-Transceiver

The Q-SMINT®O is connected to the twisted pair via a transformer. **Figure 26** shows the recommended external circuitry. The recommended protection circuitry is not displayed.

Note: The integrated hybrid as specified for Version 1.1 is no more available in Version 1.3 and an external hybrid is required.

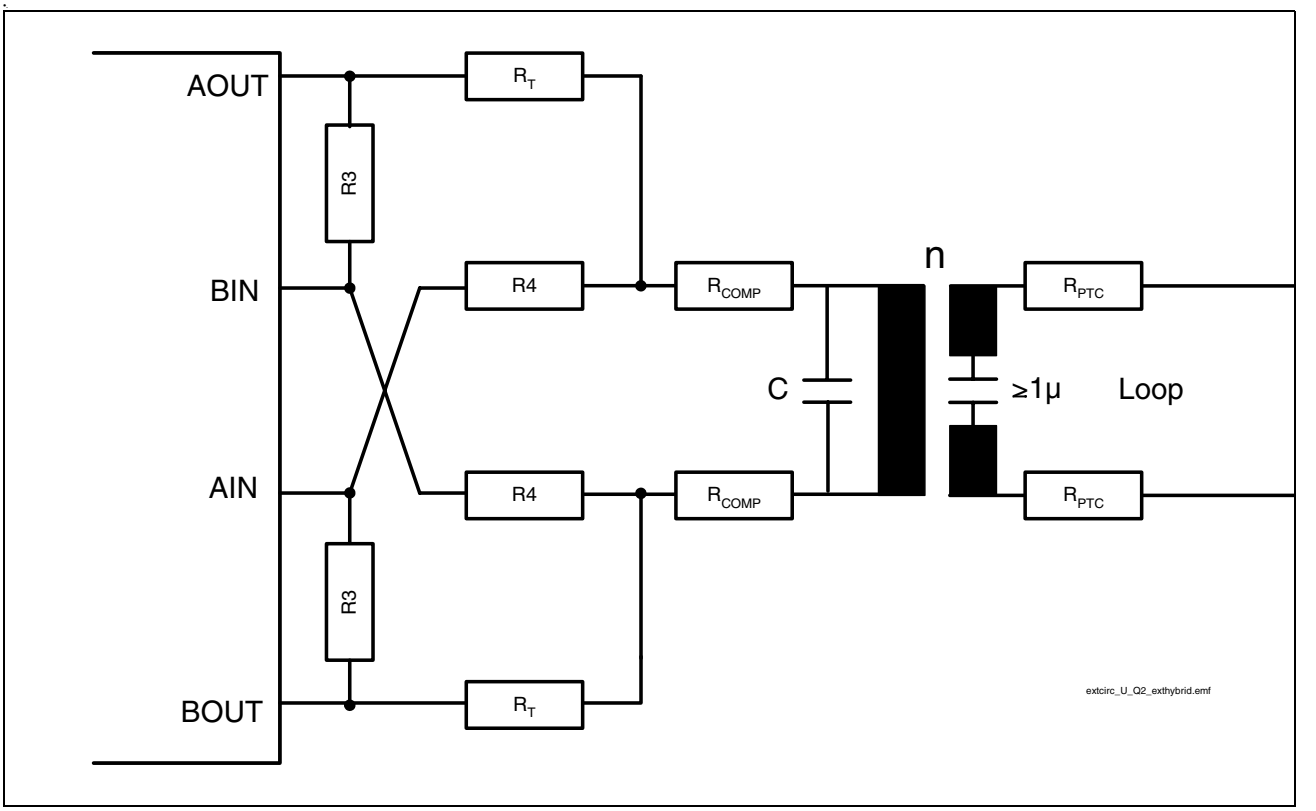


Figure 26 External Circuitry U-Transceiver

U-Transformer Parameters

The following **Table 14** lists parameters of typical U-transformers:

Table 14 U-Transformer Parameters

U-Transformer Parameters	Symbol	Value	Unit
U-Transformer ratio; Device side : Line side	n	1 : 2	
Main inductance of windings on the line side	L_H	14.5	mH
Leakage inductance of windings on the line side	L_S	<75	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	100	pF
DC resistance of the windings on device side	R_B	2.5[1)]	Ω
DC resistance of the windings on line side	R_L	5[1)]	Ω

[1)] R_B / R_L according to equation[2]

Resistors of the External Hybrid R3, R4 and R_T

R3 = 1.3 kΩ

R4 = 1.0 kΩ

R_T = 9.5 Ω

Resistors on the Line Side R_{PTC} / Chip Side R_T

Optional use of up to 2x20 Ω resistors (2xR_{PTC}) on the line side of the transformer requires compensation resistors R_{COMP} depending on R_{PTC}:

$$2R_{PTC} + 8R_{COMP} = 40\ \Omega \quad (1)$$

$$2R_{PTC} + 4(2R_{COMP} + 2R_T + R_{OUT} + R_B) + R_L = 135\ \Omega \quad (2)$$

R_B, R_L : see **Table 14**
R_{OUT} : see **Table 19**

27 nF Capacitor C

To achieve optimum performance the 27 nF capacitor should be MKT. A Ceramic capacitor is not recommended.

Tolerances

- Rs: ±1%
- C=27 nF: ±10-20%
- L=14.5 mH: ±10%

3.3.3 S-Transceiver

In order to comply to the physical requirements of ITU recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the S-transceiver needs some additional circuitry.

S-Transformer Parameters

The following **Table 15** lists parameters of a typical S-transformer:

Table 15 S-Transformer Parameters

Transformer Parameters	Symbol	Value	Unit
Transformer ratio; Device side : Line side	n	2 : 1	
Main inductance of windings on the line side	L_H	typ. 30	mH
Leakage inductance of windings on the line side	L_S	typ. <3	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	typ. <100	pF
DC resistance of the windings on device side	R_B	typ. 2.4	Ω
DC resistance of the windings on line side	R_L	typ. 1.4	Ω

Transmitter

The **transmitter** requires external resistors R_{stx} = 47Ω in order to adjust the output voltage to the pulse mask (nominal 750 mV according to ITU I.430, to be tested with the test mode “TM1”) on the one hand and in order to meet the output impedance of minimum 20 Ω on the other hand (to be tested with the testmode ’Continuous Pulses’) on the other hand.

Note: The resistance of the S-transformer must be taken into account when dimensioning the external resistors R_{stx}. If the transmit path contains additional components (e.g. a choke), then the resistance of these additional components must be taken into account, too.

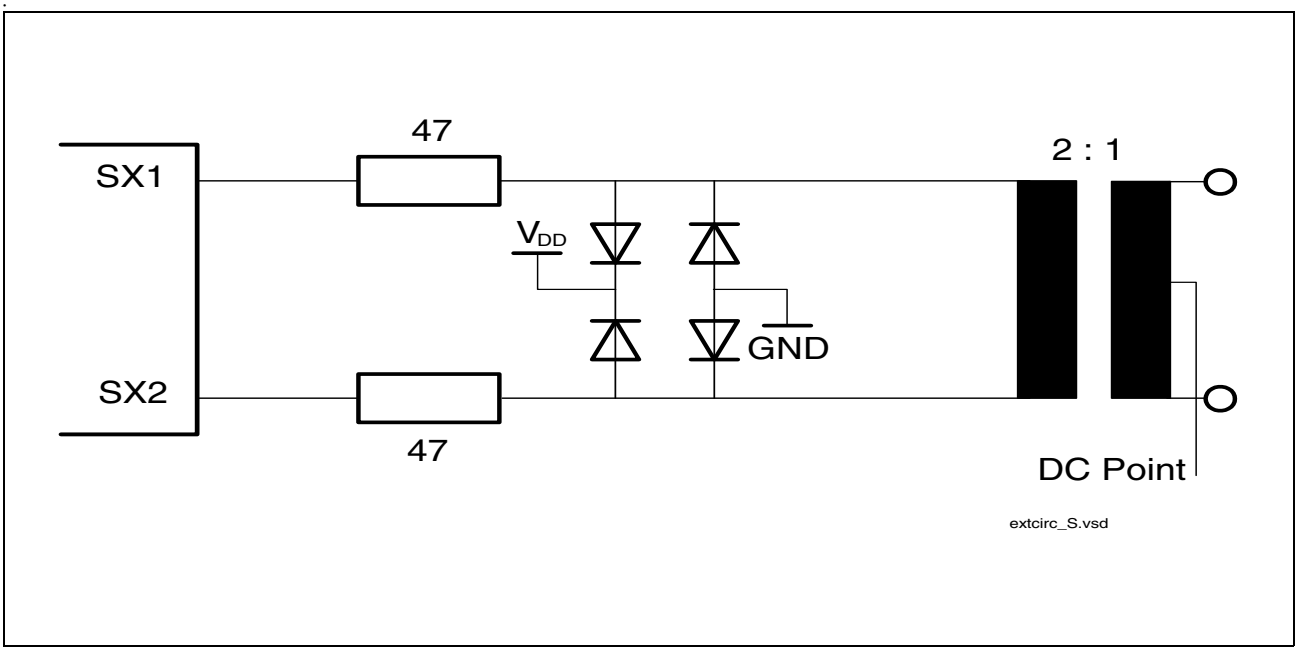


Figure 27 External Circuitry S-Interface Transmitter

Receiver

The **receiver** of the S-transceiver is symmetrical. 10 kΩ overall resistance are recommended in each receive path. It is preferable to split the resistance into two resistors for each line. This allows to place a high resistance between the transformer and the diode protection circuit (required to pass 96 kHz input impedance test of ITU I.430 [8] and ETS 300012-1). The remaining resistance (1.8 kΩ) protects the S-transceiver itself from input current peaks.

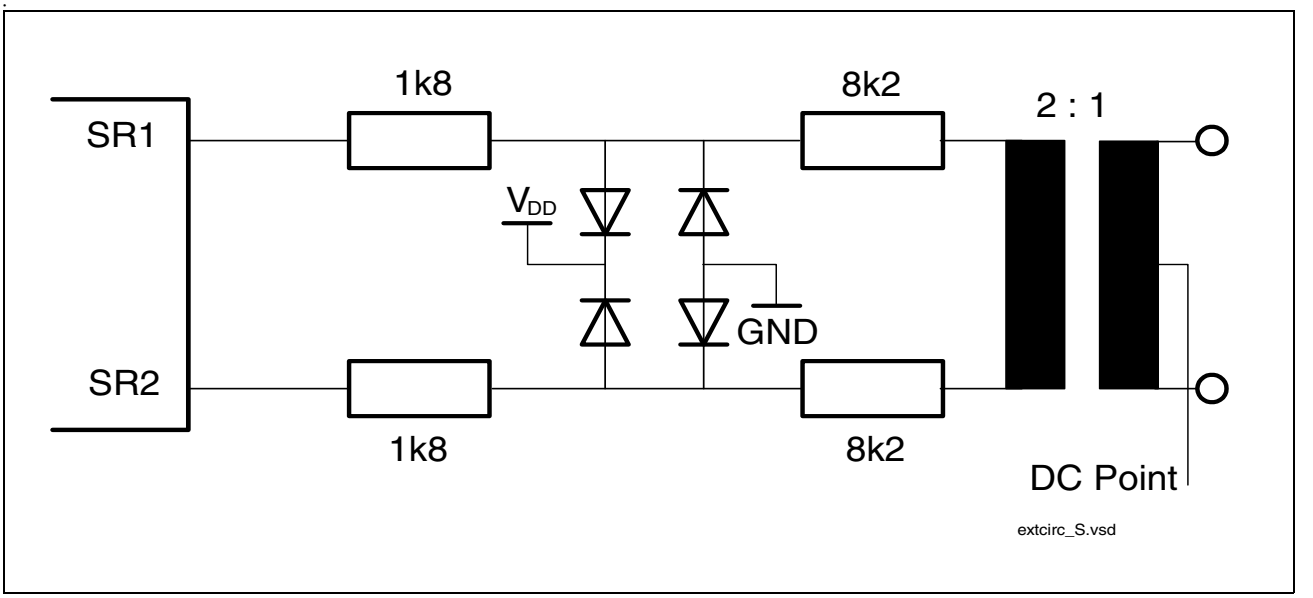


Figure 28 External Circuitry S-Interface Receiver

3.3.4 Oscillator Circuitry

Figure 29 illustrates the recommended oscillator circuit.

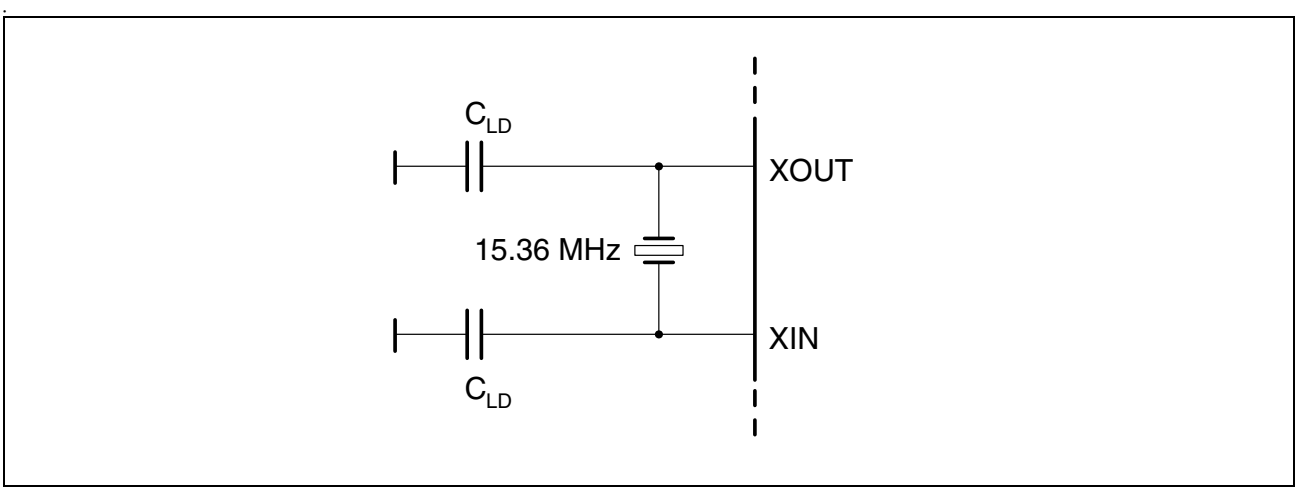


Figure 29 Crystal Oscillator

Table 16 Crystal Parameters

Parameter	Symbol	Limit Values	Unit
Frequency	f	15.36	MHz
Frequency calibration tolerance		+/-60	ppm
Load capacitance	C_L	20	pF
Max. resonance resistance	R1	20	Ω
Max. shunt capacitance	C_0	7	pF
Oscillator mode		fundamental	

External Components and Parasitics

The load capacitance C_L is computed from the external capacitances C_{LD}, the parasitic capacitances C_{Par} (pin and PCB capacitances to ground and V_{DD}) and the stray capacitance C_{IO} between XIN and XOUT:

$$C_L = \frac{(C_{LD} + C_{Par}) \times (C_{LD} + C_{Par})}{(C_{LD} + C_{Par}) + (C_{LD} + C_{Par})} + C_{IO}$$

For a specific crystal the total load capacitance is predefined, so the equation must be solved for the external capacitances C_{LD}, which is usually the only variable to be determined by the circuit designer. Typical values for the capacitances C_{LD} connected to the crystal are 22 - 33 pF.

3.3.5 General

- low power LEDs
- MLT input supports
  - APC13112
  - AT&T LH1465AB
  - discrete as proposed by Infineon

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-40 to 85	°C
Storage temperature	T_{STG}	– 65 to 150	°C
Maximum Voltage on V_{DD}	V_{DD}	4.2	V
Maximum Voltage on any pin with respect to ground	V_S	-0.3 to V_{DD} + 3.3 (max. < 5.5)	V

ESD integrity (according EIA/JESD22-A114B (HBM)): 2 kV

Note: Stress above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Line Overload Protection

The Q-SMINT®O is compliant to ESD tests according to ANSI / EOS / ESD-S 5.1-1993 (CDM), EIA/JESD22-A114B (HBM) and to Latch-up tests according to JEDEC EIA / JESD78. From these tests the following max. input currents are derived (**Table 17**):

Table 17 Maximum Input Currents

Test	Pulse Width	Current	Remarks
ESD	100 ns	1.3 A	3 repetitions
Latch-up	5 ms	+/-200 mA	2 repetitions, respectively
DC	--	10 mA	

4.2 DC Characteristics

V_{DD}/V_{DDA} = 3.3 V +/- 5% ; V_{SS}/V_{SSA} = 0 V; T_A = -40 to 85 °C

Digital Pins	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
All	Input low voltage	V_{IL}	-0.3	0.8	V	
	Input high voltage	V_{IH}	2.0	5.25	V	
All except DD/DU $\overline{ACT}$,$\overline{LP2}$I MCLK	Output low voltage	V_{OL1}		0.45	V	I_{OL1} = 3.0 mA
	Output high voltage	V_{OH1}	2.4		V	I_{OH1} = 3.0 mA
DD/DU $\overline{ACT}$,$\overline{LP2}$I MCLK	Output low voltage	V_{OL2}		0.45	V	I_{OL2} = 4.0 mA
	Output high voltage (DD/DU push-pull)	V_{OH2}	2.4		V	I_{OH2} = 4.0 mA
All	Input leakage current	I_{LI}		10	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Output leakage current	I_{LO}		10	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Input leakage current (internal pull-up)	I_{LIPU}	50	200	µA	0 V ≤ V_{IN} ≤ V_{DD}
Analog Pins						
AIN, BIN	Input leakage current	I_{LI}		70	µA	0 V ≤ V_{IN} ≤ V_{DD}

Table 18 S-Transceiver Characteristics

Pin	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
SX1,2	Absolute value of output pulse amplitude (V_{SX2} - V_{SX1})	V_X	2.03	2.2	2.31	V	R_L = 50 Ω
SX1,2	S-Transmitter output impedance	Z_X	10	34		kΩ	see [1]
			0				see [2][3]
SR1,2	S-Receiver input impedance	Z_R	10 100			kΩ Ω	V_{DD} = 3.3 V V_{DD} = 0 V

1) Requirement ITU-T I.430, chapter 8.5.1.1a): 'At all times except when transmitting a binary zero, the output impedance , in the frequency range of 2kHz to 1 MHz, shall exceed the impedance indicated by the template in Figure 11. The requirement is applicable with an applied sinusoidal voltage of 100 mV (r.m.s value)'

2) Requirement ITU-T I.430, chapter 8.5.1.1b): 'When transmitting a binary zero, the output impedance shall be > 20 Ω.': Must be met by external circuitry.

3) Requirement ITU-T I.430, chapter 8.5.1.1b), Note: 'The output impedance limit shall apply for a nominal load impedance (resistive) of 50 Ω. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value +/- 10%. The peak amplitude shall be defined as the the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.'

Table 19 U-Transceiver Characteristics

	Limit Values			Unit
	min.	typ.	max.	
Receive Path				
Signal / (noise + total harmonic distortion)[1]	65[2]			dB
DC-level at AD-output	45	50	55	%[3]
Threshold of level detect (measured between AIN and BIN with respect to zero signal)	4	5	16 (PEF 80912)	mV peak
			9 (PEF 80913)	
Input impedance AIN/BIN	80			kΩ
Transmit Path				
Signal / (noise + total harmonic distortion)[4]	70			dB
Common mode DC-level	1.61	1.65	1.69	V
Offset between AOUT and BOUT			35	mV
Absolute peak voltage for a single +3 or -3 pulse measured between AOUT and BOUT[5]	2.42	2.5	2.58	V
Output impedance AOUT/BOUT: Power-up Power-down		 0.8 3	 1.5 6	 Ω Ω

1) Test conditions: 1.4 Vpp differential sine wave as input on AIN/BIN with long range (low, critical range).

2) Versions PEF 8x913 with enhanced performance of the U-interface are tested with tightened limit values

3) The percentage of the "1 "-values in the PDM-signal.

4) Interpretation and test conditions: The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 70 dB below the signal for an evenly distributed but otherwise random sequence of +3, +1, -1, -3.

5) The signal amplitude measured over a period of 1 min. varies less than 1%.

4.3 Capacitances

T_A = 25 °C, 3.3 V ± 5 % V_{SSA} = 0 V, V_{SSD} = 0 V, f_c = 1 MHz, unmeasured pins grounded.

Table 20 Pin Capacitances

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Digital pads: Input Capacitance I/O Capacitance	 C_{IN} $C_{I/O}$		 7 7	 pF pF	
Analog pads: Load Capacitance	 C_L		 3	 pF	 pin AIN, BIN

4.4 Power Consumption

Power Consumption

VDD=3.3 V, VSS=0 V, Inputs at VSS/VDD, no LED connected, 50% bin. zeros, no output loads except SX1,2 (50 Ω[1])

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
Operational U and S enabled, IOM®-2 off		 235 200		 mW mW	 U: ETSI loop 1 (0 m) U: ETSI Loop 2.(typical line)
Power Down		15		mW	

1) 50 Ω (2 x TR) on the S-bus.

4.5 Supply Voltages

VDD_D = + Vdd ± 5%
VDD_A = + Vdd ± 5%

The maximum sinusoidal ripple on VDD is specified in the following figure:

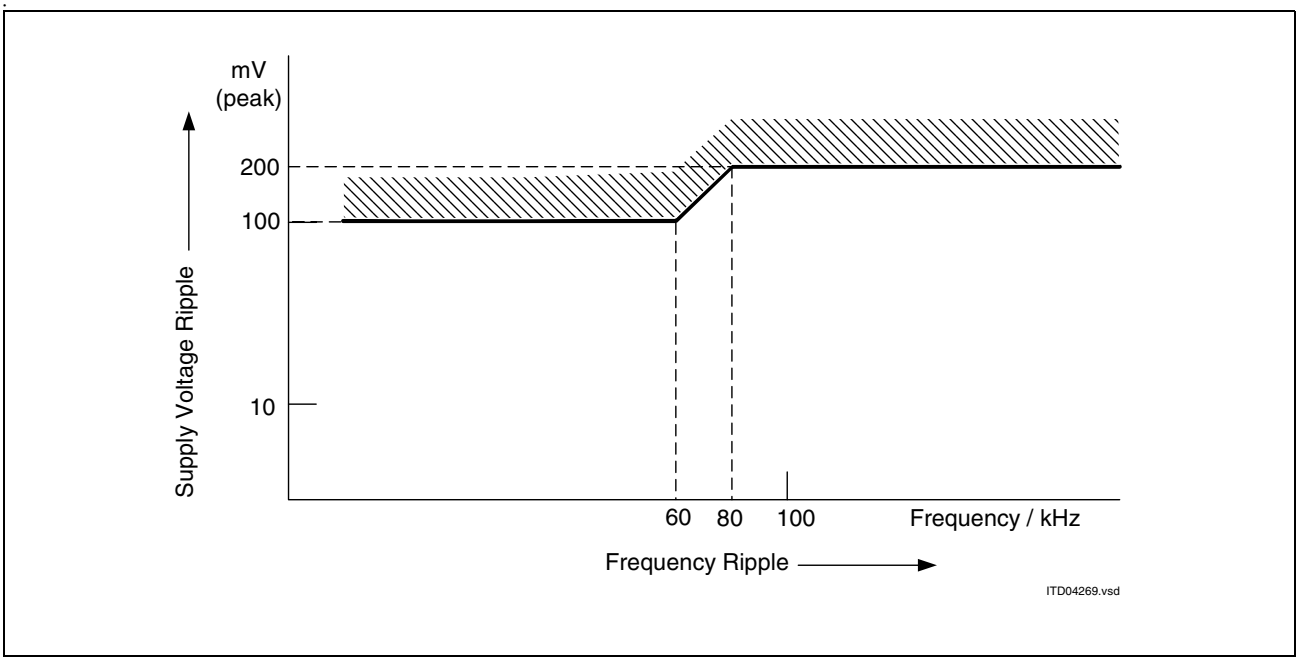


Figure 30 Maximum Sinusoidal Ripple on Supply Voltage

4.6 AC Characteristics

T_A = -40 to 85 °C, V_{DD} = 3.3 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **Figure 31**.

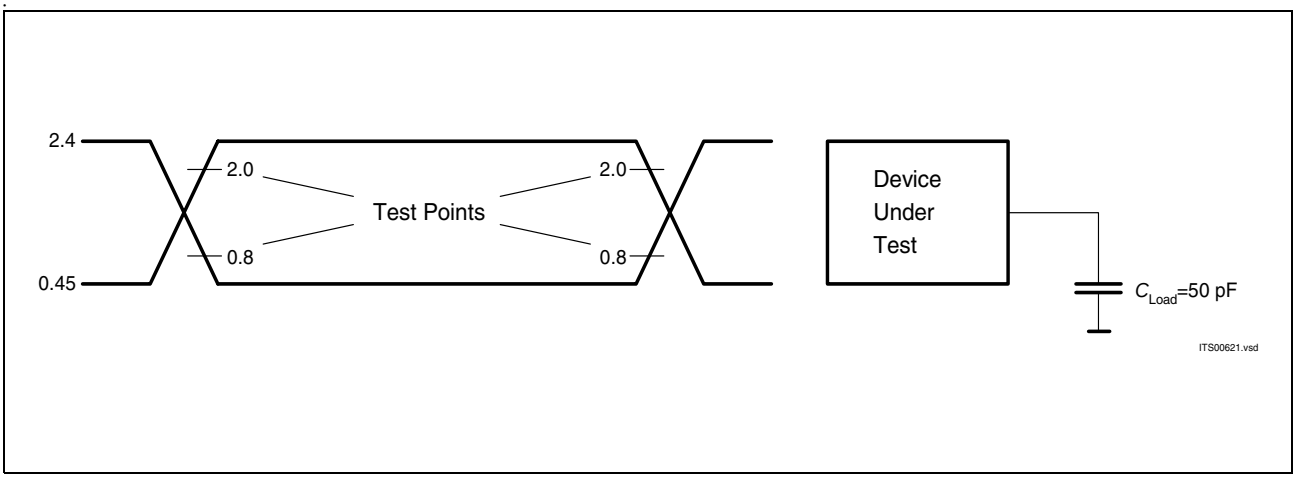


Figure 31 Input/Output Waveform for AC Tests

Parameter All Output Pins	Symbol	Limit values		Unit
		Min	Max	
Fall time			30	ns
Rise time			30	ns

4.6.1 IOM-2 Interface

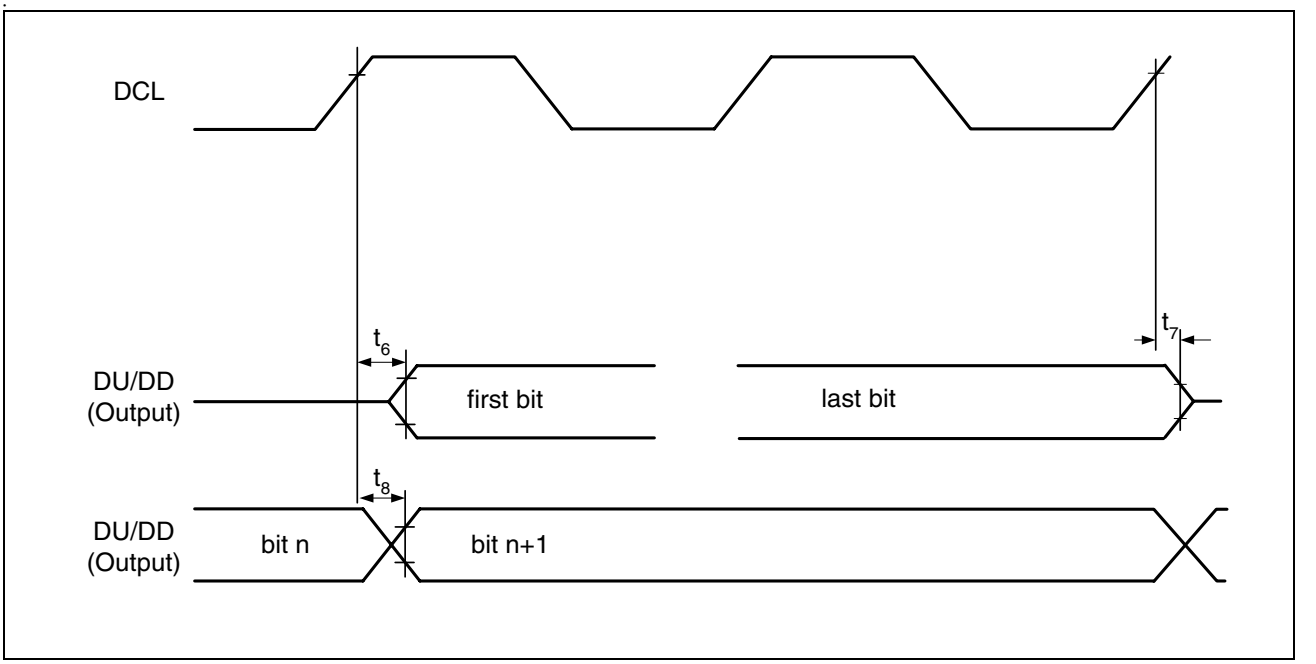


Figure 32 IOM®-2 Interface - Bit Synchronization Timing

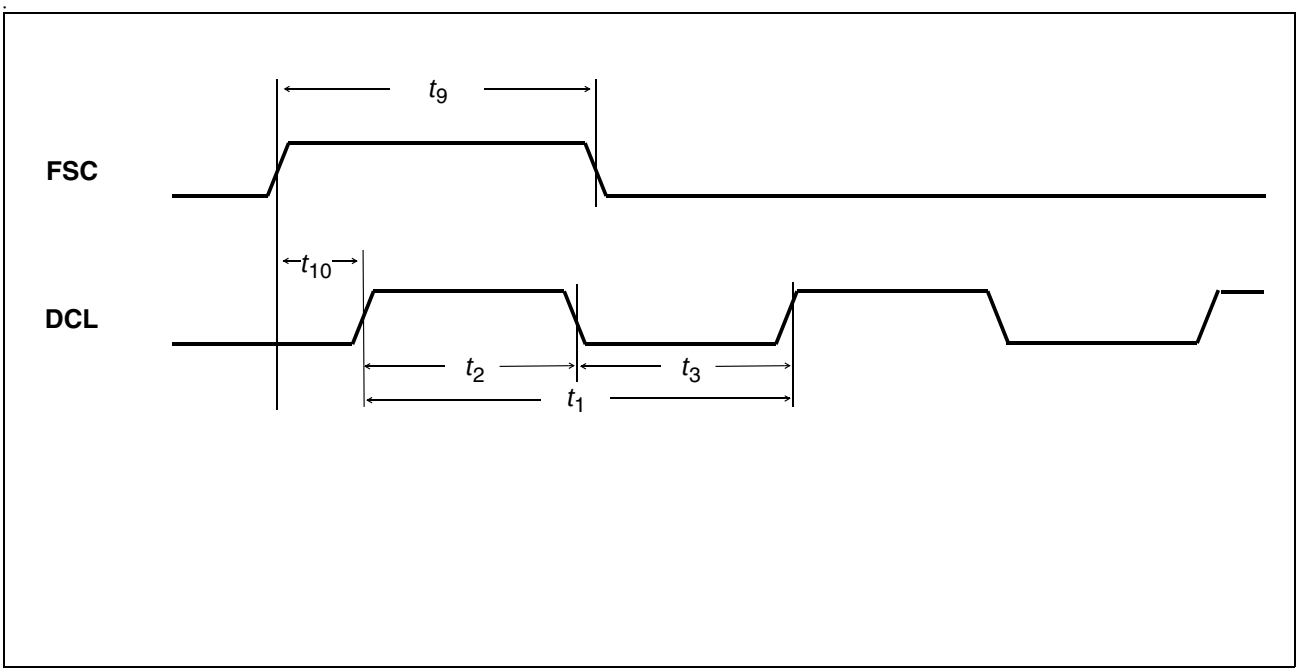


Figure 33 IOM-2 Interface - Frame Synchronization Timing

Note: At the start and end of a reset period, a frame jump may occur. This results in a DCL and FSC high time of min. 130 ns after this specific event.

Parameter IOM®-2 Interface	Symbol	Limit values			Unit
		Min	Typ	Max	
DCL period	t_1	1875	1953	2035	ns
DCL high	t_2	850	960	1105	ns
DCL low	t_3	850	960	1105	ns
Output data from high impedance to active (FSC high or other than first timeslot)	t_6			100	ns
Output data from active to high impedance	t_7			100	ns
Output data delay from clock	t_8			80	ns
FSC high	t_9		50% of FSC cycle time		ns
FSC advance to DCL	t_{10}	65	130	195	ns
DCL, FSC rise/fall	t_{15}			30	ns
Data out rise/fall (C_L = 50 pF, tristate)	t_{17}			150	ns

4.6.2 Reset

Table 21 Reset Input Signal Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Length of active low state	$t_{\overline{RST}}$	4			ms	Power On the 4 ms are assumed to be long enough for the oscillator to run correctly
		2 x DCL clock cycles + 400 ns				After Power On

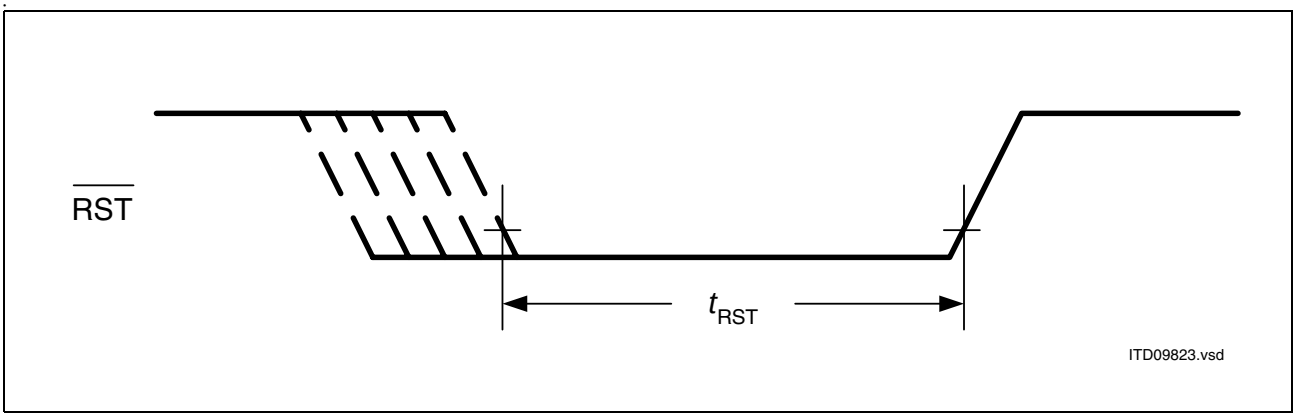


Figure 34 Reset Input Signal

4.6.3 Undervoltage Detection Characteristics

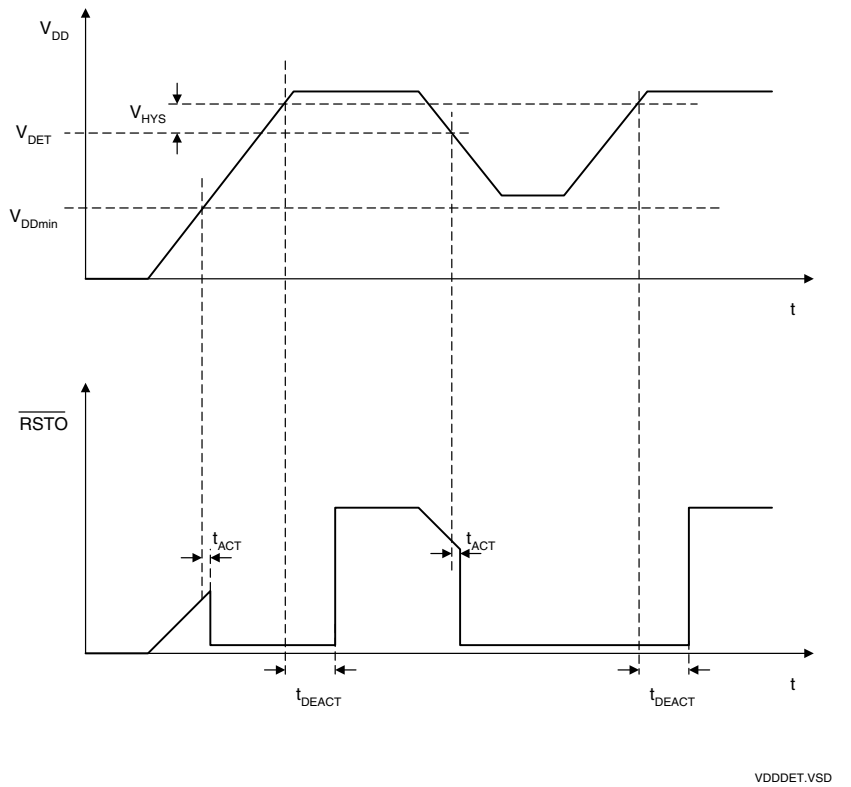


Figure 35 Undervoltage Control Timing

Table 22 Parameters of the UVD/POR Circuit

V_{DD}= 3.3 V ± 5 %; V_{SS}= 0 V; T_A = -40 to 85 °C

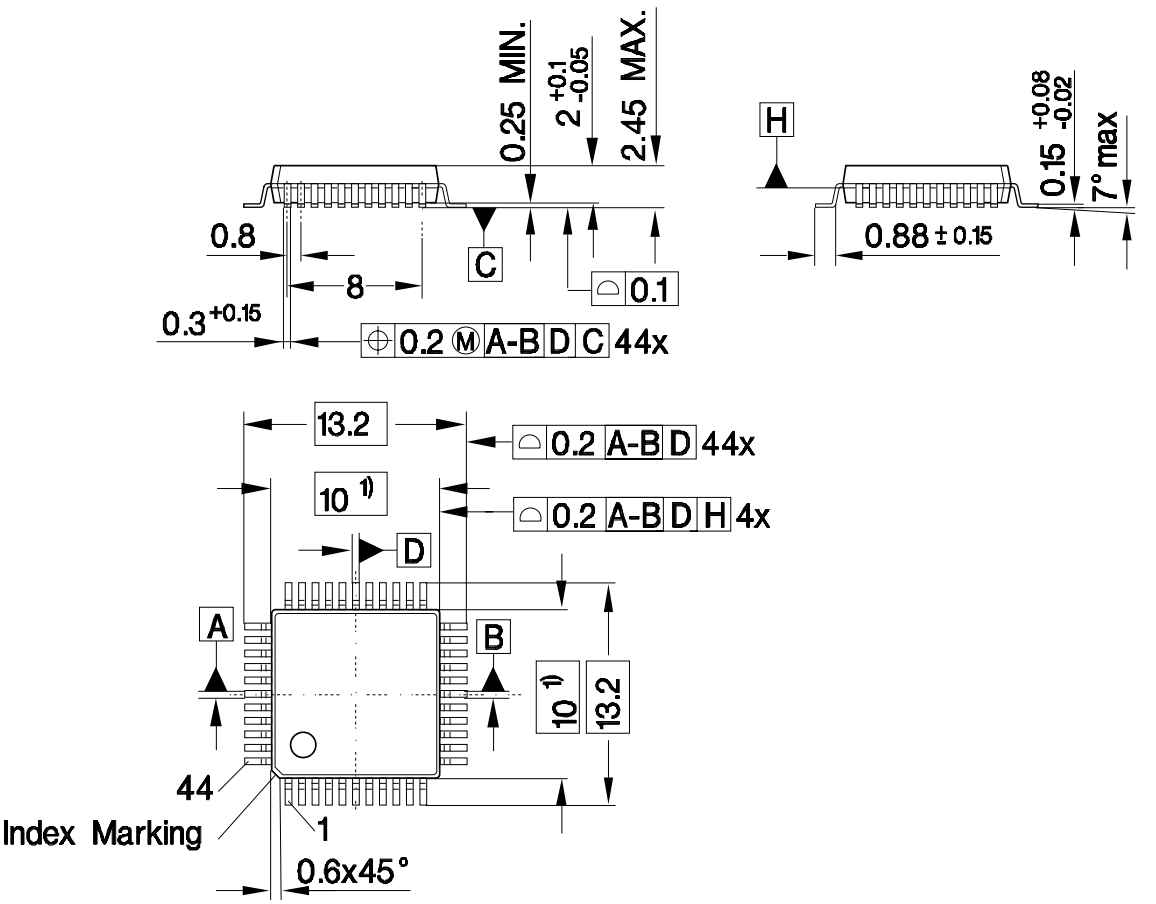
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Detection Threshold[1]	V_{DET}	2.7	2.8	2.92	V	V_{DD} = 3.3 V ± 5 %
Hysteresis	V_{Hys}	30		90	mV	
Max. rising/falling V_{DD} edge for activation/ deactivation of UVD	dV_{DD}/dt			0.1	V/µs	
Max. rising V_{DD} for power-on[2]				0.1	V/ ms	
Min. operating voltage	V_{DDmin}	1.5			V	
Delay for activation of $\overline{\text{RSTO}}$	t_{ACT}			10	µs	
Delay for deactivation of $\overline{\text{RSTO}}$	t_{DEACT}		64		ms	

1) The Detection Threshold V_{DET} is far below the specified supply voltage range of analog and digital parts of the Q-SMINT®O. Therefore, the board designer must take into account that a range of voltages is existing, where neither performance and functionality of the Q-SMINT®O are guaranteed, nor a reset is generated.

2) If the integrated Power-On Reset of the Q-SMINTO is selected ($\overline{\text{VDDDET}}$ = '0') and the supply voltage V_{DD} is ramped up from 0V to 3.3V +/- 5%, then the Q-SMINTO is kept in reset during $V_{DDmin} < V_{DD} < V_{DET} + V_{Hys}$. V_{DD} must be ramped up so slowly that the Q-SMINTO leaves the reset state after the oscillator circuit has already finished start-up. The start-up time of the oscillator circuit is typically in the range between 3ms and 12ms.

5 Package Outlines

Plastic Package, P-MQFT-44
(Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

6 Appendix: Differences between Q- and T-SMINT®O

The Q- and T-SMINT®O have been designed to be as compatible as possible. However, some differences between them are unavoidable due to the different line codes 2B1Q and 4B3T used for data transmission on the U_{k0} line.

Especially the pin compatibility between Q- and T-SMINT®O allows for one single PCB design for both series with only some mounting differences.

The following chapter summarizes the main differences between the Q- and T-SMINT®O.

6.1 Pinning

Table 23 Pin Definitions and Functions

Pin MQFT-44		Q-SMINT®O: 2B1Q	T-SMINT®O: 4B3T
10		Triple-Last-Look ($\overline{\text{TLL}}$)	Tie to ‘1‘
11		Metallic Termination Input (MTI)	Tie to ‘1‘
16		Auto U Activation (AUA)	Tie to ‘1‘
17		Cold Start Only (CSO)	Tie to ‘1‘
38		Power Status (primary) (PS1)	Tie to ‘1‘
26		Power Status (secondary) (PS2)	Tie to ‘1‘

6.2 U-Transceiver

6.2.1 U-Interface Conformity

Table 24 Related Documents to the U-Interface

Document	Q-SMINT®O: 2B1Q	T-SMINT®O: 4B3T
ETSI: TS 102 080	conform to annex A compliant to 10 ms interruptions	conform to annex B
ANSI: T1.601-1998 (Revision of ANSI T1.601-1992)	conform MLT input and decode logic	not required
CNET: ST/LAA/ELR/DNP/ 822	conform	not required
RC7355E	conform	not required
FTZ-Richtlinie 1 TR 220	not required	conform

6.2.2 U-Transceiver State Machines

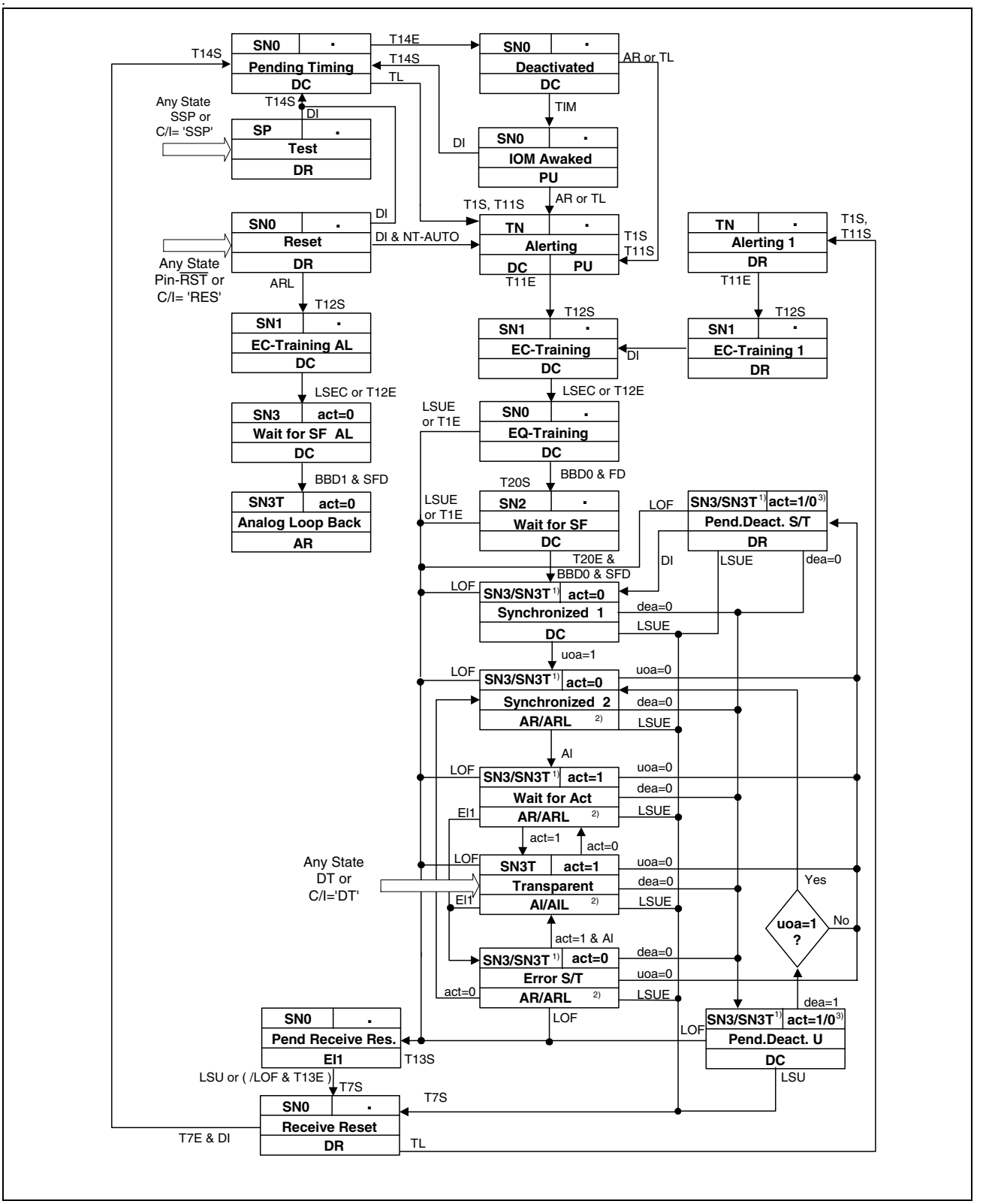


Figure 36 NTC-Q Compatible State Machine Q-SMINT®O: 2B1Q

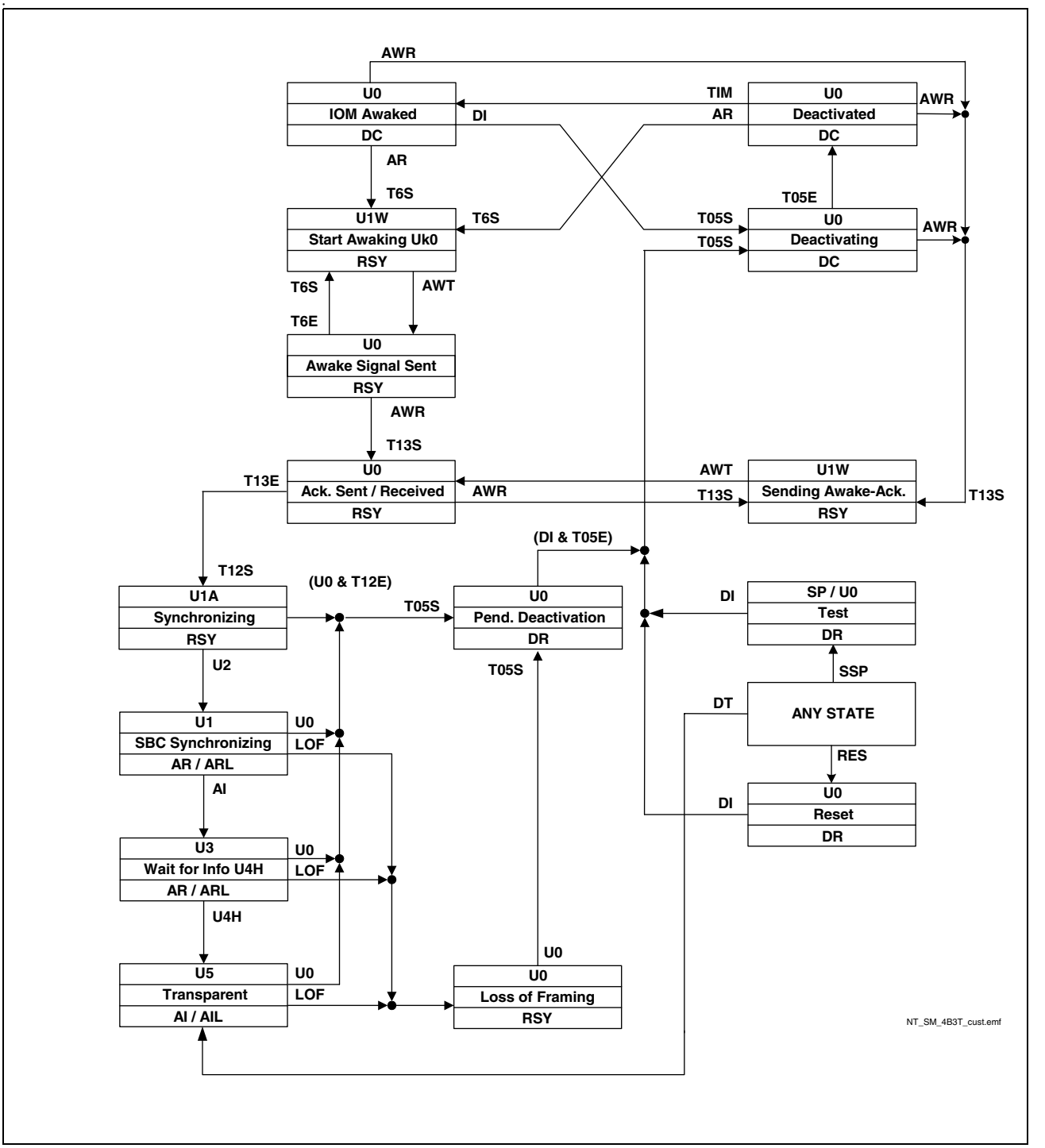


Figure 37 IEC-T/NTC-T Compatible State Machine T-SMINT®O: 4B3T

6.2.3 Command/Indication Codes

Table 25 C/I Codes

Code	Q-SMINT®O: 2B1Q		T-SMINT®O: 4B3T	
	IN	**OUT**	**IN**	**OUT**
0000	TIM	DR	TIM	DR
0001	RES	–	–	–
0010	–	–	–	–
0011	–	–	–	–
0100	EI1	EI1	–	RSY
0101	SSP	–	SSP	–
0110	DT	–	DT	–
0111	–	PU	–	–
1000	AR	AR	AR	AR
1001	–	–	–	–
1010	ARL	ARL	–	ARL
1011	–	–	–	–
1100	AI	AI	AI	AI
1101	–	–	RES	–
1110	–	AIL	–	AIL
1111	DI	DC	DI	DC

6.3 External Circuitry

The external circuitry of the Q- and T-SMINT®O is equivalent; however, some external components of the U-transceiver hybrid must be dimensioned different for 2B1Q and 4B3T. All information on the external circuitry is preliminary and may be changed in future documents.

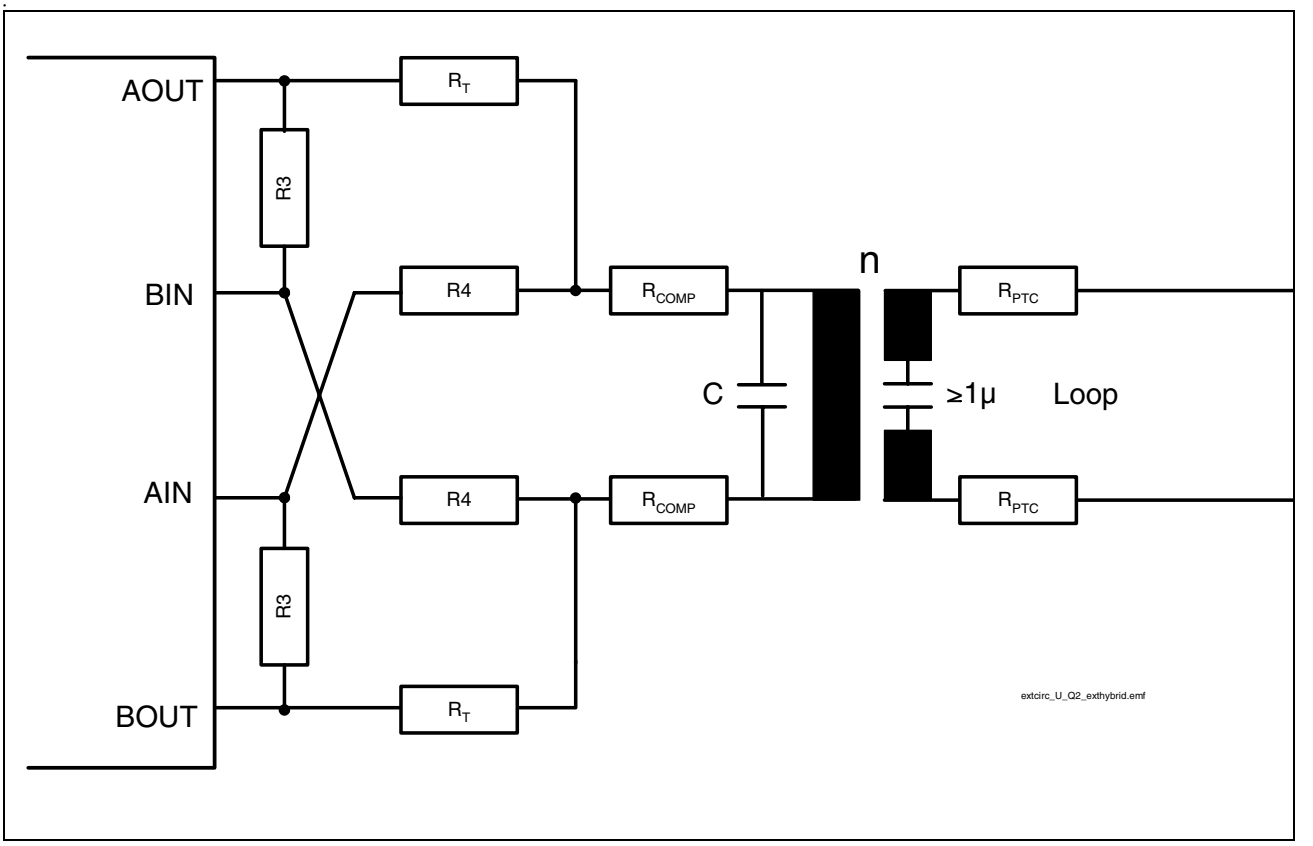


Figure 38 External Circuitry Q- and T-SMINT®O

the necessary protection circuitry is not displayed in ***Figure 38***

Appendix: Differences between Q- and T-SMINT,O

Table 26 Dimensions of External Components.

Component	Q-SMINT®O: 2B1Q	T-SMINT®O: 4B3T
Transformer: Ratio Main Inductivity	 1:2 14.5 mH	 1:1.6 7.5 mH
Resistance R3	1.3 kΩ	1.75 kΩ
Resistance R4	1.0 kΩ	1.0 kΩ
Resistance R_T	9.5 Ω	25 Ω
Capacitor C	27 nF	15 nF
R_{PTC} and R_{Comp}	$2R_{PTC} + 8R_{Comp} = 40\ \Omega$	$n^2 \times (2R_{COMP} + R_B) + R_L = 20\Omega$

7 Index

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

Published by Infineon Technologies AG