Data Sheet, DS1, April 2001

NTC-T AM Network Termination Controller (4B3T All Modes)

PEB 80900 Version 1.1

Wired Communications

Infineon technologies

Never stop thinking.

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Network Termination Controller (4B3T All Modes) **PEB 80900**
NTC-T AM

Version 1.1

1 Overview

P-TQFP-64-1

P-MQFP-64-1,

The Network Termination Controller (4B3T All Modes) NTC-T AM PEB 80900 features two fundamental modes:

- NTC-T Functionality
  When 'NTC-T functionality' is selected, the NTC-T AM PEB 80900 provides all features known from the Network Termination Controller NTC-T PEB8090 V1.1 [1].
- IEC-T Functionality
  When 'IEC-T functionality' is selected, the NTC-T AM PEB 80900 offers the full functionality of the IEC-T 4B3T two chip set PEB 20901 (IEC -TD) and PEB 20902 (IEC - TA) [2] and can hence replace the latter in all applications.

The NTC-T AM is a CMOS device which is available in a P-MQFP-64 and P-TQFP-64 package and operates from a single + 5 V supply with very low power consumption.

References

[1] NTC-T, Network Termination Controller (4B3T), PEB 8090 V1.1, Data Sheet 6.98, Siemens AG, 1998

[2] IEC-T, ISDN Echocancellation Circuit IEC-T 4B3T Two Chip Set, PEB 2090-1/2 , Target Specification 11.88, Siemens AG, 1988

Type	Package
PEB 80900	P-MQFP-64
	P-TQFP-64

1.1 Selection between NTC-T and IEC-T Functionality

The selection between NTC-T and IEC-T functionality is possible by clamping the factory test pins TP0..2:

- TP0...2 = ’000’: NTC-T functionality according to [1]
- TP0...2 = ’011’: IEC-T functionality according to [2]
- TP0...2 = ’1xx’, ’010’, ’001’: reserved

Table 1 gives an overview of functions, which are available with ’NTC-T’ and ’IEC-T-Functionality’ selected, respectively.

Table 1 Overview of ’NTC-T’ and ’IEC-T’ Functionality

Function	’NTC-T’-Funct.	’IEC-T’-Funct.
Test Pins TM0-2	’000’	’011’
U-Transceiver Statemachine		
NT-mode	+	+
LT-mode	-	+
NT-TE/NT-PABX-mode	-	+
NT-RP-mode	-	+
LT-RP-mode	-	+
S-Transceiver Statemachine		
NT-mode	+	-
IOM-1 Interface		
IOM-NT-mode (DCL = 512 kHz)	-	+
IOM-Linecard-burst-mode (DCL = 4096 kHz)	-	+
IOM-2 Interface		
IOM-NT-mode (DCL = 512 kHz)	+	-
Auxilliary IOM-2 Interface		
IOM-NT-mode (DCL = 512 kHz)	+	-
IOM-TE-mode (DCL = 1536 kHz)	+	-

1.2 Organization of the Document

The document consists of three major parts:

- Part I ’NTC-T’ specifies all features provided with NTC-T functionality selected
- Part II ’IEC-T’ specifies all features provided with IEC-T functionality selected
- Part III ’Common’ lists information, which is common to both modes

1.3 Pin Configuration of the NTC-T AM with NTC-T and IEC-T Functionality

P-TQFP-64 / P-MQFP-64

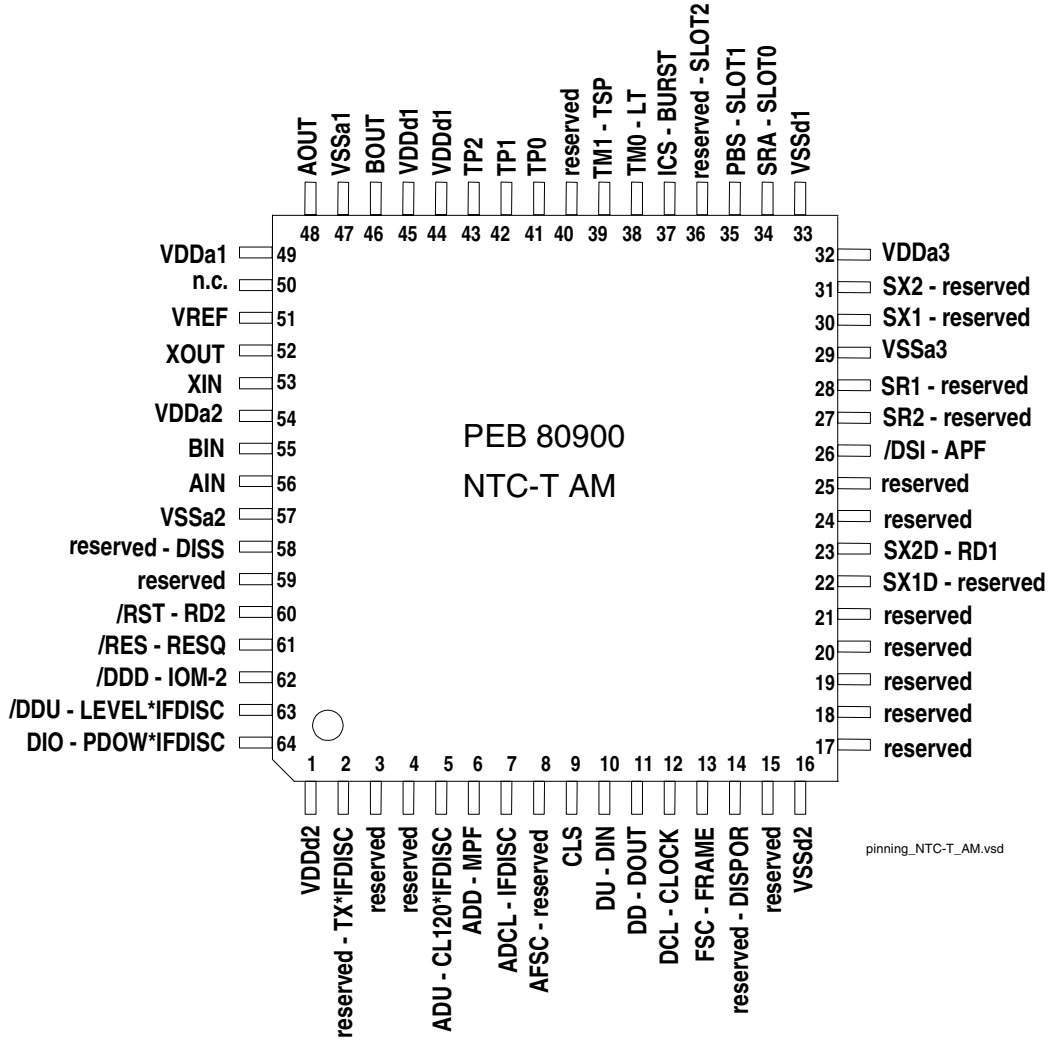


Figure 1 Pin Configuration of the NTC-T AM with NTC-T and IEC-T Functionality

Pins with different functions in NTC-T and IEC-T mode are denoted in the order: ’$function_{NTC\text{-}T}$ - $function_{IEC\text{-}T}$’.

1.4 Pin Definitions and Functions

The setting of the Factory Testpins TP0...2 influences the pin definitions and functions according to **Table 2**.

Table 2 Pin Definitions and Functions of the NTC-T AM for NTC-T and IEC-T Functionality

Pin	PEB 80900 with NTC-T Functionality			PEB 80900 with IEC-T Functionality		
	I/O	Symbol	Function	I/O	Symbol	Function
	according to [1]			according to [2]		
1		VDD_D2	+ 5 V +/- 5% supply voltage, digital		VDD_D2	+ 5 V +/- 5% supply voltage, digital
2	O	reserved	Leave open	O	IFDISC=0: reserved	Leave open
					IFDISC=1: TX	120 kHz Clock Output (from IEC-TD)
3	O	reserved	Leave open	O	reserved	Leave open
4	O	reserved	Leave open	O	reserved	Leave open
5	I/O	ADU	Auxiliary Data Upstream	I	IFDISC=0: reserved	Tie to VSS_D
					IFDISC=1: CL 120	120 kHz Clock Input (to IEC-TA)
6	I/O	ADD	Auxiliary Data Downstream	I	MPF	Monitor Power Feed
7	I	ADCL	Auxiliary Data Clock	I	IFDISC	Interface Disconnect
8	I	AFSC	Auxiliary Frame Synchronization Clock	I	reserved	Tie to VSS_D
9	O	CLS	Clock Signal	I/O	CLS	LT: Power Feed Off Signal from Power Controller NT/TE: Clock Output
10	I/O	DU	Data Upstream	I	DIN	IOM Data Input
11	I/O	DD	Data Downstream	O	DOUT	IOM Data Output
12	O	DCL	Data Clock	I/O	CLOCK	Double IOM Clock
13	O	FSC	Frame Synchronization Clock	I/O	FRAME	IOM Frame Signal

Table 2 Pin Definitions and Functions of the NTC-T AM for NTC-T and IEC-T Functionality (cont'd)

Pin	PEB 80900 with NTC-T Functionality			PEB 80900 with IEC-T Functionality		
	I/O	Symbol	Function	I/O	Symbol	Function
	according to [1]			according to [2]		
14	I	reserved	Tie to VSS_D	I	DISPOR	Disable Power-On Reset
15	I	reserved	Tie to VSS_D	I	reserved	Tie to VSS_D
16		VSSD2	Digital GND		VSSD2	Digital GND
17	I	reserved	Tie to VSS_D	I	reserved	Tie to VSS_D
18	I	reserved	Tie to VSS_D	I	reserved	Tie to VSS_D
19	I	reserved	Tie to VSS_D	I	reserved	Tie to VSS_D
20	I	reserved	Tie to VSS_D.	I	reserved	Tie to VSS_D.
21	I	reserved	Tie to VSS_D.	I	reserved	Tie to VSS_D.
22	O	SX1D	S/T-interface positive transmit output, digital	O	reserved	Leave open
23	O	SX2D	S/T-interface negative transmit output, digital	O	RD1	Relay Driver Pin 1
24	O	reserved	Leave open.	O	reserved	Leave open
25	O	reserved	Leave open.	O	reserved	Leave open
26	I	$\overline{DSI}$	Digital S-Interface Transmitter	I	APF	Alarm Power Feed
27	I	SR2	Differential S/T-interface receive input	I		Tie to VSS_A
28	I	SR1	Differential S/T-interface receive input	I		Tie to VSS_A
29		VSSA3	Analog GND		VSSA3	Analog GND
30	O	SX1	S/T-interface positive transmit output	O		Leave open
31	O	SX2	S/T-interface negative transmit output	O		Leave open
32		VDDA3	+ 5 V +/- 5% supply voltage, analog		VDDA3	+ 5 V +/- 5% supply voltage, analog
33		VSSD1	Digital GND		VSSD1	Digital GND

Table 2 Pin Definitions and Functions of the NTC-T AM for NTC-T and IEC-T Functionality (cont'd)

Pin	PEB 80900 with NTC-T Functionality			PEB 80900 with IEC-T Functionality		
	I/O	Symbol	Function	I/O	Symbol	Function
	according to [1]			according to [2]		
34	I	SRA	S-Receiver Amplifier	I	SLOT0	Selection of Different 256 kbit/s Modes/ Time Slot Selection
35	I PU	PBS	Point-to-point / Bus Selection	I	SLOT1	Selection of Different 256kbit/s Modes/ Time Slot Selection
36	I	reserved	Tie to VSS_D.	I	SLOT2	Selection of Different 256kbit/s Modes/ Time Slot Selection
37	I	ICS	IOM®-2 Channel S-Transceiver	I	BURST	Burst Mode
38	I PU	TM0	Test Mode 0	I	LT	NT/LT Mode
39	I PU	TM1	Test Mode 1	I	TSP	Test Single Pulses
40	I	reserved	Tie to VSS_D	I	reserved	Tie to VSS_D
41	I	TP0	Factory Testpin. Tie to VSS_D.	I	TP0	see **Chapter 1.1**
42	I	TP1	Factory Testpin. Tie to VSS_D.	I	TP1	
43	I	TP2	Factory Testpin. Tie to VSS_D.	I	TP2	
44		VDD_D1	+ 5 V +/- 5% supply voltage, digital		VDD_D1	+ 5 V +/- 5% supply voltage, digital
45		VDD_D1	+ 5 V +/- 5% supply voltage, digital		VDD_D1	+ 5 V +/- 5% supply voltage, digital
46	O	BOUT	Differential U-interface output	O	BOUT	Differential U-interface output
47		VSS_A1	Analog GND		VSS_A1	Analog GND
48	O	AOUT	Differential U-interface output	O	AOUT	Differential U-interface output

Table 2 Pin Definitions and Functions of the NTC-T AM for NTC-T and IEC-T Functionality (cont'd)

Pin	PEB 80900 with NTC-T Functionality			PEB 80900 with IEC-T Functionality		
	I/O	Symbol	Function	I/O	Symbol	Function
	according to [1]			according to [2]		
49		VDDA1	+ 5 V +/- 5% supply voltage, analog		VDDA1	+ 5 V +/- 5% supply voltage, analog
50		n.c.	Leave open		n.c.	Leave open
51	I/O	VREF	Reference Voltage. Connect 100 nF vs. VSSA to buffer internally generated reference voltage.	I/O	VREF	Reference Voltage. Connect 100 nF vs. VSSA to buffer internally generated reference voltage.
52	O	XOUT	Crystal OUT. Connect a 15.36 MHz crystal	O	XOUT	Crystal OUT. Connect a 15.36 MHz crystal
53	I	XIN	Crystal IN. Connect a 15.36 MHz crystal	I	XIN	Crystal IN. Connect a 15.36 MHz crystal
54		VDDA2	+ 5 V +/- 5% supply voltage, analog		VDDA2	+ 5 V +/- 5% supply voltage, analog
55	I	BIN	Differential U-interface input	I	BIN	Differential U-interface input
56	I	AIN	Differential U-interface input	I	AIN	Differential U-interface input
57		VSSA2	Analog GND		VSSA2	Analog GND
58	O	reserved	Leave open	O	DISS	Disable Supply
59	O	reserved	Leave open	O	reserved	Leave open
60	O	$\overline{\text{RST}}$	Reset Output	O	RD2	Relay Driver Pin 2
61	I	$\overline{\text{RES}}$	Reset Input	I	RESQ	Power On Reset
62	I	$\overline{\text{DDD}}$	Disconnect Data Downstream	I	IOM2	Tie to VSSD

Table 2 Pin Definitions and Functions of the NTC-T AM for NTC-T and IEC-T Functionality (cont'd)

Pin	PEB 80900 with NTC-T Functionality			PEB 80900 with IEC-T Functionality		
	I/O	Symbol	Function	I/O	Symbol	Function
	according to [1]			according to [2]		
63	I	$\overline{\text{DDU}}$	Disconnect Data Upstream	I	IFDISC=0: reserved	Tie to V_{SSD}
					IFDISC=1: LEVEL	Awake Signal Detection (input to IEC-TD)
64	I	DIO	Disable IOM®-2	I	IFDISC=0: reserved	Tie to V_{SSA}
					IFDISC=1: PDOW	Power Down (input to IEC-TA)

1.4.1 Special Pin IFDISC: Interface Disconnect (Available only with TP0..2 = '011')

The IEC-T is available only in a two-chip set (IEC-TA and IEC-TD). Therefore, signals between the IEC-TA and IEC-TD may be accessed for special applications (e.g. repeater application). In contrast to the IEC-T, the NTC-T AM is delivered in a single package. Access to signals corresponding to those between IEC-TA and IEC-TD may be selected with pin IFDISC:

– With TP0...2 = '011' and IFDISC = '0' selected, all user interfaces of the IEC-T are accessible, but no signals corresponding to those between IEC-TA and IEC-TD.
– By setting TP0...2 = '011' and IFDISC = '1', all user interfaces of the IEC-T are accessible, too. In addition, some important signals of the internal interface between IEC-TD and IEC-TA are disconnected and accessible externally. In this case, the user must take care to apply the corresponding inputs for proper operation.

1.5 Functional Differences between PEB 80900 with IEC-T Functionality and PEB 20901/2

1.5.1 Data Output on IOM

Pin 23 ’DOUT: IOM data output synchronous to CLOCK’ of the IEC-TD PEB 20901 operates always in open-drain mode. In contrast to PEB 20901, pin 11 of the NTC-T AM PEB 80900 with IEC-T functionality selected operates always in push-pull mode (see also **Chapter 6.3.2**). Especially in modes with DOUT operating in burst mode, pin 11 drives during inactive timeslots a logical ’1’.

This difference must be taken into account, when an NTC-T AM with IEC-T functionality selected shall be connected to an IOM bus configuration. In this case, the different data output lines must be ANDed with external logic.

1.5.2 Power-On Reset and Undervoltage Detection

In addition to the IEC-T PEB 20901/2, the NTC-T AM PEB 80900 with IEC-T functionality provides the Power-On Reset and Undervoltage detection function as specified in Ref. [1]. It can be disabled by setting DISPOR = ’1’.

1.5.3 External Circuitry for Connection to the U-Interface

The IEC-TA PEB 20902 is connected to the twisted pair of the U-interface via an external hybrid. In contrast, the NTC-T AM provides an integrated U-interface hybrid for both NTC-T and IEC-T mode. The recommended external circuitry is displayed in **Chapter 8.2.2**.

1.6 Editorial Changes between the IEC-T Target Specification [2] and Part II 'IEC-T' of the NTC-AM Data Sheet

"Part II 'IEC-T': General Description" on Page 69

Removed: 'At present, the IEC is available in a two chip set only.'

"Basic System Functions" on Page 70

Removed: 'Low power consumption:
Standby:max. 20 mW
Active:max. 250 mW'

Removed: '40 pin DIL package or 44 pin PLCC package.'

Reworked pin configuration

"Related Documents" on Page 73

The following documents have been removed from the list 'Related Documents':

- Technische Lieferbedingungen 163 TL 31 für digitale Fernsprechvermittlungstechnik EWSD/0
- Technische Lieferbedingungen 163 TL 311 für die Anpassung EWSD/0 an ISDN
- Technische Lieferbedingungen Basisanschluss-Multiplexgerät (BAMX)
- FTZ-Richtlinie 1 TR 211, Speisekonzept für den Basisanschluss
- FTZ-Richtlinie 1 TR 212, Prüfen und Messen von digitalen Anschlüssen
- IC's for Telecommunications, IOM®-ISDN oriented Modular Interface Edition 5.86

The documentation for ICC and SBC is updated.

"IOM, Concept and Applications of the IEC" on Page 75

According to the Delta Sheet IEC-T/D PEB 20901 Version 5.1, the IOM-2 mode is not functional in any version of PEB 20901. Therefore, the whole part II of this document refers only to IOM-1 mode.

"Interfaces" on Page 78

Updated pinning in all figures and table.

"Mode Dependent Functions" on Page 88

Removed all IOM-2 modes

"Data and Clocks in NT, NT-RP, NT-TE1 Mode" on Page 90

CLS output: .

NT, NT-RP: 7.68 MHz clock, synchronized to received data on Uk0.
NT-TE1: 1.536 MHz, synchronized to received data on Uk0.

"Suggestion for the Generation of the Master Clock in the Repeater" on Page 103

Reworked figure for NTC-T AM.

"Remote Control of Loop 4 and Loop 2 by the NTC-T AM with IEC-T Functionality Selected" on Page 107

Added Note: ’The IEC in NT mode does not close loop2 itself.

NT-RP: The polarity of the E-bit is high when detecting positive M-symbols and low when detecting negative or zero M symbols.

“Monitoring of Code Violations” on Page 108
LT-RP: The polarity of the E-bit is high when detecting positive M-symbols.

“Access to MONITOR Channel in the IOM,-1 Mode” on Page 111
Detection of a valid command in the MONITOR channel will be acknowledged by setting the E Bit to 0 in the frame containing the response.

“Summary of IOM, Control Informations in Different Applications” on Page 129
Added FJ in NT and NT-RP mode (in table and state diagrams).

“Control of the Analog Loop and Loop Commands on Uk0” on Page 138
ARL: removed: ’(in the C/I channel input or RESQ pin low) always causes the chip to be reset.’

2 Part I 'NTC-T': Overview

The NTC-T AM with NTC-T functionality selected is a Network Termination (NT) circuit for the basic rate Integrated Services Digital Network (ISDN). It combines a U-transceiver and an S-transceiver on one chip. The NTC-T AM with NTC-T functionality selected provides the 4B3T U-interface as defined by FTZ Guideline 1TR 220, ETSI ETR 080 1995 together with the S/T-interface as specified in ITU Rec. I.430 and ETS 300 012.

The NTC-T AM with NTC-T functionality selected works as a stand-alone NT1 with completely automatic handling of all layer-1 procedures without a microcontroller. It transparently exchanges the 144 kbit/s user data rate between the U- and the S/T-interface (see [1]).

An optional IOM-2 interface and various test modes ease chip evaluation and testing.

2.1 Features

- Single chip solution including U- and S-transceiver
- Perfectly suited for the NT1 in the ISDN
- Fully automatic activation and deactivation of U_{k0} interface and S/T-interface
- U-interface (4B3T) conform to the FTZ Guideline 1 TR 220 of the Deutsche Telekom AG (DTAG) and ETR 080 of ETSI:
  - 4B3T ternary block code
  - Meets all transmission requirements on all ETSI and FTZ loops with margin
  - Function compatible to IEC-T
- S/T-interface conform to ITU Rec. I.430 and ETS 300 012:
  - Meets and exceeds all FTZ and ETSI transmission requirements
  - Supports point-to-point and bus configurations
  - Function compatible to SBCX
- Minimized external component count:
  - Integrated U interface hybrid
  - Integrated pull-up resistors
  - On-chip reset generation at power-on and undervoltage detection; no external components needed.
- IOM-2 interface eases chip testing and design of an Intelligent NT
- Single 5 Volt power supply
- Low power CMOS technology with power-down mode
- 240 mW typical power consumption with random data over typical lines

2.2 Logic Symbol

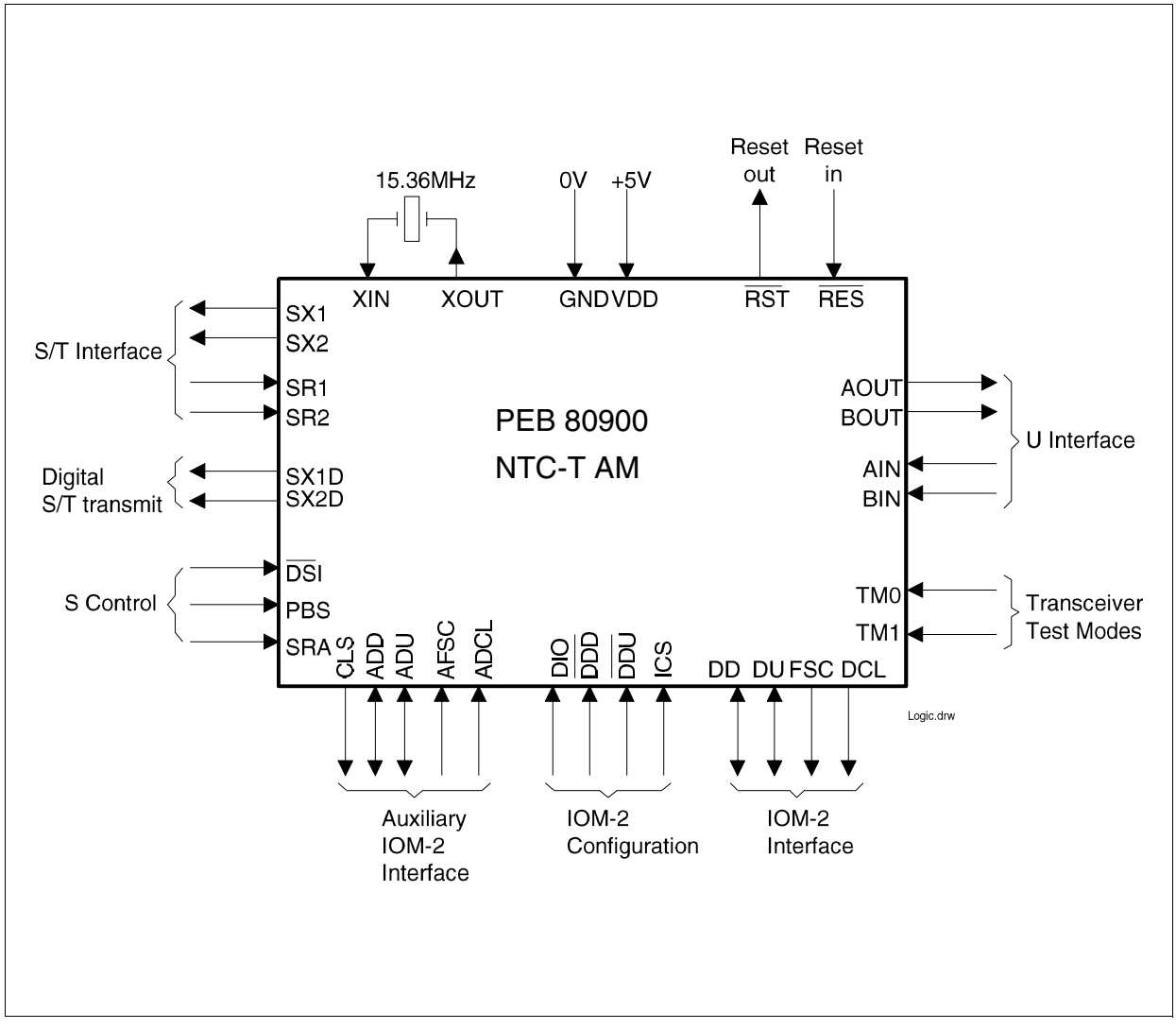


Figure 2 Logic Symbol

2.3 Pin Configuration of the NTC-T AM with NTC-T Functionality

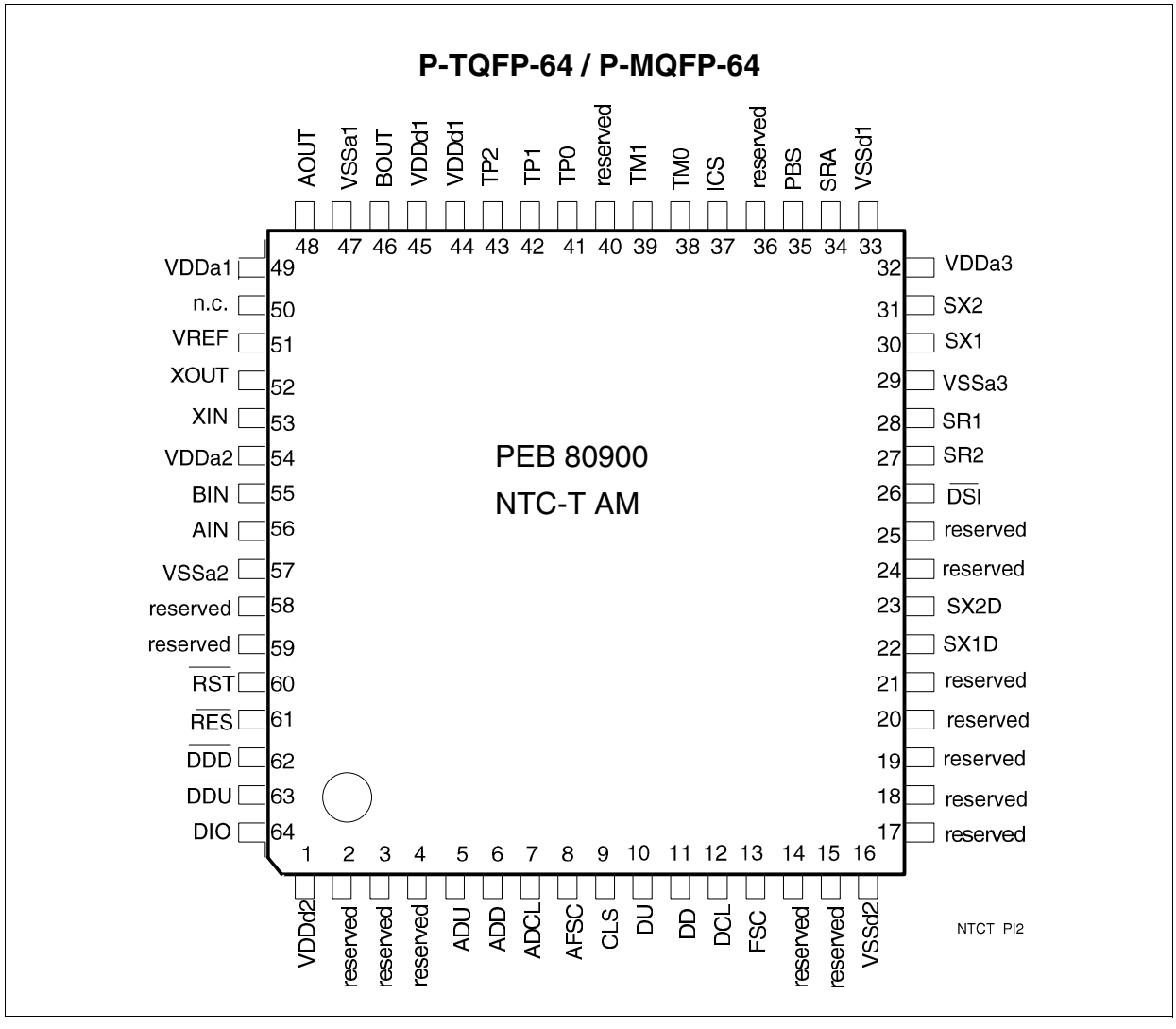


Figure 3 Pin Configuration of the NTC-T AM with NTC-T Functionality

2.4 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type and a brief description of the function.

Pin No.	Symbol	I/O	Description
Power Supply Pins			
1, 44, 45 32, 49, 54	V_{DD}D1-2 V_{DD}A1-3		+ 5 V +/- 5% supply voltage, digital + 5 V +/- 5% supply voltage, analog
16, 33 29, 47, 57	V_{SS}D1,2 V_{SS}A1-3		Digital GND Analog GND
U-Interface			
48	AOUT	O	Differential U-interface output
46	BOUT	O	Differential U-interface output
56	AIN	I	Differential U-interface input
55	BIN	I	Differential U-interface input
S/T-Interface			
30	SX1	O	S/T-interface positive transmit output
31	SX2	O	S/T-interface negative transmit output
28	SR1	I	Differential S/T-interface receive input
27	SR2	I	Differential S/T-interface receive input
22	SX1D	O	S/T-interface positive transmit output, digital
23	SX2D	O	S/T-interface negative transmit output, digital
IOM®-2 interface			
11	DD	I/O	**Data Downstream.** IOM-2 data downstream synchronous to DCL clock. High Z in normal operation. Push-pull or input in other IOM-2 configurations (**Figure 8** and **Figure 9**). Leave open if not used.

Pin No.	Symbol	I/O	Description
10	DU	I/O	**Data Upstream.** IOM-2 data upstream synchronous to DCL clock. High Z in normal operation. Push-pull or input in other IOM-2 configurations (**Figure 8** and **Figure 9**). Leave open if not used.
13	FSC	O	**Frame Synchronization Clock.** The start of the B1 channel in time slot 0 is marked with the rising edge. Leave open if not used.
12	DCL	O	Data Clock. 512 kHz, equals twice the data rate. Leave open if not used.
6	ADD	I/O	**Auxiliary Data Downstream.** Open drain if DDU=DDD=0 (**Table 3**), otherwise High Z. Gives IOM-2 access to the S-transceiver. Leave open if not used.
5	ADU	I/O	**Auxiliary Data Upstream.** Open drain if DDU=DDD=0 (**Table 3**), otherwise High Z. Gives IOM-2 access to the S-transceiver. Leave open if not used.
8	AFSC	I	**Auxiliary Frame Synchronization Clock.** Only active if DDU=DDD=0. Delivers FSC to the S-transceiver. May be connected to pin FSC or to a separate 8 kHz clock. Clamp to '1' for normal operation.
7	ADCL	I	**Auxiliary Data Clock.** Only active if DDU=DDD=0. Delivers DCL to the S-transceiver. May be connected to pin DCL or to a separate clock. Accepts 512 kHz to 4.096 MHz. Clamp to '1' for normal operation.
9	CLS	O	Clock Signal Only active if both IOM-2 interfaces are enabled (DDU = DDD = 0) and the S-transceiver operates in IOM-2 channel 1 (ICS=0). Delivers a 7.68 MHz clock synchronous to the U- and IOM-2 interface. Leave open for normal operation.

Pin No.	Symbol	I/O	Description
Control and Status Pins			
38	TM0	I (PU)	Test Mode 0 Selects the transceiver test mode (**Table 10**). Connected to a switch or left open for normal operation. Internal pull-up.
39	TM1	I (PU)	Test Mode 1 Selects the transceiver test mode (**Table 10**). Connected to a switch or left open for normal operation. Internal pull-up.
64	DIO	I	Disable IOM®-2 A '1' disables IOM-2. See also **Table 3**.
63	$\overline{\text{DDU}}$	I	Disconnect Data Upstream Selects the IOM-2 configuration (**Table 3**). Clamp to '1' for normal operation.
62	$\overline{\text{DDD}}$	I	Disconnect Data Downstream Selects the IOM-2 configuration (**Table 3**). Clamp to '1' for normal operation.
35	PBS	I (PU)	Point-to-point / Bus Selection. '1' selects point-to-point mode of the S-receiver, '0' selects bus mode. Internal pull-up.
37	ICS	I	IOM®-2 Channel S-Transceiver Only active if both IOM-2 interfaces are enabled ($\overline{\text{DDU}}$ = $\overline{\text{DDD}}$ = 0). Clamp to '1' for normal operation. '0' maps S-transceiver to IOM-2 channel 1. The S transceiver uses the LT-S state machine. '1' maps S-transceiver to IOM-2 channel 0. The S transceiver uses the NT state machine.
34	SRA	I	S-Receiver Amplifier. '1' selects internal 1:1 amplifier ratio for connection of a 2:1 transformer to pins SR1/2. '0' selects internal 2:1 amplifier ratio for connection of a 2nd generation ISFC to pins SR1/2.

Pin No.	Symbol	I/O	Description
26	$\overline{\text{DSI}}$	I	Digital S-Interface Transmitter '1' enables the analog S-transmitter pins SX1/2 for connection of a transformer. The digital pins SX1D and SX2D are disabled. '0' enables the digital S-transmitter to connect a 2nd generation ISFC to SX1/2D. The analog pins SX1 and SX2 are disabled.
61	$\overline{\text{RES}}$	I	Reset Input. Active low. Tie to '1' if not used.
60	$\overline{\text{RST}}$	O	Reset Output Active low. Is set to '0' when internal power-on reset or undervoltage detection are active.

Miscellaneous Pins

53	XIN	I	Crystal IN. Connect a 15.36 MHz crystal.
52	XOUT	O	Crystal OUT. Connect a 15.36 MHz crystal.
51	VREF	I/O	Reference Voltage. Connect 100 nF vs. VSS_A to buffer internally generated reference voltage.

Factory Test Pins and reserved

41, 42, 43	TP0..2	I	**Factory Testpins** Tie to '000' for NTC-T functionality (see **Chapter 1.1**)
2, 3, 4, 24, 25, 58, 59	reserved	O	Leave open.
14, 15, 17, 18, 19, 20, 21, 36, 40	reserved	I	Tie to VSS_D.
50	n.c.		Leave open

PU: integrated pull-up resistor

2.5 System Integration

The NTC-T AM with NTC-T functionality selected provides the NT1 function of the ITU reference model (**Figure 4**). It translates the ISDN user data (2B+D) from the format used on the two wire U-interface to the four wire S/T-interface and vice versa. Note that the NT2 is optional and the S- and the T-reference points are physically identical.

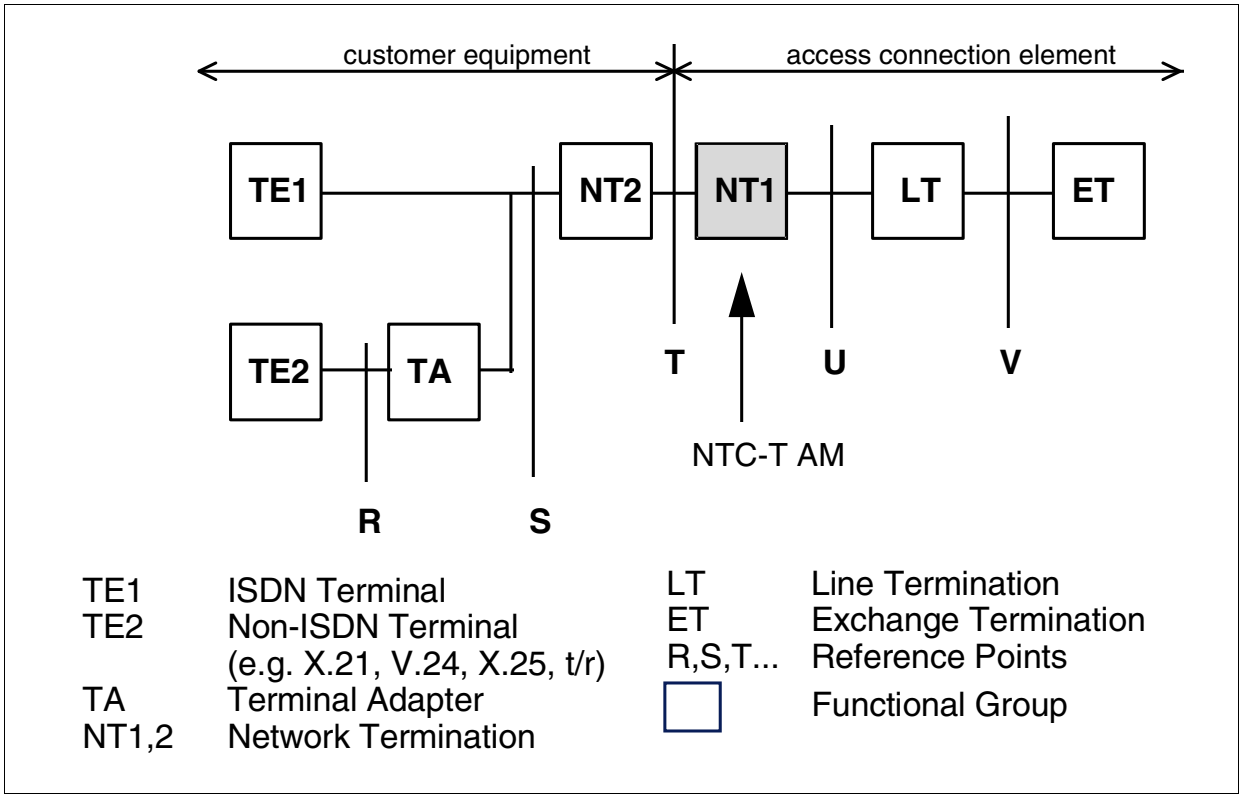


Figure 4 ITU Reference Model with NTC-T AM as NT1

Figure 5 shows a block diagram of the NTC-T AM with NTC-T functionality selected in an NT1 application. Configuration pins that are not connected directly to 5 V or GND (e.g. to a switch) have internal pull-up resistors. The S-transceiver timing mode may be switched between point-to-point and bus configuration (pin PBS). Two test patterns on the S-bus (2 kHz, 96 kHz) and one on the U interface (single pulses) can be generated via pin strapping of TM0 and TM1.

The communication between the S-transceiver and the U-transceiver can be monitored on a 512 kHz IOM-2 interface. The IOM-2 interface can be disabled to minimize power consumption (pin DIO). The power-on reset (POR) and undervoltage detection (UVD) circuit does not require any external components.

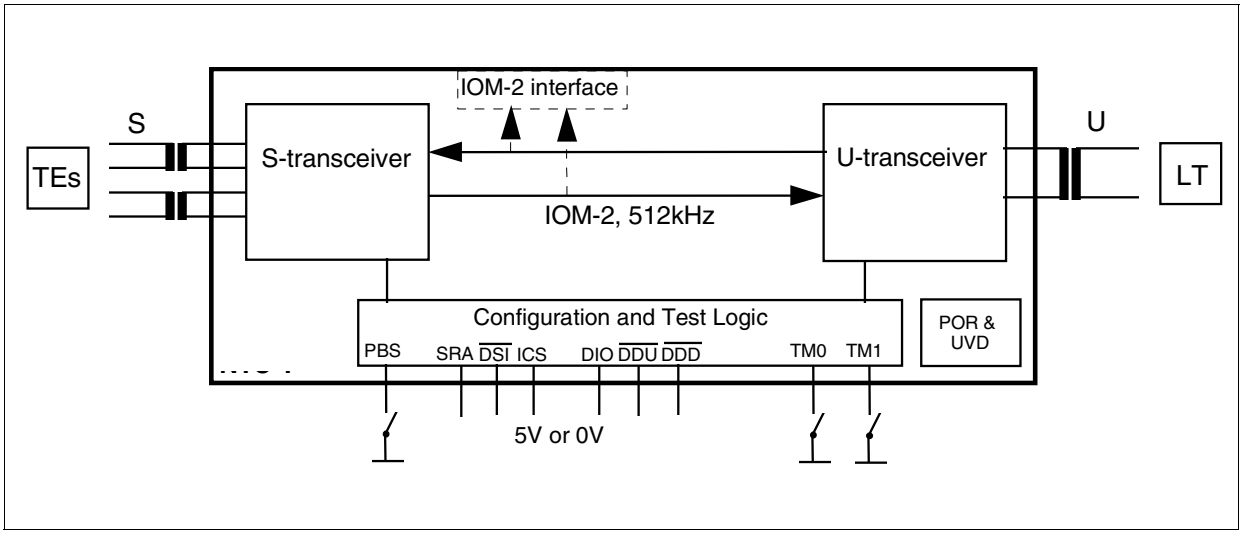


Figure 5 NTC-T AM with NTC-T Functionality Selected in NT1 Application

Figure 5 shows the NTC-T AM with NTC-T functionality selected in a typical NT1 application using the PEB2023 DC/DC converter.

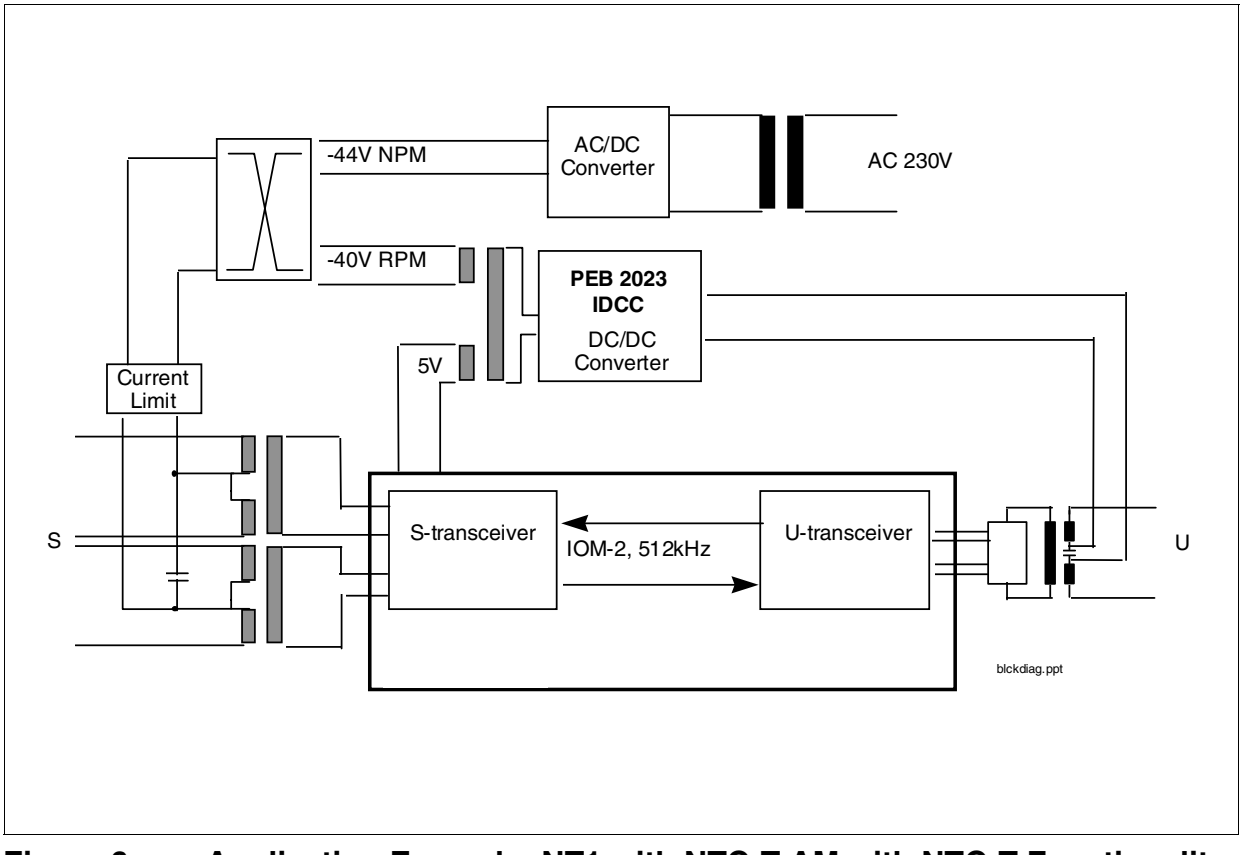


Figure 6 Application Example: NT1 with NTC-T AM with NTC-T Functionality Selected and IDCC

3 Part I 'NTC-T': Functional Description

3.1 Device Architecture

The NTC-T AM with NTC-T functionality selected contains the following interfaces and functional blocks:

- U-Transceiver (IEC-T Core) see Page 31
- S-Transceiver (SBCX Core) Page 48
- IOM-2 Interface Page 24
- Auxiliary IOM-2 Interface Page 24
- IOM-2 Control Unit Page 24
- Clock Generation Page 68
- Power-on reset, undervoltage detection Page 158
- Test Mode Unit Page 61
- Factory Test Unit

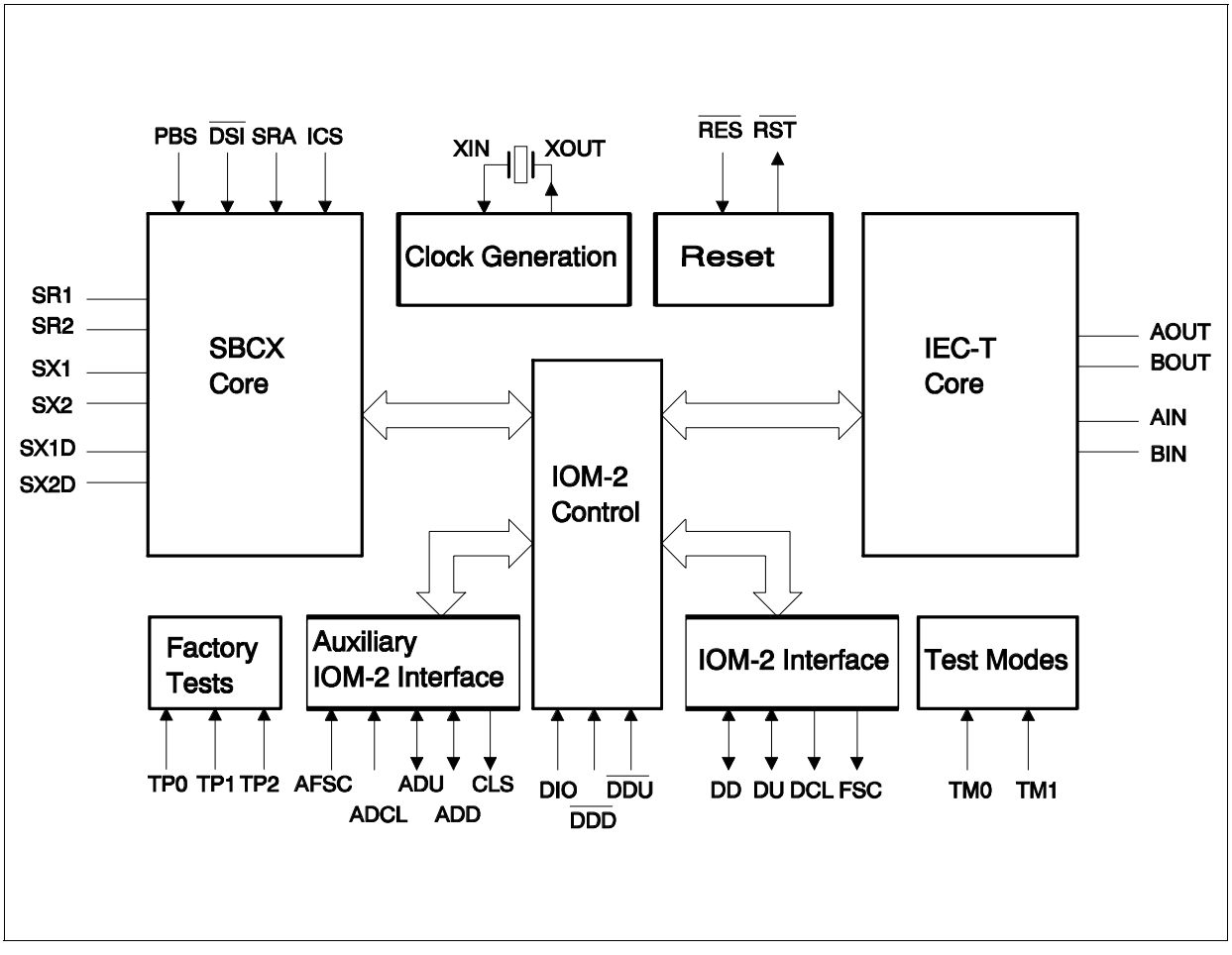


Figure 7 NTC-T AM with NTC-T Functionality Selected Device Architecture

3.2 IOM®-2 Interface

The IOM-2 interface may be used to monitor the interaction between the U- and the S-transceiver. It provides a symmetrical full-duplex communication link, containing user data, control/programming and status channels. The structure used follows the 2B + 1D-channel structure of ISDN. The ISDN user data rate of 144 kbit/s (B1 + B2 + D) is transmitted in both directions over the interface.

3.2.1 IOM®-2 Configurations

It is possible to configure the IOM-2 interface for various test and evaluation scenarios according to **Table 3**. In a normal NT1 application, the pins $\overline{\text{DDU}}$, $\overline{\text{DDD}}$ and DIO are clamped to 'high', which disables the IOM-2 interface to minimize power consumption.

Table 3 IOM®-2 Configurations

DDD	DDU	DIO	Function	IOM-2 Interface	AUX IOM-2 Interface
1	1	1	normal operation, IOM-2 down	disabled	disabled
1	1	0	normal operation, monitoring IOM-2	active	disabled
1	0	X	IOM-2 access to U-transceiver	active	disabled
0	1	X	IOM-2 access to S-transceiver	active	disabled
0	0	X	IOM-2 access to U- and S-transceiver	active	active

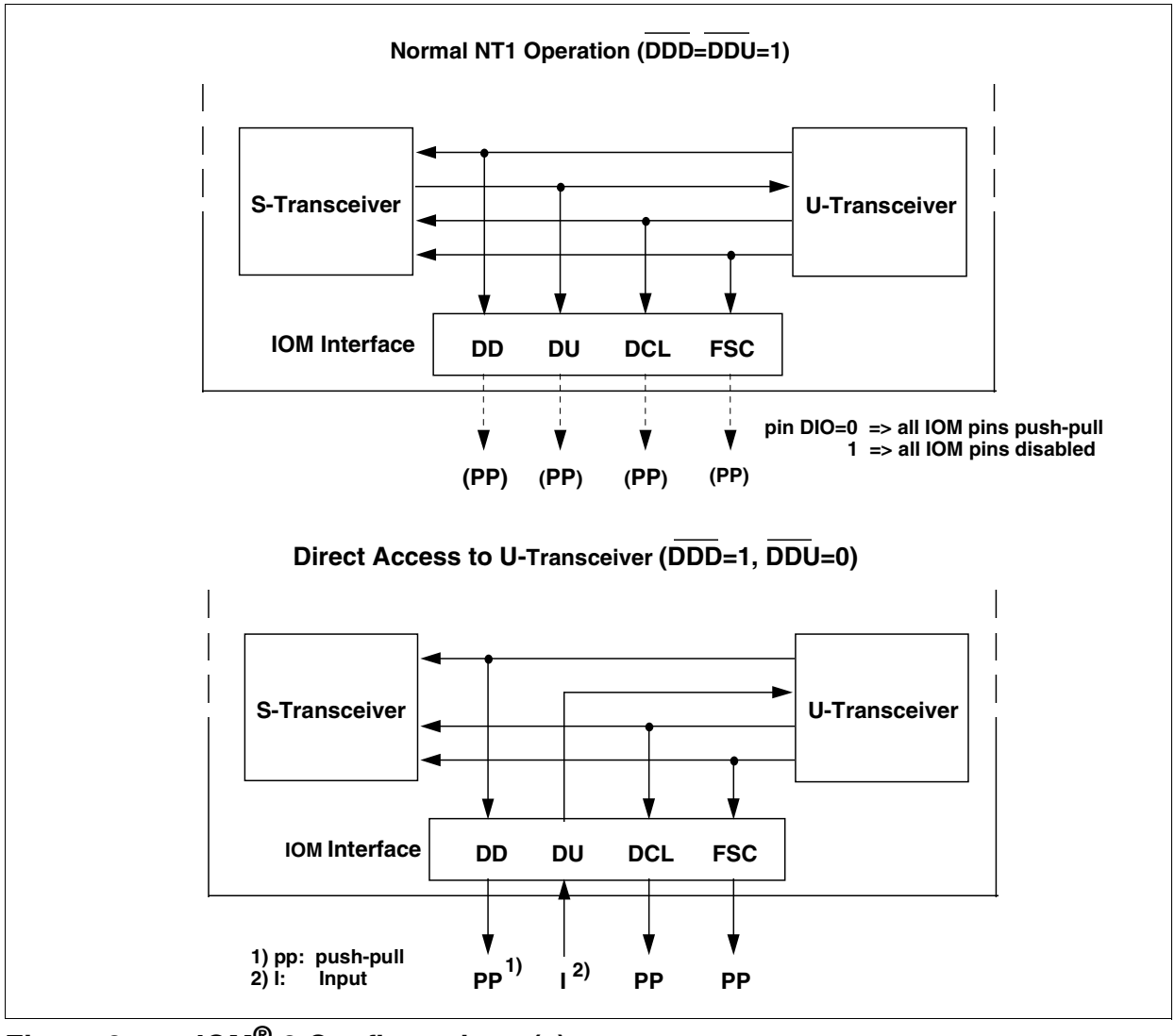


Figure 8 IOM®-2 Configurations (a)

Normal NT1 Operation

The S-and U-transceiver are internally connected via IOM-2. Activation and deactivation is performed automatically via C/I-codes. The C/I-codes, the B- channels and the D-channel can be monitored on the IOM-2 interface of the NTC-T AM with NTC-T functionality selected. The IOM-2 interface can also be set to a high impedance state to minimize power consumption.

Direct Access to U-Transceiver

This mode allows direct access to the U-transceiver via IOM-2. The IOM-2 clocks DCL (512 kHz) and FSC are output on pins DCL and FSC. Pin DU writes data to the U-transceiver and DD reads data from the U-transceiver.

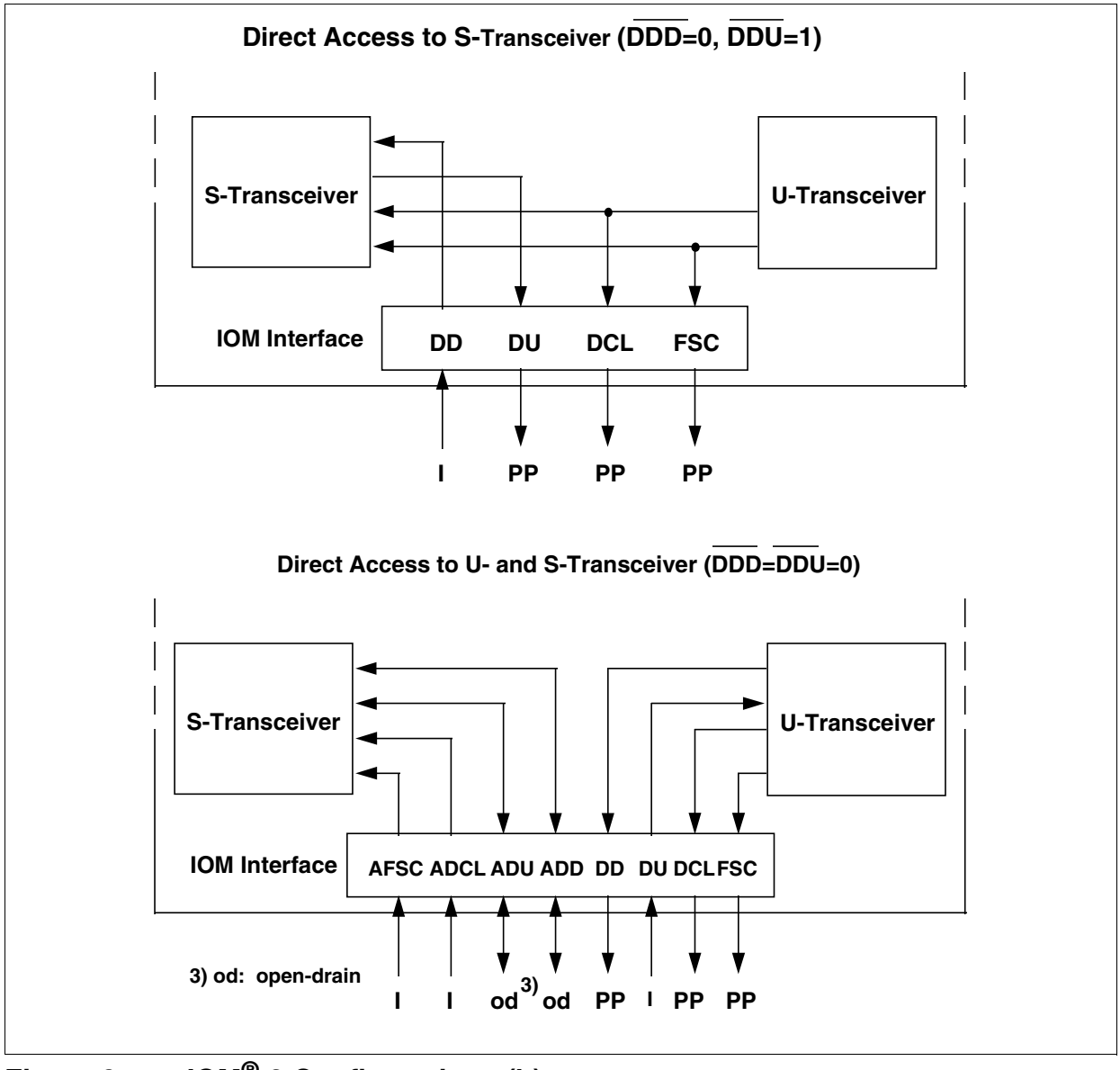


Figure 9 IOM®-2 Configurations (b)

Direct Access to S-Transceiver

This mode allows direct access to the S-transceiver via IOM-2. The IOM-2 clocks DCL (512 kHz) and FSC are output on pins DCL and FSC. Pin DU reads data from the S-transceiver and DD writes data to the S-transceiver.

Direct Access to U- and S-Transceiver

This mode allows separate access to the S- and the U-transceiver via two independent IOM-2 interfaces.

The U-transceiver is controlled via the IOM-2 interface. Pin DCL outputs 512 kHz, pin FSC outputs 8 kHz. Both clocks are synchronous to the U-interface. Pin DD reads data from the U-transceiver and pin DU writes data to the U-transceiver.

The S-transceiver is controlled via the Auxiliary IOM-2 interface. Pin ADCL is an input and accepts any data clock between 512 kHz and 4.096 MHz (multiples of 512 kHz). AFSC is an input and accepts an 8 kHz frame clock. Pin ADU reads data from the S-transceiver and pin ADD writes data to the S-transceiver.

This IOM-2 configuration also allows the design of an Intelligent NT. The S-transceiver can be mapped to IOM-2 channel 0 or channel 1 via pin ICS, allowing different architectures of an Intelligent NT (see **"Modes" on Page 48**).

3.2.2 IOM®-2 Frame Structure

The IOM-2 interface comprises two clock lines for synchronization and two data lines.

Data is carried over Data Upstream (DU) and Data Downstream (DD) signals. The downstream and upstream direction are always defined with respect to the exchange. Downstream refers to the information flow from the exchange to the subscriber and upstream vice versa, respectively.

The data is clocked by a Data Clock (DCL) that operates at twice the data rate. Frames are delimited by an 8-kHz Frame Synchronization Clock (FSC). Incoming data is sampled on every second falling edge of the DCL clock.

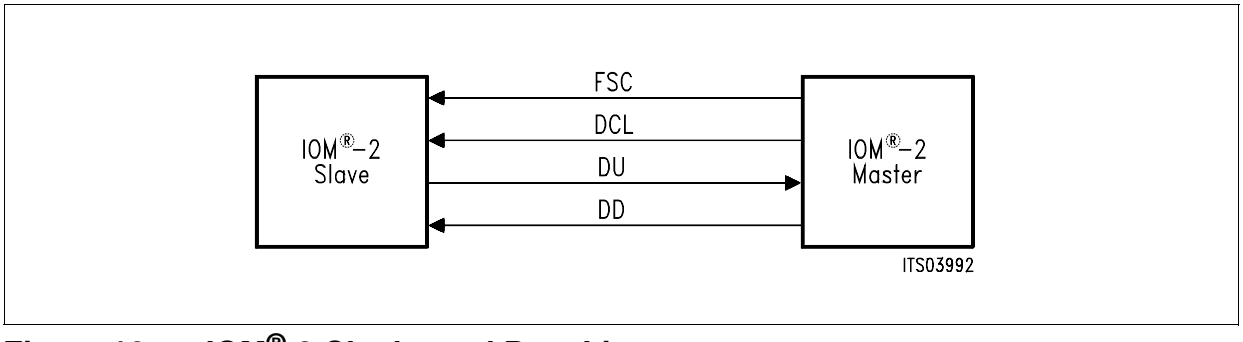


Figure 10 IOM®-2 Clocks and Data Lines

Depending on the frequency of DCL an IOM-2 frame carries one or several IOM-2 channels. The structure of an IOM-2 channel is given in **Figure 11**.

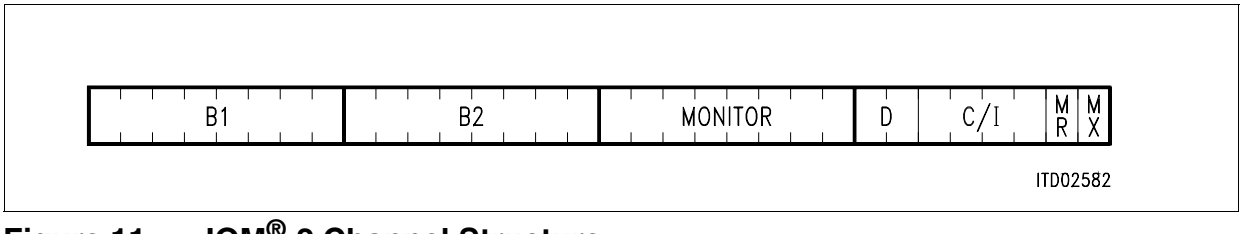


Figure 11 IOM®-2 Channel Structure

An IOM-2 channel consists of:

- two 64 kbit/s channels B1 and B2
- the Monitor channel for transferring maintenance information
- two bits for the 16 kbit/s D-channel
- four command/indication (C/I) bits for controlling of layer-1 functions (U- and S-transceiver).
- two bits MR and MX for the handshake procedure in the Monitor channel

3.2.2.1 NT1 Frame Structure (DCL = 512 kHz)

Pin DCL always delivers 512 kHz which corresponds to one IOM-2 channel with a nominal data rate of 256 kbit/s. The channel contains 144 kbit/s (for 2B+D) plus Monitor and Command/Indication channels.

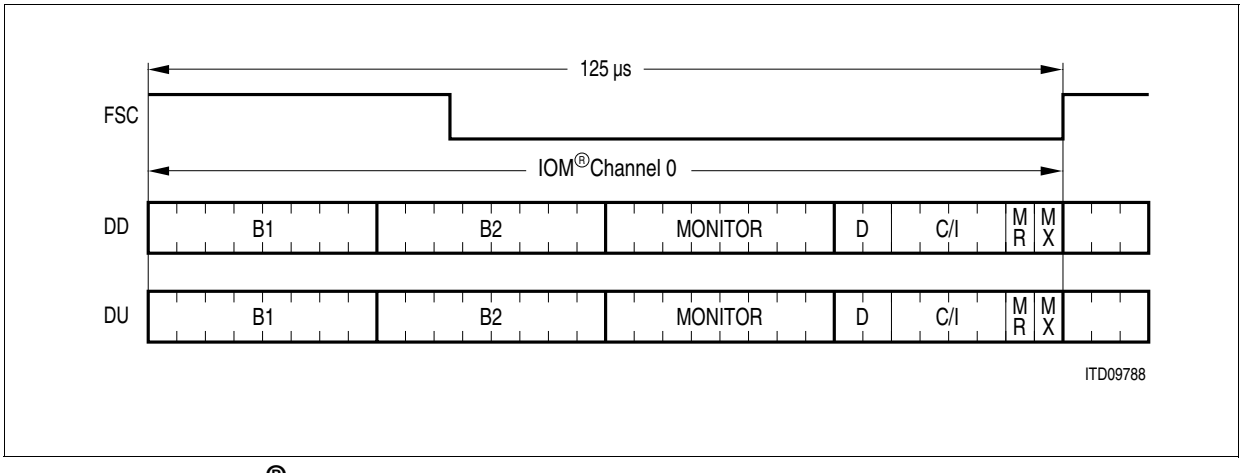


Figure 12 IOM®-2 Frame (DCL = 512 kHz)

3.2.2.2 TE Frame Structure (ADCL = 1.536 MHz)

Pin ADCL accepts any clock between 512 kHz and 4.096 MHz (multiples of 512 kHz). In case the clock is 1.536 MHz the auxiliary IOM-2 interface provides three IOM-2 channels (**Figure 13**). The S-transceiver can be mapped to either channel 0 or channel 1 via pin ICS. The last octet of channel 2 is used for the TIC bus. Please refer to the IOM-2 Interface Reference Guide for details on the terminal mode frame structure.

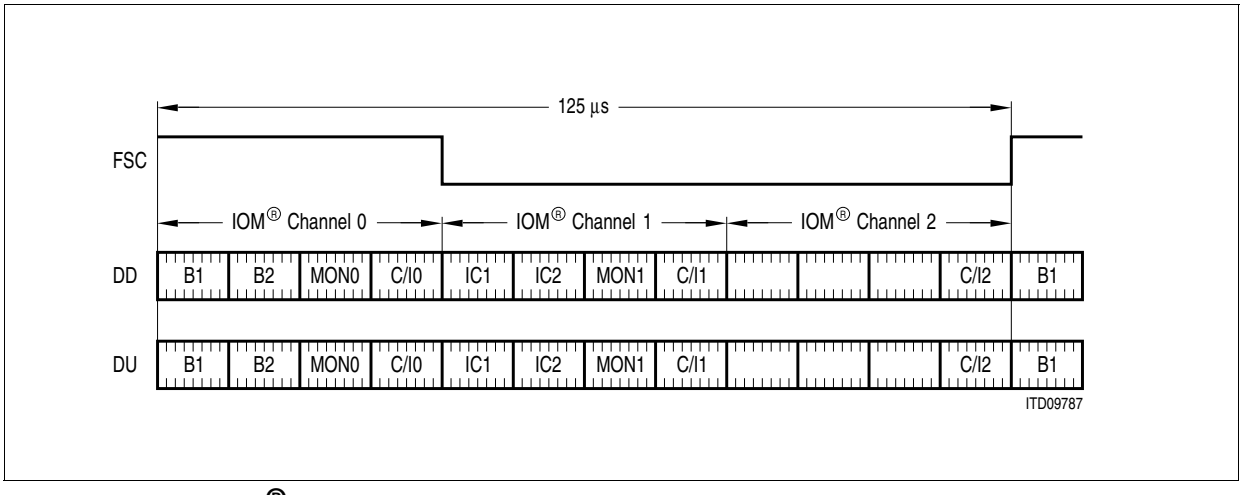


Figure 13 IOM®-2 Frame (ADCL = 1.536 MHz)

3.2.3 IOM®-2 Command / Indication Channel

The Command/Indication (C/I) channel carries real-time control and status information between the U- and the S-transceiver. A new code must be detected in two consecutive IOM-2 frames to be considered valid (double last look criterion).

The C/I code is four bits long. A listing and explanation of the U-transceiver and S-transceiver C/I codes can be found on **Page 43** and **Page 57**.

3.2.4 IOM®-2 Monitor Channel

The Monitor channel protocol is a handshake protocol used for programming and monitoring devices in the Monitor channel. In an NT1 application the Monitor channel is not used.

3.2.5 Activation/Deactivation of IOM®-2 Clocks

The IOM-2 clocks are switched off after the U-transceiver enters state 'Power-down'. This reduces power consumption to a minimum. During power-down the clock lines are held low and the data lines are high.

The **deactivation procedure** is shown in **Figure 14**. After detecting C/I code DI the U-transceiver responds by transmitting DC during subsequent frames and stops the IOM-2 clocks synchronously with the end of the last C/I channel bit of the fourth frame.

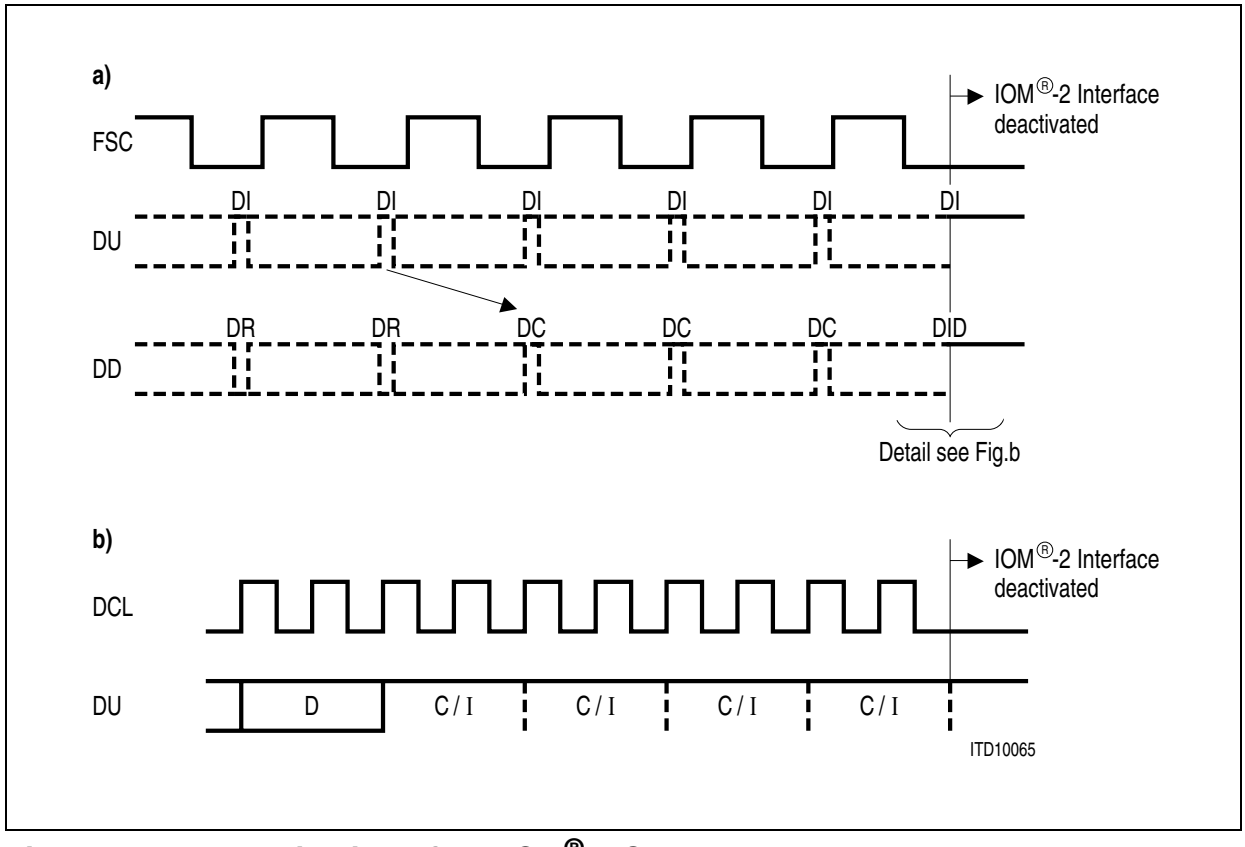


Figure 14 Deactivation of the IOM®-2 Clocks

Activation procedure

The IOM-2 clocks are activated automatically when a line activation is detected either on the S- or the U-interface. DCL is activated such that its first rising edge occurs with the beginning of the bit following the C/I channel.

3.3 U-Transceiver

3.3.1 General

The U-interface performs full duplex data transmission and reception at the U-reference point according to ETSI ETR 080 and FTZ 1TR 220. It applies the 4B3T block code together with adaptive echo cancelling and equalization. Transmission performance is such that it meets all ETSI and FTZ test loops with margin.

The U-interface is designed for data transmission on twisted pair wires in local telephone loops, with basic access to ISDN and a user bit rate of 144 kbit/s.

The following information is transmitted over the twisted pair:

- Bidirectional:
  - B1, B2, D data channels
  - 120 kHz Symbol clock, 160 kbit/s Transmission rate
  - 1 kHz Frame and 40 kHz block clock
  - Activation
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops
- From NT to LT side:
  - Indication of monitored code violations

On the U-interface, transmission ranges of 4.2 km on wires of 0.4 mm diameter and 8 km on 0.6 mm wires are achieved without additional signal regeneration on the loop. The transmission ranges can be doubled by inserting a repeater for signal regeneration.

3.3.2 Frame Structure of the U-Interface

1 ms frames are transmitted via the U-interface, each consisting of:

- 108 symbols: 144 bit scrambled and coded B1 + B2 + D data
- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, resp. 36 bits) contains the user data of two IOM-2 frames in the same order (8B + 8B + 2D + 8B + 8B + 2D).

Different synchwords are used for each direction:

- Downstream from LT to NT + + + – – – + – – + –
- Upstream from NT to LT – + – – + – – – + + +

On the NT side, the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

After successful synchronization, resynchronization will occur if the synchword is not detected in the expected position in 64 consecutive frames.
The U-transceiver is synchronized, if it detects the synchword four times consecutively within a period of 1 ms.

Table 4 Frame Structure for Downstream Transmission LT to NT

1 D_1	2 D_1	3 D_1	4 D_1	5 D_1	6 D_1	7 D_1	8 D_1	9 D_1	10 D_1	11 D_1	12 D_1
13 $D_{1/2}$	14 $D_{1/2}$	15 $D_{1/2}$	16 D_2	17 D_2	18 D_2	19 D_2	20 D_2	21 D_2	22 D_2	23 D_2	24 D_2
25 D_2	26 D_2	27 D_2	28 D_3	29 D_3	30 D_3	31 D_3	32 D_3	33 D_3	34 D_3	35 D_3	36 D_3
37 D_3	38 D_3	39 D_3	40 $D_{3/4}$	41 $D_{3/4}$	42 $D_{3/4}$	43 D_4	44 D_4	45 D_4	46 D_4	47 D_4	48 D_4
49 D_4	50 D_4	51 D_4	52 D_4	53 D_4	54 D_4	55 D_5	56 D_5	57 D_5	58 D_5	59 D_5	60 D_5
61 D_5	62 D_5	63 D_5	64 D_5	65 D_5	66 D_5	67 $D_{5/6}$	68 $D_{5/6}$	69 $D_{5/6}$	70 D_6	71 D_6	72 D_6
73 D_6	74 D_6	75 D_6	76 D_6	77 D_6	78 D_6	79 D_6	80 D_6	81 D_6	82 D_7	83 D_7	84 D_7
85 M	86 D_7	87 D_7	88 D_7	89 D_7	90 D_7	91 D_7	92 D_7	93 D_7	94 D_7	95 $D_{7/8}$	96 $D_{7/8}$
97 $D_{7/8}$	98 D_8	99 D_8	100 D_8	101 D_8	102 D_8	103 D_8	104 D_8	105 D_8	106 D_8	107 D_8	108 D_8
109 D_8	110 +	111 +	112 +	113 –	114 –	115 –	116 +	117 –	118 –	119 +	120 –

D_1 ... D_8 Ternary 2B + D data of IOM-2 frames 1 ... 8
M Maintenance symbol
+, – Synchword

Transparent access to the M bit is not possible via the IOM-2 interface.

Table 5 Frame Structure for Upstream Transmission NT to LT

1 U_1	2 U_1	3 U_1	4 U_1	5 U_1	6 U_1	7 U_1	8 U_1	9 U_1	10 U_1	11 U_1	12 U_1
13 $U_{1/2}$	14 $U_{1/2}$	15 $U_{1/2}$	16 U_2	17 U_2	18 U_2	19 U_2	20 U_2	21 U_2	22 U_2	23 U_2	24 U_2
25 M	26 U_2	27 U_2	28 U_2	29 U_3	30 U_3	31 U_3	32 U_3	33 U_3	34 U_3	35 U_3	36 U_3
37 U_3	38 U_3	39 U_3	40 U_3	41 $U_{3/4}$	42 $U_{3/4}$	43 $U_{3/4}$	44 U_4	45 U_4	46 U_4	47 U_4	48 U_4
49 U_4	50 –	51 +	52 –	53 –	54 +	55 –	56 –	57 –	58 +	59 +	60 +
61 U_4	62 U_4	63 U_4	64 U_4	65 U_4	66 U_4	67 U_5	68 U_5	69 U_5	70 U_5	71 U_5	72 U_5
73 U_5	74 U_5	75 U_5	76 U_5	77 U_5	78 U_5	79 $U_{5/6}$	80 $U_{5/6}$	81 $U_{5/6}$	82 U_6	83 U_6	84 U_6
85 U_6	86 U_6	87 U_6	88 U_6	89 U_6	90 U_6	91 U_6	92 U_6	93 U_6	94 U_7	95 U_7	96 U_7
97 U_7	98 U_7	99 U_7	100 U_7	101 U_7	102 U_7	103 U_7	104 U_7	105 U_7	106 $U_{7/8}$	107 $U_{7/8}$	108 $U_{7/8}$
109 U_8	110 U_8	111 U_8	112 U_8	113 U_8	114 U_8	115 U_8	116 U_8	117 U_8	118 U_8	119 U_8	120 U_8

U_1 ... U_8 Ternary 2B + D data of IOM-2 frames 1... 8

M Maintenance symbol

+, - Synchword

Transparent access to the M bit is not possible via the IOM-2 interface.

3.3.3 Coding from Binary to Ternary Data

Each 4 bit block of binary data is coded into 3 ternary symbols of MMS 43 block code according to **Table 6**.

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

Table 6 MMS 43 Coding Table

				S1				S2				S3				S4			
t →				t →				t →				t →				t →			
0	0	0	1	0	–	+	1	0	–	+	2	0	–	+	3	0	–	+	4
0	1	1	1	–	0	+	1	–	0	+	2	–	0	+	3	–	0	+	4
0	1	0	0	–	+	0	1	–	+	0	2	–	+	0	3	–	+	0	4
0	0	1	0	+	–	0	1	+	–	0	2	+	–	0	3	+	–	0	4
1	0	1	1	+	0	–	1	+	0	–	2	+	0	–	3	+	0	–	4
1	1	1	0	0	+	–	1	0	+	–	2	0	+	–	3	0	+	–	4
1	0	0	1	+	–	+	2	+	–	+	3	+	–	+	4	–	–	–	1
0	0	1	1	0	0	+	2	0	0	+	3	0	0	+	4	–	–	0	2
1	1	0	1	0	+	0	2	0	+	0	3	0	+	0	4	–	0	–	2
1	0	0	0	+	0	0	2	+	0	0	3	+	0	0	4	0	–	–	2
0	1	1	0	–	+	+	2	–	+	+	3	–	–	+	2	–	–	+	3
1	0	1	0	+	+	–	2	+	+	–	3	+	–	–	2	+	–	–	3
1	1	1	1	+	+	0	3	0	0	–	1	0	0	–	2	0	0	–	3
0	0	0	0	+	0	+	3	0	–	0	1	0	–	0	2	0	–	0	3
0	1	0	1	0	+	+	3	–	0	0	1	–	0	0	2	–	0	0	3
1	1	0	0	+	+	+	4	–	+	–	1	–	+	–	2	–	+	–	3

3.3.4 Decoding from Ternary to Binary Data

Decoding is done in the reverse manner of coding. The received blocks of 3 ternary symbols are converted into blocks of 4 bits. The decoding algorithm is given in **Table 7**.

As in the encoding table, the left hand symbol of each block (both binary and ternary) is the first bit and the right hand is the last. If a ternary block "0 0 0" is received, it is decoded to binary "0 0 0 0". This pattern usually occurs only during deactivation.

Table 7 4B3T Decoding Table

Ternary Block	Binary Block
0 0 0, + 0 +, 0 – 0	0 0 0 0
0 + –	0 0 0 1
+ – 0	0 0 1 0
0 0 +, – – 0	0 0 1 1
– + 0	0 1 0 0

Table 7 4B3T Decoding Table

0 + +, – 0 0	0	1	0	1
– + +, – – +	0	1	1	0
– 0 +	0	1	1	1
+ 0 0, 0 – –	1	0	0	0
+ – +, – – –	1	0	0	1
+ + –, + – –	1	0	1	0
+ 0 –	1	0	1	1
+ + +, – + –	1	1	0	0
0 + 0, – 0 –	1	1	0	1
0 + –	1	1	1	0
+ + 0, 0 0 –	1	1	1	1

3.3.5 Monitoring of Code Violations

The running digital sum (RDS) monitor computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+ 1, 0, –1). At the end of each block, the running digital sum is the number of the next column in **Table 6** which should contain the next received block. A code violation has occurred if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0, three user symbols with zero polarity, is found in the received data.

When, at the end of a ternary block, no error was found, the running digital sum is left at its current value for the next ternary block. If the counter value is greater than 4, it is set to 3 at the beginning of the next ternary block, if its value is 0 or less, it is set to one. So after a code violation has been detected, the RDS monitor synchronizes itself within a period depending on the received data pattern.

Some transmission errors do not cause a code violation.

3.3.6 Scrambler / Descrambler

The binary transmit data from the IOM-2 interface is scrambled with a polynomial of 23 bits, before it is sent to the 4B3T coder. The scrambling algorithm ensures that no sequences of permanent binary 0 s or 1 s are transmitted.

The scrambler polynomial is:

$$z^{-23} + z^{-18} + 1$$

The received data (after decoding from ternary to binary) is multiplied with a polynomial of 23 bits in order to recover the original data before it is sent to the S-transceiver. The descrambler is self synchronized after 23 symbols. The descrambler polynomial is:

$$z^{-23} + z^{-5} + 1$$

3.3.7 Awake Protocol

To awake the U-interface and the remote transceiver, an awake and an acknowledge signal U1W and U2W have been defined (**Table 12**)

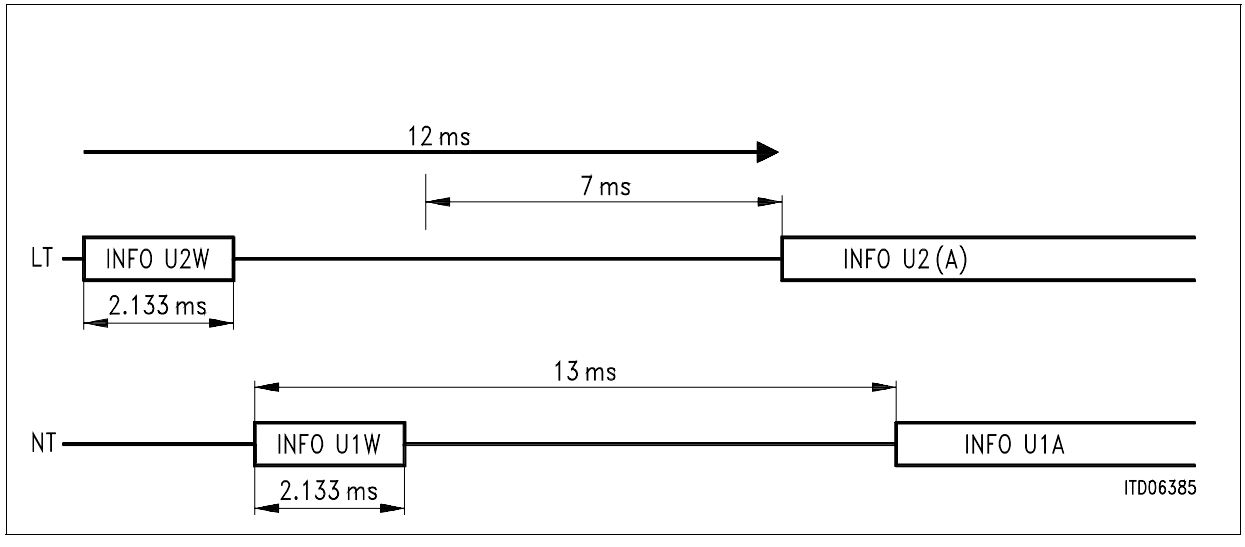


Figure 15 Procedure for Awake Downstream

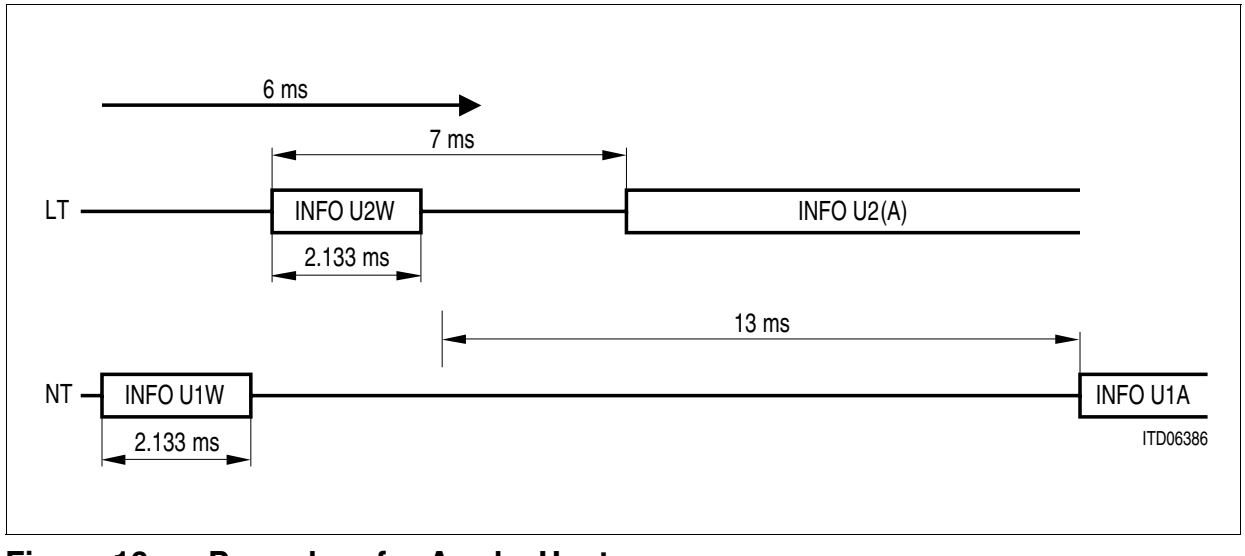


Figure 16 Procedure for Awake Upstream

3.3.8 State Machine Notation

The following state diagram describes all the actions/reactions resulting from any command or detected signal and resulting from the various operating modes.

The states, inputs and outputs are characterized as shown in the following example:

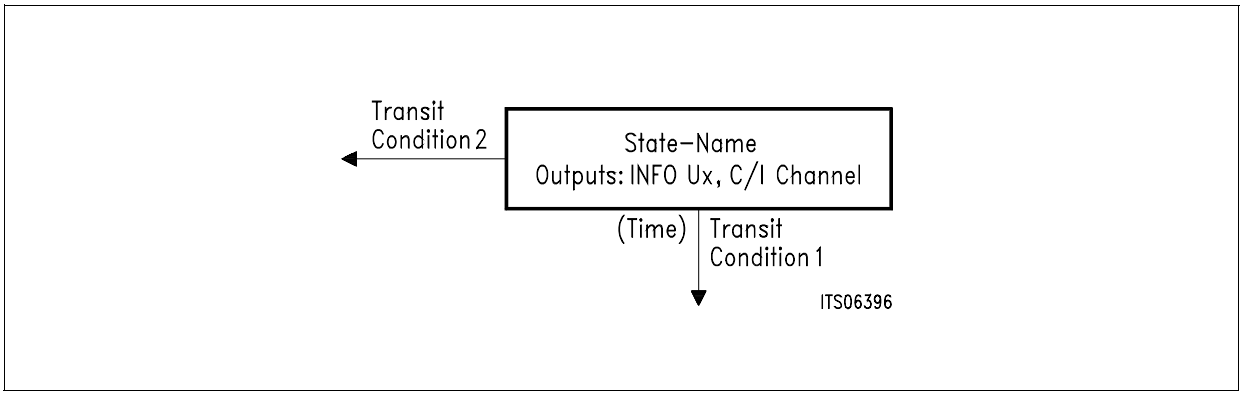


Figure 17 Example of a State with Outputs and Inputs

Each state has one or more exits to other states. These transitions depend on certain conditions which are noted next to the transition lines. These conditions are the only possibility to leave a state. If more conditions have to be fulfilled together, they are put into parentheses with an AND operator (&). If more than one condition leads to the same transition, they are put into parentheses with an OR operator (|). The meaning of a condition may be inverted by the NOT operator (/). Only the described states and transitions can exist.

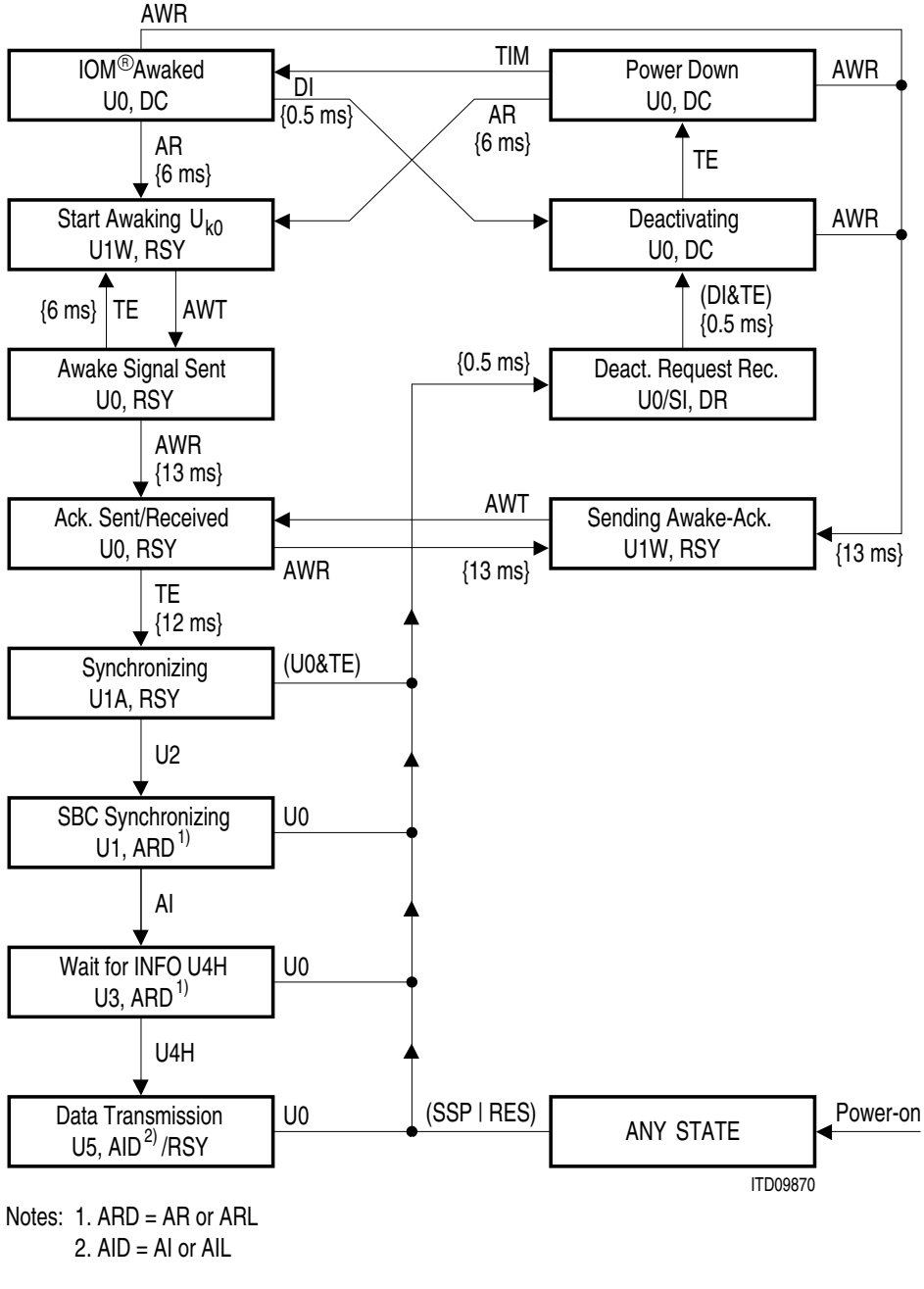
Some conditions lead from each state to the same target state. To reduce the number of lines and the complexity of the figures, a state named “ANY STATE” exists standing for each state.

At some transitions, an internal timer is started. The time until the timer runs out, is noted in curly brackets { } next to the transition line. If the end of the started time leads to a transition from one state to another, this condition is indicated by TE (timer ended).

These actions are chosen to cope with all ISDN devices with IOM-2 standard interfaces. The states and transitions have been prepared to prevent undefined situations. In any case, the involved devices will enter defined conditions when the line is deactivated.

3.3.9 State Machine

3.3.9.1 NT Mode State Diagram



Notes: 1. ARD = AR or ARL
2. AID = AI or AIL

Figure 18 State Diagram of the NT

3.3.9.2 Inputs to the U-Transceiver

C/I-Commands

AI — Activation Indication Upstream
The S-transceiver issues this indication to announce that the S-receiver is synchronized. The U-transceiver informs the LT side by transmitting U3.

AR — Activation Request Upstream
INFO1 has been received by the S-transceiver. The U-transceiver is requested to start the activation process by sending the wake-up signal U1W.

DI — Deactivation Indication Upstream
This indication is used during a deactivation procedure to inform the U-transceiver that timing signals are no longer needed and that the U-transceiver may enter the Power Down state.

RES — Reset
Unconditional command which resets any stored settings of the U-transceiver; no line signal will be sent out.

SSP — Send Single Pulses
Unconditional command which requests the transmission of single pulses with a period of 1 ms.

TIM — Timing
In power-down, the S-transceiver has detected an awake signal on the line and requests IOM clocks and timing.

Pins

RES — Pin-Reset
Corresponds to a low-level at pin $\overline{\text{RES}}$, a power-on reset or an undervoltage detection. The function of this pin is the same as of the C/I-code RES. C/I-message DR will be issued.

SSP — Pin-Send Single Pulses
Corresponds to a high-level at pin TM0 and a low-level at pin TM1 (refer to **Chapter 3.6**). The function of this pin is the same as of the C/I-code SSP. C/I-message DR will be issued.

U-Interface Events

The U-interface signals U0, U2W, U2 and U4H can be detected. They are defined in **Table 12**.

The U-transceiver detects U2 if continuous binary data is found on the descrambler output after 8 subsequent U-frames. U2 is detected after 8 to 9 ms.

U4H is recognized if the U-transceiver detects 16 subsequent binary 1's in the data stream.

U0 is recognized after one complete frame with continuous zero level.

Other terms used in the state diagram:

AWR Awake signal (INFO U2W) detected

AWT INFO U1W has been sent out

TE Timer ended, the started timer has run out

3.3.9.3 Outputs of the U-Transceiver

Signals and indications are issued on IOM-2 (C/I-indications) and on the U-interface (predefined U-signals).

C/I Indications

AI Activation Indication
The U-transceiver has detected INFO U4H on the U-interface. The S-transceiver is requested to send INFO4 and to achieve transparency of transmission in the direction IOM to S/T-interface.

AIL Activation Indication Loop-back. The U-transceiver has detected continuous plus polarity within 8 subsequent frames in the M channel. The S-transceiver is requested to send INFO4 and to keep loop-back 2 active.

AR Activation Request
The U-transceiver has synchronized on the incoming U2 signal. The S-transceiver is requested to start the activation procedure on the S/T-interface by sending INFO2.

ARL Activation Request Loop-back
The U-transceiver has detected continuous plus polarity within 8 subsequent frames in the M channel. The S-transceiver is requested to send INFO2 and to operate loop-back 2.

DC Deactivation Confirmation
DC informs the S-transceiver that the U-interface is deactivated. The U-transceiver is now ready to receive the awake signal; the IOM-2 interface is powered down after four IOM frames.

DR Deactivation Request
The U-transceiver has detected a deactivation request command from the
LT-side for a complete deactivation. The S-transceiver is requested to start the deactivation procedure on the S/T-interface by sending INFO0.

RSY Resynchronizing Indication
RSYS informs the S-transceiver that the U-transceiver is not synchronous.

The state diagrams specify only ARD and AID, which are groups of C/I channel codes, to indicate the activated states. Depending on the last recognized received loop command, the U-transceiver decides whether it sends AR, ARL, AI or AIL into the C/I channel.

If it receives 8 consecutive M symbols with zero polarity, the U-transceiver sends AR for ARD and AI for AID in the state diagram.

If it receives 8 consecutive M symbols with plus polarity, the U-transceiver sends ARL for ARD and AIL for AID in the state diagram.

Signals on U-Interface

The signals U0, U1W, U1A, U1, U3, U5 can be transmitted on the U-interface. They are defined in **Table 12**.

SI Single Pulses
The U-transceiver sends periodically single pulses spaced 1 ms eg. for pulse mask measurements.

3.3.9.4 NT-States

In this section, each state is described with its inputs, its outputs and its meaning.

The C/I-channel output and the transmitted INFO on U are already specified by the state diagrams; below they are only referred to, if within a state there are more than one of them specified. In this case, the C/I-channel output and the transmitted INFO depend on the given inputs.

Acknowledge Sent/Received

After having sent the awake signal, the U-transceiver has received the acknowledge signal. If being awoken the U-transceiver has sent the acknowledge. Anyway, the U-transceiver waits for possible repetition or time-out. The user data (2B + D) on pin DD is clamped to high to avoid undesired false data in the D-channel during activation.

Awake Signal Sent

The U-transceiver is awaking the U-interface and waits for the acknowledge or for the time-out after sending the awake signal. The user data (2B + D) on pin DD is clamped to high.

Deactivation Request Received

The U-transceiver has received INFO U0 or one of the deactivating maintenance requests, RES or SSP. If it receives SSP, the U-transceiver sends a single pulse every 1 ms on the line, otherwise INFO U0 is sent. The U-transceiver remains at least 0.5 ms in this state before accepting DI. The user data (2B + D) on pin DD is clamped to high.

Deactivating

The U-transceiver deactivates U sending INFO U0; it remains at least 0.5 ms in this state. The user data (2B + D) on pin DD is clamped to high .

Data Transmission

The transmission of user data is enabled (INFO U5). If in 64 subsequent U-frames the Barker-code is not found at the expected position, the U-transceiver issues RSY on the C/I-channel until it has resynchronized, i.e. found the Barker-code on the same position in 4 subsequent frames.

IOM Awaked

The U-transceiver is awoken by the S-transceiver keeping line DU low (TIM). When it receives DI again in the C/I channel, the U-transceiver goes back to power-down within at least 0.5 ms. The user data (2B + D) on pin DD is clamped to high.

Power Down

Entering this state, the U-transceiver powers down within 0.5 ms stopping most parts of the U-transceiver, so that these CMOS circuits cannot consume further power. The U-transceiver stops clocking the IOM-2 interface, if it has received four times DI in the C/I channel. If the IOM-2 interface clock is stopped, it can be activated by the S-transceiver by forcing DU to low.

SBC (S-Transceiver) Synchronizing

After being synchronized and indicating this with AR/ARL, the U-transceiver waits for the message AI from the S-transceiver which indicates that it is also synchronized. The user data (2B + D) on pin DD is clamped to high.

Sending Awake Acknowledge

The U-transceiver has received the awake signal and acknowledges this in this state. The user data (2B + D) on pin DD is clamped to high.

Synchronizing

After successful awake procedure, the U-transceiver tries to recognize INFO U2. The user data (2B + D) on pin DD is clamped to high.

Start Awaking U

Receiving AR in the C/I-channel, the U-transceiver has powered up and is sending the awake signal. The user data (2B + D) on pin DD is clamped to high.

Wait for INFO U4H

In this state, the U-transceiver is synchronized. It has received the information that the S-transceiver is synchronized itself, and it waits now for the permission to go to the transparent state. The user data (2B + D) on pin DD is clamped to high.

3.3.10 C/I Codes

Both commands and indications depend on the data direction. **Table 8** presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM frames (Double last-look criterion). Indications are strictly state orientated. Refer to the state diagrams in the previous sections for commands and indications applicable in various states.

Table 8 U-Transceiver C/I Codes

Code	NT Mode	
	IN	OUT
0000	TIM	DR
0001	–	–
0010	–	–
0011	–	–
0100	–	RSY

Code	NT Mode	
0101	SSP	–
0110	–	–
0111	–	–
1000	AR	AR
1001	–	–
1010	–	ARL
1011	–	–
1100	AI	AI
1101	RES	–
1110	–	AIL
1111	DI	DC

AIL	Activation Indication Loop 2	DR	Deactivation Request
AI	Activation Indication	RES	Reset
ARL	Activation Request Loop 2	RSY	Resynchr. Indication
AR	Activation Request	SSP	Send-Single-Pulses
DC	Deactivation Confirmation	TIM	Timing request
DI	Deactivation Indication.		

3.3.11 Loop-Back 2

Loop-backs are specified for maintenance purposes and in order to facilitate the location of defect systems. The NTC-T AM with NTC-T functionality selected automatically recognizes and executes a loop-back 2 command.

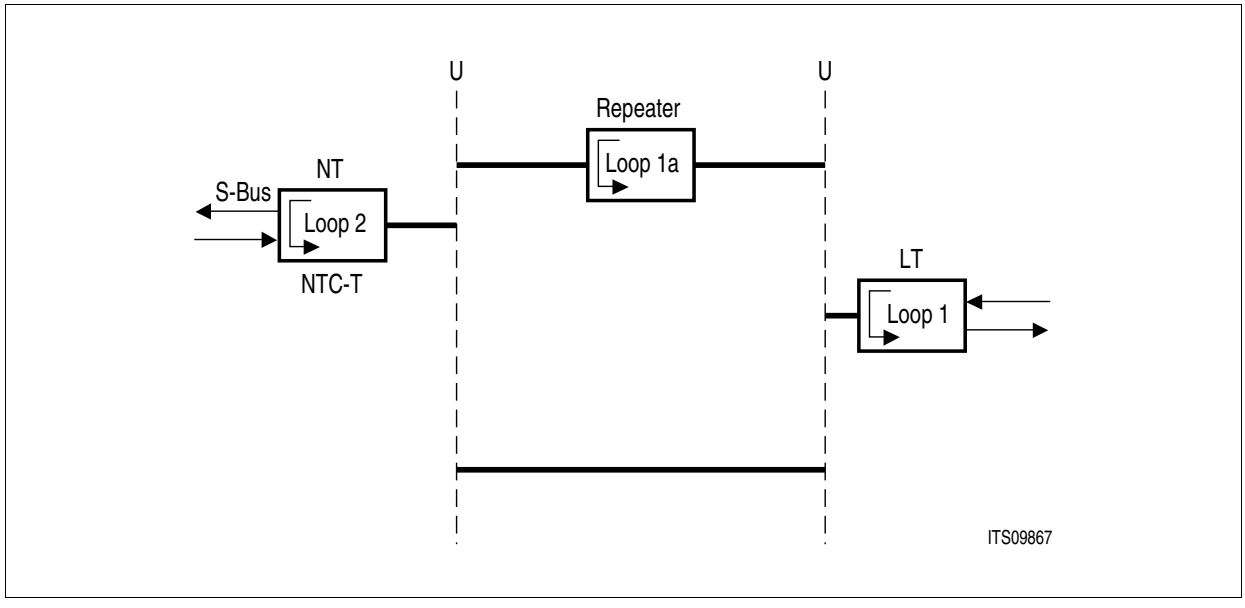


Figure 19 Test Loop-Backs

Loop-back 2 is controlled by the exchange. It is transparent which means that all bits that are looped back are also passed on to the S-bus. The commands for closing and opening loop-back 2 are transmitted from the exchange on the U-interface in the 1 kBaud M channel (position 85 downstream in the U-frame from LT to NT).

Loop-back 2 is closed after the U-transceiver has received 8 consecutive pulses with plus polarity in the M channel.

Loop-back 2 is opened after the U-transceiver has received 8 consecutive zeros in the M channel or at deactivation. During normal transmission without loops, the M symbol is set to zero or minus.

The loop-back comprises both B-channels and the D-channel. It is closed in the NTC-T AM with NTC-T functionality selected as close to the S-transceiver as possible. The U-transceiver passes the request on to the S-transceiver by issuing C/I-code AIL in the "Data Transmission" state or C/I-code ARL in other states.

3.3.12 Analog Line Port

The analog part of the U-transceiver consists of three main building blocks:

– The analog-to-digital converter in the receive path
– The digital-to-analog converter in the transmit path
– The output buffer in the transmit path

Furthermore it contains some special functions. These are:

– Analog test loop-back
– Level detect function

Analog-to-Digital Converter

The ADC is a sigma-delta modulator of second order using a clock rate of 15.36 MHz.

The peak input signal measured between AIN and BIN must be below 4 Vpp. In case the signal input is too low (long range), the received signal is amplified internally by 6 dB. The maximum signal to noise ratio is achieved with 1.3 Vpp (long range) and 2.6 Vpp (short range) input signal voltage.

Digital-to-Analog Converter

The output pulse is shaped by a special DAC. The DAC was optimized for excellent matching between positive and negative pulses and high linearity. It uses a fully differential capacitor approach. The staircase-like output signal of the DAC drives the output buffers. The shape of a DAC-output signal is shown in **Figure 20**, the peak amplitude is normalized to one. This signal is fed to an RC-lowpass filter of the first order with a corner frequency of 1 MHz ± 50%.

The duration of each pulse is 11 steps, with T0 = 1/960 ms per step. On the other hand, the pulse rate is 120-kHz or one pulse per 8 steps. Thus, the subsequent pulses are overlapping for a duration of 3 steps.

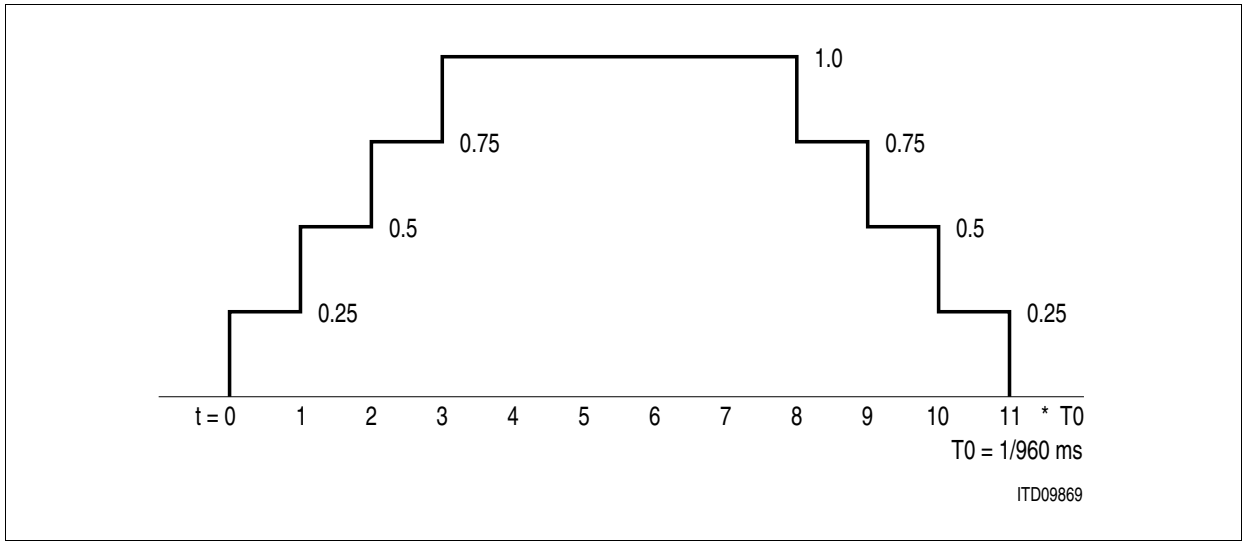


Figure 20 DAC Output for a Single Pulse

Output Stage

The output stage consists of two identical buffers, operated in a differential mode. This concept allows an output-voltage swing of 6.4 Vpp at the output pins of the U-transceiver. The buffers are optimized for:

– High output swing
– High linearity
– Low quiescent current to minimize power consumption

Level Detect

The level detect circuit evaluates the differential signal between AIN and BIN. The differential threshold level is between 15 mV and 45 mV. The DC-level (common mode level) may be between 0 V and 3 V. Level detect is not effected by the range setting.

Pulse Shape

The pulse mask for a single positive pulse measured between AOUT and BOUT at a load of 172 Ω is given in the following figure.

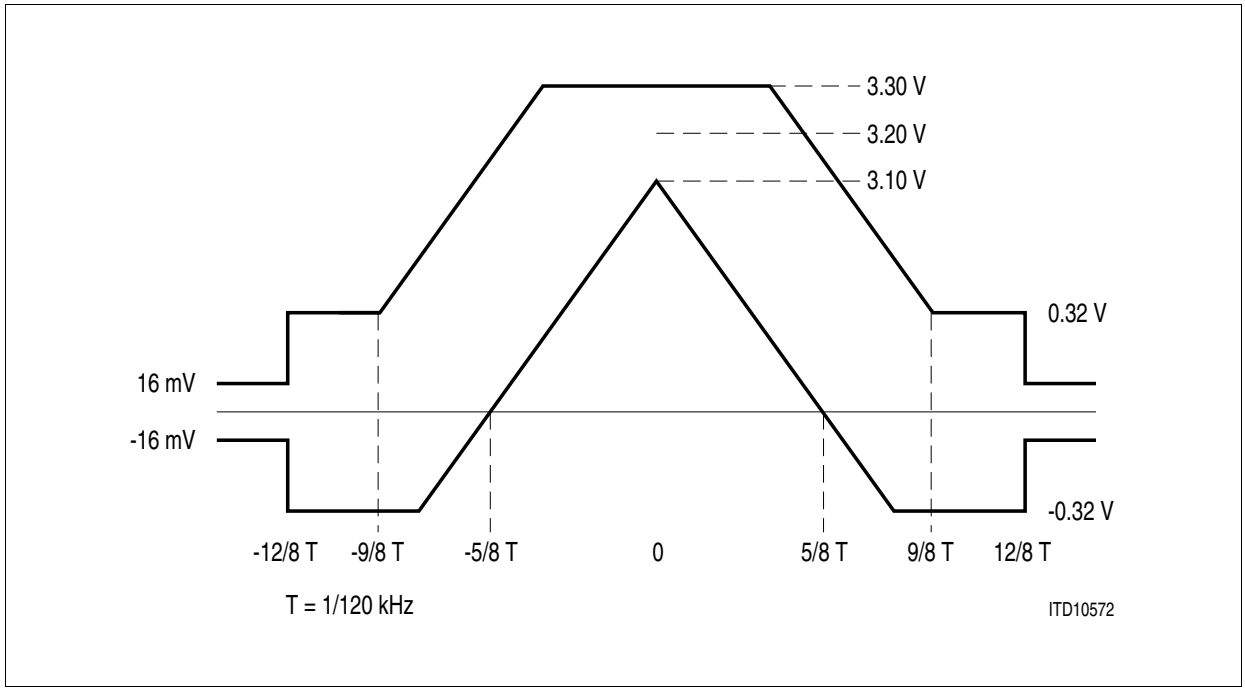


Figure 21 Pulse Mask for a Single Positive Pulse

Hybrid

Please refer to **Chapter 8.2.2**.

3.4 S-Transceiver

Transmission over the S/T-interface is performed at a rate of 192 kbit/s. Pseudo-ternary coding with 100 % pulse width is used. 144 kbit/s are used for user data (B1+B2+D), 48 kbit/s are used for framing and maintenance information. The NTC-T AM with NTC-T functionality selected uses two symmetrical, differential outputs (SX1, SX2) and two symmetrical, differential inputs (SR1, SR2). These signals are coupled via external circuitry (**Figure 29**) and two transformers onto the 4 wire S-interface. The nominal pulse amplitude on the S-interface is 750 mV (zero-peak).

3.4.1 Modes

In NT1 applications the S-transceiver is in NT mode.

However, if pins $\overline{\text{DDD}}$ = $\overline{\text{DDU}}$ = '0' (Auxiliary IOM-2 interface active) the timeslot and state machine mode of the S-transceiver can be selected according to the application. In todays intelligent NTs it is recommended to select the NT-state machine which requires activation of the U-interface for completion of an S-bus activation. On the other hand, if the intelligent NT allows internal calls it may be more convenient to use the LT-S state machine. This state machine is typically used in PBX applications and allows complete activation of the S-interface independently of the U-interface.

Pin ICS selects the timeslot of the S-transceiver as well as the default setting of the state machine. The S-transceiver is mapped to IOM-2 channel 0 and uses the NT mode state machine if ICS = 1. Otherwise, if ICS = 0, IOM-2 channel 1 is selected and the LT-S state machine is applied.

The state machine can be toggled between LT-S and NT mode by programming the internal registers of the S-transceiver. The internal registers are accessed via the Monitor channel. Please refer to the data sheet of the PEB 8191 (INTC-Q) or the PEB 2081 (SBCX) manual for a description of the S-transceiver's internal registers, the LT-S state machine and the S/Q channel access.

The main functions of the S-transceiver are:

- line transceiver functions for the S/T interface according to the electrical specifications of ITU I.430 and ETSI ETS 300 012;
- conversion of the frame structure between IOM and S/T interface;
- conversion from/to binary to/from pseudo-ternary code;
- level detection
- receive timing recovery for point-to-point, passive bus and extended passive bus configuration;
- S/T timing generation using IOM timing synchronous to system;
- D-channel echo bit generation by handling of the global echo bit;
- activation/deactivation procedures, triggered by primitives received over the IOM C/I channel or by INFO's received from the line;
- execution of test loops.

The wiring configurations in user premises, in which the NTC-T AM with NTC-T functionality selected can be used are illustrated in **Figure 22**.

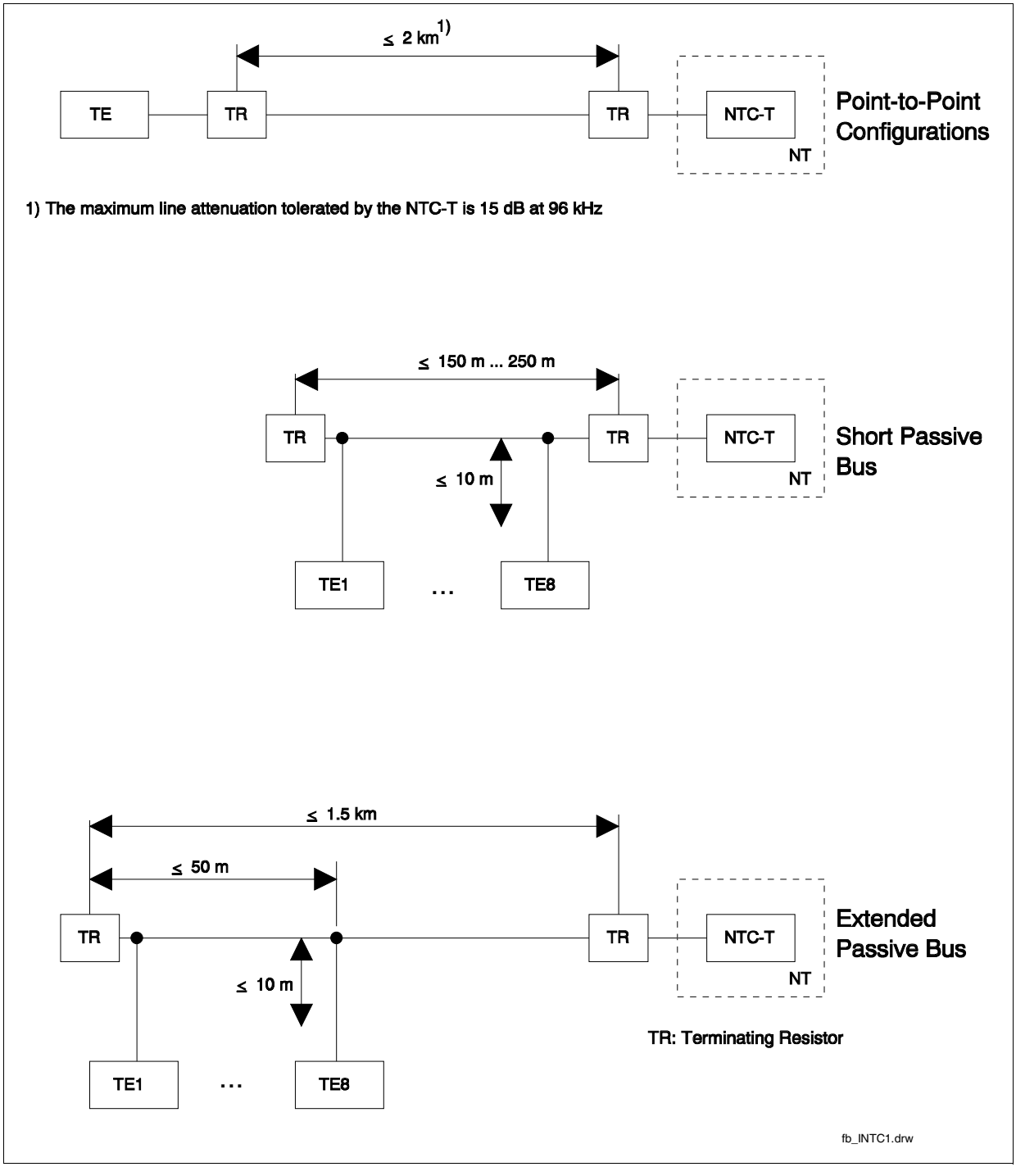


Figure 22 Wiring Configurations in User Premises

3.4.2 S/T-Interface Coding

The following figure illustrates the code used. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with a single exception: the first binary ZERO following the framing balance bit is of the same polarity as the framing-balancing bit (required code violation).

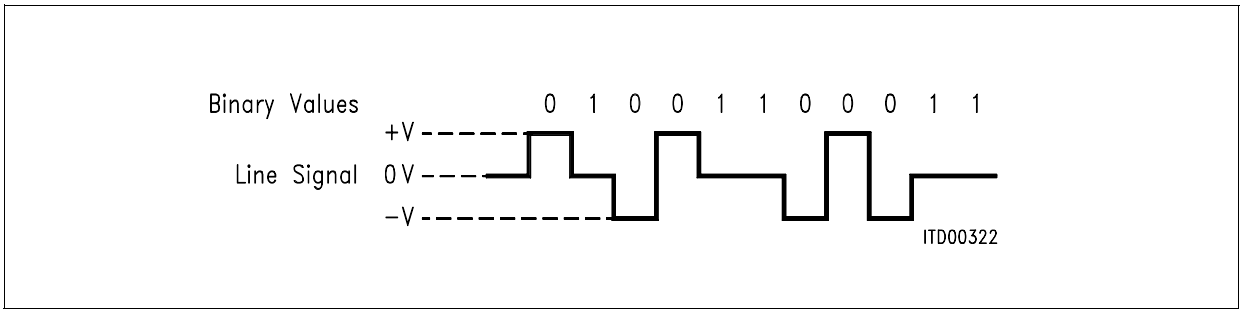


Figure 23 S/T -Interface Line Code (without code violation)

A standard S/T frame consists of 48 bits. In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

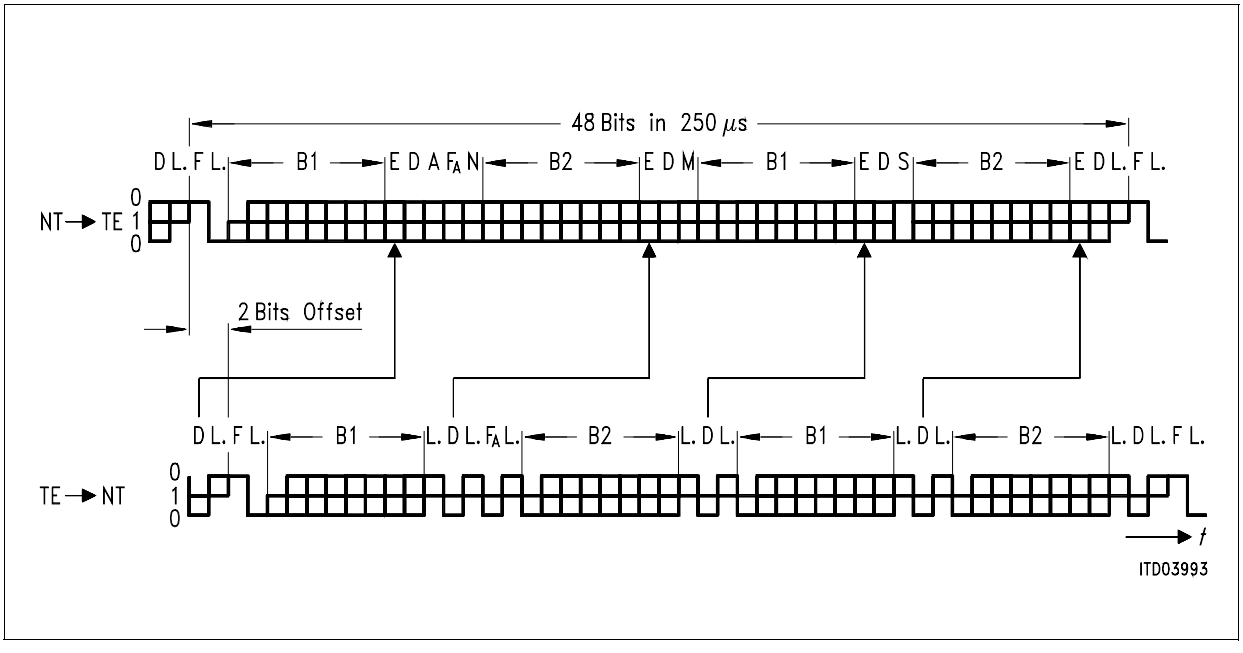


Figure 24 Frame Structure at Reference Points S and T (ITU I.430)

– F	Framing Bit	F = (0b) → identifies new frame (always positive pulse)
– L.	D.C. Balancing Bit	L. = (0b) → number of binary ZEROs sent after the last L. bit was odd
– D	D-Channel Data Bit	Signalling data specified by user
– E	D-Channel Echo Bit	E = D → no D-channel collision. ZEROs overwrite ONEs
– F_A	Auxiliary Framing Bit	See section 6.3 in ITU I.430
– N		N = $\overline{F_A}$
– B1	B1-Channel Data Bit	User data
– B2	B2-Channel Data Bit	User data
– A	Activation Bit	A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
– S	S-Channel Data Bit	S_1 or S_2 channel data
– M	Multiframing Bit	M = (1b) → Start of new multi-frame

3.4.3 State Machine Notation

The state machines include all the information necessary for the user to understand and predict the behavior of the S-transceiver. The information contained in a state bubble is:

State (state name, based on ITU I.430), ***i_x*** (S/T signal transmitted), ***i_r*** (S/T signal received), ***Ind.*** (C/I code transmitted) and ***Cmd.*** (C/I code received). Received S/T signals and C/I codes are transition criterias.

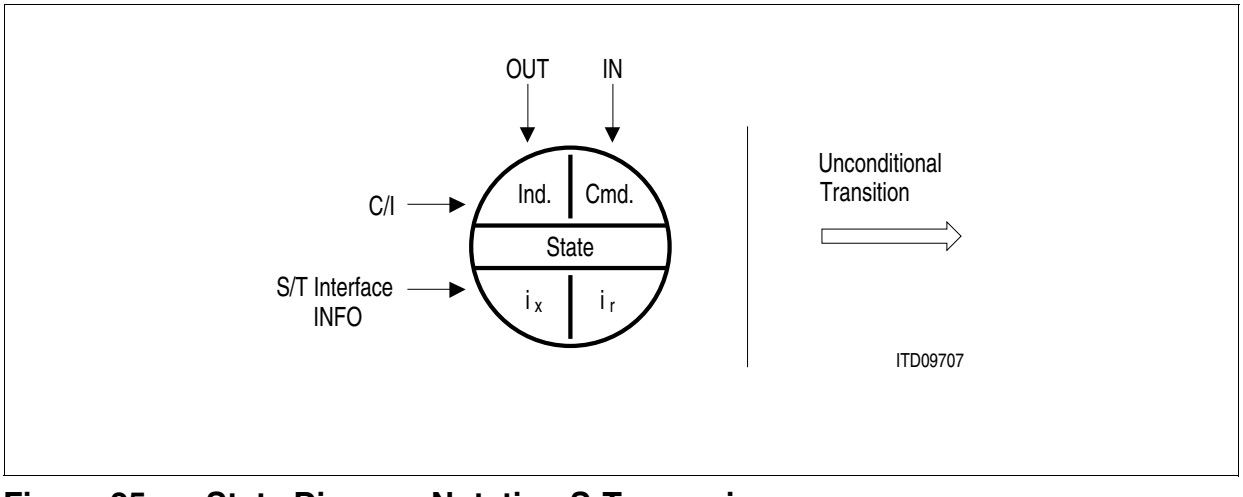


Figure 25 State Diagram Notation S-Transceiver

The following example illustrates the use of a state diagram with an extract of the NT state diagram (**Chapter 3.4.4**). The explained state is "G1 $\overline{i0}$ Detected".

Example:

The state is entered:

– *from state "Deactivated" after $\overline{i0}$ has been received.*

The following S/T signal and C/I code are transmitted:

– *INFO 0 (no signal) is sent on the S/T-interface.*
– *C/I message "AR" is issued on the IOM-2 interface.*

The state is left at occurrence of one of the following events:

– *Leave for the state "G2 Pend. Act" after "ARD" code has been received on IOM-2.*

Leave for the state "G4 Pend. Deact." in case C/I = DR is received.

Combinations of multiple conditions are possible as well. A "&" stands for a logical AND combination. An "or" indicates a logical OR combination. Negated arguments are overlined (e.g. $\overline{X}$).

3.4.4 State Machine

3.4.4.1 NT Mode State Diagram

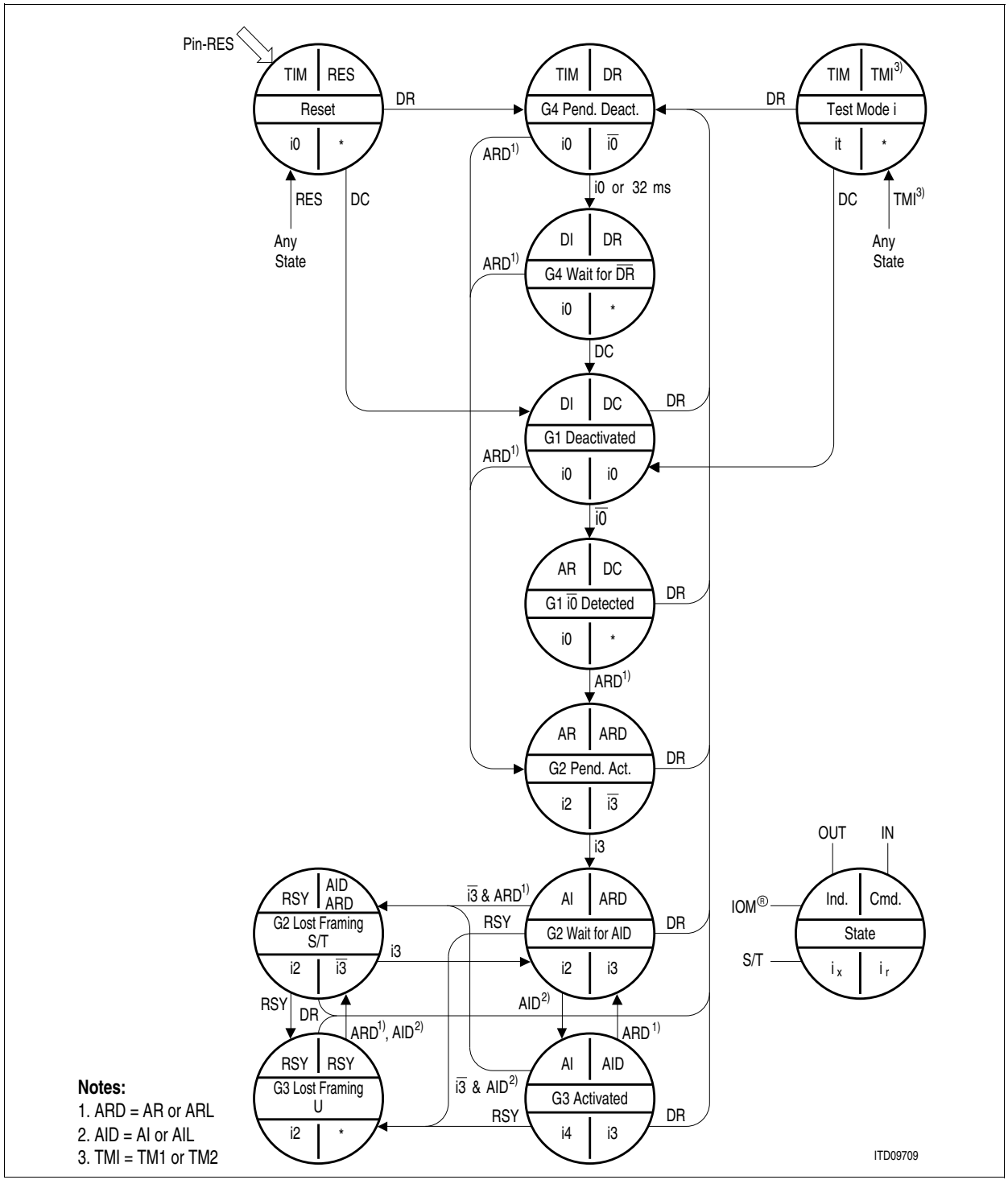


Figure 26 State Diagram

3.4.4.2 Inputs to the S-Transceiver

The transition criteria used by the S-transceiver are described in the following sections. They are grouped into:

– C/I commands
– Pin states
– Events on the S/T-interface.

C/I Commands

AR	Activation Request. This command is used to start an exchange initiated activation.
ARL	Activation request loop. The S-transceiver is requested to operate an analog loop-back close to the S/T-interface.
AI	Activation Indication. Confirms that the U-interface is fully transparent, D-channel data transfer is allowed.
AIL	Activation Indication loop. Command to close the analog loop on the S-interface.
DC	Deactivation Confirmation. Transfers the S-transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).
DR	Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. Unconditional command.
RES	Reset of state machine. Transmission of Info 0. No reaction to incoming infos. RES is an unconditional command.
RSY	Resynchronizing. The U-interface has not obtained or lost synchronization. INFO 2 is transmitted consequently by the S-transceiver.
TM1	Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is an unconditional command.
TM2	Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a frequency of 96 kHz. TM2 is an unconditional command.

Pin States

Pin-$\overline{\text{RES}}$ Pin-Reset. Corresponds to a low level at pin $\overline{\text{RES}}$, a power-on reset or an undervoltage detection. The function of this pin is identical to the C/I code RES concerning the state machine.

Pin-TM1 Selected if pins TM0=0 and TM1=1. Transfers the S-transceiver into the "Test mode i" state. Here a 2-kHz signal of alternating pulses is transmitted on the S/T-interface.

Pin-TM2 Selected if pins TM0=TM1=0. Transfers the S-transceiver into "Test Mode i" state. Here a signal consisting of continuous binary ZEROs is sent at the rate of 96 kHz.

S/T-Interface Events

i0 INFO 0 detected

$\overline{\text{i0}}$ Level detected (any signal different from I0)

i3 INFO 3 detected

$\overline{\text{i3}}$ Any INFO other than INFO 3.

3.4.4.3 Outputs of the S-Transceiver

The following signals and indications are issued on the IOM-2 and S/T-interface.

C/I Indications

TIM Timing. S-transceiver requires clock pulses.

RSY Resynchronizing. Receiver is not synchronous.

AR Activate request. $\overline{\text{INFO 0}}$ or command AR received.

AI Activate indication. Synchronous receiver.

DI Deactivation Indication. Timer (32 ms) expired or INFO 0 received after received C/I code DR.

S/T-Interface Signals

The signals transmitted on the S-interface are defined in **Table 11**.

i0 INFO 0

i2 INFO 2

i4 INFO 4

it Pseudo ternary pulses at 2-kHz frequency (TM1).
Pseudo ternary pulses at 96-kHz frequency (TM2).

3.4.4.4 States

G1 Deactivated

The S-transceiver is not transmitting. No signal is detected on the S/T-interface, and no activation command is received in C/I channel. DI is output in the normal deactivated state, and TIM is output as a first step when an activation is requested from the S/T-interface ($\overline{i0}$).

G1 $\overline{I0}$ Detected

An $\overline{INFO\ 0}$ is detected on the S/T-interface, translated to an "Activation Request" indication in the C/I channel. The S-transceiver is waiting for an AR command, which normally indicates that the transmission line upstream (the two-wire U-interface) is synchronized.

G2 Pending Activation

As a result of the ARD command INFO 2 is sent on the S/T-interface. INFO 3 is not yet received.

G2 Wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the S-transceiver waits for a "switch-through" command AID from the device upstream.

G3 Activated

INFO 4 is sent on the S/T-interface as a result of the "switch through" command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

G2 Lost Framing S/T

This state is reached when the S-transceiver has lost synchronism in the state 'G3 activated' or 'G2 Wait for AID'.

G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the two-wire U-interface, the S-transceiver transmits INFO 2.

G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state "G4 wait for $\overline{DR}$") is issued by the S-transceiver when:

- either INFO 0 is received
- or an internal timer of 32 ms expires.

G4 Wait for $\overline{DR}$

Final state after a deactivation request. The S-transceiver remains in this state until an C/I code DC is received.

Test Mode 1

Single alternating pulses are sent on the S/T-interface (2-kHz repetition rate).

Test Mode 2

Continuous alternating pulses are sent on the S/T-interface (96 kHz).

Reset state

A hardware or software reset (RES) forces the S-transceiver to an idle state where the analog components are disabled (transmission of INFO0) and the S/T line awake detector is inactive. Thus activation from the TE is not possible.

3.4.5 C/I Codes

Both commands and indications depend on the data direction. **Table 9** presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM frames (Double last-look criterion). Indications are strictly state orientated. Refer to the state diagrams in the previous sections for commands and indications applicable in various states.

Table 9 S-Transceiver C/I Codes

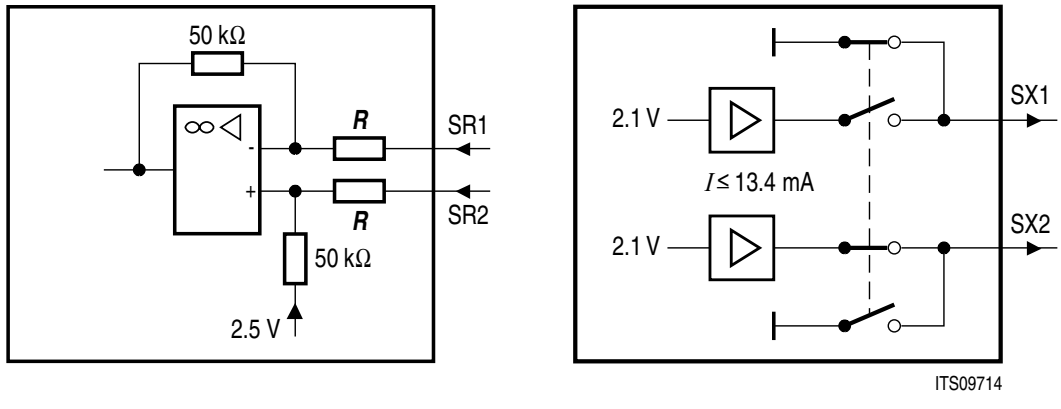
Code	NT	
	IN	OUT
0000	DR	TIM
0001	RES	–
0010	TM1	–
0011	TM2	–
0100	RSY	RSY
0101	–	–
0110	–	–
0111	–	–
1000	AR	AR
1001	–	–
1010	ARL	–

Code	NT	
	IN	OUT
1011	–	–
1100	AI	AI
1101	–	–
1110	AIL	–
1111	DC	DI

AI	Activation Indication	DR	Deactivation Request
AIL	Activation Indication Loop	RES	Reset
AR	Activation Request	RSY	Resynchronizing
ARL	Activation Request Loop	TIM	Timer
DC	Deactivation Confirmation	TIM1	Test Mode 1 (2-kHz signal)
DI	Deactivation Indication	TM2	Test Mode 2 (96-kHz signal)

3.4.6 Analog Line Port

The equivalent circuits of the integrated receiver and transmitter stages are shown in Figure 27.



R = 40 kΩ if transformer ratio is 2:1
R = 20 kΩ if transformer ratio is 1:1

Figure 27 Receiver and Transmitter Stages

The S-bus receiver is designed as a threshold detector with adaptively switched threshold levels. The S-bus receiver is symmetrical, which allows for a simple external circuitry and printed circuit board layout to meet the I.430 receiver input impedance specification.

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as two current limited voltage sources. A voltage of 2.1 V is delivered between SX1-SX2, which yields a current of 7.5 mA over 280 Ω.

S/T-Interface Circuitry

In order to comply to the physical requirements of ITU recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the S-transceiver needs some additional circuitry.

The **transmitter** requires external resistors (20 … 40 Ω) in order to adjust the output voltage to the pulse mask (nominal 750 mV according to ITU I.430, to be tested with the test mode "TM1") on the one hand and in order to meet the output impedance of minimum 20 Ω on the other hand.

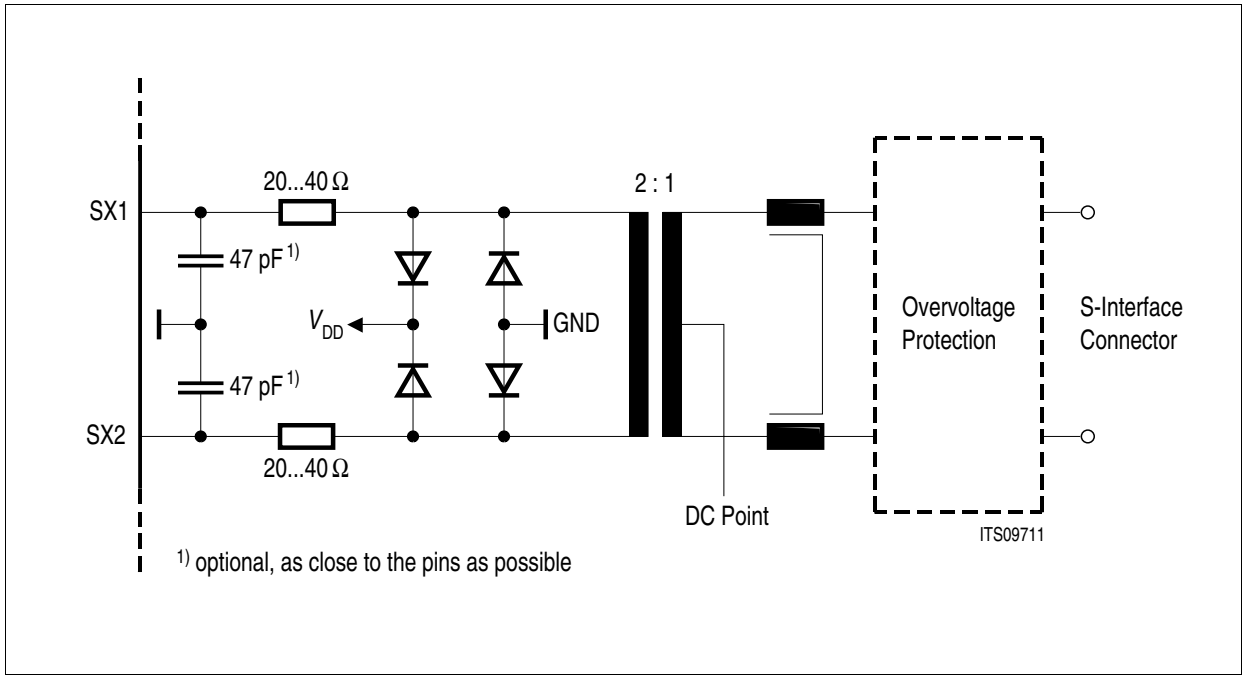


Figure 28 S-Interface Transmitter External Circuitry

The **receiver** of the S-transceiver is symmetrical. 10 kΩ overall resistance are recommended in each receive path. Although it is possible to place two single 10 kΩ resistors, either between transformer and diode circuit or between chip and diode circuit, it is preferable to split the resistance into two resistors for each line. This allows to place a high resistance between the transformer and the diode protection circuit (required to

pass 96 kHz input impedance test of ITU I.430). The remaining resistance (1.8 kΩ) protects the S-transceiver itself from input current peaks.

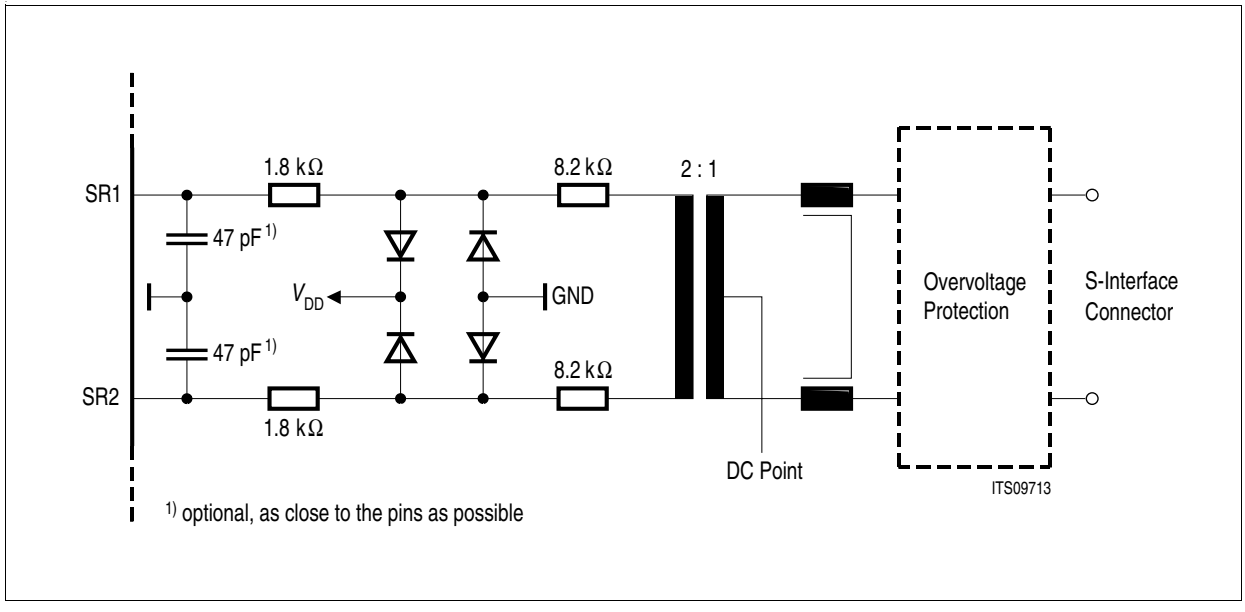


Figure 29 S-Interface Receiver External Circuitry

3.4.7 Timing Recovery

The transmit PLL (XPLL) synchronizes a 192 kHz transmit bit clock to the IOM-2 clock FSC (8 kHz).

– In a point-to-point or extended bus configuration the Receive PLL (RPLL) recovers bit timing from the detector´s output signal and provides a synchronous 1536-kHz clock (adaptive timing recovery from the receive data stream on the S-interface). Divided by eight this clock is used as 192-kHz receive data clock (PP).
– In a passive bus configuration, a 192-kHz receive clock (MP) generated by the transmit PLL (XPLL) is used to sample the input data (fixed timing recovery).

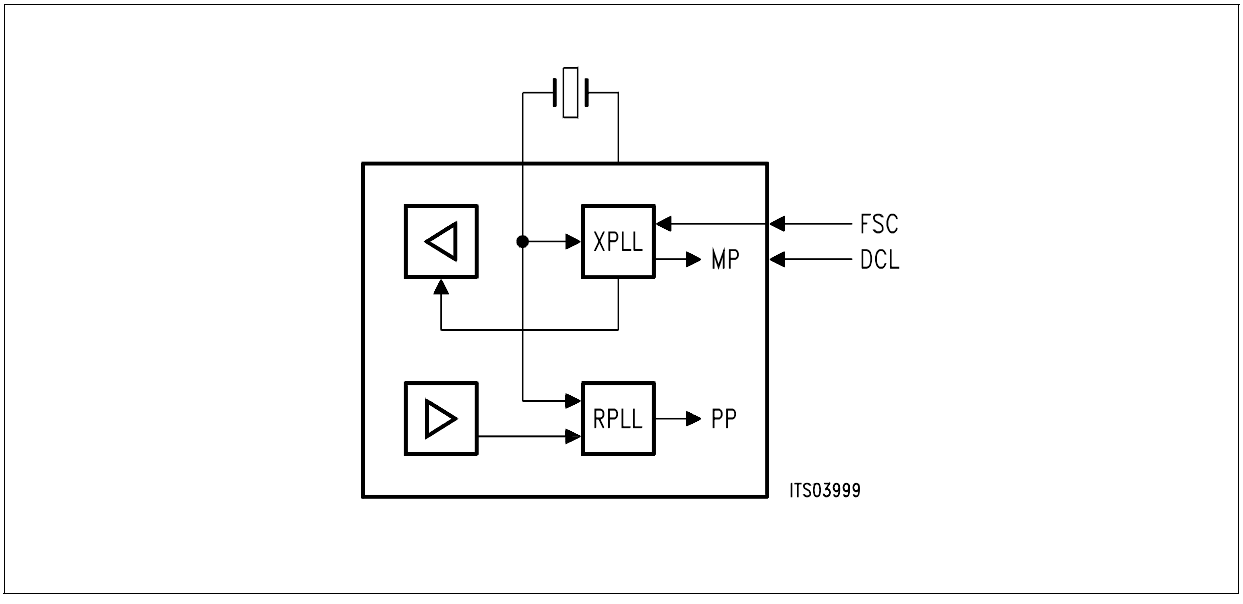


Figure 30 Clock System of the S-Transceiver

3.5 Reset

Please refer to **Chapter 8.1**.

3.6 Test Modes

Pins TM0-1 are used to select the different transceiver test modes as given in **Table 10**.

Table 10 Transceiver Test Modes

TM0	TM1	U-transceiver	S-transceiver
0	0	normal operation	Test Mode 2 (SCZ)
0	1		Test Mode 1 (SSZ)
1	0	Test Single Pulses	normal operation
1	1	normal operation	

In Test Mode 1 the S-transceiver transmits alternating pulses at a frequency of 2 kHz. In Test Mode 2 alternating pulses at a frequency of 96 kHz are transmitted.

Test Single Pulses requests the transmission of single pulses on the U-interface. The pulses are issued at 1.0 ms intervals and have equal polarity.

4 Part I 'NTC-T': Operational Description

4.1 Layer 1 Activation/Deactivation

This chapter illustrates the interactions during activation and deactivation between the U- and the S-interface. The information presented in this section is extracted from the U- and S-transceiver state machines.

All S/T-interface signals used in the following sections as defined by ITU I.430 are explained in **Table 11**. **Table 12** shows all U-interface signals.

Table 11 S/T-Interface Signals

Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal.	INFO 0	No signal.
		INFO 1	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs.
INFO 2	Frame with all bits of B, D, and D-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.		
		INFO 3	Synchronized frames with operational data on B and D-channels.
INFO 4	Frames with operational data on B, D, and D-echo channels. Bit A set to binary ONE.		

Table 12 U-Interface Signals

Upstream from NT to LT	Downstream from LT to NT
INFO U1W: 16 times ternary + + + + + + + + − − − − − − − − A tone of: Frequency: 7.5 kHz Width: 2.13 ms	INFO U2W 16 times ternary + + + + + + + + − − − − − − − − A tone of: Frequency: 7.5 kHz Width: 2.13 ms
INFO U1A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code	INFO U2A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code
INFO U1: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)	INFO U2: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)
INFO U3: Binary continuous "1" before scrambling. Frame (Transmitting Barker code)	INFO U4H: Binary continuous "1" before scrambling with duration of 1 ms. Frame (Transmitting Barker code)
INFO U5: Binary data from the digital interface. Frame (Transmitting Barker code)	INFO U4: Binary data from the digital interface. Frame (Transmitting Barker code)
INFO U0: Ternary continuous "0" No frame, no signal level	INFO U0: Ternary continuous "0" No frame, no signal level

Activation Initiated by Exchange

Figure 31 depicts the procedure if activation has been initiated by the exchange side (LT).

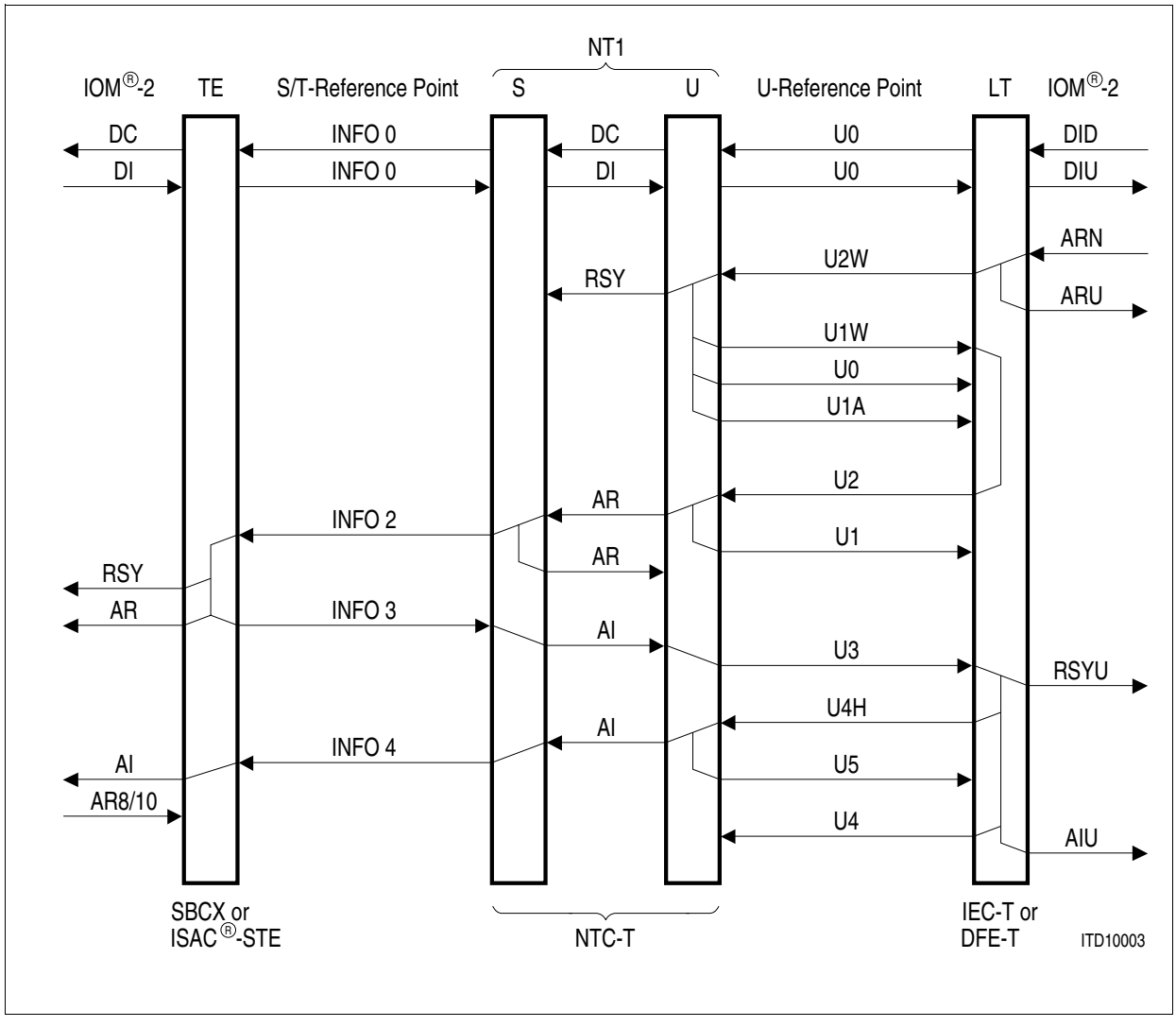


Figure 31 Activation Initiated by Exchange

Activation Initiated by TE

Figure 32 depicts the procedure if activation has been initiated by the terminal side (TE).

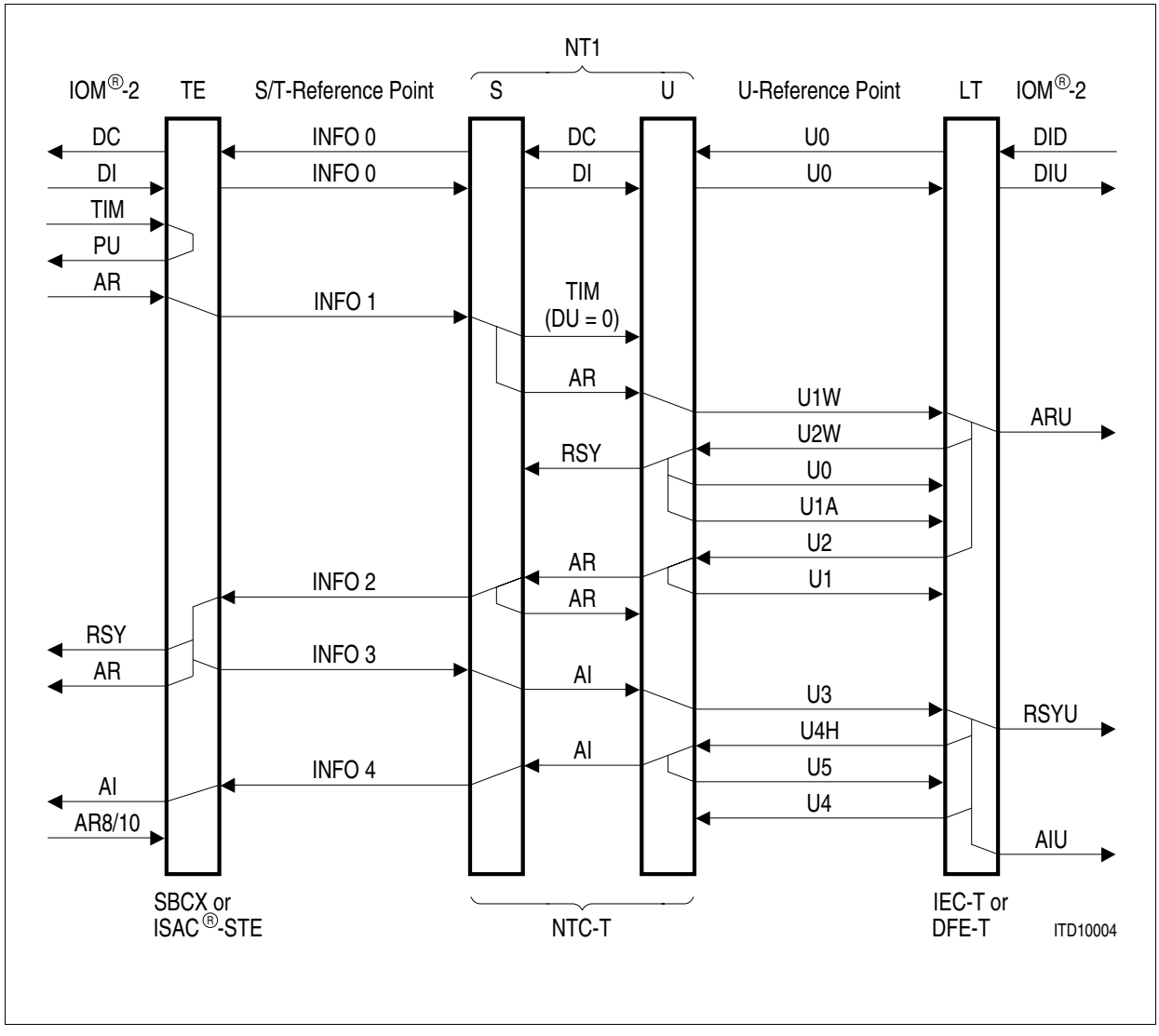


Figure 32 Activation Initiated by Terminal (TE)

Deactivation

Figure 33 depicts the procedure if deactivation has been initiated. Deactivation of layer 1 is always initiated by the exchange (LT)

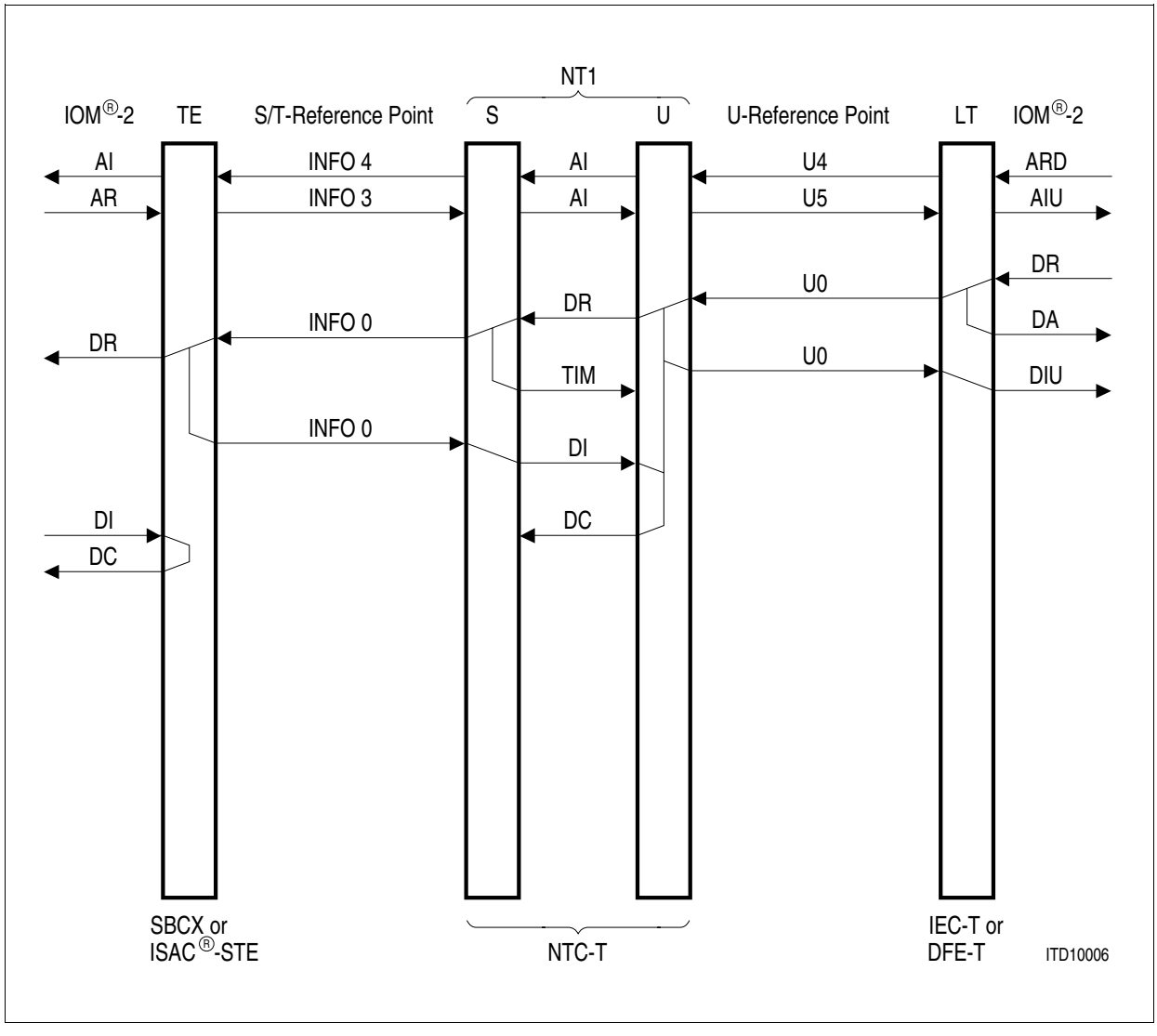


Figure 33 Deactivation

Activation of Loop 2

Figure 34 depicts the procedure if activation of loop 2 has been initiated by the exchange (LT).

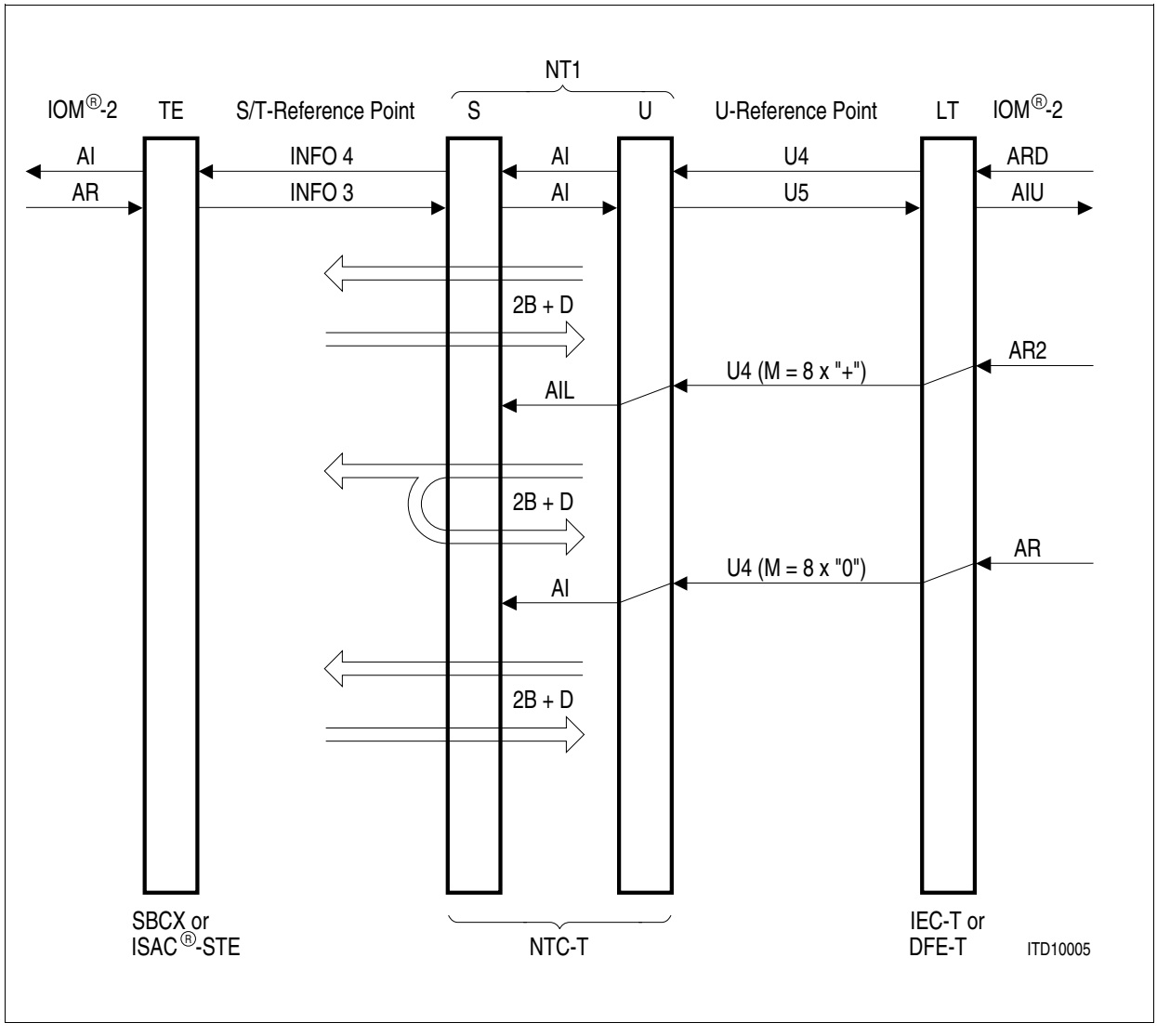


Figure 34 Activation of Loop 2

4.2 External Circuitry

Please refer for information on:

- Power supply blocking recommendation to **Chapter 8.2.1**.
- U-interface hybrid to **Chapter 8.2.2**.
- S-interface external circuitry to **Chapter 3.4.6**.

4.3 Oscillator Circuit

Figure 35 illustrates the recommended oscillator circuit.

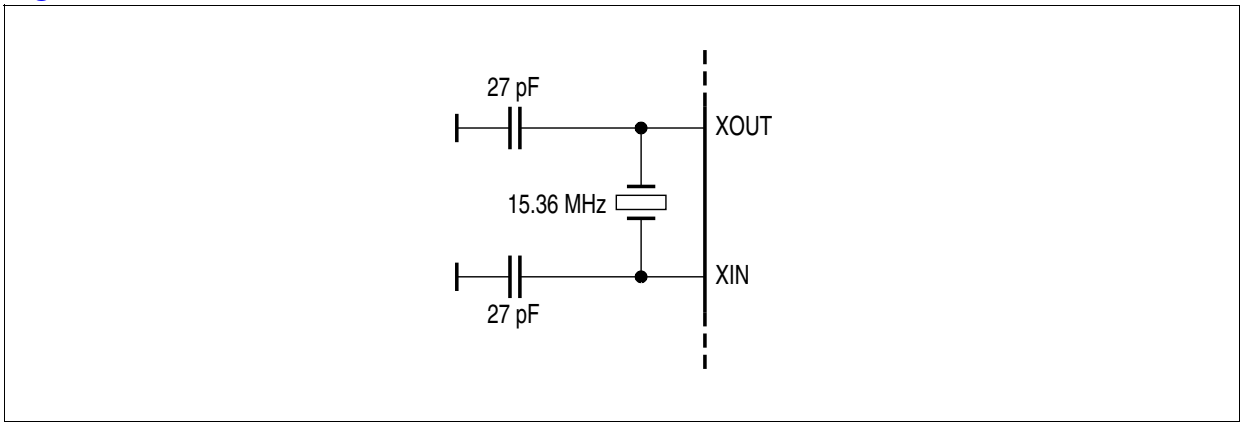


Figure 35 Crystal Oscillator

Crystal Parameters

Frequency:	15.36 MHz
Load capacitance:	20 pF +/- 0.3 pF
Frequency tolerance:	60 ppm
Resonance resistance:	20 Ω
Max. shunt capacitance:	7 pF
Oscillator mode:	fundamental

Note: Typical values for the capacitances connected to the crystal are 22 ... 33 pF.

5 Part II 'IEC-T': General Description

The NTC-T AM PEB 80900 with IEC-T functionality selected is an advanced CMOS circuit for transmission over public telephone lines. The transmission technique used is according to the Uk0 interface specification of the Deutsche Bundespost. The adaptive filter concept of the NTC-T AM with IEC-T functionality selected is based on a highly digital approach which utilizes sophisticated digital signal processing capability.

The NTC-T AM PEB 80900 with IEC-T functionality selected enables digital full duplex voice/data transmission via the standard twisted pair telephone cable (U Interface) with a user bit rate of 144 kbit/s according to the ISDN standards. Together with the flexible IOM® interface, it is fully compatible to operate with the PEB 2070 (ICC) and PEB 2080 (SBC) devices and also enables a repeater (two NTC-T AM PEB 80900 with IEC-T functionality selected back to back) for longer telephone loops.

The NTC-T AM PEB 80900 with IEC-T functionality selected is capable of operating in the following applications by means of pin strapping: the exchange, the network termination, the terminal equipment, and the trunk module connecting a PABX to the public network.

The Data Sheet gives a complete description of all the functions of the NTC-T AM PEB 80900 with IEC-T functionality selected. These functions are mainly derived from the general ISDN system concept based on CCITT recommendations and Deutsche Bundespost standards. More specific functions are due to internal requirements of the switching system and to the chosen approach of realization.

5.1 Basic System Functions

- Full duplex transmission and reception of the Uk0 interface signals according to the FTZ Guideline 1 TR 220 of the Deutsche Bundespost (DBP).
  - 144 kbit/s user bit rate over standard local telephone loops.
  - 1 kbit/s maintenance channel for transmission of data loop back commands and detected transmission errors.
  - 4B3T ternary block code (subscriber line symbol rate 120 kbaud).
  - Monitoring of transmission errors.
  - Subscriber loop length without repeater:
    up to 4.2 km on 0.4 mm wire
    up to 8.0 km on 0.6 mm wire
- Adaptive echo cancellation.
- Adaptive equalization.
- Automatic polarity adaption.
- Clock recovery (frame and bit synchronization) in all applications.
- Transposition of ternary to binary data and vice versa (coding, decoding, scrambling, descrambling, phase adaption).
- Built in wake-up unit for activation from power-down state.
- Activation and deactivation procedure according to CCITT I.430 and to FTZ Guideline 1 TR 210 of the DBP.
- Adaption of internal interfaces to the current signal direction by programmable operation modes:
  - LT: Line termination in public or private exchange
  - NT: Network termination connected to SBC
  - NT-PABX: Trunk module (TMD)
  - NT-TE: Terminal equipment
  - LT-RP: U Repeater unit subscriber side
  - NT-RP: U Repeater unit exchange side
- Optimized for working in conjunction with SBC and ICC telecom IC's via IOM® interface.
- Data speed conversion between the Uk0 frames and the IOM® frames. In the LT and NT-PABX modes, absorption of received phase-wander of up to 18 µs peak to peak (CCITT Rec. Q.512).
- Handling of commands and indications contained in the IOM® C/I channel for (de-) activation, supervision of power supply unit and equipment for wire testing.
- Data availability via the MONITOR channel:
  - accumulated RDS transmission errors; in the LT mode for the whole Uk0 link, in the NT mode only for those detected in the circuit itself.
  - measurement value of the loop current.
  - Echo canceller coefficients and status values, which can be used to indicate the state of the Uk0 interface.

- Switching of an analog test loop at the Uk0 interface for testing as many units of the NTC-T AM with IEC-T functionality selected as possible (loop 1 in LT, loop 4 in the repeater and loop 3 in the NT-PABX mode in reverse direction to the public exchange).
- Switching of a digital test loop as near to the IOM® interface as possible (loop 2 in NT-PABX and NT-TE).
- Remote control of test loop switching via maintenance channel.
  - Test loop 2 in the SBC (NT mode).
  - Test loop 2 in the NTC-T AM with IEC-T functionality selected near to the IOM® interface in the NT-PABX and TE modes.
  - Test loop4 in the NTC-T AM with IEC-T functionality selected LT-repeater mode near to the U-line.
- Generation of a synchronized 7.68 MHz clock for the SBC in the NT mode.

5.1.1 Pin Configuration of the NTC-T AM with IEC-T Functionality

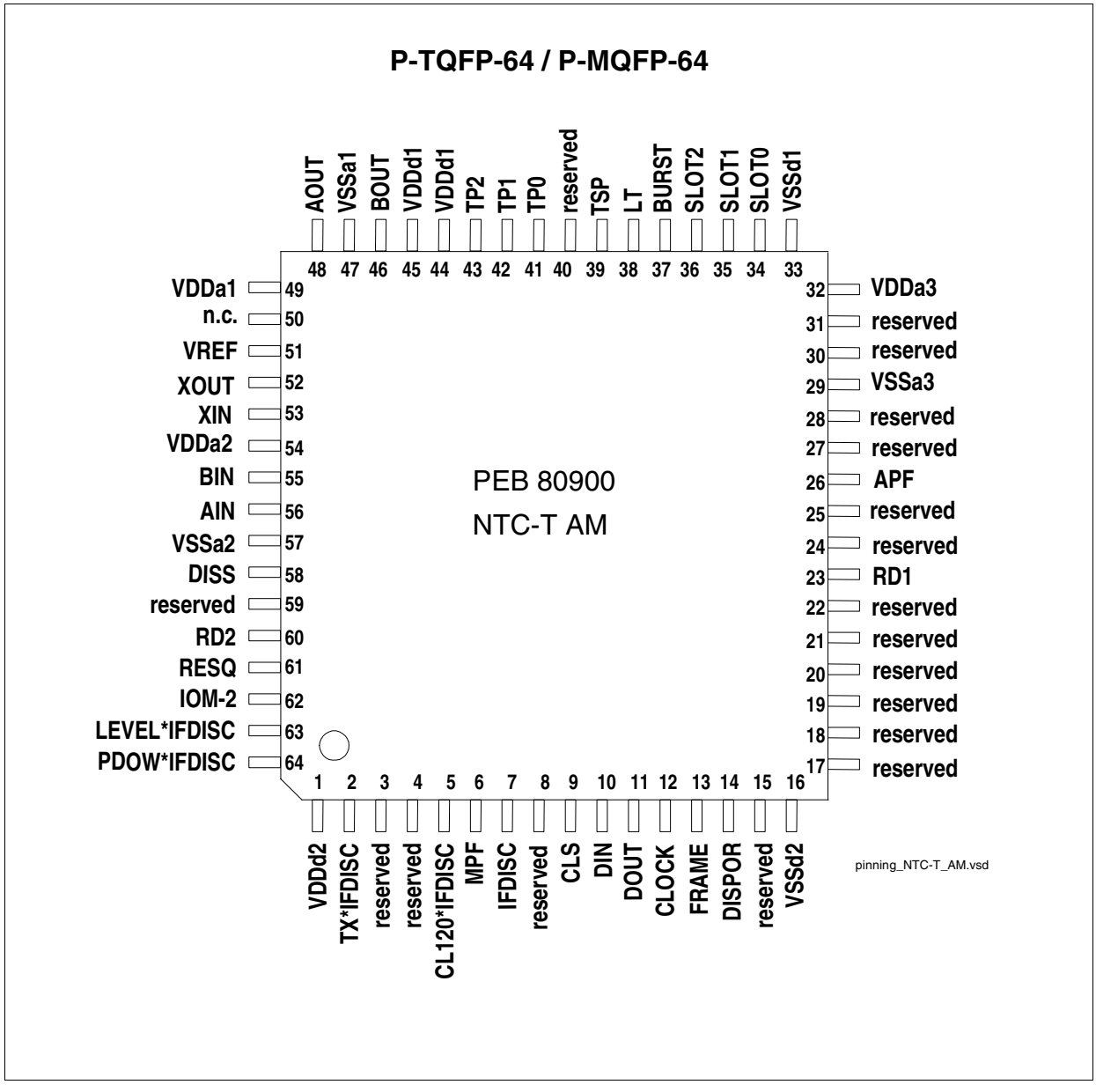


Figure 36 Pin Configuration of the NTC-T AM with IEC-T Functionality

5.2 Related Documents

- FTZ-Richtlinie 1 TR 210, Aktivierung/Deaktivierung des Basisanschlusses (Schicht 1)
- FTZ-Richtlinie 1 TR 220, Spezifikation der Schnittstelle Uk0 (Schicht 1)
- ISDN oriented Modular Interface Specification Rev. 2.1
- PBC Peripheral Board Controller PEB 2050, Technical Description
- ICC ISDN Communications Controller PEB 2070, Technical Description Edition 3.86, User´s Manual 01.94
- SBC S-Bus Controller PEB 2080, Technical Description Edition 4.86, User´s Manual 06.92

5.3 Operation Modes and Functions

5.4 The ISDN Telecom IC Family from Siemens

The NTC-T AM with NTC-T functionality selected is designed to operate optimally together with the other telecom components from Siemens. Each family member fits into a complete self-sufficient device concept for ISDN systems.

5.4.1 PEB 2070 ISDN Communications Controller (ICC)

Besides switching functions for the 64 kbit/s B channels, D channel protocol handling is the main task of the microprocessor compatible ICC. Its characteristic features are determined by a sophisticated on-chip data link access protocol controller on D channel (LAPD) and a sophisticated FIFO structure. The 16 kbit/s D channel carries signaling information, telemetry data, and packet-switched data.

5.4.2 PEB 2080 S-Bus Interface Circuit (SBC)

The SBC realizes the four-wire S-interfacing between subscriber terminal and network termination. The NTC-T AM with NTC-T functionality selected is designed to meet all the requirements stipulated by CCITT. Moreover, it implements additional features necessary in specific applications. The device contains transceiver functions, timing recovery for different modes of operation, circuitry for collision resolution, and a state control block to handle the activation/deactivation procedure. It also allows up to 8 terminals to be connected to the same network termination.

5.4.3 PEB 2085 ISDN Subscriber Access Controller (ISAC-S)

The ISAC-S, the implementation of the SBC and ICC on one chip, provides a mono chip solution for interfacing a subscriber terminal to the four-wire S-bus.

5.4.4 PEB 2095 ISDN Burst Transceiver Circuit (IBC)

The IBC solves the problems of data transmission via twisted pair telephone cables (U interface) in a time compression multiplex method. As an alternative to the NTC-T AM with NTC-T functionality selected the IOM® compatible device is optimized to the needs of PABX systems.

5.4.5 PEB 20950 ISDN Subscriber Access Controller (ISAC-P)

The ISAC-P, the implementation of the IBC and ICC on one chip, provides a monochip solution for the direct access of two-wire terminals In PABX systems.

5.4.6 PEB 2050 Peripheral Board Controller (PBC)

The microprocessor compatible PBC performs the control of voice, data, and signaling for up to 8 subscribers in digital line boards. This device implements the interface between the standard SLD bus, the PCM highways, and the on-board microprocessor. The high flexibility permits the use of this chip in various parts of a digital exchange system and enables its operation as a general purpose controller for data switching and mux/demux applications.

5.4.7 SAB 82520 High Level Serial Communications Controller (HSCC)

The HSCC is designed to interface high speed communication lines using the X.25 layer 2 protocol or the link access procedure for the D-channel (LAPD) to a microcomputer system. Special telecom features make this device extremely attractive for applications in switching and virtual circuit switching.

5.5 IOM® Concept and Applications of the IEC

The NTC-T AM with NTC-T functionality selected is designed to be used in: the Line Terminator (LT) part of the digital subscriber module (DSM), the Network Termination (NT), the Digital Trunk Basic Access (PABX) and in the Terminal Equipment (TE).

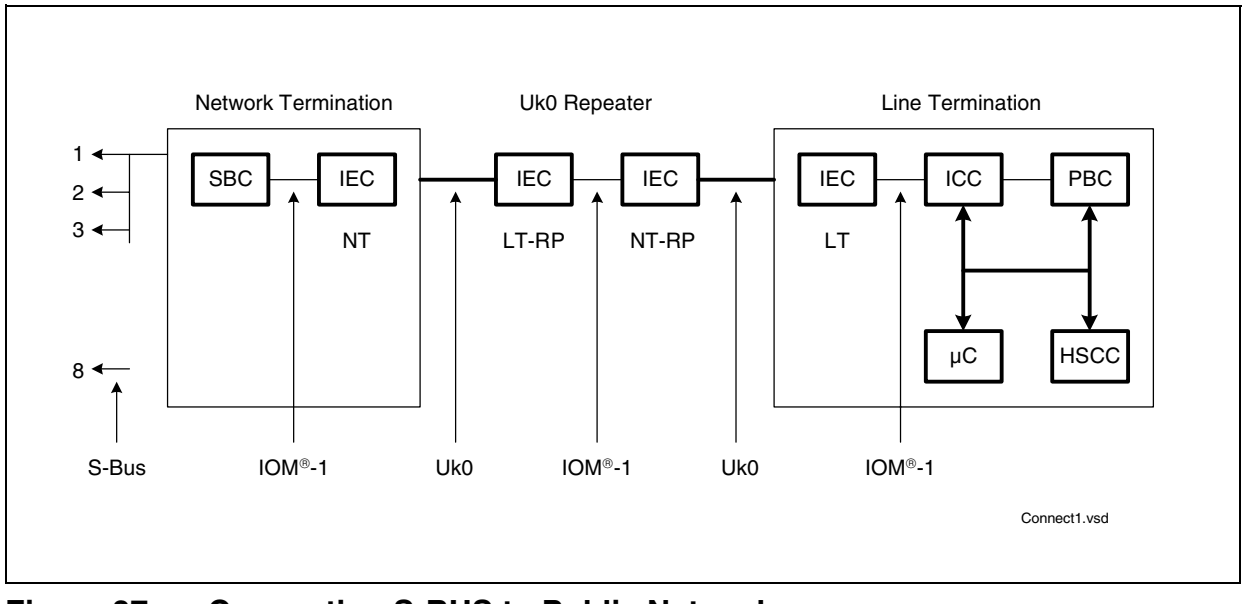


Figure 37 Connecting S-BUS to Public Network

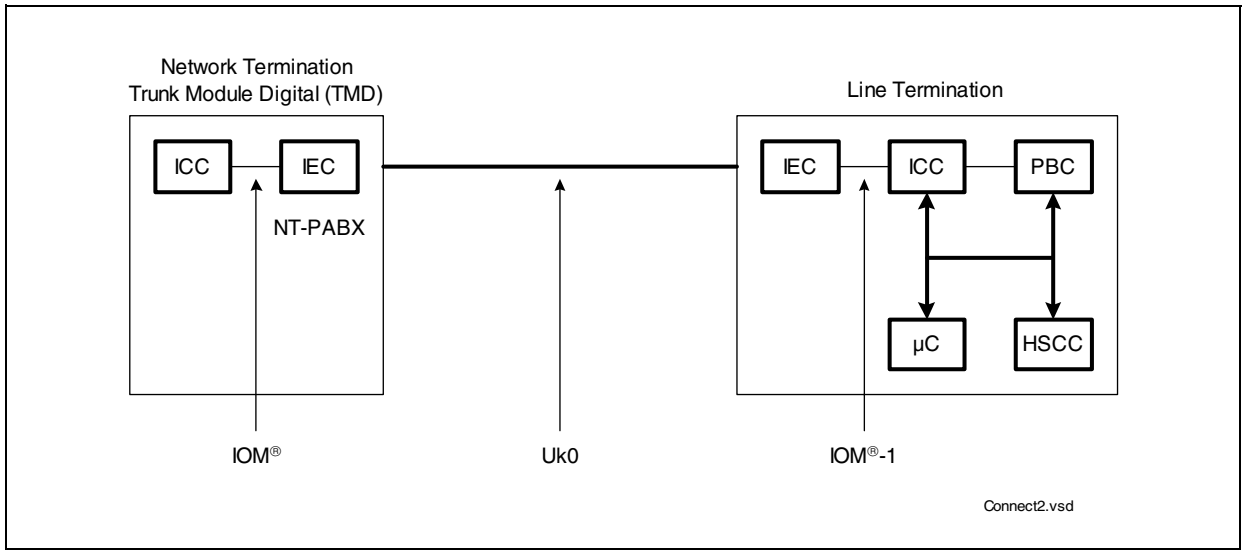


Figure 38 Connecting Private to Public Network

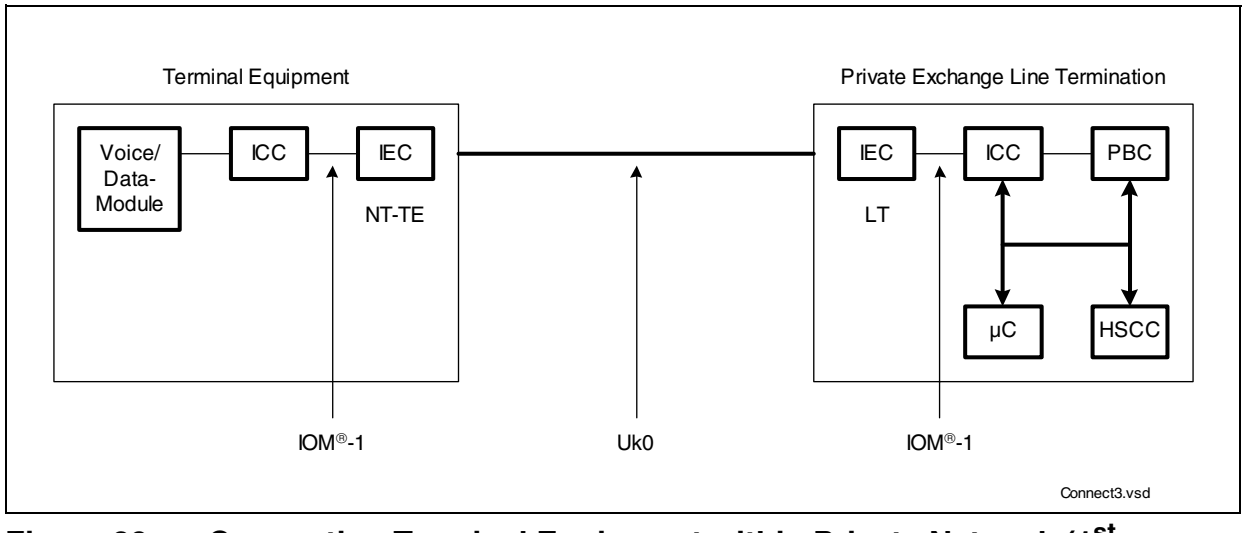


Figure 39 Connecting Terminal Equipment within Private Network (1st Generation)

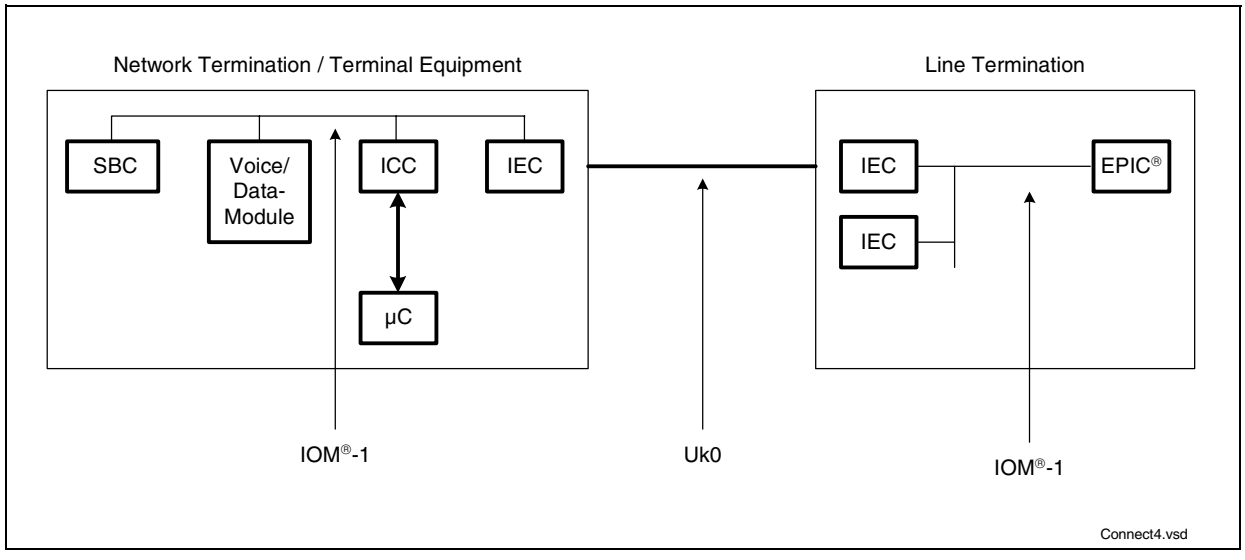


Figure 40 Connecting Network Termination or Terminal Equipment to Exchange (2nd Generation)

Table 13 Programming the NTC-T AM with IEC-T Functionality Operation Modes

Signal on Input Pin					Mode
LT	BURST	SLOT2	SLOT1	SLOT0	
1	0	0	0	0	LT
1	0	0	0	1	LT-RP: repeater downstream
1	1	*	*	*	LT-BURST: LT MUX mode
0	0	0	0	0	NT
0	0	0	0	1	NT-RP: repeater upstream
0	0	1	0	0	NT-PABX: PABX continuous mode
0	0	1	0	1	NT-TE: terminal equipment
0	1	*	*	*	NT-PABX BURST: PABX MUX mode

* In these modes SLOT2, SLOT1, SLOT0 are used for selecting the time slot rather than the mode.

5.6 Interfaces

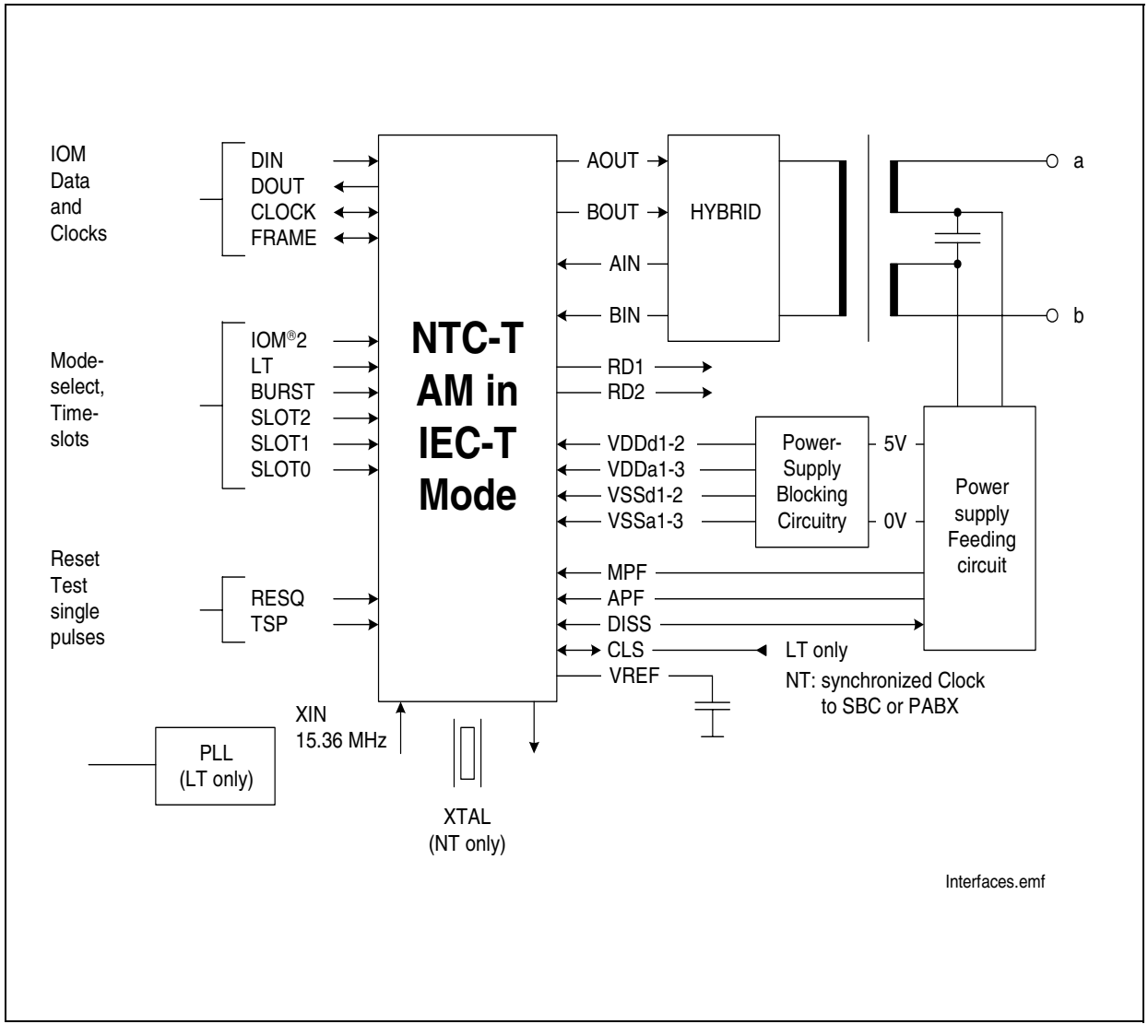


Figure 41 Interfaces of the NTC-T AM with IEC-T Functionality Selected

5.6.1 Interfaces in the Different Applications of the NTC-T AM with IEC-T Functionality Selected

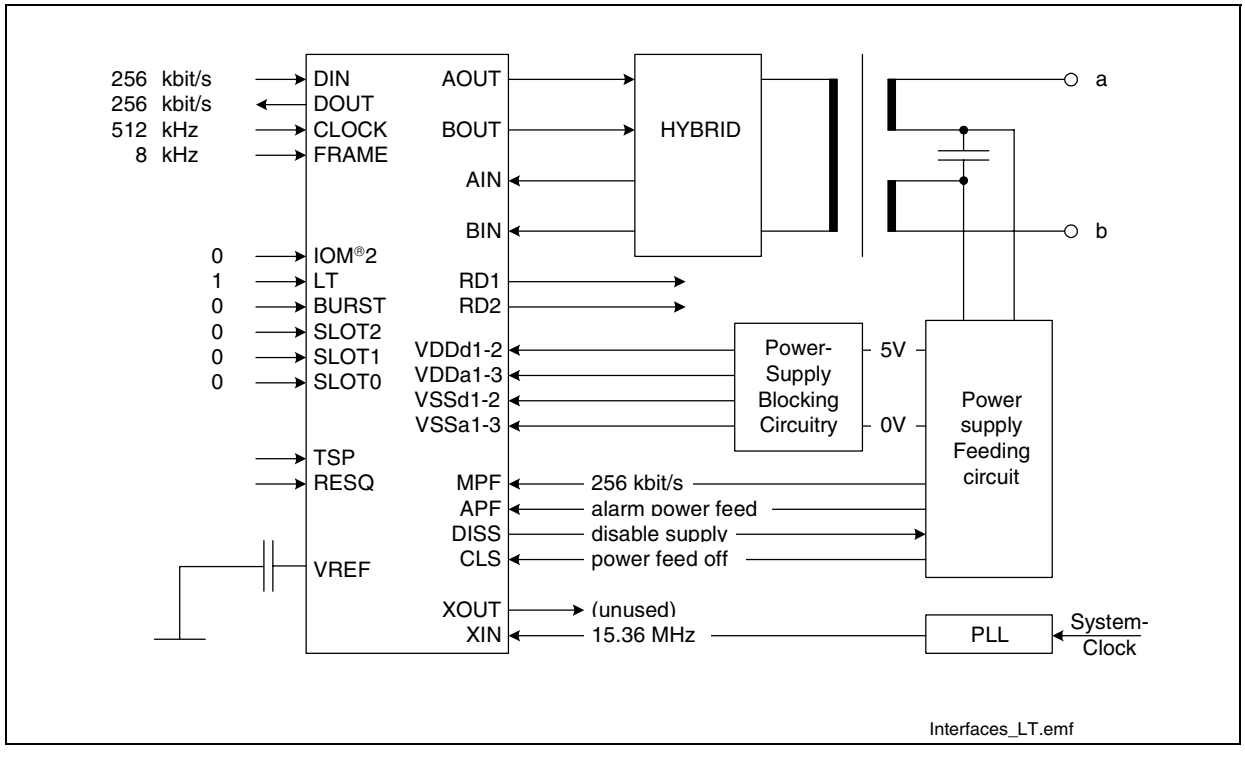


Figure 42 Interfaces of the NTC-T AM with IEC-T Functionality Selected in LT-Mode

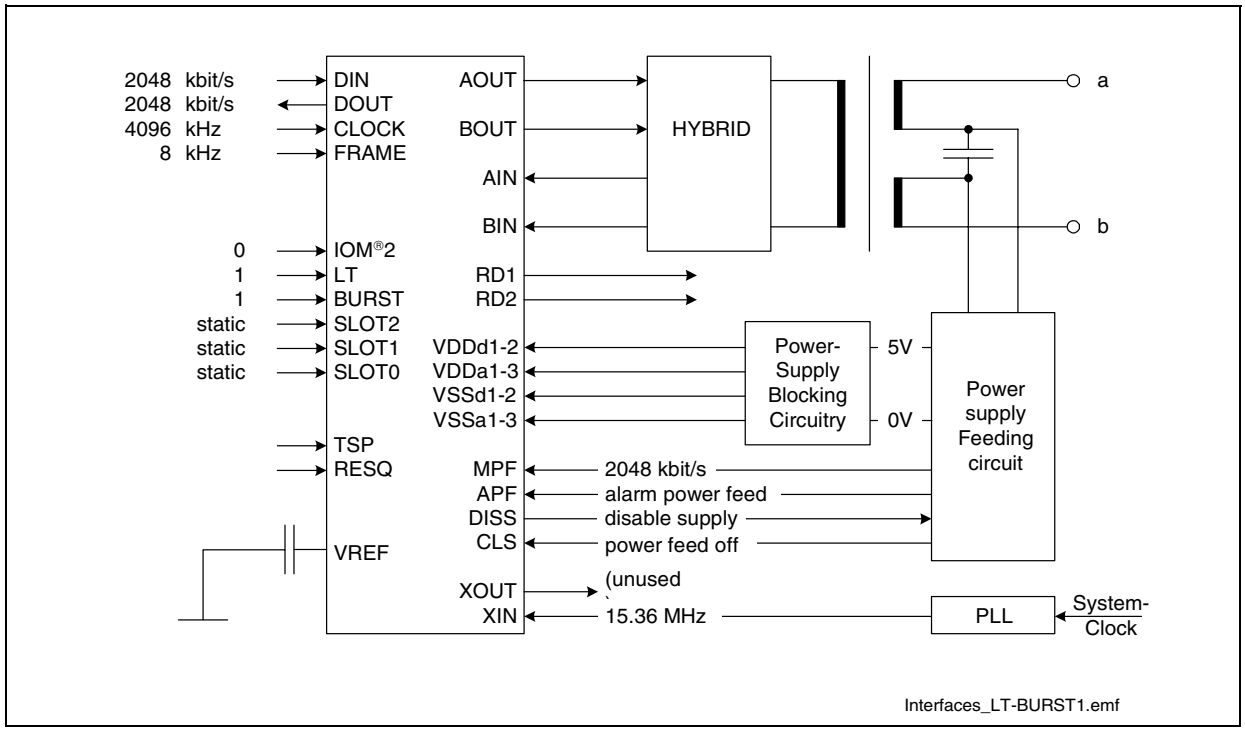


Figure 43 Interfaces of the NTC-T AM with IEC-T Functionality Selected in LT-BURST1 Mode

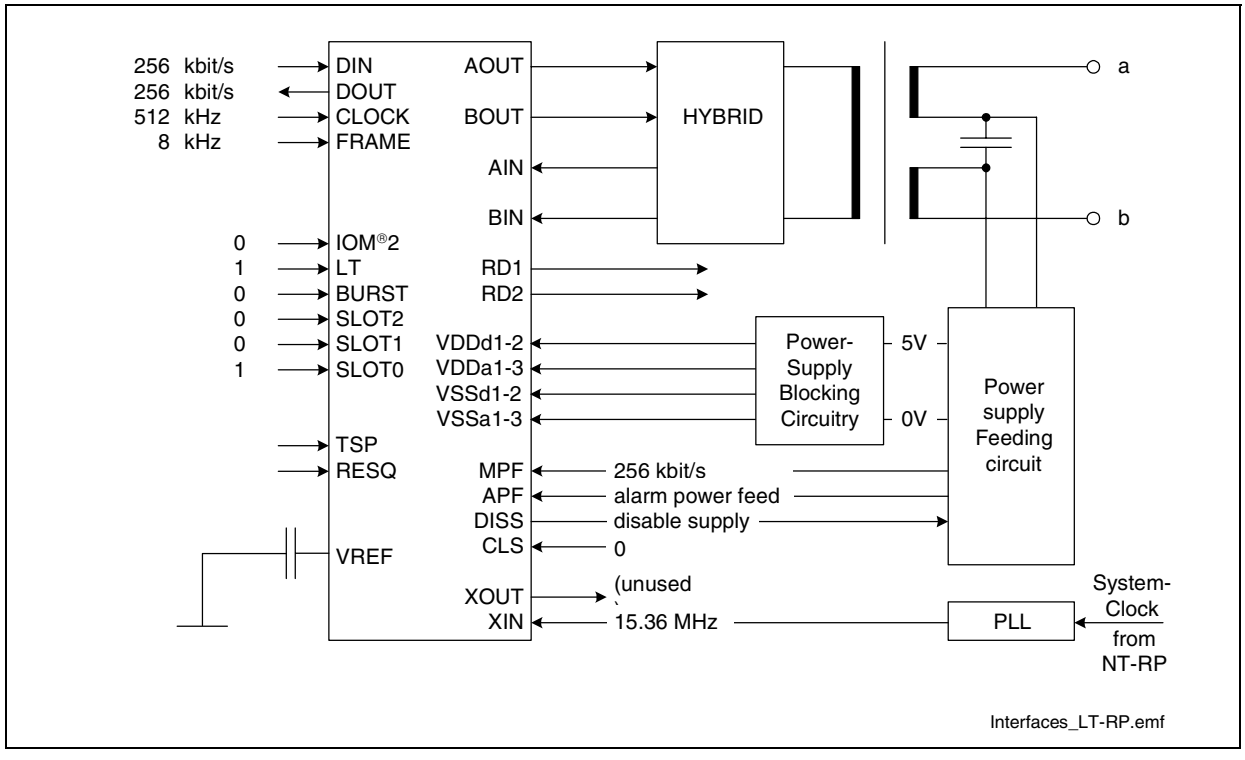


Figure 44 Interfaces of the NTC-T AM with IEC-T Functionality Selected in LT-RP Mode

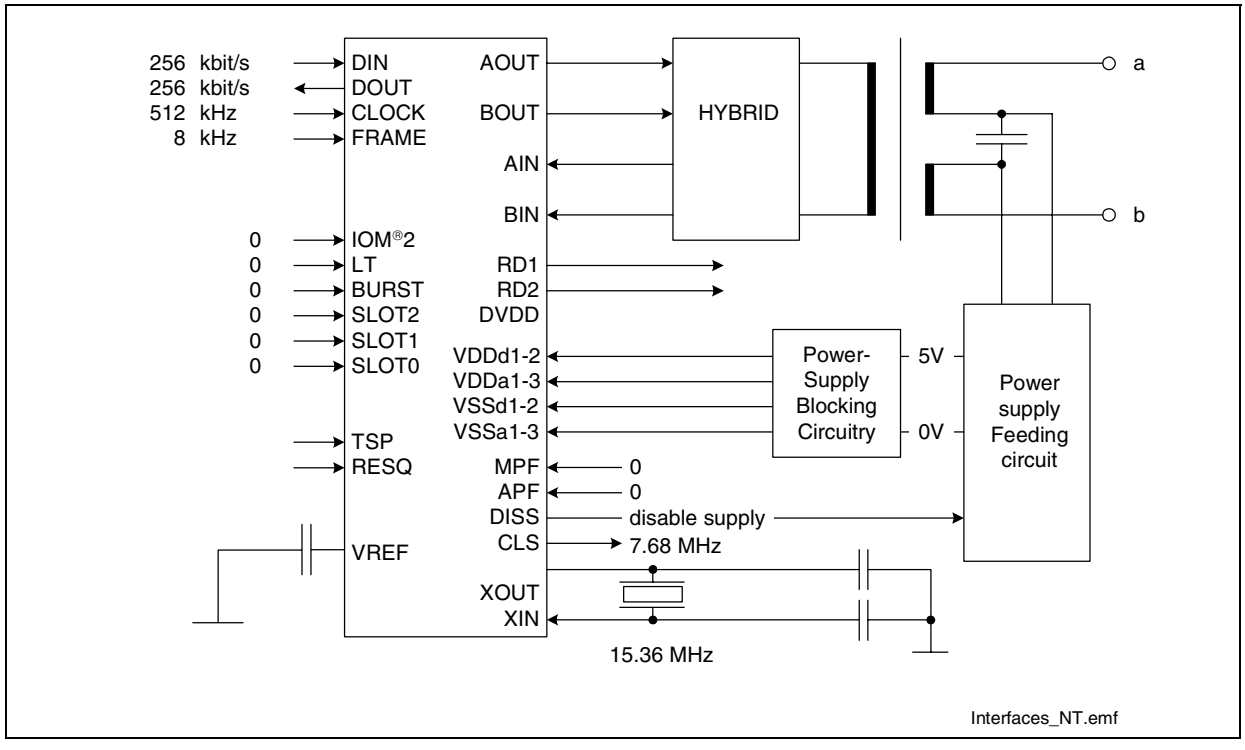


Figure 45 Interfaces of the NTC-T AM with IEC-T Functionality Selected in NT Mode

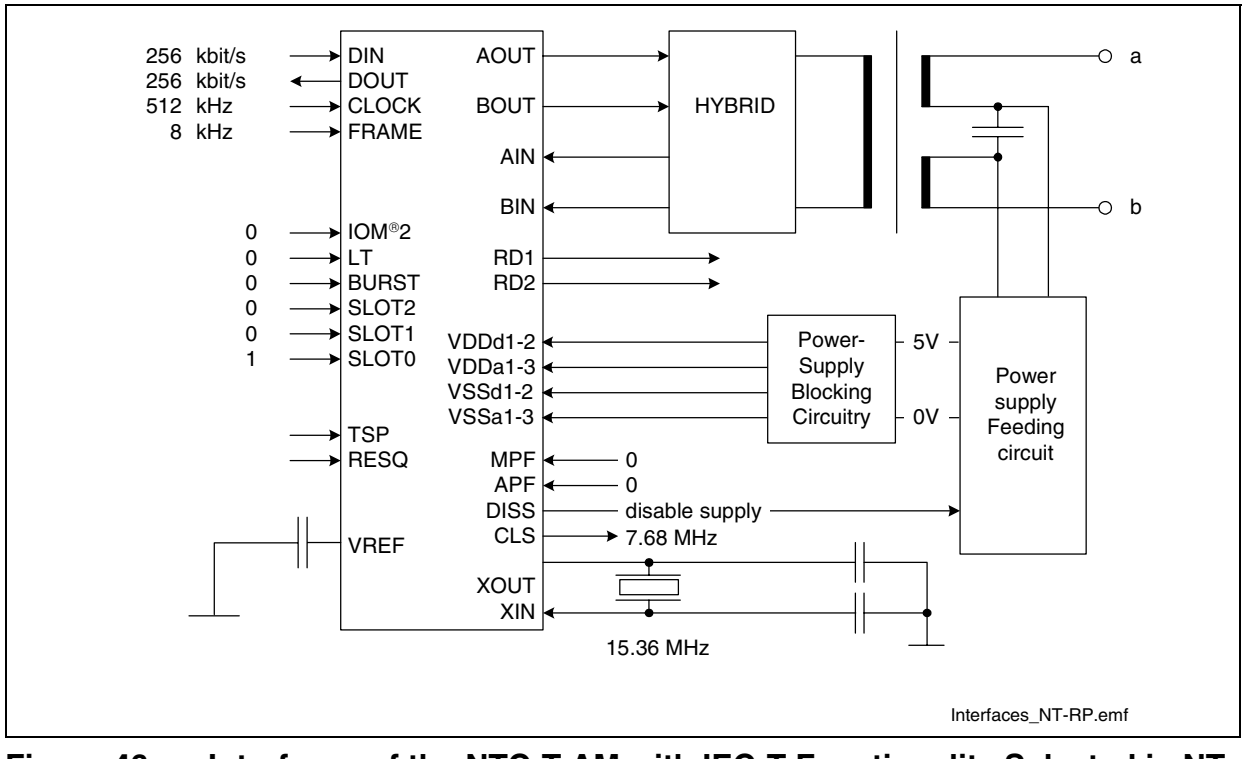


Figure 46 Interfaces of the NTC-T AM with IEC-T Functionality Selected in NT-RP Mode

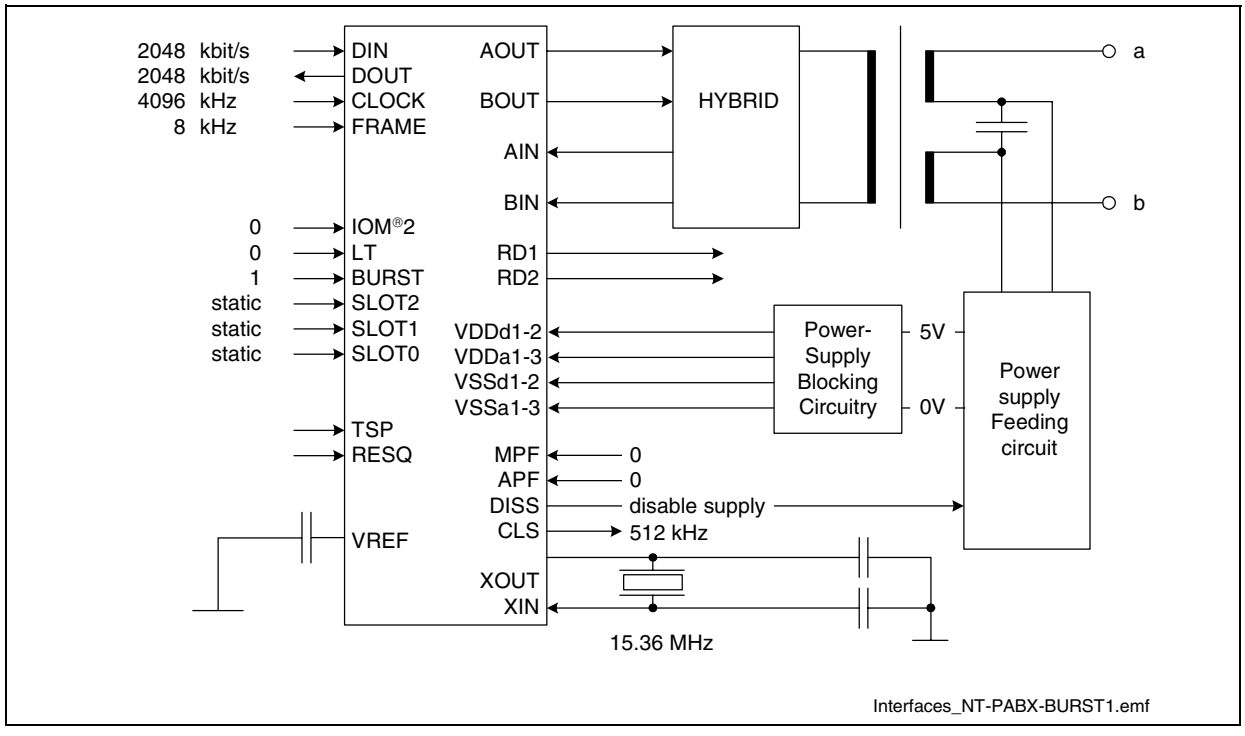


Figure 47 Interfaces of the NTC-T AM with IEC-T Functionality Selected in NT-PABX-BURST1 Mode

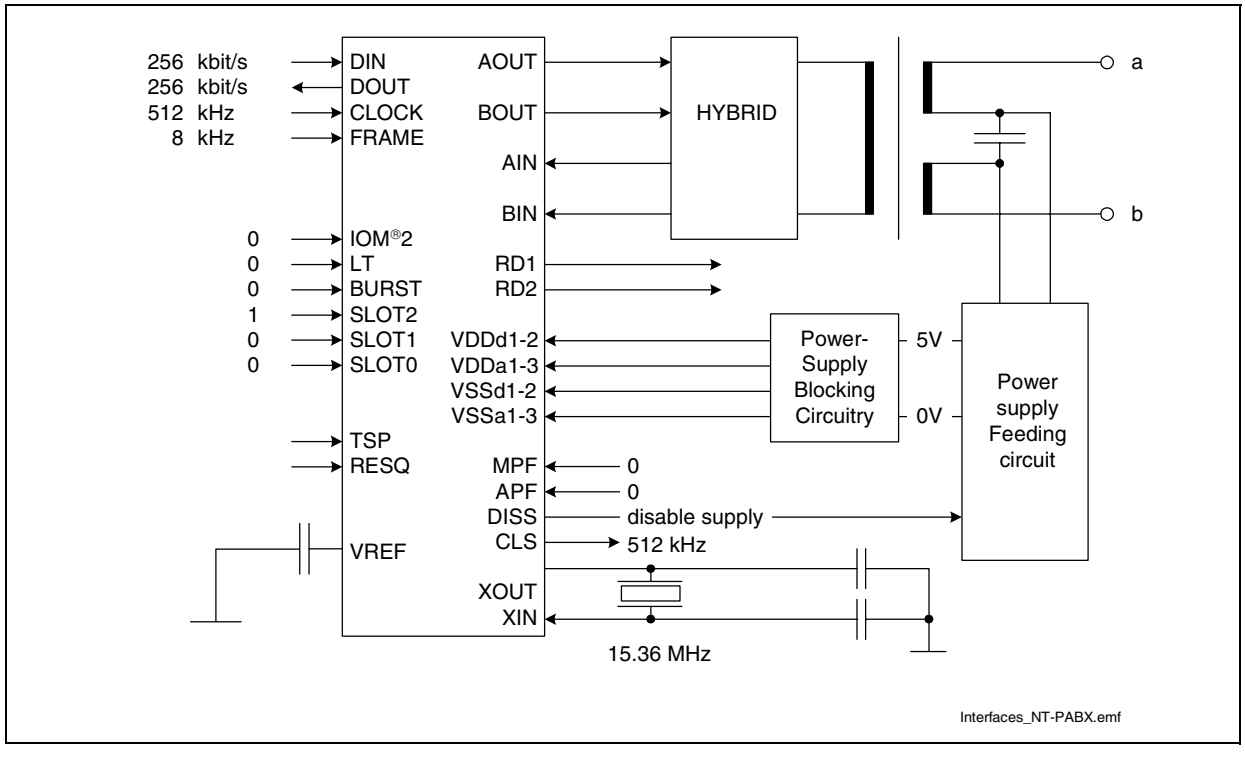


Figure 48 Interfaces of the NTC-T AM with IEC-T Functionality Selected in NT-PABX Mode

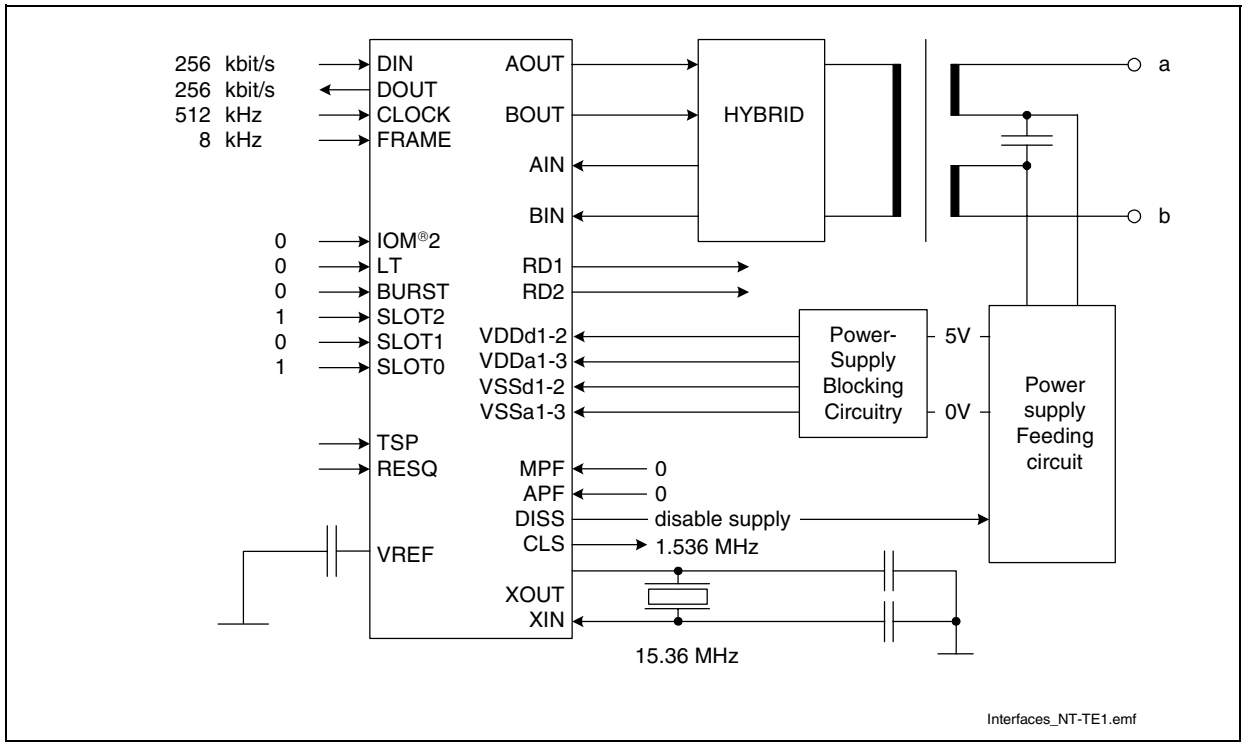


Figure 49 Interfaces of the NTC-T AM with IEC-T Functionality Selected in NT-TE1 Mode

5.6.2 Pin Definitions and Functions

Table 14 Pin Definitions and Functions of the NTC-T AM with IEC-T Functionality Selected

Pin	I/O	Symbol	Function
1		$V_{DDD}2$	**Supply Voltage, Digita** + 5 V +/- 5% I
2	O	IFDISC=0: reserved	Leave open
		IFDISC=1: TX	**120 kHz Clock Output** (from IEC-TD) The transmitted data are synchronized to this clock.
3	O	reserved	Leave open
4	O	reserved	Leave open
5	I	IFDISC=0: reserved	Tie to VSS_D
		IFDISC=1: CL 120	**120 kHz Clock Input** (to IEC-TA) The transmitted data are synchronized to this clock.

Table 14 Pin Definitions and Functions of the NTC-T AM with IEC-T Functionality Selected (cont'd)

Pin	I/O	Symbol	Function
6	I	MPF	**Monitor Power Feed** Serial data of power feed current (active high).
7	I	IFDISC	**Interface Disconnect** see **Chapter 1.4.1**
8	I	reserved	Tie to VSS_D
9	I/O	CLS	In all LT modes: Power Feed Off Signal from Power Controller Must be clamped to low, if not used. In NT/NT-RP modes: 7.68 MHz clock output synchronized to the line signal. In NT-PABX modes: 512 kHz clock output synchronized to the line signal. In NT-TE1 mode: 1.536 MHz clock synchronized to the line signal.
10	I	DIN	**IOM Data Input** synchronous to CLOCK
11	O	DOUT	**IOM Data Output** synchronous to CLOCK
12	I/O	CLOCK	**Double IOM Clock**
13	I/O	FRAME	**IOM Frame Signal**
14	I	DISPOR	**Disable Power-On Reset** see **Chapter 1.5.2**
15	I	reserved	Tie to VSS_D
16		VSS_D2	**Digital GND**
17	I	reserved	Tie to VSS_D
18	I	reserved	Tie to VSS_D
19	I	reserved	Tie to VSS_D
20	I	reserved	Tie to VSS_D.
21	I	reserved	Tie to VSS_D.
22	O	reserved	Leave open
23	O	RD1	**Relay Driver Pin 1** Control of a relay driver. Can be set via IOM MONITOR channel.
24	O	reserved	Leave open
25	O	reserved	Leave open

Table 14 Pin Definitions and Functions of the NTC-T AM with IEC-T Functionality Selected (cont'd)

Pin	I/O	Symbol	Function
26	I	APF	**Alarm Power Feed** Power feed overload with short response time. If not used, the APF-pin must be clamped to low (active high).
27	I		Tie to VSS_A
28	I		Tie to VSS_A
29		VSSA3	**Analog GND**
30	O		Leave open
31	O		Leave open
32		VDDA3	+ 5 V +/- 5% supply voltage, analog
33		VSSD1	**Digital GND**
34	I	SLOT0	**Selection of Different 256 kbit/s Modes/ Time Slot Selection** These pins program the NTC-T AM with IEC-T mode selected to the different 256kBit/s modes if BURST pin is low or assign the time slot in the BURST modes.
35	I	SLOT1	
36	I	SLOT2	
37	I	BURST	**Burst Mode** Programs the NTC-T AM with IEC-T mode selected to 256 kBit/s LT, LT-RP, NT, NT-PABX, NT-RP, or NT-TE mode (BURST pin low) or to 2048 kBit/s LT-BURST, NT-PABX-BURST mode (BURST pin high)
38	I	LT	**NT/LT Mode** Programs the NTC-T AM with IEC-T mode selected to LT mode (LT pin high) or NT mode (LT pin low).
39	I	TSP	**Test Single Pulses** NTC-T AM with IEC-T mode selected transmits single pulses of equal polarity spaced 1ms (active high). If not used, the TSP pin must be clamped to low.
40	I	reserved	Tie to VSS_D
41	I	TP0	**Factory Testpins** Tie to '011' for IEC-T functionality (see **Chapter 1.1**)
42	I	TP1	
43	I	TP2	
44		VDDD1	**Supply Voltage, Digital** + 5 V +/- 5%

Table 14 Pin Definitions and Functions of the NTC-T AM with IEC-T Functionality Selected (cont'd)

Pin	I/O	Symbol	Function
45		VDDD1	**Supply Voltage, Digital** + 5 V +/- 5%
46	O	BOUT	**Differential U-interface Output** Transmitted line signal from hybrid
47		VSSA1	**Analog GND**
48	O	AOUT	**Differential U-interface Output** Transmitted line signal from hybrid
49		VDDA1	**Supply Voltage, Analog** + 5 V +/- 5%
50		n.c.	Leave open
51	I/O	VREF	**Reference Voltage** Connect 100 nF vs. VSSA to buffer internally generated reference voltage.
52	O	XOUT	**Crystal OUT** Connect a 15.36 MHz crystal
53	I	XIN	**Crystal IN** Connect a 15.36 MHz crystal
54		VDDA2	**Supply Voltage, Analog** + 5 V +/- 5%
55	I	BIN	**Differential U-interface Input** Received line signal from hybrid
56	I	AIN	**Differential U-interface Input** Received line signal from hybrid
57		VSSA2	**Analog GND**
58	O	DISS	**Disable Supply** (active high)
59	O	reserved	Leave open
60	O	RD2	**Relay Driver Pin 2** Control of a relay driver. Can be set via IOM MONITOR channel.
61	I	RESQ	**Power On Reset** Power On Reset (active low) must be low at least 300 µs. The clock on CLOCK-pin has to be applied during reset in the LT modes and in NT-PABX mode. If not used, the RESQ-pin must be clamped to high.

Table 14 Pin Definitions and Functions of the NTC-T AM with IEC-T Functionality Selected (cont'd)

Pin	I/O	Symbol	Function
62	I	IOM2	**Enable IOM-2 Mode** Tie to VSS.
63	I	IFDISC=0: reserved	Tie to V_{SSD}
		IFDISC=1: LEVEL	**Awake Signal Detection** (input to IEC-TD) Detects the zero crossing of the differential input signal and is used to activate the IEC-TD.
64	I	IFDISC=0: reserved	Tie to V_{SSA}
		IFDISC=1: PDOW	**Power Down** (input to IEC-TA) Activates power-down mode, only oscillator and level detect are operating during power-down.

5.6.3 Mode Dependent Functions

Table 15 Mode Dependent Functions

Pin	LT	LT-BURST1	LT-RP	NT-RP	NT	NT-PABX	NT-PABX-BURST1	NT-TE1
LT BURST IOM®-2	1 0 0	1 1 0	1 0 0	0 0 0	0 0 0	0 0 0	0 1 0	0 0 0
SLOT0 SLOT1 SLOT2	0 0 0	Time-slot-select	1 0 0	1 0 0	0 0 0	0 0 1	Time-slot-select	1 0 1
DIN DOUT	256 kbit/s 256 kbit/s	2.048 Mbit/s 2.048 Mbit/s	256 kbit/s 256 kbit/s	256 kbit/s 256 kbit/s	256 kbit/s 256 kbit/s	256 kbit/s 256 kbit/s	2.048 Mbit/s 2.048 Mbit/s	256 kbit/s 256 kbit/s
CLOCK FRAME CLS	512 kHz in 8 kHz in Pfoff in	4096 kHz in 8 kHz in Pfoff in	512 kHz in 8 kHz in Pfoff in	512 kHz out 8 kHz 1:1 out 7.68 MHz out	512 kHz out 8 kHz 1:1 out 7.68 MHz out	512 kHz in 8 kHz in 512 kHz out	4096 kHz in 8 kHz in 512 MHz out	512 kHz out 8 kHz 1:1 out 1.536 MHz out
XIN XOUT	15.36 MHz nc	15.36 MHz nc	15.36 MHz nc	Xtal Xtal	Xtal Xtal	Xtal Xtal	Xtal Xtal	Xtal Xtal

5.6.4 Data and Clocks in LT, LT-RP Mode

DIN	input	Data input, 256 kbit/s continuous.
DOUT	output	Data output (open drain), 256 kbit/s continuous.
CLOCK	input	512 kHz Clock input. This clock provides the reference for DIN and DOUT
FRAME	input	Frame clock input, 8 kHz. This clock provides the reference for the identification of DIN and DOUT

CLS	input	Input from power supply. Indicates “Power feed off” (active high). If not used in this mode, the CLS-pin must be clamped to low.
XIN	input	Master clock input, 15.36 MHz. Synchronized to CLOCK.

5.6.5 Data and Clocks in LT-BURST1 Mode

DIN	input	Data input, 2048 kbit/s (bursts of 15.625 µs, 8 times per ms).
DOUT	output	Data output (open drain), 2048 kbit/s (bursts of 15.625 µs, 8 times per ms).
CLOCK	input	4096 kHz Clock input. This clock provides the reference for DIN and DOUT
FRAME	input	Frame clock input, 8 kHz. This clock provides the reference for the identification of DIN and DOUT.
SLOT2, SLOT1, SLOT0	input	Address straps - static inputs which define the time slots that carry information.
CLS	input	Input from power supply. Indicates “Power feed off” (active high). If not used in this mode, the CLS-pin must be clamped to low.
XIN	input	Master clock input, 15.36 MHz. Synchronized to CLOCK.

5.6.6 Data and Clocks in NT-PABX Mode

DIN	input	Data input, 256 kbit/s continuous.
DOUT	output	Data output (open drain), 256 kbit/s continuous.
CLOCK	input	512 kHz Clock input. This clock provides the reference for DIN and DOUT, synchronized to CLS.
FRAME	input	Frame clock input, 8 kHz. This clock provides the reference for the identification of DIN and DOUT, synchronized to CLS.
CLS	output	512 kHz clock, synchronized to received data on Uk0.
XIN, XOUT	input	15.36 MHz Xtal connections.

5.6.7 Data and Clocks in NT-PABX BURST1 Mode

DIN	input	Data input, 2048 kbit/s (bursts of 15.625 µs, 8 times per ms).
DOUT	output	Data output (open drain), 2048 kbit/s (bursts of 15.625 µs, 8 times per ms).
CLOCK	input	4096 kHz Clock input. This clock provides the reference for DIN and DOUT, synchronized to CLS.
FRAME	input	Frame clock input, 8 kHz. This clock provides the reference for the identification of DIN and DOUT, synchronized to CLS.
SLOT2, SLOT1, SLOT0	input	Address straps - static inputs which define the time slots that carry information.
CLS	output	512 kHz clock, synchronized to received data on Uk0.
XIN, XOUT	input	15.36 MHz Xtal connections.

5.6.8 Data and Clocks in NT, NT-RP, NT-TE1 Mode

DIN	input	Data input, 256 kbit/s continuous.
DOUT	output	Data output (open drain), 256 kbit/s continuous.
CLOCK	output	512 kHz Clock output. This clock provides the reference for DIN and DOUT, synchronized to CLS.
FRAME	output	Frame clock output, 8 kHz. This clock provides the reference for the identification of DIN and DOUT, synchronized to CLS.
CLS	output	NT, NT-RP: 7.68 MHz clock, synchronized to received data on Uk0. NT-TE1: 1.536 MHz, synchronized to received data on Uk0.
XIN, XOUT	input	15.36 MHz Xtal connections.

6 Part II 'IEC-T': Functional Description

6.1 Description of the Digital Module Interface

The NTC-T AM with IEC-T functionality selected is provided with an IOM® interface which operates in both a continuous and a burst mode in order to interface units which realize OSI layer 1 functions like the SBC (PEB 2080) and to layer 2 functions like the ICC (PEB 2070).

The NTC-T AM with IEC-T functionality selected is designed for the original IOM® interface (IOM®-1). An IOM®-2 interface is not functional. Therefore, the IOM®-2 pin must be clamped to '0'.

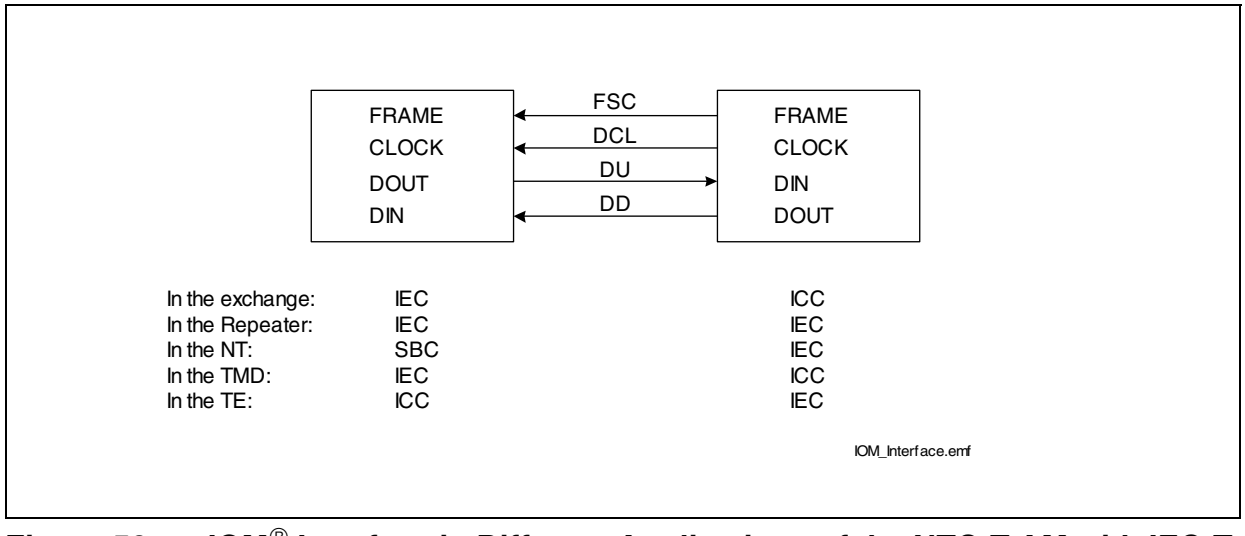


Figure 50 IOM® Interface in Different Applications of the NTC-T AM with IEC-T Functionality Selected

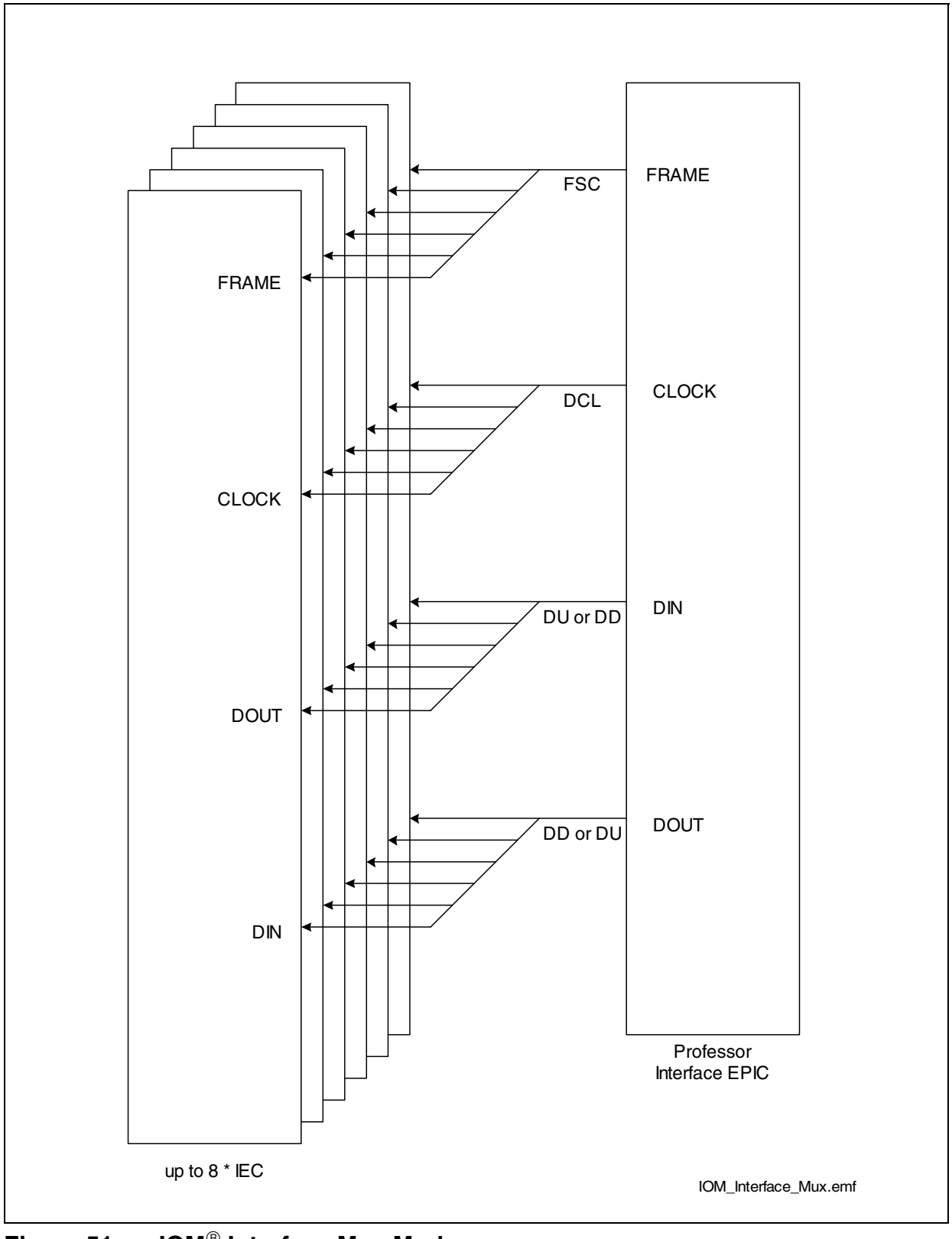


Figure 51 IOM® Interface Mux Mode

6.2 Frame Structure of the Module Interface

For each application, the ISDN data rate of 144 kbit/s (2B+D) is transmitted transparently via the modular interface. It is necessary to exchange control information for means of activation and deactivation of OSI layer 1 functions and switching of testloops. In some applications, access to maintenance information is additionally provided.

This information is transferred in a time multiplex procedure based on an 8 kHz frame structure (see **Figure 52**).

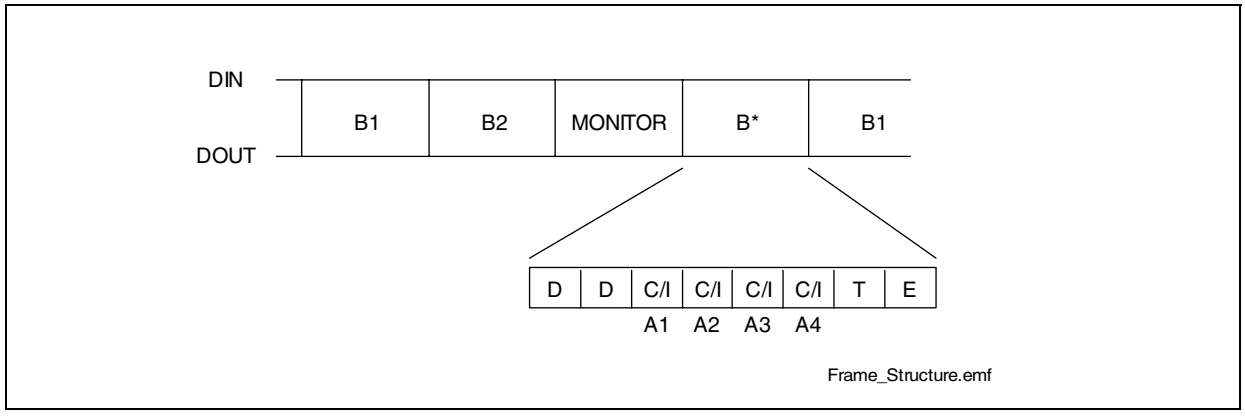


Figure 52 Frame Structure of the Digital Interface of the NTC-T AM with IEC-T Functionality Selected

Four octets are transmitted in each frame:

1st octet B1	B channel (64 kbit/s data) MSB first.
2nd octet B2	B channel (64 kbit/s data) MSB first.
3rd octet	MONITOR (8 bit monitor address for DIN, 8 bit monitor data with MSB first for DOUT. See **Chapter 6.7**).
4th octet B*	2 bit D channel 16 kbit/s data. 4 bit C/I channel (see **Chapter 6.7**). T channel for 1 kbit/s transparent data with IOM®-1. E extension bit for control of MONITOR channel and to hand over the maintenance bit of Uk0 (see section 8. "Maintenance Functions").

6.3 Serial I/O Data Format and Timing

6.3.1 Continuous Modes (256 kbit/s)

Nominal bit rate of data (DIN, DOUT):	256 kbit/s
Nominal frequency of CLOCK:	512 kHz
Nominal frequency of FRAME:	8 kHz
Mark to space ratio of FRAME:	1 : 1

Transitions of the data occur after even numbered rising edges of CLOCK. Even numbered rising edges of the clock are defined as the second rising edge following the rising edge of FRAME and every second rising edge thereafter.

The frame is identified by the rising edge of FRAME.

The data streams consist of 4 octets per frame. The input data (DIN) and the output data (DOUT) are synchronous and in phase (see **Figure 53**).

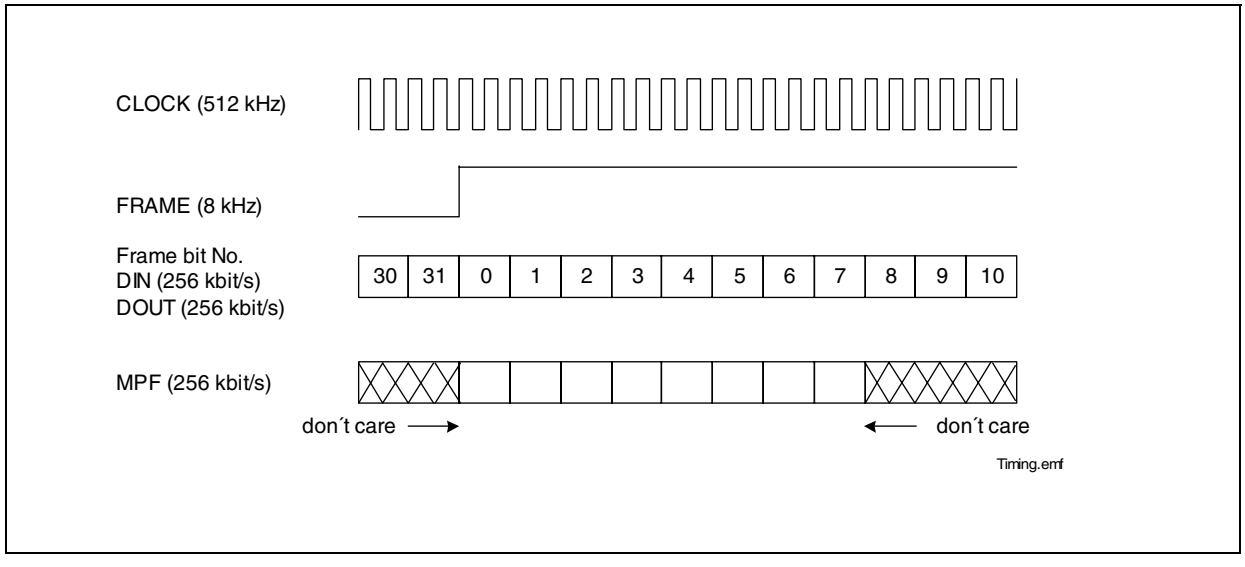


Figure 53 Timing of Data and Clocks at the 256 kbit/s Interface

6.3.2 IOM® Multiplexed Modes

In the multiplexed modes, the IOM® data of up to eight NTC-T AMs with IEC-T functionality selected are multiplexed. The data streams consist of bursts of 4 octets per frame. The bursts are allocated to consecutive time slots in a frame by the static inputs SLOT0, SLOT1, SLOT2. Outside of the allocated time slot, the NTC-T AM with IEC-T functionality selected must not read from DIN-pin. The DOUT-pin drives outside of the allocated timeslot a logical '1' (see also **Chapter 1.5.1**). **Table 16** indicates the allocations.

Table 16 Allocation of Time Slots in IOM®-1 Modes

Time Slot No.	SLOT0	SLOT1	SLOT2	Bit No.
0	0	0	0	0 ... 31
1	0	0	1	32 ... 63
2	0	2	0	64 ... 95
3	0	1	1	96 ... 127
4	1	0	0	128 ... 159
5	1	0	1	160 ... 191
6	1	1	0	192 ... 223
7	1	1	1	224 ... 255

6.3.2.1 IOM®-1 Burst Modes (2048 kbit/s)

Nominal bit rate of data bursts (DIN, DOUT): 2048 kbit/s

Nominal frequency of CLOCK: 4096 kHz

Nominal frequency of FRAME: 8 kHz

Nominal pulse width of FRAME: 244.14 ns

The frame clock FRAME is an active low strobe clock. Its nominal pulse width is half the length of a bit slot. The strobe identifies the second half of bit no. 251 in the frame. The low state of the strobe is detected with the rising edge of CLOCK.

The data of the input, DIN, is valid on the even numbered rising edge of CLOCK. Transitions of the data on DOUT occur after even numbered falling edges of CLOCK. The rising edge identified by the frame strobe is an even numbered rising edge of CLOCK. The following falling edge is an even numbered falling edge.

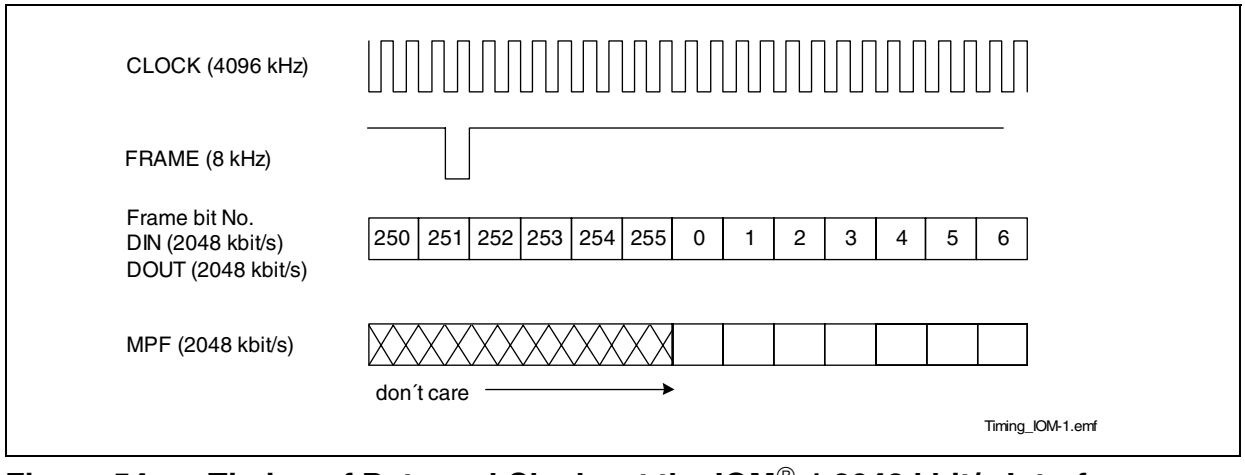


Figure 54 Timing of Data and Clocks at the IOM®-1 2048 kbit/s Interface

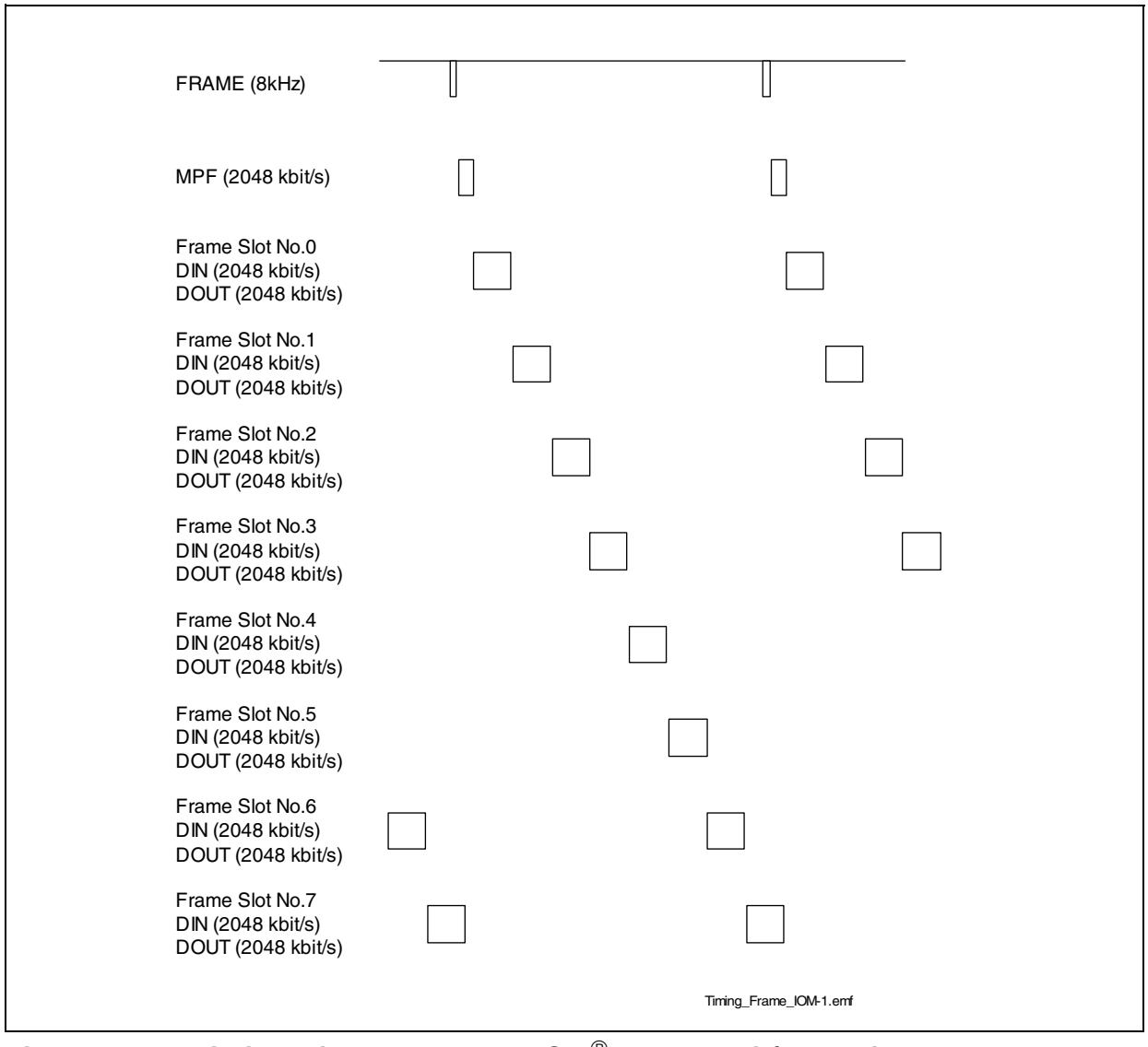


Figure 55 Timing of Frames at the IOM®-1 2048 kbit/s Interface

6.4 Synchronous and Deactivated States of the Module Interface

Depending on the application, two different cases have to be distinguished:

- In the repeater (NT-RP or LT-RP) modes and in the NT and TE modes, the module interface will be switched to power-down in the deactivated state. This means that the clocks are stopped. This is necessary to reduce power consumption in case of remote power supply. Depending on the direction of the clock signals, the NTC-T AM with IEC-T functionality selected in NT, NT-RP, and NT-TE modes serves as upstream unit while the NTC-T AM with IEC-T functionality selected in LT-RP mode serves as a downstream unit.
- In the exchange (LT or LT-BURST) modes and TMD (NT-PABX or NT-PABX-BURST) modes, the interface remains in the synchronous state. In this case, commands may also be given to the NTC-T AM with IEC-T functionality selected in the power-down state. A low power consumption is not very important in these applications.

6.4.1 Transition from Synchronous to Power-Down State

Deactivation of the IOM®- interface is controlled solely through the upstream unit. Such deactivation occurs whenever the corresponding Uk0 interface is deactivated.

The corresponding procedure is shown in the following figure. The upstream unit starts by transmitting the DR command in the C/I channel. After detecting the code DIU from the downstream unit, the upstream unit responds by transmitting the DID command during subsequent frames and stops the timing signals at the end of bit A4 of the 4^{th} frame. In the power-down state, both of the data lines are logically high and the timing signals CLOCK and FRAME are logically low. The voltage of the CLS clock may be high or low.

The downstream unit may be powered down after detection of code DID during two subsequent frames. When the IOM®-interface enters the power-down state, the downstream unit must also have entered its power-down state.

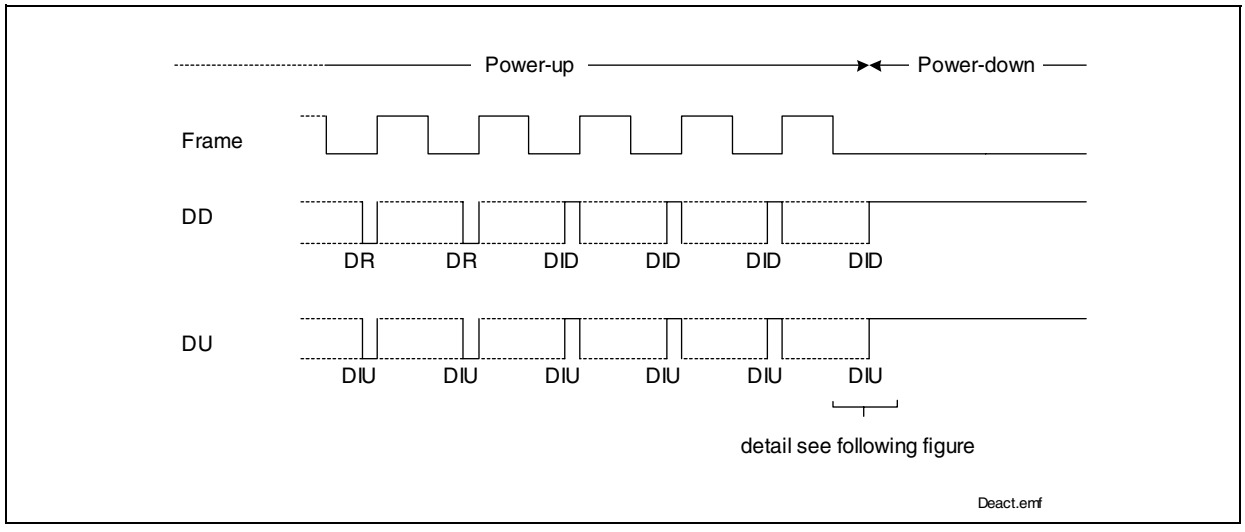


Figure 56 Deactivation of the IOM® Interface

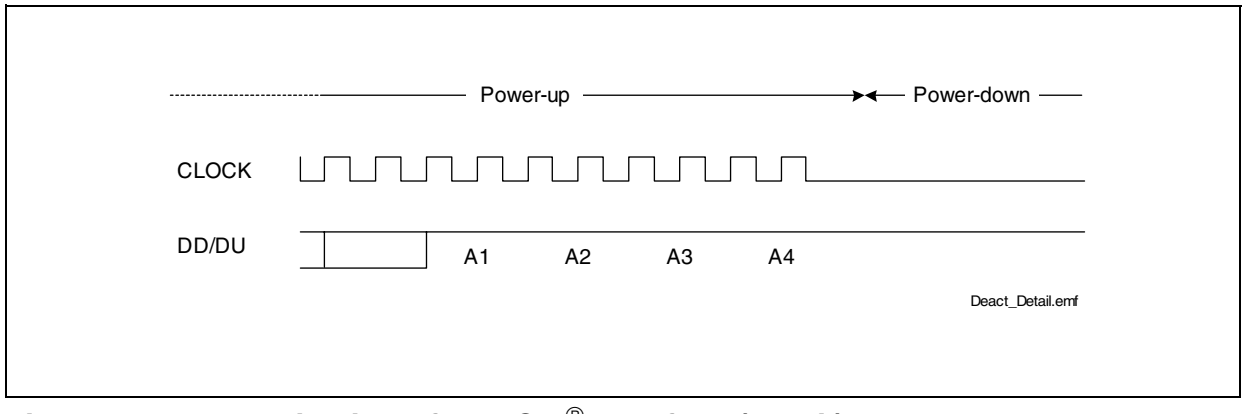


Figure 57 Deactivation of the IOM® Interface (Detail)

6.4.2 Wake-Up of the IOM® Interface Originated by the Downstream Unit

Transition from power-down to synchronous operation is done by the downstream unit by transmitting binary "O" on line DU.

The upstream unit responds by going into the power-up state and begins sending timing signals within less than 1 µs.

After the interface clocks have activated, the downstream unit may insert a valid code in the C/I channel. The continuous supply of timing signals by the upstream unit is ensured as long as the downstream unit sends no DIU code in the C/I channel. If timing signals are no longer required and activation isn't yet requested, the downstream unit may indicate this to the upstream unit by applying code DIU to the C/I channel or by transmitting continuous "1" on line DU. The upstream unit will respond by deactivating the timing signals.

The upstream unit will start monitoring line DU for binary "O" only after deactivation of timing signals.

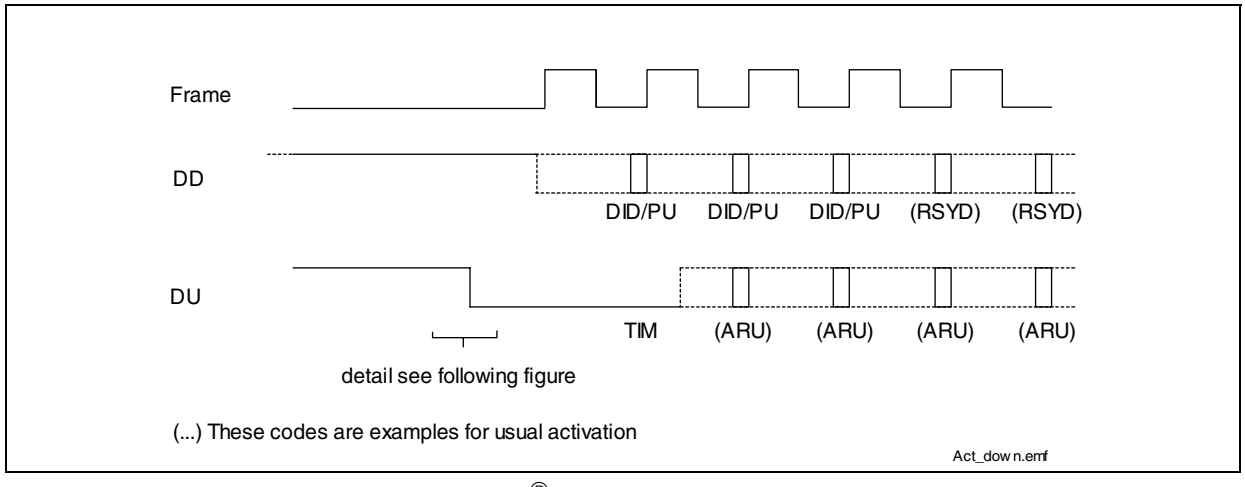


Figure 58 Activation of the IOM® Interface by the Downstream Unit

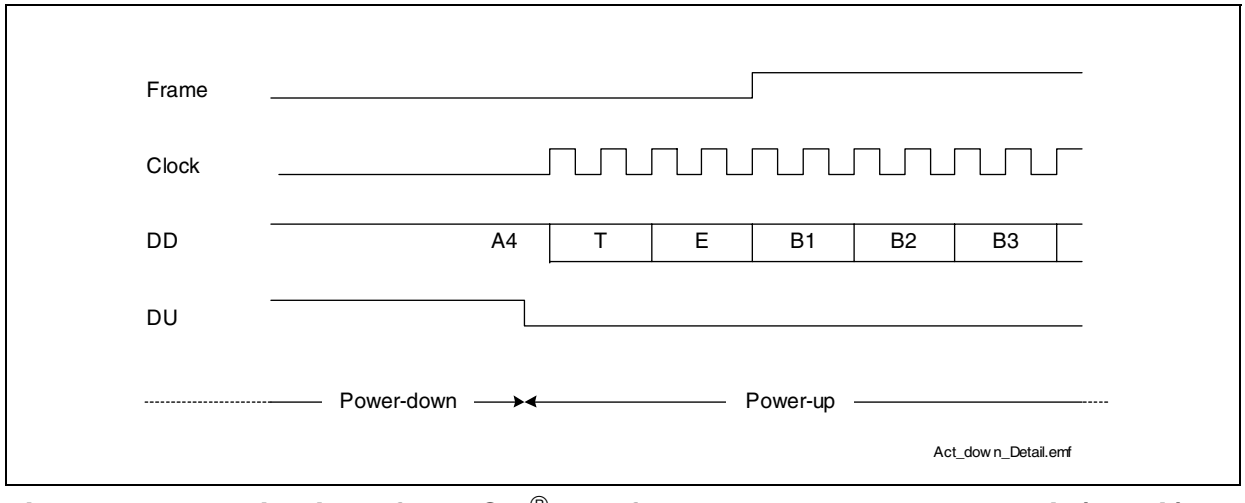


Figure 59 Activation of the IOM® Interface by the Downstream Unit (Detail)

6.4.3 Wake-Up of IOM® Interface Originated by the Upstream Unit

Wake-up of the IOM® interface from the power-down to the synchronous state can be initiated by the upstream unit simply by activation of the timing signals. Simultaneously, the upstream unit must apply the desired command onto the C/I channel.

The downstream unit may enter the power-up state immediately after the timing signals have been applied or after evaluating the received command code in two subsequent frames.

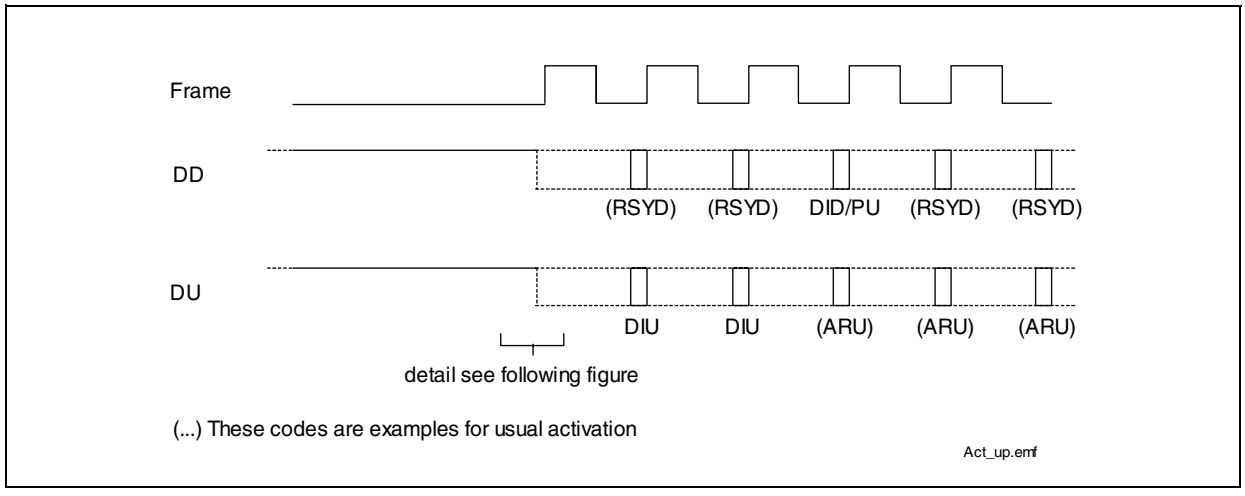


Figure 60 Activation of the IOM® Interface by the Upstream Unit

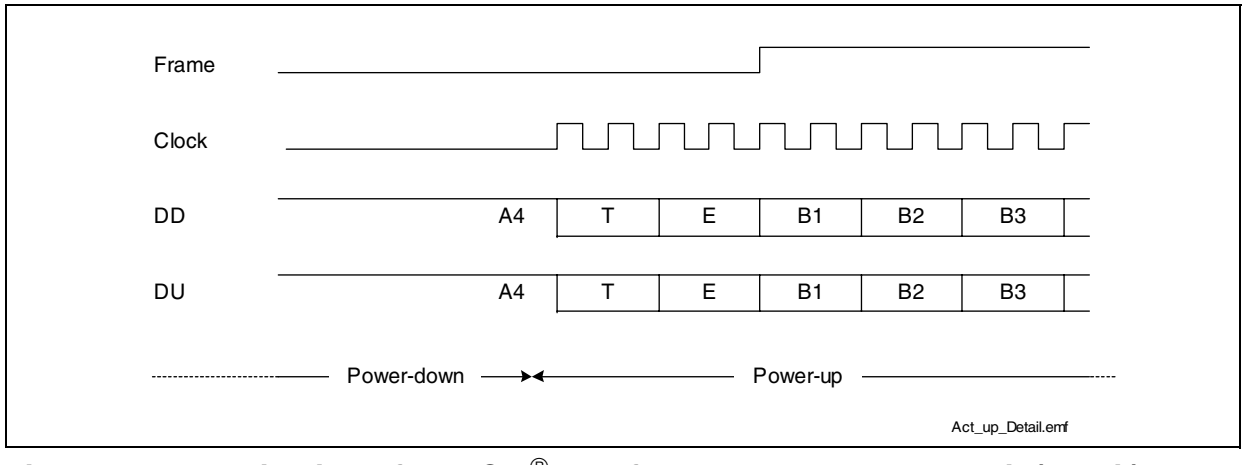


Figure 61 Activation of the IOM® Interface by the Upstream Unit (Detail)

6.5 Clock Generation

6.5.1 Master Clock

The master clock is the clock signal with the highest frequency in the system.

NT Modes:

The master clock is derived from a built in crystal oscillator in the NT operating modes. The crystal is connected to the pins XIN and XOUT. The maximum capacitive load at XIN and XOUT is 60 pF each.

Nominal frequency:	15.36 Mhz
Overall tolerance:	±100 ppm

We recommend using a crystal (serial resonance) which meets the following specification:

Nominal frequency:	15.36 Mhz
Overall tolerance:	±60 ppm
Load capacitance:	20 pF
Resonance resistance:	20 Ω
Shunt capacitance:	7 pF

LT Modes:

In the LT modes, the timing signal is derived from the system clock via an external phase locked loop. The master clock is fed to pin XIN.

Nominal frequency:	15.36 Mhz
Duty ratio:	0.4 ... 0.6
Rise and fall times:	< 10 ns
Max. Difference of phase deviations of Master clock and FSC:	±18 µs
Max. low freq. phase wander within 1 period:	±0.85 ps
Jitter (peak-to-peak):	see

In the deactivated state, while no data has to be recognized on the line, no particular jitter requirements have to be kept.

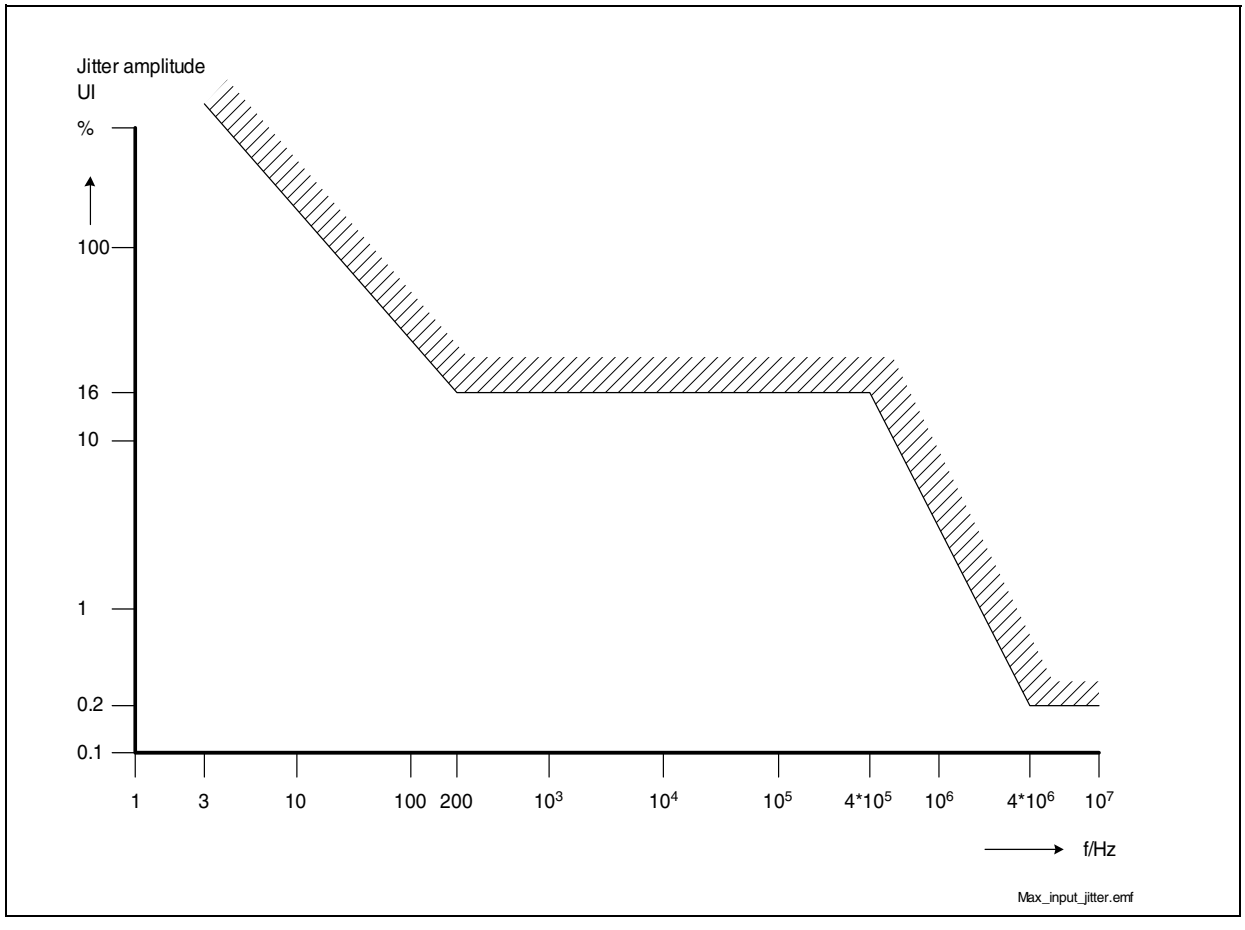


Figure 62 Maximum Sinusoidal Input Jitter of Master Clock 15.36 MHz

6.5.2 Suggestion for the Generation of the Master Clock in the Repeater

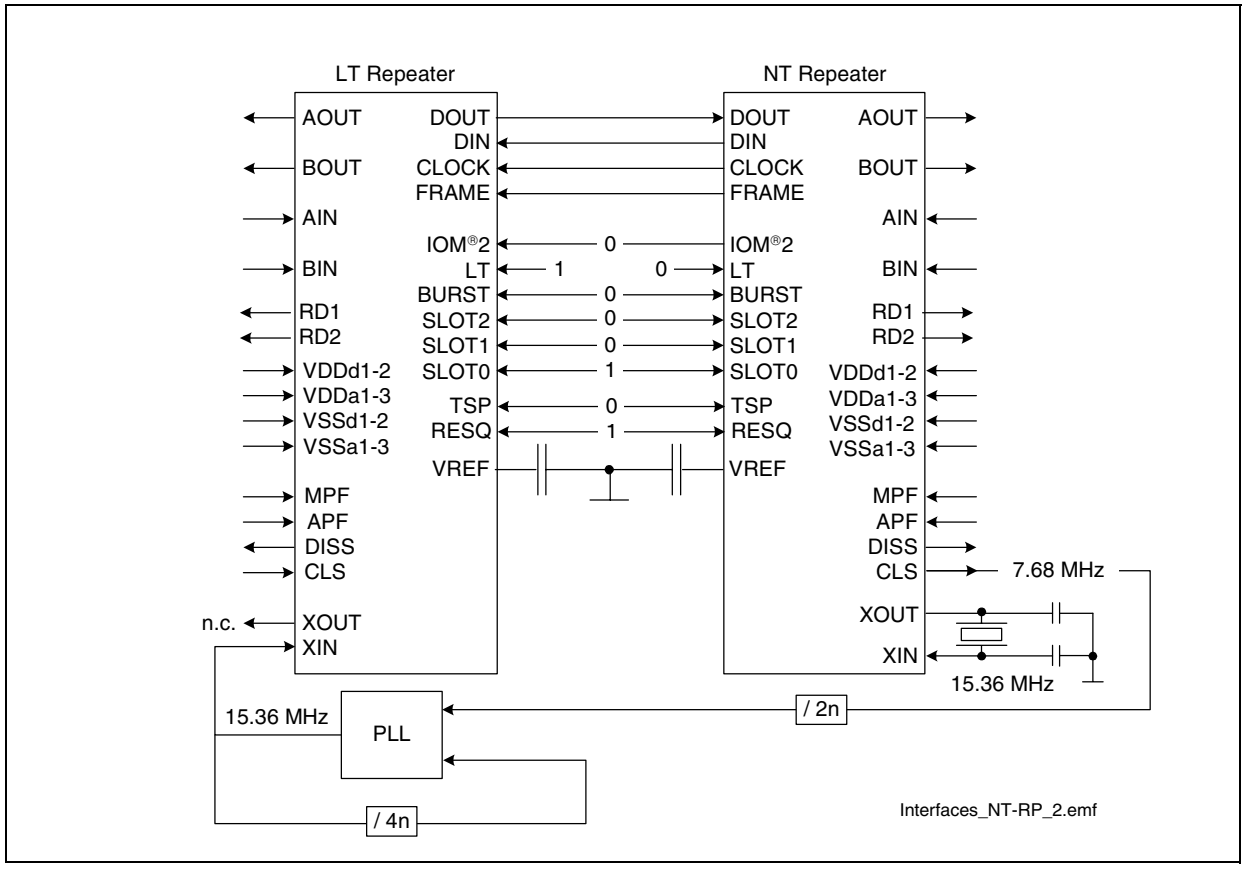


Figure 63 Interfaces of the NTC-T AM with IEC-T Functionality Selected in RP Mode

Note: The 7.68 MHz clock output on pin CLS is regulated in steps of 1/15.36MHz. Therefore, it should be diveded in order to avoid phase jumps at the input of the PLL.

6.5.3 Synchronous Half Master Clock

In the NT mode, the NTC-T AM with IEC-T functionality selected is able to provide the SBC with a 7.68 MHz clock which is synchronous to the received data. The clock is derived from a free running master clock (15.36 MHz) by dividing by 2 and additional adjustment steps. Adjustments are made by dividing by 1 or by 3. Up to 7 adjustment steps (in the synchronized state usually 0 or 1) will be performed within each 1 ms period with each step spaced 8.33 µs apart.

Nominal frequency:	7.68 MHz
Jitter (peak to peak):	≤ 260 ns

Minimum low phase duration: ≥ 26 ns

Minimum high phase duration: ≥ 26 ns

The jitter is to be measured with a highpass filter having a cutoff frequency of 50 Hz. (FTZ-Richtlinie 1 TR 230).

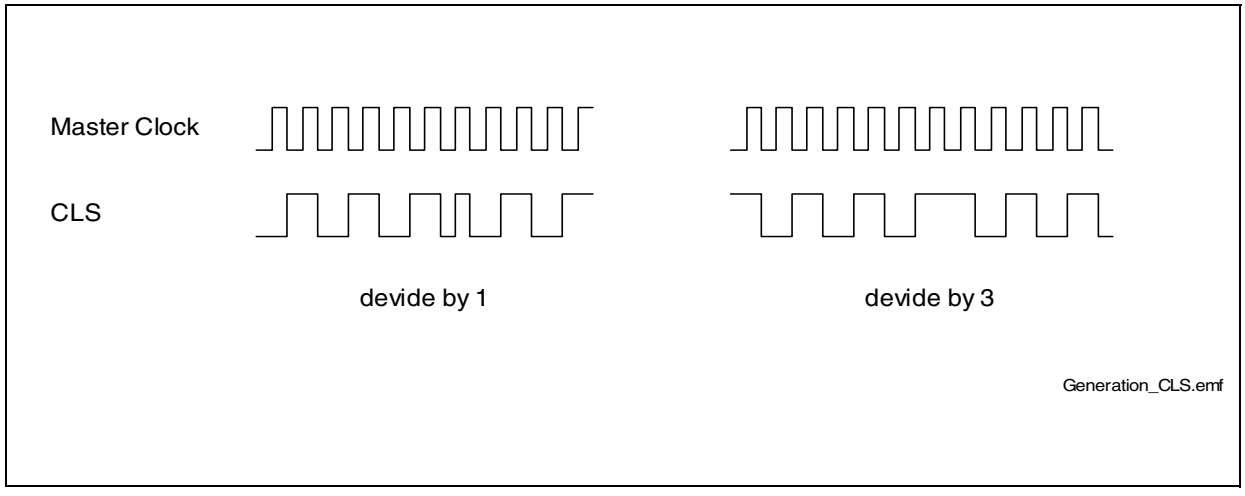


Figure 64 Generation of CLS from the Master Clock

6.6 Description of the Line Port

6.6.1 General

Please refer to **Chapter 3.3.1**.

6.6.2 Frame Structure of the Uk0-Interface

Please refer to **Chapter 3.3.2**.

Note: Transparent access to the M bit is possible via the IOM-1 interface.

6.6.3 Coding from Binary to Ternary Data

Please refer to **Chapter 3.3.3**.

6.6.4 Decoding from Ternary to Binary Data

Please refer to **Chapter 3.3.4**.

6.6.5 Monitoring of Code Violations

Please refer to **Chapter 3.3.5**.

6.6.6 Scrambler / Descrambler

Scrambler

The binary transmit data from the IOM®-1 interface is scrambled with a polynomial of 23 bits, before it is sent to the 4B3T coder.

– The scrambler polynomial in **LT mode** and **NT-TE mode with loop 3** is:

$$z^{-23} + z^{-5} + 1$$

– The scrambler polynomial in **NT mode without loop 3** is:

$$z^{-23} + z^{-18} + 1$$

Descrambler

The received data (after decoding from ternary to binary) is multiplied with a polynomial of 23 bits in order to recover the original data before it is forwarded to the IOM®-1 interface. The descrambler is self synchronized after 23 symbols.

– The descrambler polynomial in **LT mode without local loop** is:

$$z^{-23} + z^{-18} + 1$$

– The descrambler polynomial in **NT mode** or in **LT with local loop closed** is:

$$z^{-23} + z^{-5} + 1$$

6.6.7 Signal Elements used for Activation and Deactivation

Please refer to **Table 12**.

6.6.8 Analog Functions of the Line Port

Please refer to **Chapter 3.3.12**. The recommended hybrid is depicted in **Chapter 8.2.2**..

6.7 Maintenance Functions

6.7.1 Loops

For test of the line cards, several test loops are provided which can be controlled from the exchange. When a test loop is closed, all channels (B+B+D) are looped back and data from the other end of the line is ignored. There are no separate loops for single channels.

All test loops are transparent loops. During test loops, the line signal is still transmitted. Nevertheless, the NTC-T AM with IEC-T functionality selected in NT or NT-RP mode receives this signal and synchronizes on it. They cannot distinguish between line signals sent from LT or LT-RP during loop 1 or loop 4, and signals sent during normal operation.

6.7.1.1 Switching an Analog Loop in the NTC-T AM with IEC-T Functionality Selected

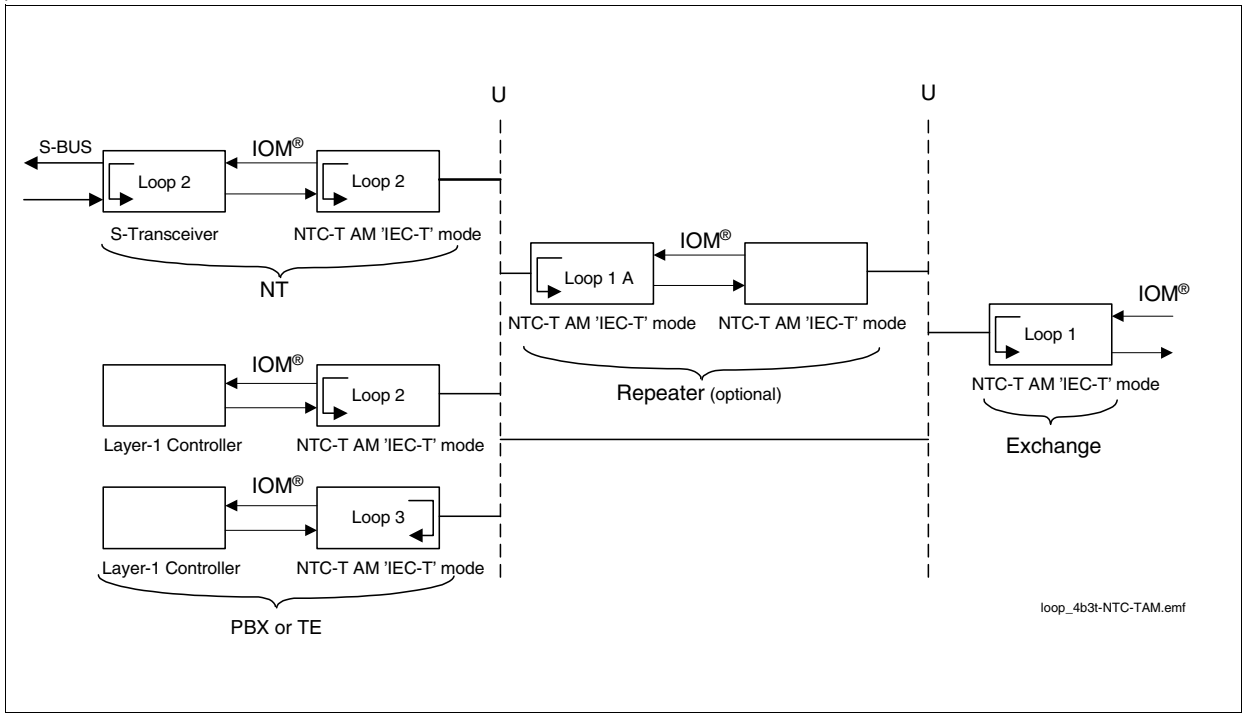


Figure 65 Test Loops Closed by the NTC-T AM with IEC-T Functionality Selected or under its Remote Control

Loop 1, loop 4, and loop 3 are closed in the NTC-T AM with IEC-T functionality selected as near to the Uk0 Interface as possible. Using internal switches, the signal from the line driver is fed back directly to the input. It is like a short-circuit between the pins AOUT and AIN as well as between BOUT and BIN. The input signal from the hybrid is ignored in this mode.

The analog loop mode is controlled via the IOM® C/I channel (see **Chapter 6.7**).

In an analog loop, the transmit path is set to LT mode and the receive path is set to the NT mode independently of the polarity of the LT pin.

6.7.1.2 Switching Loop 2 in the NTC-T AM with IEC-T Functionality Selected in NT-PABX and TE Modes

The loop 2 can be closed in the NTC-T AM with IEC-T functionality selected in NT-PABX, NT-PABX-BURST and NT-TE modes. With an internal switch, the user data on DOUT (B+B+D+T) is directly fed back into DIN. The control input (MONITOR and C/I channel) is still read from the IOM® interface. Although loop 2 is closed by command from the exchange, the NTC-T AM with IEC-T functionality selected can still be deactivated by RES and SSP C/I channel commands from the layer 2 device.

The loop 2 is under remote control from the exchange, identical to the loop 2 switched in the SBC.

In the NT-PABX and NT-TE modes, loop 2 can't be closed while the local loop 3 is activated. The activation of loop 3 leads to the deactivation of an activated loop 2.

6.7.1.3 Remote Control of Loop 4 and Loop 2 by the NTC-T AM with IEC-T Functionality Selected

These remote loops are controlled by the exchange via C/I channel of the NTC-T AM with IEC-T functionality selected (LT-mode). The command for closing loop 4 or loop 2 is transmitted from the exchange on the Uk0 interface in the 1 kbaud M channel (position 85 downstream in the Uk0 frame from LT to NT).

To command the NTC-T AM with IEC-T functionality selected in LT-repeater mode to close loop 4, the NTC-T AM with IEC-T functionality selected in NT-repeater mode has to find alternating plus and zero polarity within 8 subsequent frames in the M channel (+0+0+0+0...).

To command the SBC in the NT to close loop 2, the NTC-T AM with IEC-T functionality selected in the NT has to find continuous plus polarity within 8 subsequent frames in the M channel (+++++++++...). The same code has to be found by the NTC-T AM with IEC-T functionality selected in NT-PABX or NT-TE mode to close loop 2 itself.

Note: The NTC-T AM with IEC-T functionality selected in NT mode does not close loop2 itself.

To open closed loops, the NTC-T AM with IEC-T functionality selected in NT, NT-RP, NT-PABX, NT-TE mode has to find continuous zero polarity within 8 subsequent frames in the M channel (00000000...) or at deactivation. During normal transmission without loops, the M symbol is set to zero (or minus see **Chapter 6.7.3 "Transparent Maintenance Channel" on Page 109**).

The NT-RP, when detecting positive M symbols, does not close loop 2, but hands them over to LT-RP via the IOM® interface with a high in the E bit of 8 subsequent IOM® frames. Negative or zero M symbols cause 8 low E bits.

6.7.2 Monitoring of Code Violations

In the NT modes, a positive M symbol is transmitted upstream if any code error has been detected within a frame (position 25 upstream in the Uk0 frame from NT to LT).

The NTC-T AM with IEC-T functionality selected contains an error counter which counts Uk0 frames with at least one detected code violation. In the LT mode, additionally, the frames with a received positive M symbol are counted. The error counter can be read and simultaneously reset from a certain state of activation via the IOM® interface in all modes except the repeater modes. The counter is always stopped after reaching 255 which is the maximum value passed to the MONITOR channel.

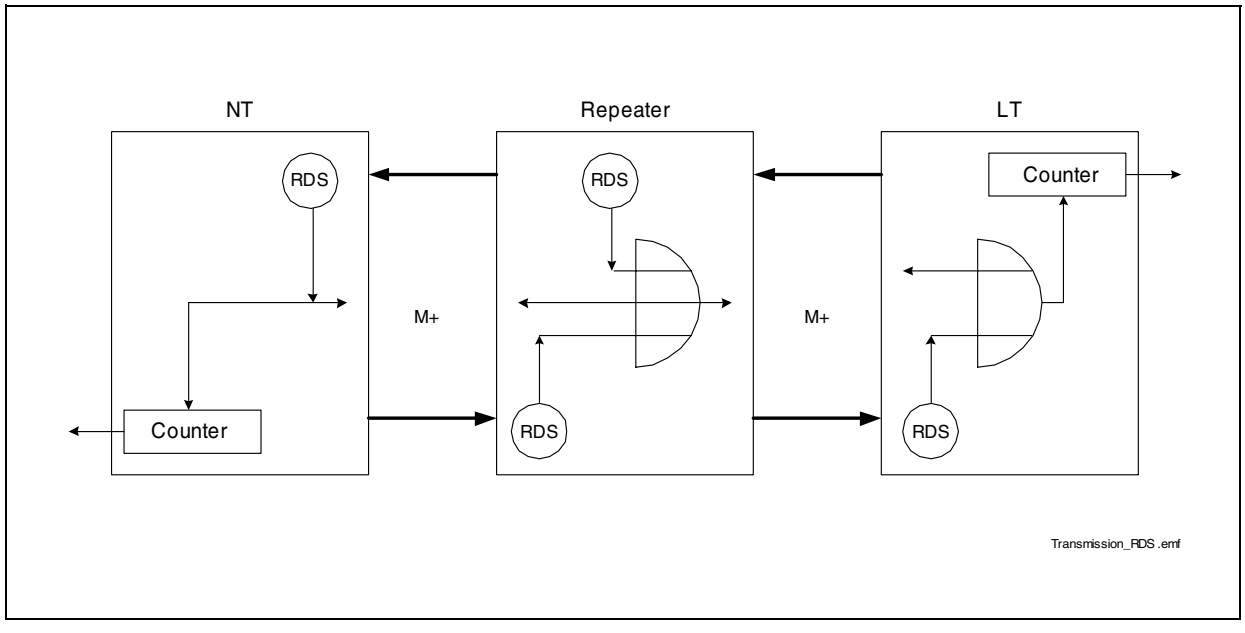


Figure 66 Transmission of Detected Frames with RSD Errors

The counter is automatically reset during deactivation of the Uk0 line. In the LT modes, it is enabled again to count code violations from the moment the RDS code is written into the IOM® C/I channel, indicating that the line is synchronized. In the NT modes, it is enabled again from the moment the AID code is written into the IOM® C/I channel.

Each counted frame with a detected code violation leads to 10 to 20 binary bit errors on average. So a bit error rate of 10^{-7} in both directions leads to about 2 detected frame errors within 1000 s in the LT (1 frame error detected in the NT and transmitted via M symbol).

In the LT-Repeater, detected code errors and received positive M symbols are given to the NT-RP via the IOM® interface with 8 times high in the E bits.

6.7.3 Transparent Maintenance Channel

A 1 kHz transparent channel is provided via the T bit on the IOM®-1 interface in both directions. Every 8th T bit is transmitted via the Uk0 M channel. A low in the T bit causes the M symbol to be set to minus polarity, overwriting any loop 4, loop 2 requests or RDS errors that might be transmitted via Uk0. A high in the T bit causes the M symbol to be set to zero or plus polarity depending on any loop 4, loop 2 requests or RDS errors. So it is obvious, that during activation it is essential to keep the T bit high to enable the NT (NT-RP) to recognize the loop status.

Each received M symbol with zero or plus polarity causes 8 consecutive T bits set to high. Each received M symbol with minus polarity causes 8 consecutive T bits set to low.

6.7.4 Interfaces to the Power Supply Circuit

The two-wire interface Uk0 provides power for the equipment repeater, network termination (NT) and possibly one telephone terminal in emergency conditions, when they must be fed by the exchange in the ISDN basic access. The NTC-T AM with IEC-T functionality selected has an interface to the power supply/feeding circuit of the exchange.

6.7.4.1 Scanning of Measured Values (MPF)

Using the common clocks 8 kHz and 512 or 4096 kHz, the feeding circuit transmits serially an octet via the MPF pin into the NTC-T AM with IEC-T functionality selected at the beginning of each IOM®-frame, which represents the measured loop feeding current.

As shown in fig. 5.4, fig. 5.5 and fig. 5.7 , the data at pin MPF are defined with equivalent timing and therefore are clocked in at the same instants as the data an DIN pin. The octet passed by the feeding circuit is identically placed as octet B1, the first of each frame both in 256 kHz and 2048 kHz modes.

If not used, the MPF pin may be clamped either to VDD or GND.

6.7.4.2 Supervision of Power Feed (LT Mode)

For supervision of power feed control, lines DISS, APF, CLS are used in static, level sensed operation mode.

In the C/I channel, a command LTD (LT disable, see **Chapter 7.3.3**) is defined to disable the power feed, setting the pin DISS on high. If the power feed unit is disabled either by the DISS pin or by an overload condition (short circuit), it indicates this to the NTC-T AM with IEC-T functionality selected, setting the CLS pin to high. The NTC-T AM with IEC-T functionality selected hands this information over to layer 2 units putting HI (high impedance, see **Chapter 7.3.4**) into the C/I channel (see **Figure 79**).

An overload condition is indicated by the power feed unit with a short response time, by means of a high on the APF pin (alarm power feed). In this condition, further adaption

of the echocanceller, equalizer and clock phase is immediately suspended until APF returns to low.

6.7.4.3 Supervision of Power Supply (NT Mode)

For supervision of the power supply, a high on the DISS pin is used to indicate the power down of the NT. In this case, the power supply may go to a state optimized for low power consumption in the devices.

6.7.5 Signaling of Measurement Results and Setting the RD Pins via MONITOR

A set/reset of the pins RD1 and RD2 or readout of the measurement results via the MONITOR-channel (third octet of each 8 kHz IOM® frame at DIN and DOUT) is possible in all modes except the repeater modes. Change RD1 arid RD2 or readout can be performed in both the power-up and power-down state of the NTC-T AM with IEC-T functionality selected, if the IOM interface is active.

A command contained in the MONITOR channel of DIN gives the address of the requested measurement value or identification. Each command is executed after appearing in one single frame (125 µs).

Only that value (8 bit) which has been addressed by the specific command will be output in the MONITOR channel of DOUT in the frame immediately following the command frame. In the MONITOR channel, MSB is always sent first and LSB last.

If no relay driver pin is to be set or if no measurement value is requested, the MONITOR channel (on DIN) must be held in a NOP condition (No OPeration).

Table 17 Coding of MONITOR Commands

NOP	00_H, $F0_H$ ... $F6_H$ $F8_H$ ... FF_H	Inactive, output FF_H
Identification	80_H	NTC-T AM with IEC-T functionality selected responds to 80_H, distinguishing NTC-T AM with IEC-T functionality selected from other layer 1 devices
RDS	EF_H	Read and reset RDS counter
MPF	EE_H	Read power feed current
Coefficients	04_H ... 63_H	Read coefficients of echo canceller
Relay driver RD1, RD2	74_H 75_H 76_H 77_H	Set RD1, reset RD2 Reset RD1, set RD2 Set RD1, set RD2 Reset RD1, reset RD2 (output always FF_H)

6.7.5.1 Access to MONITOR Channel in the IOM®-1 Mode

Detection of a valid command in the MONITOR channel will be acknowledged by setting the E Bit to 0 in the frame containing the response. The E Bit will be reset to 1 for each successive frame until a new valid command is detected.

If no relay driver pin is to be set or if no measurement value is requested, the MONITOR channel (on DIN) must be held in a NOP condition. Then the NTC-T AM with IEC-T functionality selected keeps the E Bit and the MONITOR channel at binary 1.

6.7.6 Readout Format of Echocanceller Coefficients

The NTC-T AM with IEC-T functionality selected contains an adaptive FIR filter with 48 coefficients. This filter emulates the line characteristics in order to cancel the echoed data from the received signal and to regain the data from the far end. Because these coefficients characterize the line, being a time discrete pulse response, it is of great interest to read them out of the NTC-T AM with IEC-T functionality selected and evaluate them to localize possible faults in the two wire loop.

The 16 most significant bits of the echocanceller coefficients can be read out via the MONITOR channel, addressing the high byte and the low byte differently. To reduce internal circuitry, these coefficients have a rather complicated format.

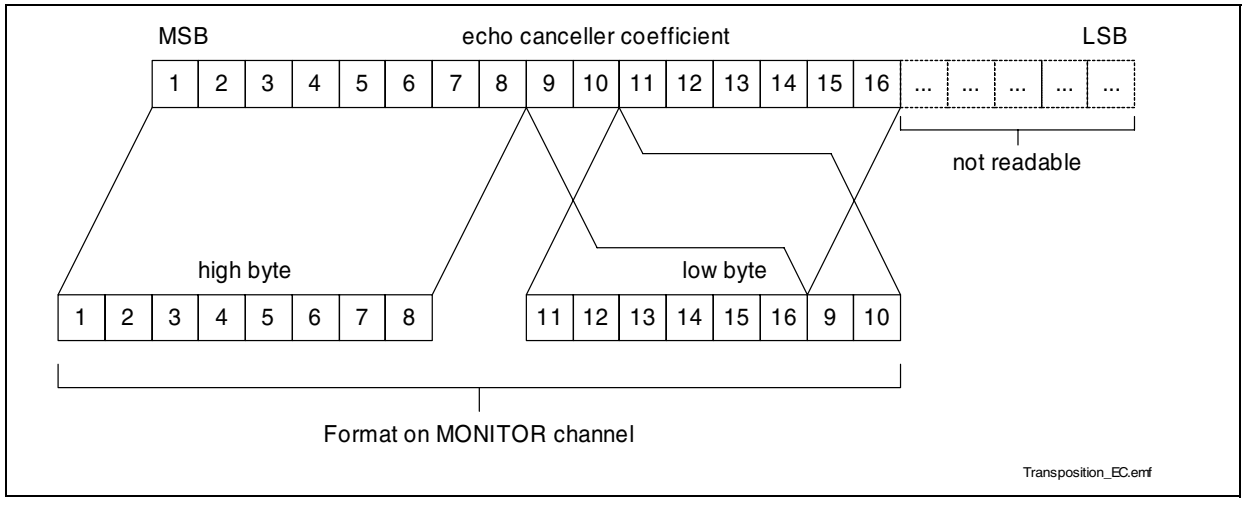


Figure 67 Transposition of EC Coefficient to MONITOR Channel

The low byte of a coefficient is to be accessed with an even numbered address in the MONITOR channel, the high byte with an odd numbered address. The coefficient to cancel the first echo is therefore accessible under addresses 04_H and 05_H; the last coefficient is found in addresses 62_H and 63_H.

To avoid a carry from low to high, caused by continuous adaption between the readouts of the low and the high byte, all coefficients are frozen for 125 µs, while one coefficient byte is read. If each coefficient is read in two subsequent IOM® frames, no carry overflow will occur and both bytes will fit together.

7 Part II 'IEC-T': Operational Description

7.1 Control Procedures

A "Call-by-Call" activation or deactivation of the transmission link is provided for ISDN basic access. In a deactivated state, the line and the terminal equipment (if it is not a remote power fed device) are powered down. The entire transmission link, consisting of one or more individual lines, has to be activated to enable the connection between terminal equipment (TE) and exchange (LT).

The activation procedure is always initiated by one of the two end points and is handled between them. The deactivation procedure can be initiated only by the exchange.

For (de-)activation procedures, no difference is made between LT, LT-BURST modes and between NT-PABX, NT-PABX-BURST, NT-TE modes.

Seven states of activation of transmission lines can be distinguished.

1.) Activation of the link is initiated by one of the two ends

1.1) Line awake: Each individual line is being awoken, but is not yet synchronized, data transmission is not yet possible.

1.2) Synchronization downstream: synchronization is always done downstream first, the whole line has to synchronize on the exchange.

1.3) Synchronization upstream: Because the delay differs from line to line, bit synchronization is necessary in the LT.

1.4) Synchronized: All layer 1 units of the link are told by the exchange that synchronization has been finished.

2) Transparent: In the activated state, the user data is transmitted from exchange to TE and vice versa.

3) Deactivation is done in two steps on each individual line separately.

3.5) Deactivation request downstream

3.6) Deactivation acknowledge upstream

The transmission link is totally deactivated thereafter.

To save time, each section of line does not have to wait for the transition of the entire line before it is able to proceed to the next state. Therefore the individual line sections may be at different states of activation.

To control the procedures, some control information has to be transmitted over the lines (Uk0 interface, S-bus). Therefore, special signal elements on the Uk0 interface have been specified. On the IOM® interface, the 8 * 4 kbit/s C/I channel (bit 27-30) is provided to exchange the necessary control information.

The IOM® interfaces and the UK0 interfaces are defined to prohibit states which cannot be left with normal commands and infos. Deactivation of the line leads all devices to defined states. Nevertheless, it is recommended to implement a power-on reset (at pin RESQ of NTC-T AM with IEC-T functionality selected) to start in a defined manner, and to shorten the first deactivation and activation.

The usage of the two input pins, RESQ and TSP, has the same effect as inputs RES and SSP in the C/I channel with one exception: If RESQ pin is low, DISS pin is set to high. If the reset is given only in the C/I channel, DISS pin is set to low. They always overwrite the IOM® C/I channel input.

For instance, the PEB 2080 (SBC) sends an EI code in the C/I channel, if RESET and TM2 pins of the SBC are set. The NTC-T AM with IEC-T functionality selected might interpret the EI code as the TEST command, but the SBC and NTC-T AM with IEC-T functionality selected reset pins (active low) are connected together in the NT. Thus, the NTC-T AM with IEC-T functionality selected ignores the EI code performing the reset request.

7.2 Activation and Deactivation of Uk0 Transmission Lines

On Uk0, the exchange of control information is partially state oriented. Some signal elements are given as long as no other information has to be transferred, other signal elements have distinct durations.

7.2.1 Awake Protocol

To awake the Uk0 interface and the Idle modules, an awake and an acknowledge signal have been defined.

Procedure for awaking NTC-T AM with IEC-T functionality selected

After sending the awake signal, the awaking device waits for the acknowledge. After 12 ms in the LT mode or 6 ms in the NT mode, the awake signal is repeated, if no acknowledge has been recognized.

If an acknowledge signal has been recognized, the NTC-T AM with IEC-T functionality selected waits for its possible repetition (in case of previous coincidence of two awake signals). If no repetition was detected, the NTC-T AM with IEC-T functionality selected starts transmitting INFO U2 in the LT mode, INFO U2A in the LT-RP mode and INFO U1A in NT modes with a delay of 7 ms in the LT mode or 13 ms in the NT mode.

If such a repetition is detected, the NTC-T AM with IEC-T functionality selected interprets it as an awake signal and the NTC-T AM with IEC-T functionality selected behaves like a device awoken by the far end.

Procedure in the NTC-T AM with IEC-T functionality selected to be awoken

If a deactivated device detects an awake signal on Uk0, an acknowledge signal is sent out. After that, the NTC-T AM with IEC-T functionality selected waits for a possible repetition of the awake signal (in case the acknowledge hasn't been recognized). If no repetition is found, the awoken NTC-T AM with IEC-T functionality selected starts sending INFO U2 in the LT mode, INFO U2A In the LT-RP mode and INFO U1A In the NT modes after 7 ms in the LT mode or 13 ms in the NT modes from detecting the awake signal. If a repeated awake signal is found, the procedure in the awoken NTC-T AM with IEC-T functionality selected starts again.

Please refer to **Figure 15** and **Figure 16**.

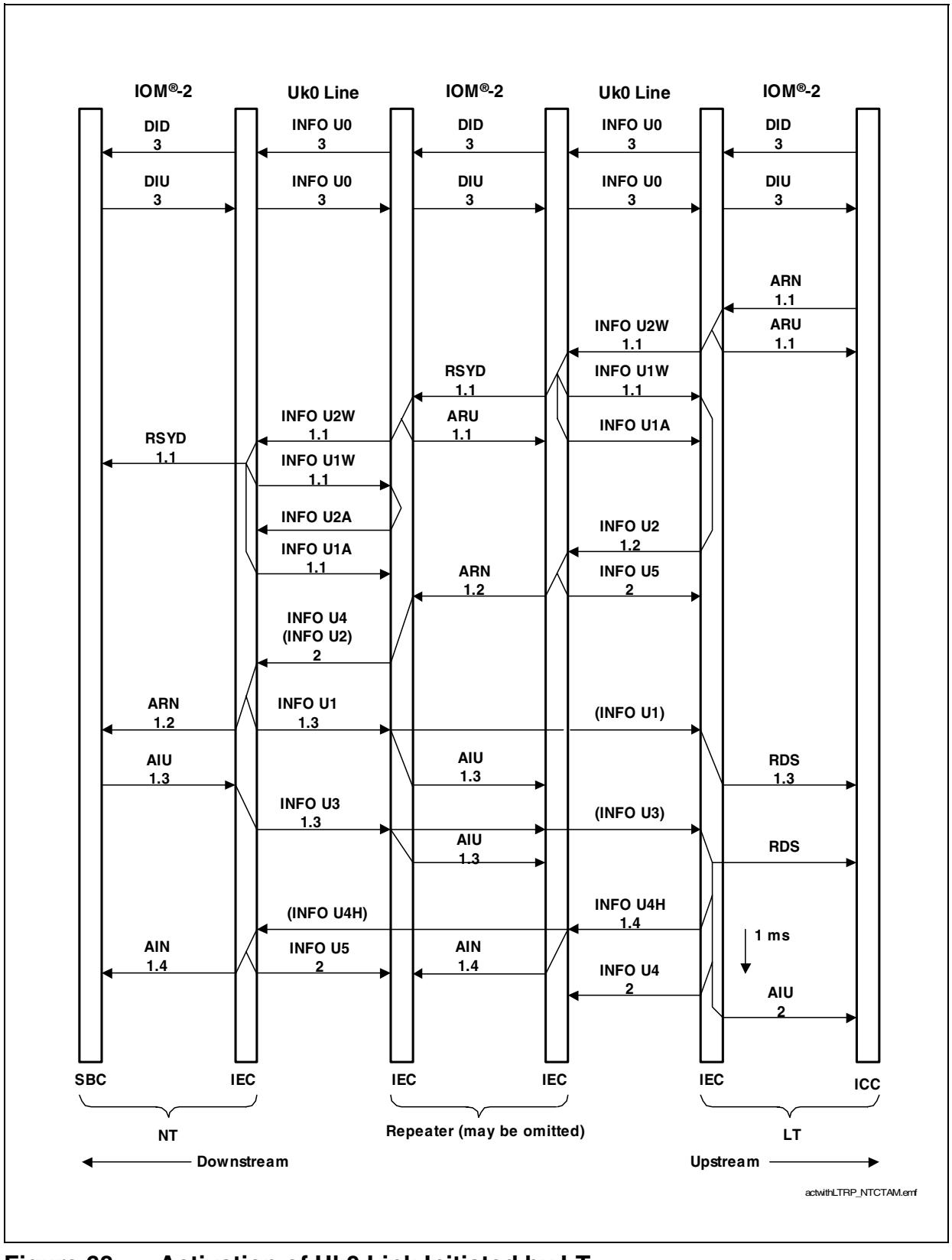


Figure 68 Activation of Uk0 Link Initiated by LT

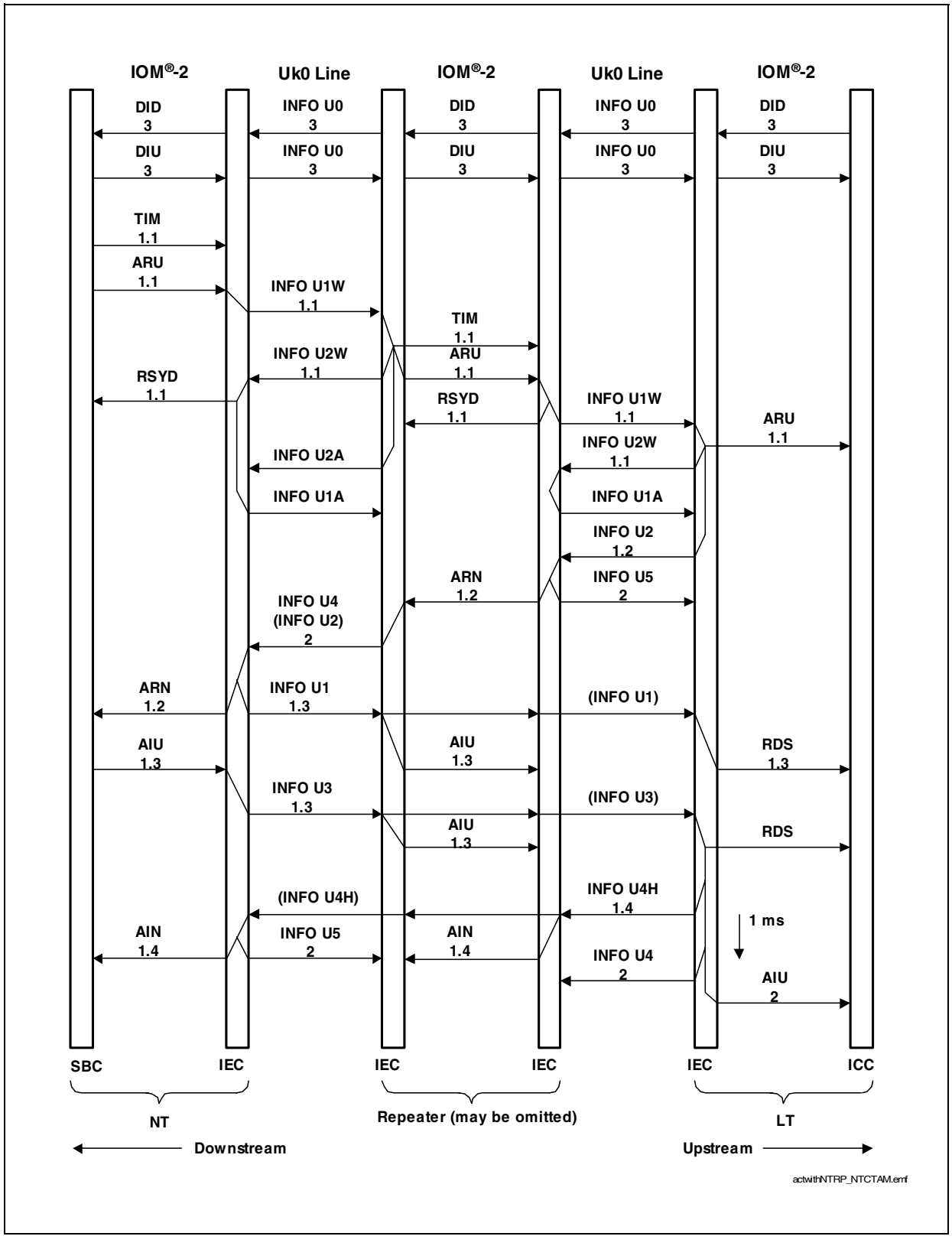


Figure 69 Activation of Uk0 Link Initiated by NT

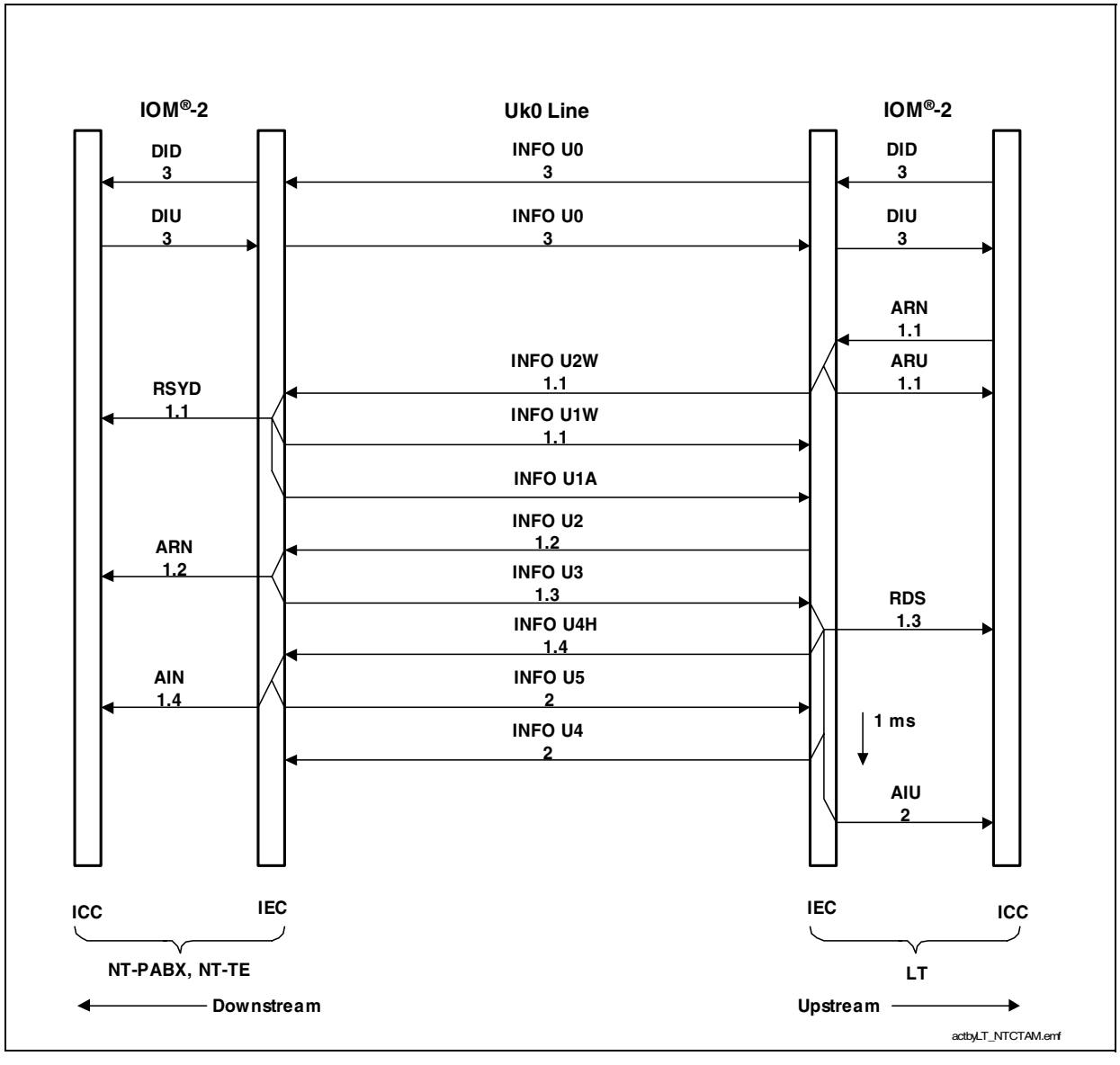


Figure 70 Activation of Uk0 Link with NT-PABX or TE Initiated by LT

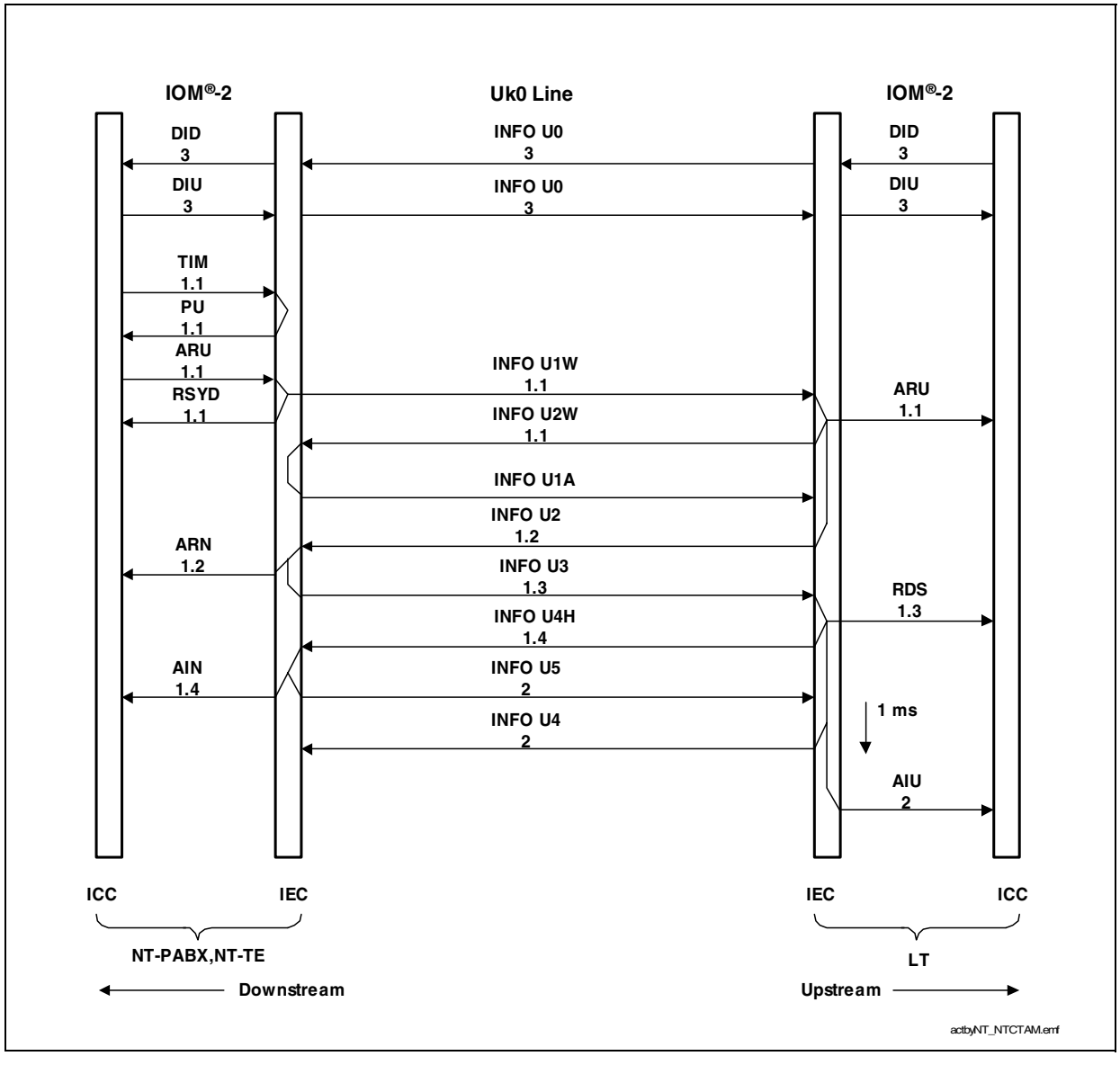


Figure 71 Activation of Uk0 Link with NT-PABX or TE Initiated by NT

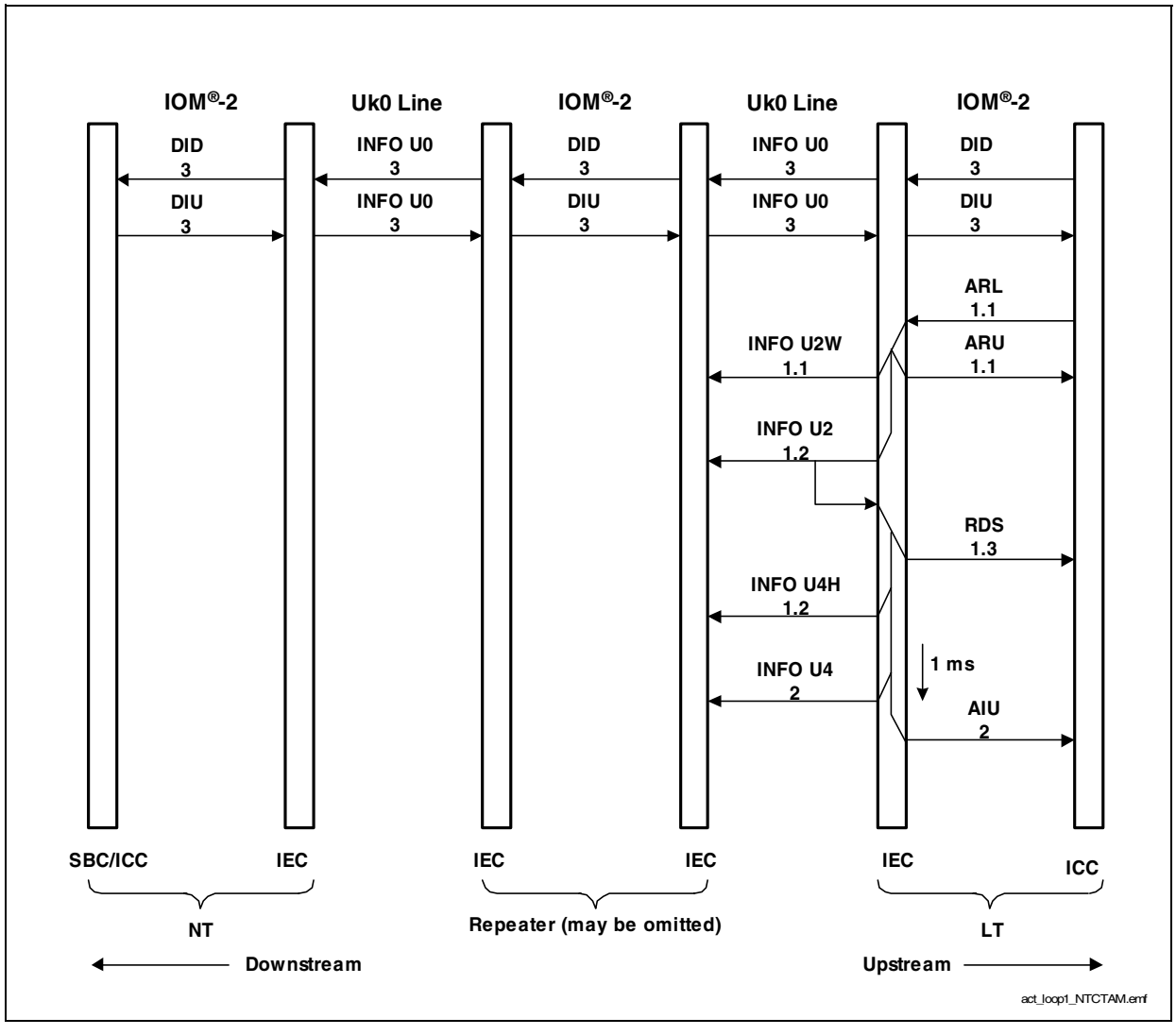


Figure 72 Activation of Loop 1

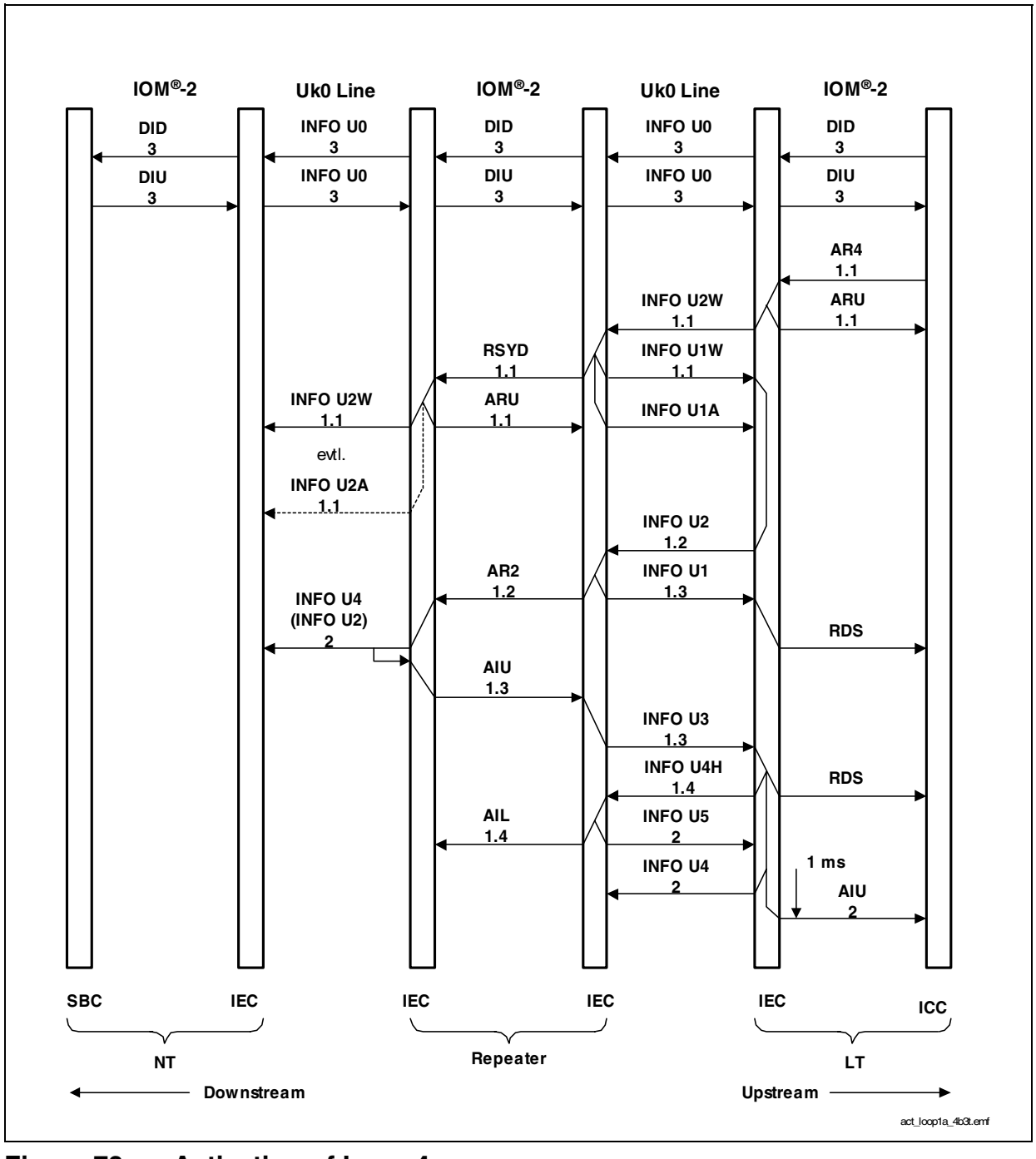


Figure 73 Activation of Loop 4

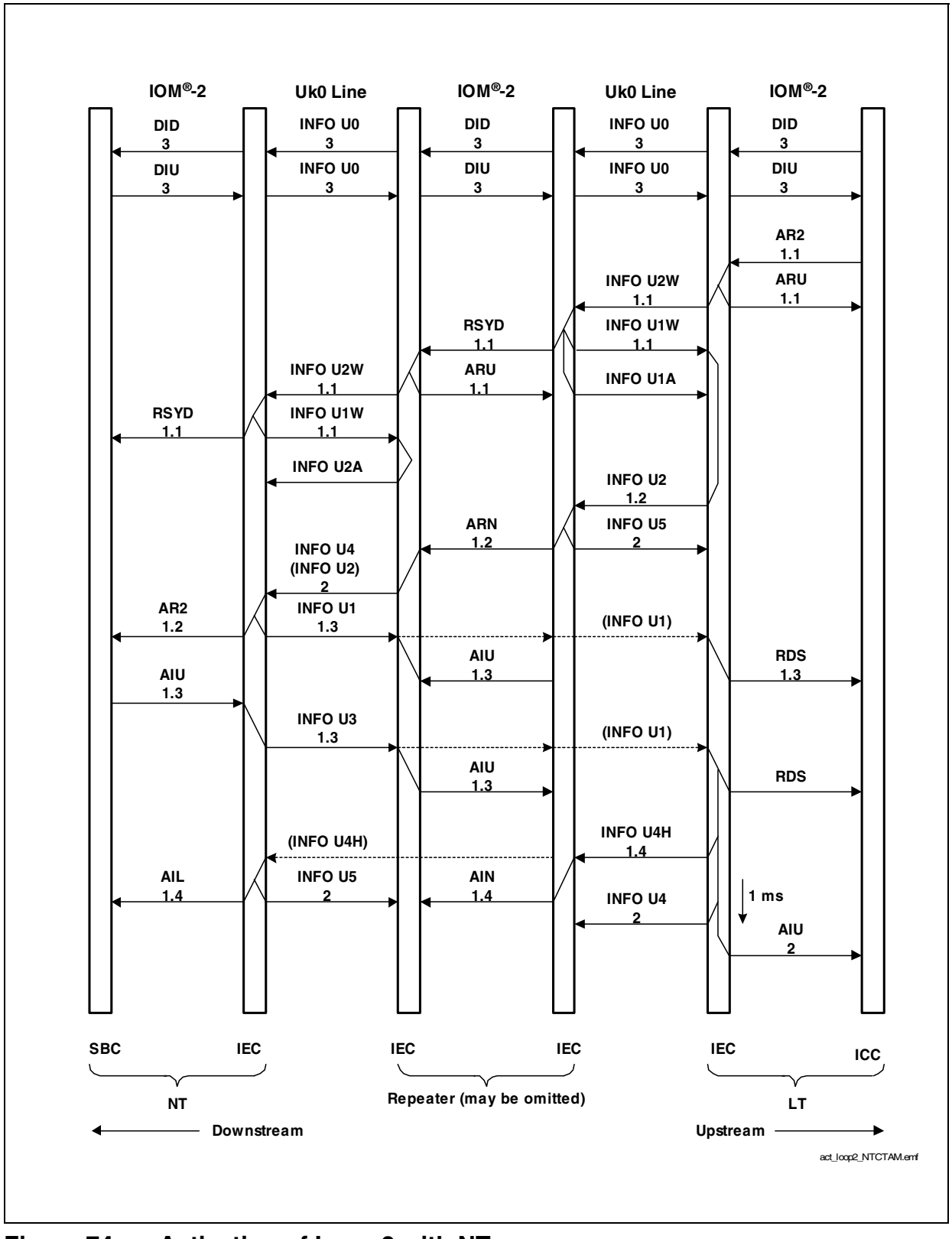


Figure 74 Activation of Loop 2 with NT

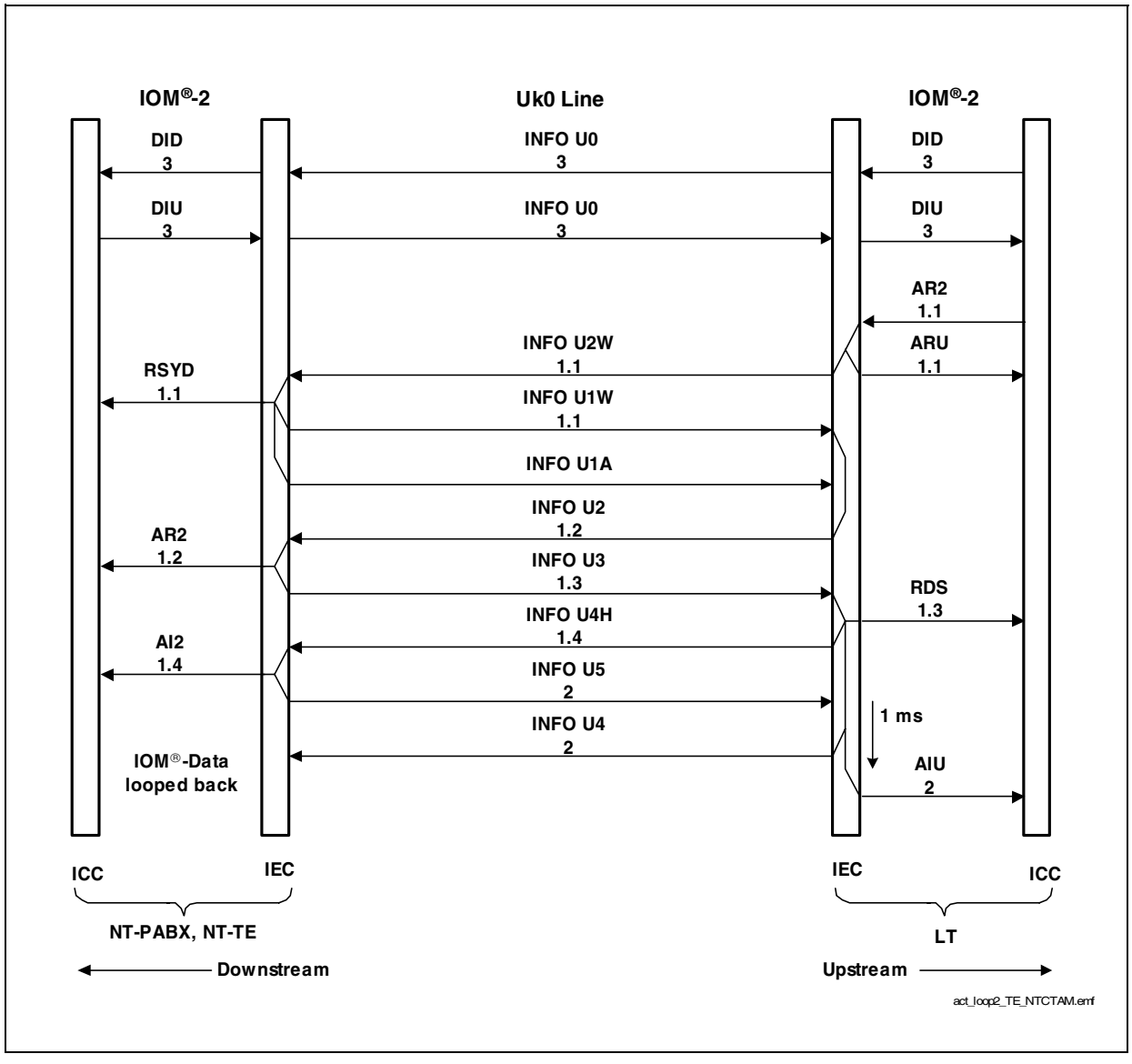


Figure 75 Activation of Loop 2 within NT-PABX or TE

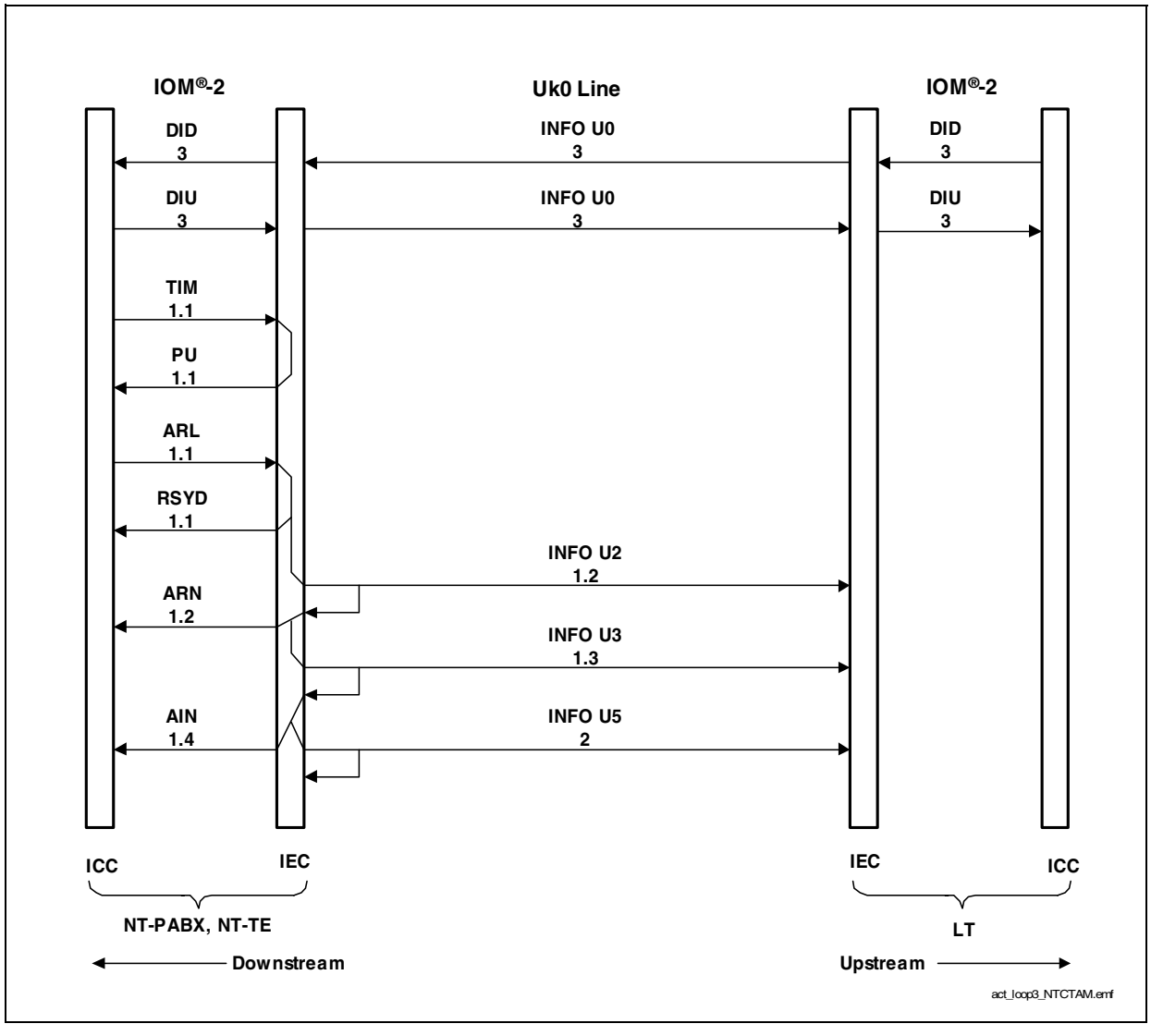


Figure 76 Activation of Loop 3 Within NT-PABX or TE

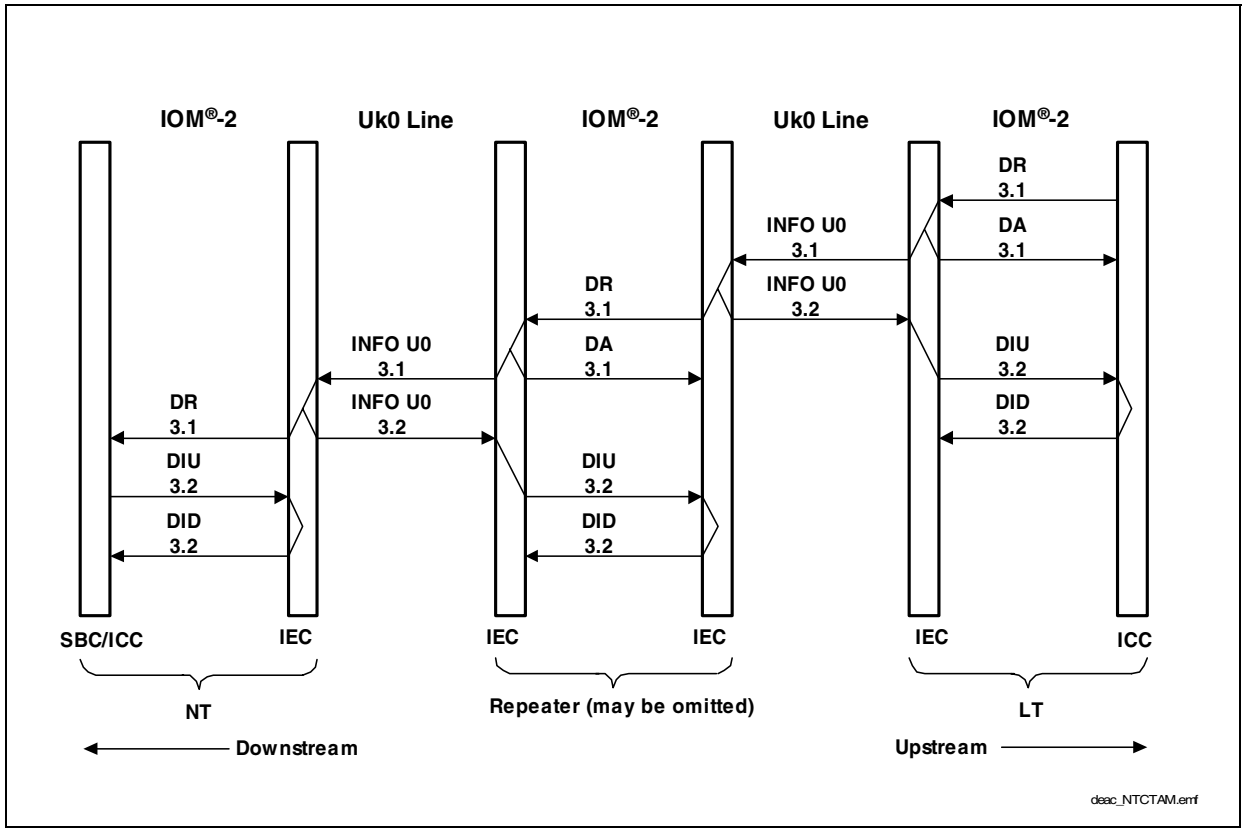


Figure 77 Deactivation of Uk0 Link Always Initiated by LT

7.3 IOM® Control Information in the C/I Channel

The control information in the C/I channel depends on the state of activation. Each code in the C/I channel is repeated in each IOM® frame until a change is necessary. In the layer 2 device (ICC PEB 2070), the code is changed by the controlling processor which overwrites a special register with a new code. In the layer 1 devices, like the NTC-T AM with IEC-T functionality selected, a change of C/I channel code is the result of a detected signal element on the line, a timeout during (de-)activation, or an emergency state of the power controller.

To detect a change in the C/I channel, the new code must be found in two successive IOM® frames to be considered valid (double last look criterion). If the receiving device accepts the new code, it results in a new line signal or in closing a loop directly in the device. A layer 2 device then gives an interrupt request to the processor to hand over the new control information.

Based on these protocols, control information is given downstream (directed from the exchange to the terminal equipment) or upstream (directed from the terminal equipment to the exchange) from one end point to the other via one or more parts of the whole transmission line.

7.3.1 IOM® Control Information for (De-)Activation Downstream

ARD 1 0 - - Activation Request Downstream. The upstream unit of the IOM® interface is a layer 1 device which has just finished synchronizing. Or, it is a layer 2 device (which doesn't synchronize of course) initiating activation. Receiving this, the NTC-T AM with IEC-T functionality selected (LT mode in the exchange) starts by sending awake signal INFO U2W. After a successful awake procedure, the NTC-T AM with IEC-T functionality selected sends INFO U2. In the deactivated state, the NTC-T AM with IEC-T functionality selected in LT-RP mode starts the same procedure on this command. But, usually the LT-RP is activated with RSYD and the awake procedure has already been done when it gets an ARD command. Then, the NTC-T AM with IEC-T functionality selected changes from sending INFO U2A to INFO U4 which means that the applied INFO U2 from the exchange is transparently handed over.

ARD represents the following group of activation requests:
ARN 1000 Activation Request no loop.
ARL 1001 Activation Request local loop only in the exchange.
AR2 1010 Activation Request loop 2 in the exchange or local loop in the repeater and the NT.
AR4 1011 Activation Request loop 4 only in the exchange.

For the description of the loops see **Chapter 6.7**.

AID 1 1 - 0 Activation Indication Downstream. The upstream unit of the IOM® interface (usually a layer 1 device) has detected the line signal which enables the transparent state of the transmission line (INFO U4H on the Uk0 interface). If the layer 2 device in the exchange sends out this code, it has no effect on the NTC-T AM with IEC-T functionality selected.

AID represents the following group of activation indications:

AIN 1100 Activation Indication with no loop.

AIL 1110 Activation Indication with local loop.

For the description of the loops see **Chapter 6.7**.

DR 0 0 0 0 Deactivation Request. The upstream unit of the IOM® Interface requests deactivation. This command must be applied at least 0.5 ms to ensure that the downstream unit has reached the requested state, after the information on the C/I channel has been evaluated.

DID	1 1 1 1	Deactivation Indication Downstream. DID informs the downstream unit that the upstream unit is also deactivated. The layer 1 devices are now ready to receive awake signals; the IOM Interface may be powered down after 4 IOM® frames.
PU	0 1 1 1	Power Up. The upstream unit (NTC-T AM with IEC-T functionality selected in NT-PABX/TE mode) acknowledges the TIM request to initialize an interrupt to the processor from ICC by changing the C/I channel contents.
FJ	0 0 1 0	Frame Jump. The NTC-T AM with IEC-T functionality selected in NT-PABX mode informs the layer 2 downstream unit that some data have been lost due to buffer over/underflow. The NTC-T AM with IEC-T functionality selected in NT-PABX mode absorbs up to 18 µs phase wander between the Uk0 interface and the IOM Interface clocks, which are not controlled by the NTC-T AM with IEC-T functionality selected (in NT-PABX modes) as in the other NT modes.
RSYD	0 1 0 0	Resynchronizing indication Downstream. RSYD informs the downstream unit that the upstream unit isn't synchronous. This occurs usually at the beginning of normal activation after an awake signal has been detected and sent out and allows the LT-RP to start the awake procedure on the second Uk0 link downstream. RSYD is also given if the NTC-T AM with IEC-T functionality selected (NT or NT-RP) was in the fully activated state and has lost synchronization afterwards (but transmission of INFO U5 will not be interrupted).

7.3.2 IOM® Control Information for (De-) Activation Upstream

TIM	0 0 0 0	Enable Timing. In power-down, the downstream unit of the IOM® interface has detected an awake signal on the line or an activation request, if it is a layer 2 device. For further activation, it requests clocks and timing on the IOM interface. Clocks are applied by the upstream unit as long as no DIU is given.
ARU	1 0 0 0	Activation Request Upstream. The downstream unit of the IOM® interface has detected an awake signal on the line or requests activation, if it is a layer 2 device.
ARL	1 0 0 1	Activation Request for Local Loop 3 Upstream. The downstream layer 2 unit of the IOM® Interface requests activation with loop 3.

RDS	0 1 1 1	Running Digital Sum is readable. The downstream unit of the IOM® interface (usually a layer 1 device) has detected the line-signal which informs that the whole Uk0 interface is synchronized (INFO U1 or U3 detected on Uk0). At this point, the counter of frames with detected code violations is enabled.
AIU	1 1 0 0	Activation Indication Upstream. The downstream unit of the IOM® interface (usually a layer 1 device) has detected the line signal which informs that the whole transmission line to the TE is synchronized (INFO U3 on Uk0). In the exchange, the NTC-T AM with IEC-T functionality selected switches itself to the transparent state and controls the transition to the transparent state of the other layer 1 devices. It informs layer 2 that the whole line is now transparent.
DA	0 0 0 1	Deactivation Acknowledge. DA informs the upstream unit that the NTC-T AM with IEC-T functionality selected is deactivating the transmission line downstream. This indication is given out to overwrite a possible DIU code in the C/I channel upstream to enable the ICC to detect the change to DIU which follows afterwards.
DIU	1 1 1 1	Deactivation Indication Upstream. DIU informs the upstream unit that the transmission line downstream is deactivated. The downstream unit is in the power-down state. The transmitter is disabled, but awake signals may be detected.
RSYU		Resynchronizing Indication Upstream. RSYU informs the upstream unit that the downstream unit isn't synchronous. RSYU is given, if the NTC-T AM with IEC-T functionality selected (LT or LT-RP) was in the fully activated state and has lost synchronization afterwards (but transmission of INFO U4 will not be interrupted).

7.3.3 IOM® Control Information to the NTC-T AM with IEC-T Functionality Selected for Test and Maintenance

LTD	0 0 1 1	Line Termination Disable. In the LT, the NTC-T AM with IEC-T functionality selected stops transmitting signals (INFO Up), ignoring awake signals. The chip is set to power-down. Additionally, the control output pin DISS is set to high. This command is used in order to switch off the power-feeding circuitry of the subscriber line and to keep the Uk0 interface deactivated (e.g. due to a continuous fault).
RES	1 1 0 1	Reset of the NTC-T AM with IEC-T functionality selected. Any stored settings are erased. The NTC-T AM with IEC-T functionality selected goes to the power-up state, but no line signal will be sent out. An applied low on RESQ pin, while TSP is low, has the same effect (with one exception regarding pin DISS).
SSP	0 1 0 1	Send Single Pulses. The NTC-T AM with IEC-T functionality selected goes to the power-up state and sends single pulses with a period of 1 ms. An applied high on the TSP pin, while RESQ is high, has the same effect.
TEST	0 1 1 0	Test mode of the NTC-T AM with IEC-T functionality selected. The NTC-T AM with IEC-T functionality selected goes from any mode and at any state of activation to the transparent state (sends INFO U4/ U5). An applied low on RESQ pin, while TSP is high, has the same effect.

7.3.4 IOM Control Information from the NTC-T AM with IEC-T Functionality Selected for Power Control

HI	0 0 1 1	High Impedance. When the control line CLS in the LT is set to high, the indication HI is output in the C/I channel as long as CLS remains high. The NTC-T AM with IEC-T functionality selected deactivates the transmission line and any received awake signal is ignored. The transmitter, however, may be controlled to transmit single pulses using the command SSP.

7.3.5 Summary of IOM® Control Informations in Different Applications

Table 18 Summary of Codes in C/I Channel

Code	LT LT-BURST		LT-RP		NT		NT-RP		NT-PABX-(BURST) NT-TE	
A1...A4	**DIN**	**DOUT**	**DIN**	**DOUT**	**DIN**	**DOUT**	**DIN**	**DOUT**	**DIN**	**DOUT**
0000	DR		DR	TIM	TIM	DR	TIM	DR	TIM	DR
0001		DA		DA						
0010						(FJ)[1]		(FJ)[2]		FJ
0011	LTD	HI								
0100		RSYU	RSYD	RSYU		RSYD	RSYU	RSYD		RSYD
0101	SSP		SSP		SSP		SSP		SSP	
0110	TEST		TEST		TEST		TEST		TEST	
0111		RDS								PU
1000	ARN	ARU	ARN	ARU	ARN	ARU	ARN	ARU	ARN	ARU
1001	ARL								ARL	
1010	AR2		AR2			AR2		AR2		AR2
1011	AR4									
1100		AIU	AIN	AIU	AIU	AIN	AIU	AIN		AIN
1101	RES		RES		RES		RES		RES	
1110			AIL			AIL		AIL		AIL
1111	DID	DIU	DID	DIU	DIU	DID	DIU	DID	DIU	DID

[1], [2]: C/I-indication 'FJ' is not issued during transparent transmission, but might be issued during start-up.

7.4 Meaning of Uk0 INFOs

INFO U0 — Deactivation signal of both directions. Downstream, it is the command to deactivate the NT. Upstream, it is the acknowledge of deactivation of the NT.

INFO U1W — Awake or acknowledge signal upstream used in the awake procedure of the Uk0 interface.

INFO U2W — Awake or acknowledge signal downstream used in the awake procedure of the Uk0 interface.

INFO U2	The LT (and LT-RP, if the NT-RP is synchronized) sends INFO U2 to enable the own echocanceller to adapt the coefficients, and with the barker code the NT at the other end is enabled to synchronize. The M channel on Uk0 may be used to transfer loop commands. Recognizing INFO U2 is used as a criterion for synchronization.
INFO U2A	While the NTC-T AM with IEC-T functionality selected in NT-RP mode is synchronizing on the received signal, the NTC-T AM with IEC-T functionality selected in LT-RP mode sends out INFO U2A to enable its echocanceller to adapt the coefficients, but sending no barker code it inhibits the NT (-TE, -PABX) to synchronize on the still asynchronous signal. Due to proceeding synchronization, the Uk0 frame may jump from time to time. INFO U2A can't be detected in the NTC-T AM with IEC-T functionality selected in NT mode at the far end.
INFO U1A	While the NTC-T AM with IEC-T functionality selected (in all NT modes) is synchronizing on the received signal, it sends out INFO U1A to enable its echocanceller to adapt the coefficients, but sending no barker code it inhibits the LT (-RP) to synchronize on the still asynchronous signal. Due to proceeding synchronization, the Uk0 frame may jump from time to time. INFO U1A can't be detected in the NTC-T AM with IEC-T functionality selected in LT mode at the far end.
INFO U1	When synchronized, the NTC-T AM with IEC-T functionality selected (in all NT modes) sends the barker code and the LT(-RP) may synchronize itself. INFO U1 indicates additionally that a terminal equipment hasn't yet activated. When receiving INFO U1, the NTC-T AM with IEC-T functionality selected indicates the synchronized state with RDS to layer 2. Usually during activation, no INFO U1 is detected in the LT because the TE is activated first and INFO U1 changes to INFO U3 before being detected. The M channel on Uk0 may be used to transfer code error indications and 1 kbit/s transparent data.
INFO U3	When detecting INFO U3, the NTC-T AM with IEC-T functionality selected in LT mode in the exchange is allowed to command the transition to the fully transparent state, because it indicates that the whole link to the TE is synchronous In both directions. The M channel on Uk0 may be used to transfer code error indications and 1 kbit/s transparent data.
SI	The NTC-T AM with IEC-T functionality selected sends periodically single pulses spaced 1 ms to the Uk0 interface to ensure that it is within the specified pulse mask.

INFO U4H	With INFO U4H, each unit is commanded to go to the transparent state. When detecting this, the NTC-T AM with IEC-T functionality selected in NT mode stops sending INFO U3 and indicates this to the SBC or layer 2 device, ICC, via the IOM® interface. The M channel on Uk0 may be used to transfer loop commands and 1 kbit/s transparent data.
INFO U4	NFO U4 means fully transparent data, the M channel on Uk0 may be used to transfer loop commands and 1 kbit/s transparent data.
INFO U5	INFO U5 means fully transparent data, the M channel on Uk0 may be used to transfer code error indications and 1 kbit/s transparent data.

7.5 State Diagrams

The following state diagrams describe all the action/reaction resulting from any command or detected signal and resulting from the various operating modes.

The states, inputs and outputs are characterized as shown in the following example:

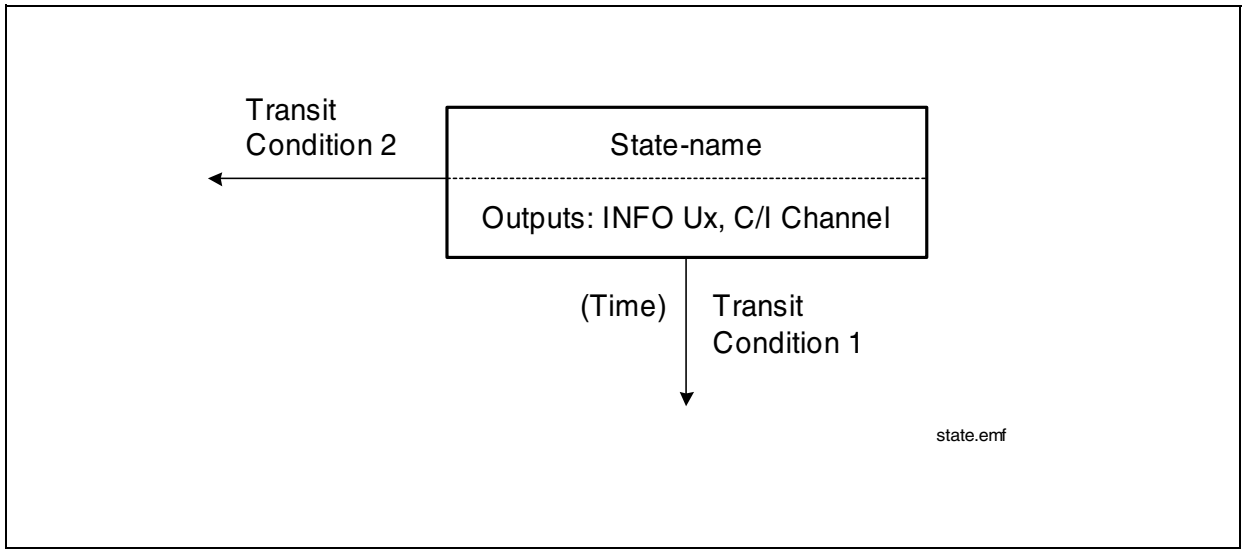


Figure 78 Example of a State with Outputs and Inputs

Each state has one or more exits to other states. These transitions depend on certain conditions which are noted next to the transition lines. These conditions are the only possibility to leave a state. If more conditions have to be fulfilled together, they are put into parentheses with an AND operator (&). If more than one condition leads to the same transition, they are put into parentheses with an OR operator (|). The meaning of a condition may be inverted by the NOT operator (/). Only the described states and transitions can exist.

Some conditions lead from each state to the same target state. To reduce the number of lines and the complexity of the figures, a state named "ANY STATE" exists standing for each state.

At some transitions, an internal timer is started. The time until the timer runs out, is noted in curly brackets { } next to the transition line. If the end of the started time leads to a transition from one state to another, this condition is indicated by TE (timer ended).

These actions are chosen to cope with all ISDN devices with IOM® standard interfaces. The states and transitions have been prepared to prevent undefined situations. In any case, the involved devices will enter defined conditions when the line is deactivated.

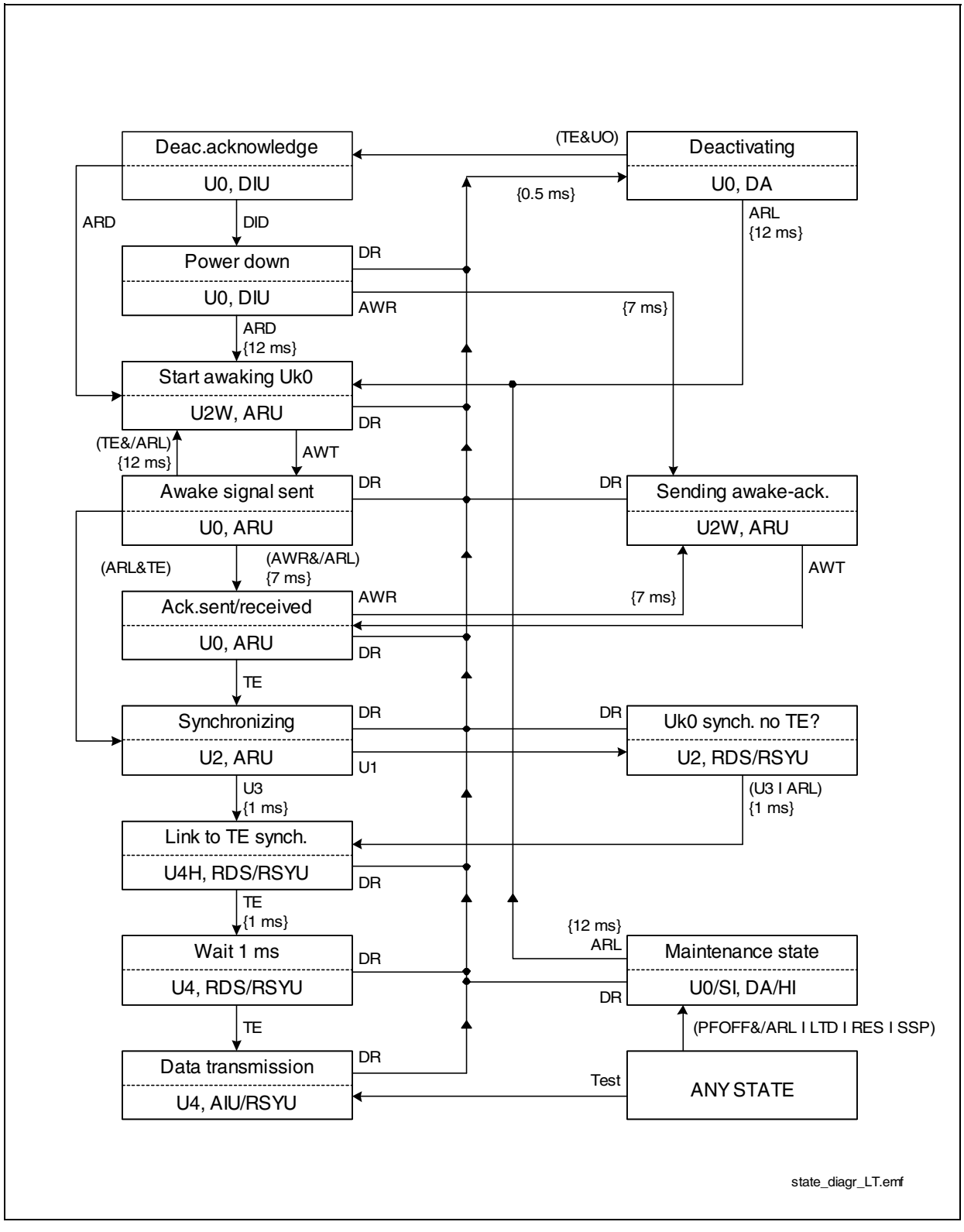


Figure 79 State Diagram of the LT Mode

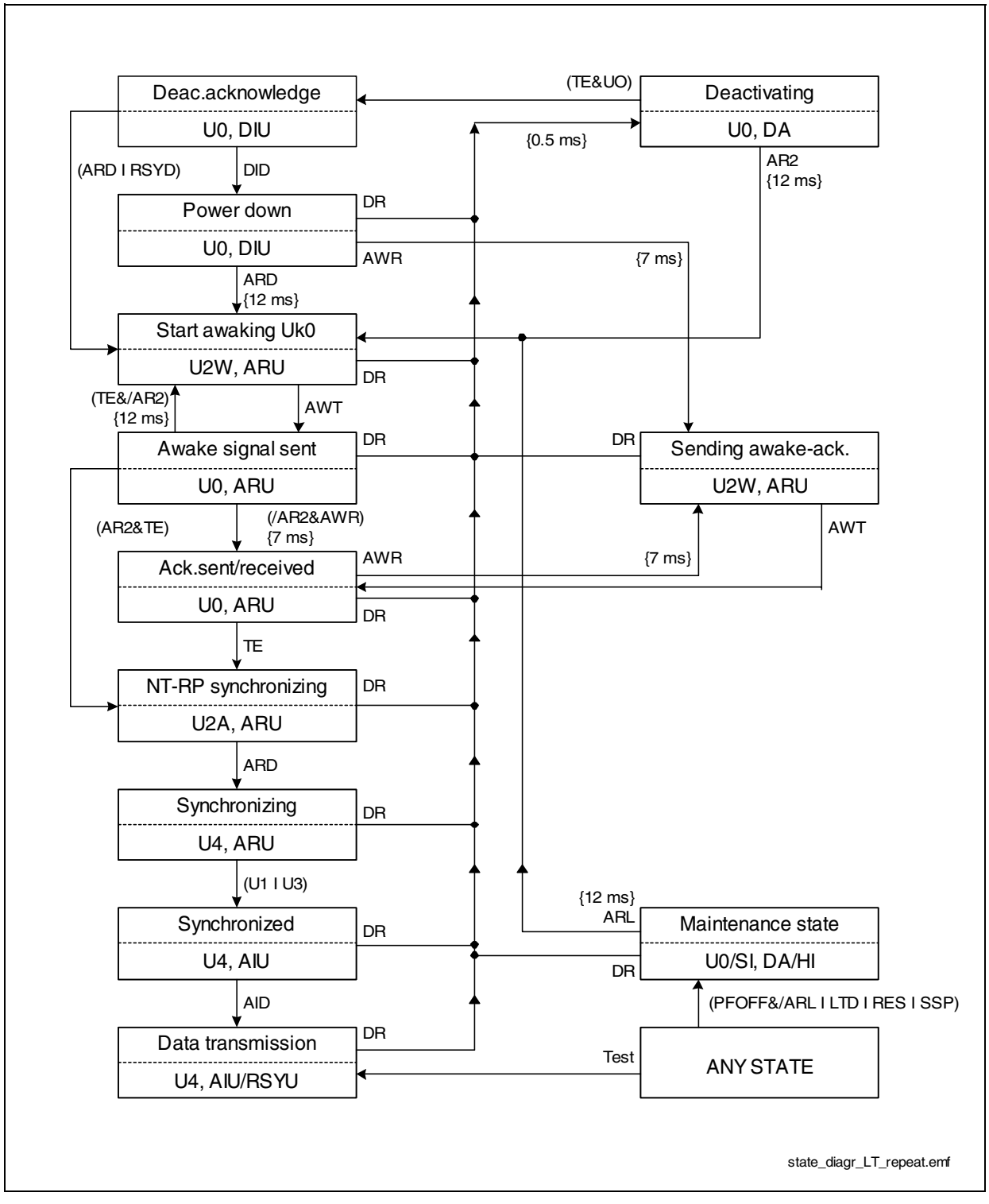


Figure 80 State Diagram of the LT-Repeater Mode

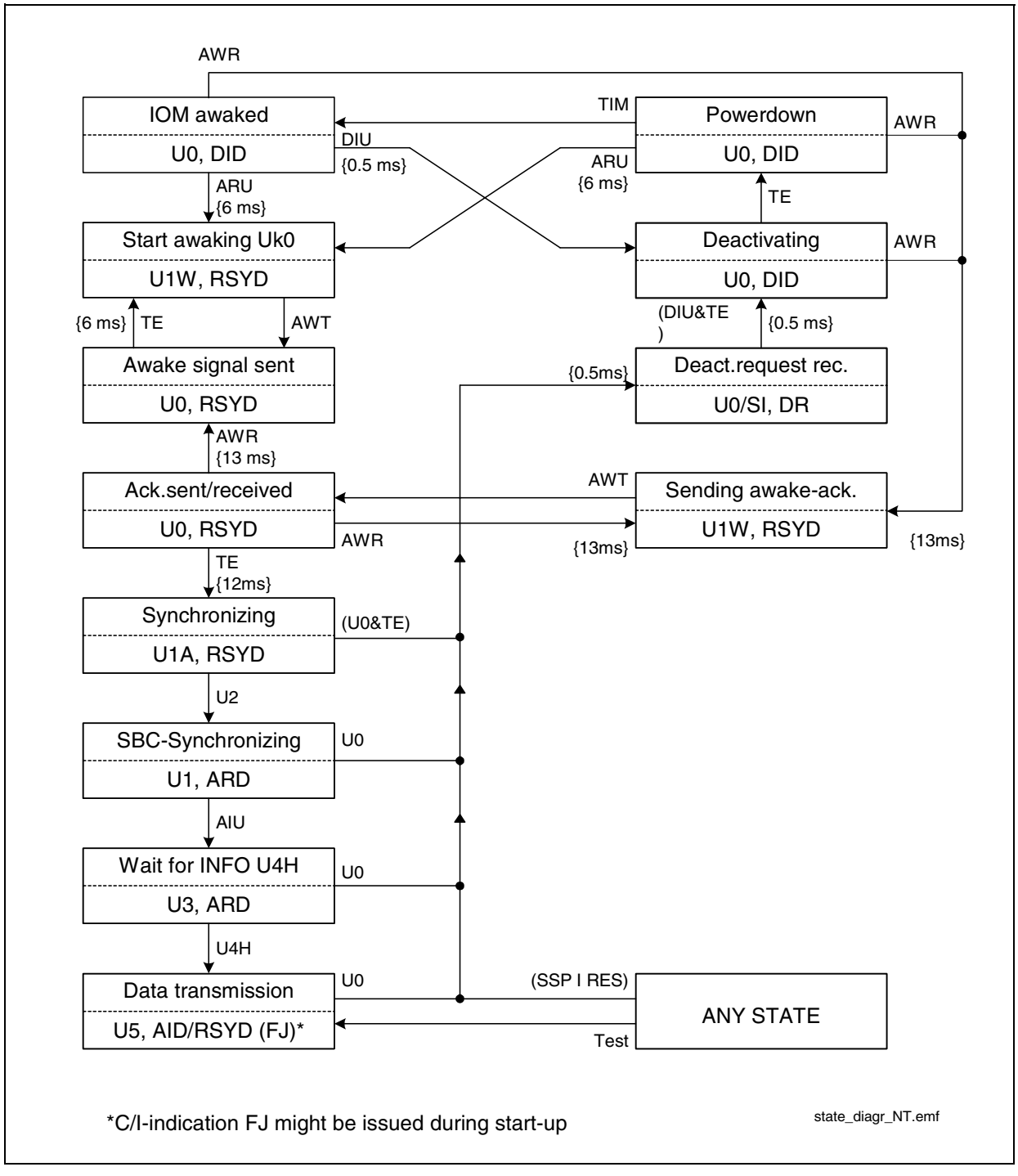


Figure 81 State Diagram of the NT Mode

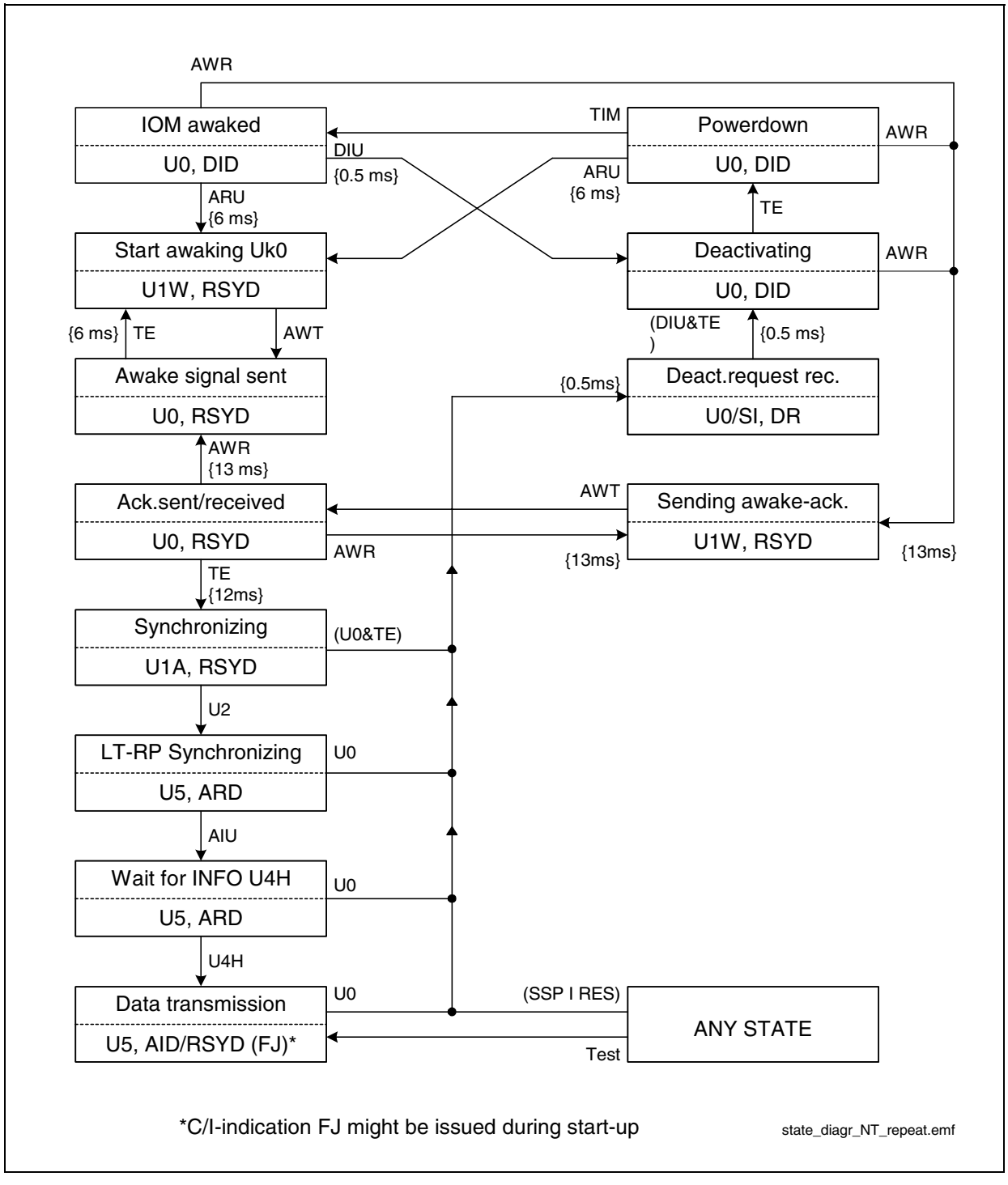


Figure 82 State Diagram of the NT-Repeater Mode

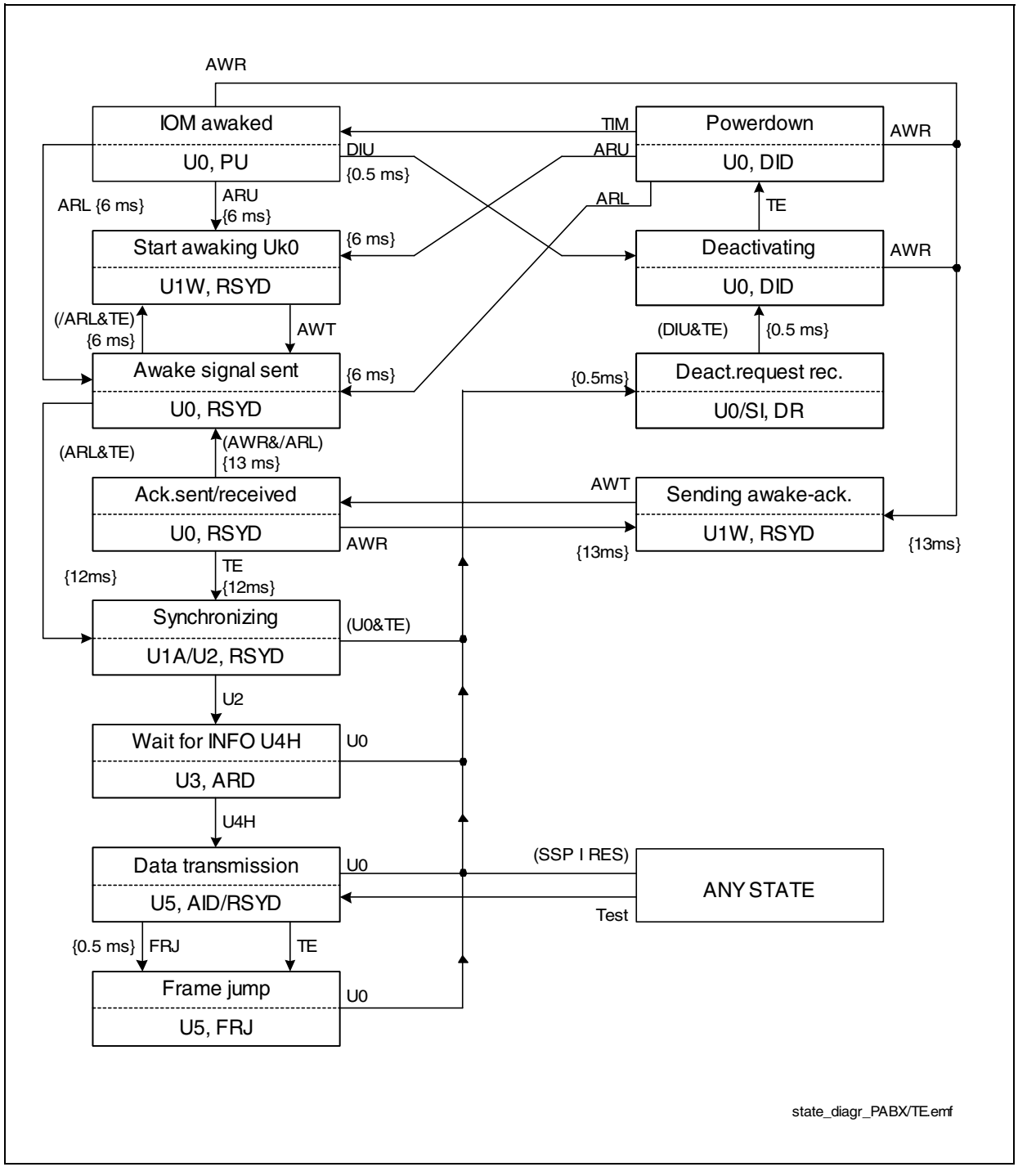


Figure 83 State Diagram of the NT-PABX and NT-TE Mode

7.5.1 Transit Conditions and their Abbreviations

In the following list, C/I channel infos are omitted.

AWR	Awake signal (INFO U1W or U2W) detected.
AWT	INFO U1W of U2W has been sent out
FRJ	Frame jump, detected by receive or transmit buffer, at least one IOM® frame (18 bit) is repeated or omitted caused by receive or transmit buffer over/underflow
TE	Timer ended, the started timer has run out
U0	INFO U0 detected
U1	INFO U1 detected
U2	INFO U2 detected
U3	INFO U3 detected
U4H	INFO U4H detected

7.5.2 Control of the Analog Loop and Loop Commands on Uk0

The output of the NTC-T AM with IEC-T functionality selected, e.g. infos on Uk0 or C/I channel contents, usually depends only on the given state of the NTC-T AM with IEC-T functionality selected control unit. In some states, several outputs are possible depending on input. If RESQ isn't set to low or TSP isn't set to high, only the control of loops is state independent and is evaluated from the C/I channel input.

ARL	(in the C/I channel) always causes the analog loop to be closed in all modes except the Repeater modes. If INFO U2A or U4 is sent, the M symbol is set to continuous plus polarity in LT-RP.
AR2	(in the C/I channel) causes the M symbol continuously to be set to plus polarity in the LT, and LT-BURST modes, if INFO U2, U4H or U4 is sent. The analog loop is closed in LT-RP.
AR4	(in the C/I channel) causes the M symbol to be set to alternating plus and zero polarity in all LT modes.
AIL	(in the C/I channel) causes the NTC-T AM with IEC-T functionality selected to close the analog loop in the repeater modes.

Any other C/I channel input, low at RESQ or high at TSP, causes the analog loop to be opened and in the LT modes the M symbol to be set to zero.

In the NT modes, the state diagrams specify only ARD and AID, which are groups of C/I channel codes, to indicate the activated states. Depending on the mode and the last recognized received loop command, the NTC-T AM with IEC-T functionality selected decides whether it sends ARN or AR2, AIN or AIL into the C/I channel.

If it receives 8 subsequent M symbols with zero polarity, in each NT mode the NTC-T AM with IEC-T functionality selected sends ARN for ARD and AIN for AID in the state diagram.

If it receives 8 subsequent M symbols with plus polarity, in NT, NT-TE and NT-PABX modes the NTC-T AM with IEC-T functionality selected gives out AR2 for ARD and AIL for AID in the state diagram.

If it receives 8 subsequent M symbols with alternating plus and zero polarity, in NT-RP mode the NTC-T AM with IEC-T functionality selected gives out AR2 for ARD and AIL for AID in the state diagram.

7.5.3 Description of the Activation/Deactivation States of NTC-T AM with IEC-T Functionality Selected

In this section, each state is described with its outputs and its meaning. Unless described otherwise, the activation controller performs the following actions:

- No RESET of the NTC-T AM with IEC-T functionality selected.
- DISS pin is low.
- The adaption of receiver coefficients is disabled.
- The RDS counter of frames with code violations is reset and disabled.
- The received user data is given transparently to the IOM® interface.
- The NTC-T AM with IEC-T functionality selected is in power-up.

The C/I channel output and the transmitted Uk0 INFO are already specified by the state diagrams; below they are only referred to, if within a state there are more than one of them specified. In this case, the C/I channel output and the transmitted Uk0 INFO depend on the given inputs.

Ack. sent/received	If awaking, the NTC-T AM with IEC-T functionality selected has received the acknowledge signal. If being awoken the IEC has sent the acknowledge. Anyway, the NTC-T AM with IEC-T functionality selected waits for possible repetition or timeout. The user data (B+B+D) on pin DOUT is clamped to high to avoid undesired false data in the D channel during activation.
Awake signal sent	The NTC-T AM with IEC-T functionality selected is awaking the Uk0 interface and waits for the acknowledge or for the timeout after sending the awake signal. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).
Deac. acknowledged	The NTC-T AM with IEC-T functionality selected has received INFO U0, indicates this to the upstream unit and waits for DID, the permission to power down. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).

Deact. request rec.	The NTC-T AM with IEC-T functionality selected has received INFO U0 or one of the deactivating maintenance requests, RES or SSP. If it receives SSP, the NTC-T AM with IEC-T functionality selected sends a single pulse every 1 ms on the line, otherwise INFO U0 is sent. The NTC-T AM with IEC-T functionality selected remains at least 0.5 ms in this state before accepting DIU to be sure that it is already valid. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).
Deactivating	The NTC-T AM with IEC-T functionality selected deactivates Uk0 sending INFO U0; it remains at least 0.5 ms in this state to make sure that the associate device on IOM® has recognized a change from a possible DIU state to DA. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).
Data transmission	The transmission of user data is enabled (INFO U4/U5). If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the NTC-T AM with IEC-T functionality selected gives out RSYD or RSYU on the C/I channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames. The RDS counter and the adaption of receiver coefficients are enabled even if RSYD/RSYU is given out.
Frame jump	In the transmit or in the receive data buffer a data over- or underflow has occurred. This is indicated to the associated layer 2 device, ICC with code FJ for 0.5 ms (4 IOM® frames). The RDS counter and the adaption of receiver coefficients are enabled.
IOM® awaked	The NTC-T AM with IEC-T functionality selected in each NT mode is awoken by the downstream unit keeping line DU of IOM® Interface (pin DIN of IEC) low (TIM). When it receives DIU again in the C/I channel, the NTC-T AM with IEC-T functionality selected goes back to power-down within at least 0.5 ms. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).

Link to TE synch.	The NTC-T AM with IEC-T functionality selected in LT mode in the exchange has received INFO U3 indicating that the link is synchronized from and to the TE. The NTC-T AM with IEC-T functionality selected in LT mode commands, with 1 ms INFO U4H, the whole link to the TE to be switched transparent. The RDS counter and the adaption of receiver coefficients are enabled. If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the NTC-T AM with IEC-T functionality selected gives out RSYD or RSYU on the C/I channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames.
LT-RP Synchronizing	After being synchronized itself and indicating this with ARN/ AR2, the NTC-T AM with IEC-T functionality selected in NT-RP mode waits for the message AIU from the LT-RP indicating that it also is synchronized. The NT-RP sends transparently on Uk0 the received data from LT-RP. Because the LT-RP issues only the AIU C/I-code when it has detected INFO U1 or U3, it is ensured that the NT-RP did not send out INFO U1 or U3 itself until the LT-RP is synchronized.
Maintenance state	With a low on pin CLS in LT modes, RES, SSP or LTD In the CA channel or with a low on pin RESQ as well as a high on pin TSP, the NTC-T AM with IEC-T functionality selected goes to the maintenance state. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes). If the NTC-T AM with IEC-T functionality selected in LT mode detects a high on pin CLS indicating “Power feed off” it puts in this state code HI in the C/I channel, otherwise DA. If pins TSP and RESQ are high or code SSP is in the C/I channel input, the NTC-T AM with IEC-T functionality selected sends each ms a single pulse on the line to enable the test whether it fits into the specified pulse mask. Detecting LTD in the C/I channel is the only possibility for the NTC-T AM with IEC-T functionality selected in LT mode to set output pin DISS high. IF pins RESQ and TSP are low or RES is in the C/I channel input, the NTC-T AM with IEC-T functionality selected is reset in this state erasing all stored coefficients. If RESQ pin is low, DISS pin is set to high. If the reset is given only in the C/I channel, DISS-pin is set to low. In the LT mode, the NTC-T AM with IEC-T functionality selected leaves the maintenance state only if CLS and TSP are low, RSQ is high and code DR or ARL is in the C/I channel.

NT-RP synchronizing	The LT-RP waits for a command ARD from NT-RP indicating that it is synchronized. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).
Power down	Entering this state, the NTC-T AM with IEC-T functionality selected powers down within 0.5 ms stopping most parts of the NTC-T AM, so that these CMOS circuits cannot consume further energy. In the LT modes and NT-PABX modes the IOM® interface units remain active as long as they are clocked via CLOCK pin, and the user data (B+B+D) on pin DOUT is clamped to high (except repeater modes). In modes NT, NT-RP and NT-TE, the NTC-T AM with IEC-T functionality selected stops clocking the IOM® interface, if it has received four times DIU in the C/I channel. In all NT modes pin DISS is set to high to indicate to the power controller device that now less power is consumed. If the IOM® interface clock is stopped, it can be activated by the downstream unit by forcing line DU to low, when an awake signal is recognized. The upstream unit activates simply by restarting the IOM® clock, when a low on DIN or an awake signal is recognized.
SBC Synchronizing	After being synchronized and indicating this with ARN/AR2, the NTC-T AM with IEC-T functionality selected in NT mode waits for the message AIU from the SBC which indicates that it is also synchronized. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).
Sending awake-ack.	The NTC-T AM with IEC-T functionality selected has received the awake signal and acknowledges this in this state. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).
Synchronized	The NTC-T AM with IEC-T functionality selected in LT-RP mode has recognized INFO U1 or U3, so 1152 subsequent bits have been transferred without any bit error. This indicates synchronization. Now the NTC-T AM with IEC-T functionality selected itself is ready to go to the transparent state.
Synchronizing	After successful awake procedure, the NTC-T AM with IEC-T functionality selected tries to recognize INFO U1, U2 or U3 (mode dependent). The user data (B+B+D) on pin DOUT is clamped to high (except LT-RP).
Start awaking Uk0	Receiving ARU or ARD In the C/I channel, the NTC-T AM with IEC-T functionality selected has powered up and is sending the awake signal. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes).

Uk0 synch. no TE?	The NTC-T AM with IEC-T functionality selected in LT mode in the exchange has recognized INFO U1, so 1152 subsequent bits have been transferred without any bit error. This is an indication for synchronization of Uk0, but no terminal equipment has announced its presence yet. The NTC-T AM with IEC-T functionality selected is now ready to go to the transparent state, if a TE was connected. From this state of activation, the RDS counter and the adaption of receiver coefficients are enabled until deactivation is performed. In case of an analog loop, the NTC-T AM with IEC-T functionality selected leaves this state again at once. If no loop should be closed, the NTC-T AM with IEC-T functionality selected waits for INFO U3 indicating that at least one TE is at the end of the link or for deactivation. If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the NTC-T AM with IEC-T functionality selected gives out RSYD or RSYU on the C/I channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames.
Wait for INFO U4H	In this state, the NTC-T AM with IEC-T functionality selected in all NT modes is synchronized. It has received the information that the associated downstream device is synchronized itself, and it waits now for the permission to go to the transparent state. The user data (B+B+D) on pin DOUT is clamped to high (except NT-RP).
Wait 1 ms	Before indicating to the layer 2 device that the transparent state has been reached, the NTC-T AM with IEC-T functionality selected in LT mode in the exchange waits 1 ms to be sure that the whole link is already transparent upstream too. The user data (B+B+D) on pin DOUT is clamped to high (except repeater modes). If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the NTC-T AM with IEC-T functionality selected gives out RSYD or RSYU on the C/I channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames.

8 Part III 'Common': Functional Description

8.1 Reset

A power-on reset and an undervoltage detection are integrated on the chip. Both resets are visible on the reset output pin $\overline{\text{RST}}$. Furthermore, it is possible to reset the NTC-T AM via an externally generated impulse applied at pin $\overline{\text{RES}}$.

8.2 External Circuitry

8.2.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.

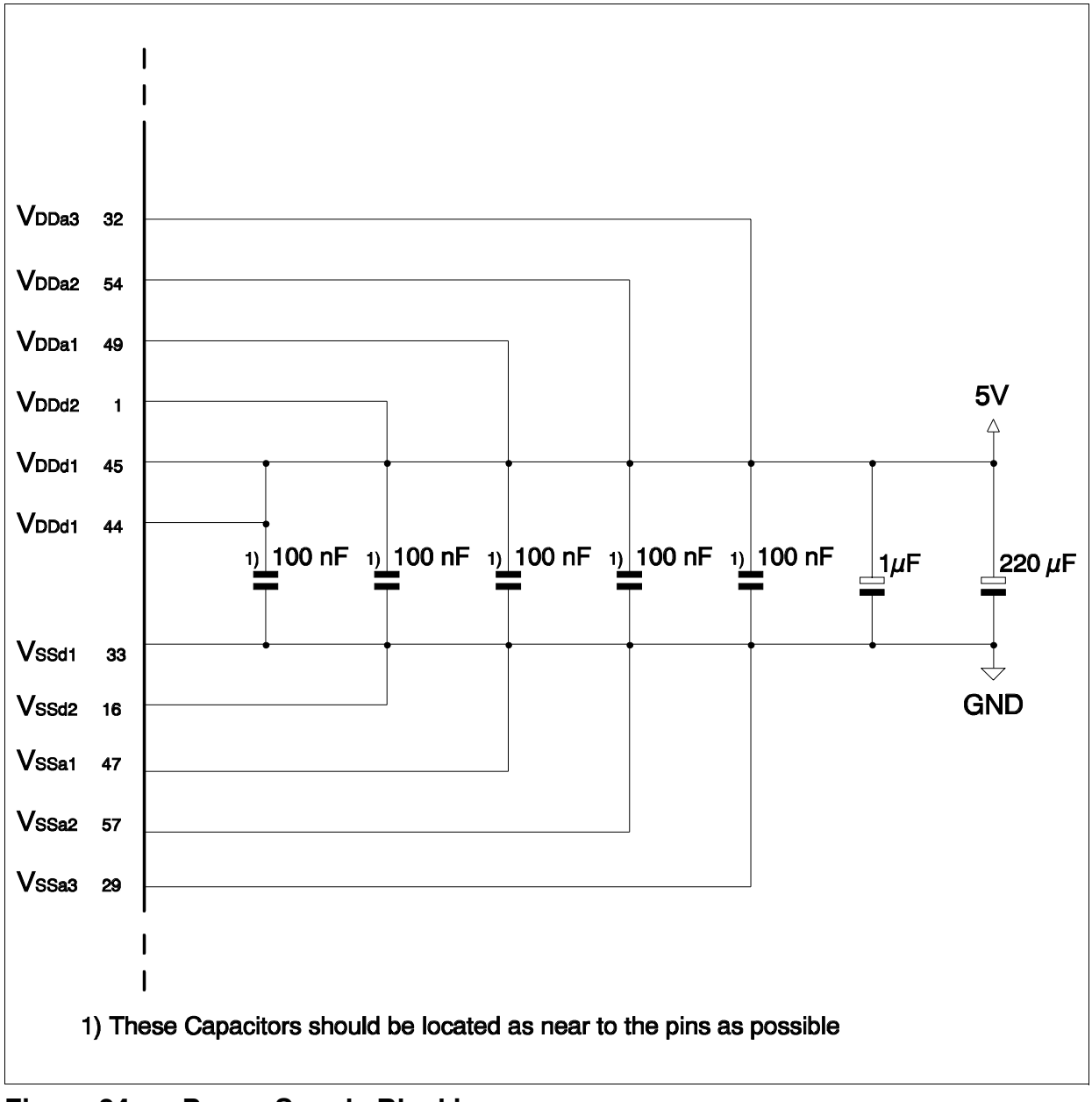


Figure 84 Power Supply Blocking

8.2.2 U-Interface

The NTC-T AM is connected to the twisted pair via a transformer. **Figure 85** shows the recommended external circuitry.

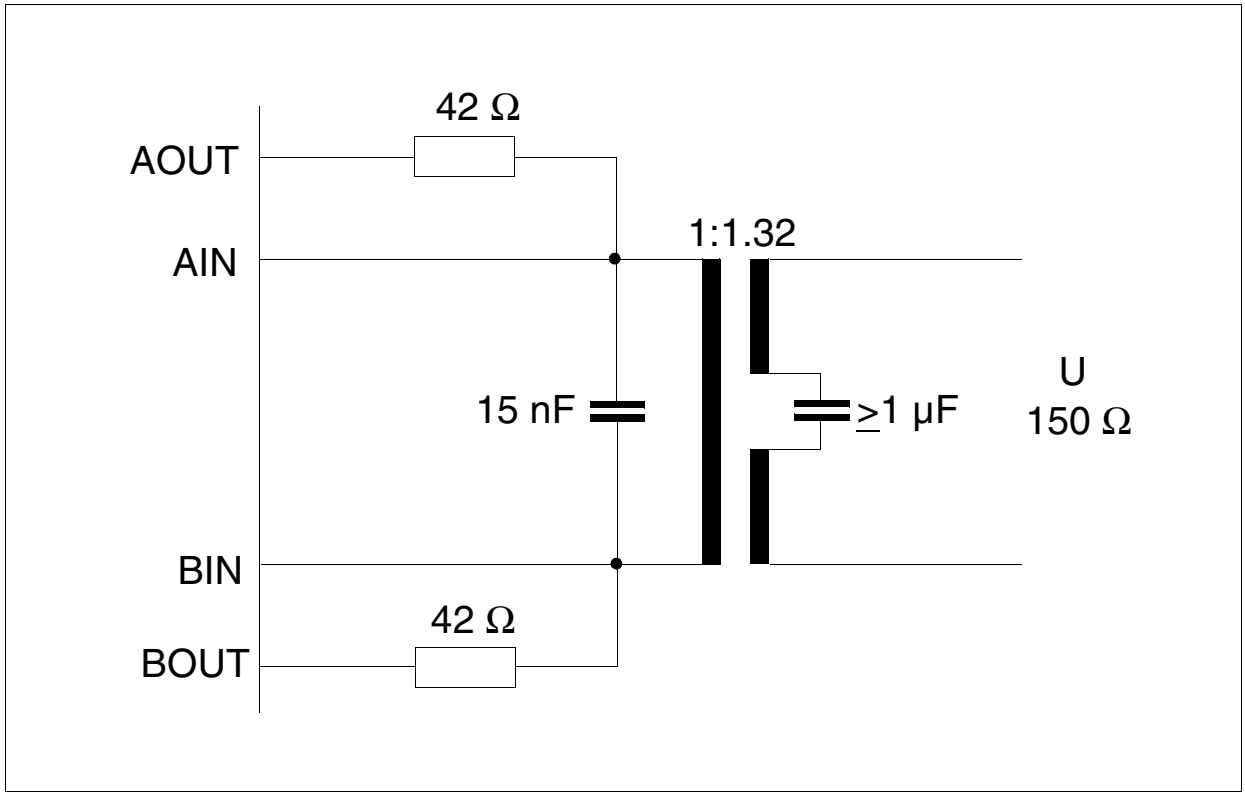


Figure 85 U-Interface Hybrid Circuit

The transformer should have a ratio of 1:1.32 (circuit / line side) and the total inductivity seen from the line side should be between 5 and 10 mH.

Note: To achieve optimum performance the 10 nF capacitor should be MKT. A Ceramic capacitor is not recommended.

Note: In the NTC-T Data Sheet 06.98 the value proposed for the capacitor on the chip side was 10 nF.
The recommendation has been changed to 15 nF in order to meet the power spectral density requirements of the new ETSI TS 102080 standard.

Note: Information on the recommended protection circuitry is given in the 'Application Hint NTC-T (8.00)'.

9 Part III 'Common': Electrical Characteristics

9.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias:PEB	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V
ESD robustness [1)] HBM: 1,5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) According to MIL-STD 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse as outlined in the following figure.

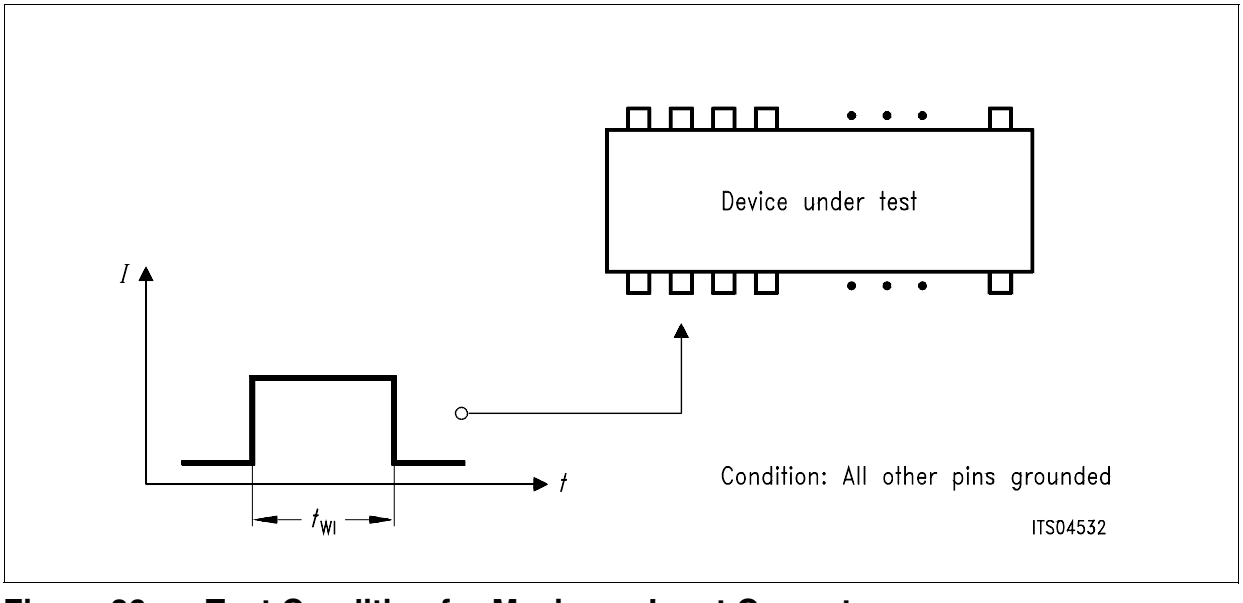


Figure 86 Test Condition for Maximum Input Current

S-Transmitter Input Current

(Relevant only when NTC-T functionality selected).

The destruction limits for negative input signals ($R_i \geq 2\ \Omega$) and for positive input signals ($R_i \geq 200\ \Omega$) are given in **Figure 87**.

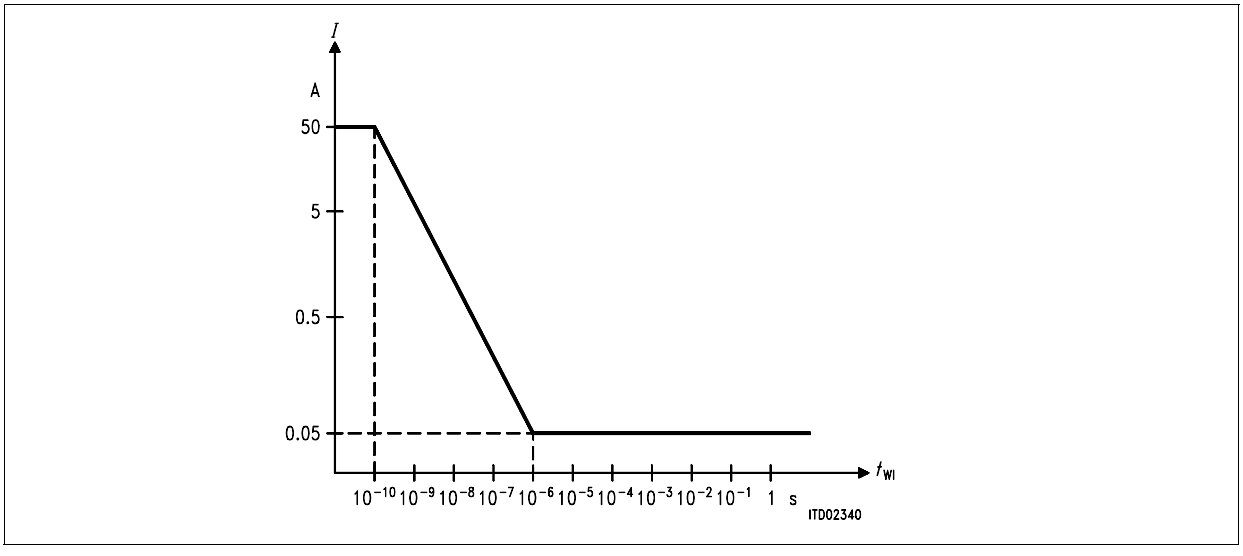


Figure 87 S-Transmitter Input Current

S-Receiver Input Current

(Relevant only when NTC-T functionality selected).

The destruction limits ($R_i \geq 300\ \Omega$) are given in **Figure 88**.

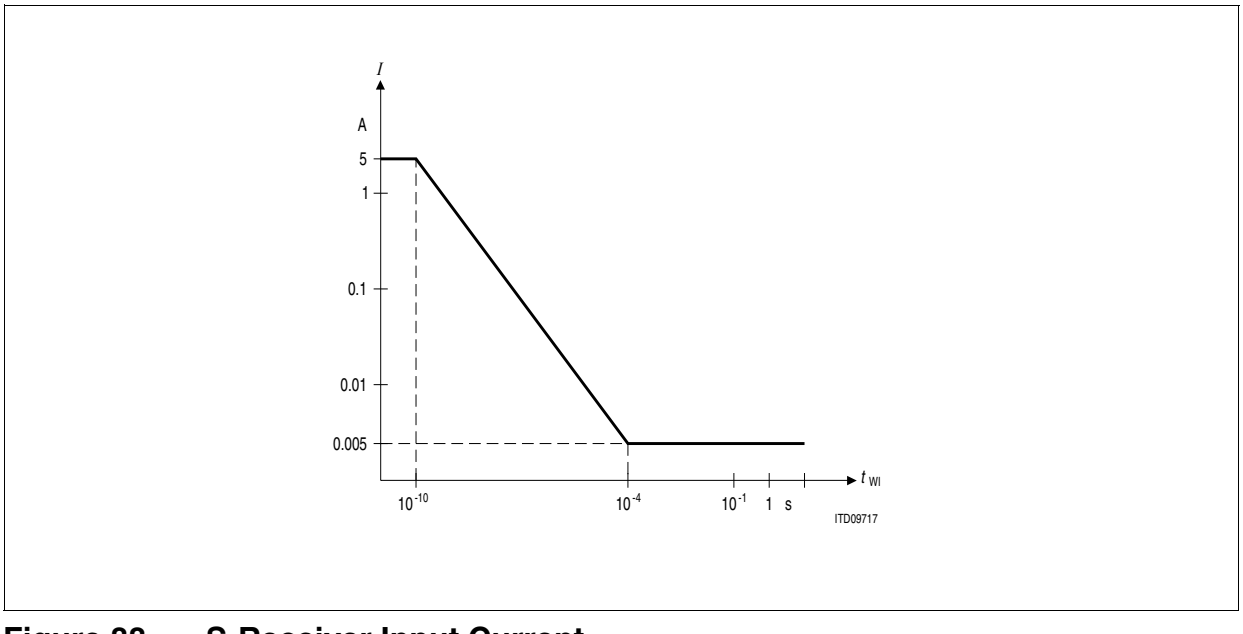


Figure 88 S-Receiver Input Current

U-Transceiver Input Current

The destruction limits for AOUT, BOUT, AIN and BIN are given in **Figure 89**.

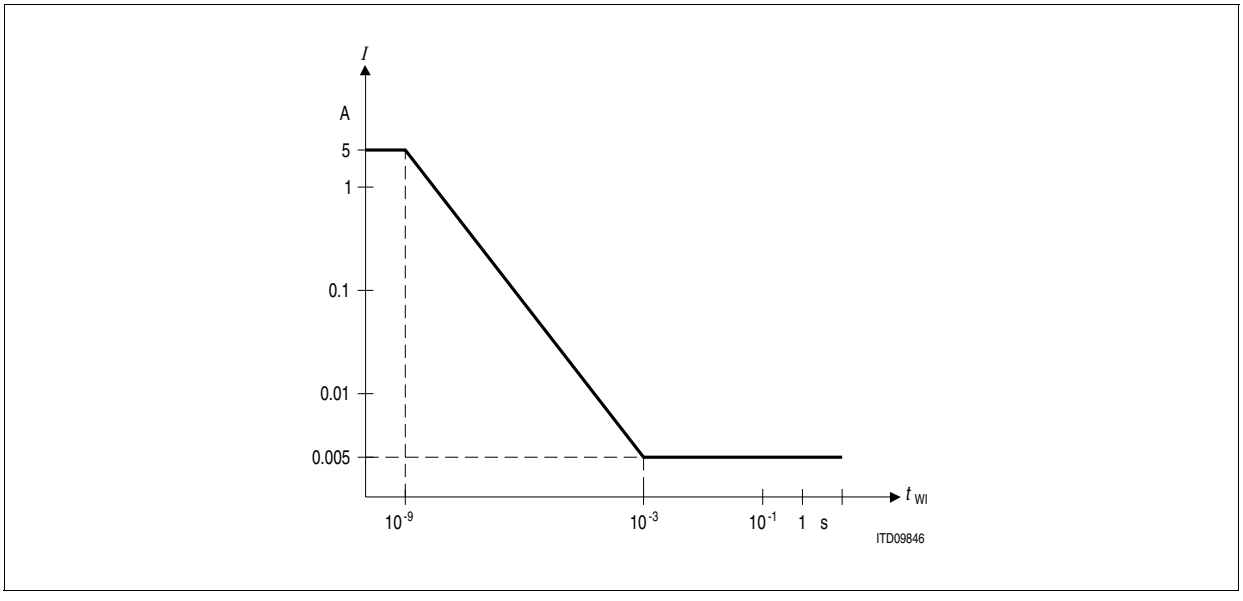


Figure 89 U-Transceiver Input Current

9.2 Power Consumption

V_{DD} = 5 V; V_{SS} = 0 V; Inputs at V_{SS} / V_{DD}; no output loads except SX1,2 (280 Ω [1]) and AOUT, BOUT (172 Ω [2]).

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
S and U active					**50% bin. zeros, IOM-2 disabled**
Operational		**240**	**270**	**mW**	**T_A = 0 - 70 °C**
Power Down		**15**	**20**	**mW**	**T_A = 25 °C**
			30	**mW**	**T_A = 70 °C**

1) 280 Ω at pins SX1,2 correspond to 50 Ω (2 x TR) on the S-bus.
2) 172 Ω between pins AOUT and BOUT correspond to 150 Ω line impedance of the U-interface.

9.3 DC Characteristics

Pin	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
All except SR1, 2	Input low voltage	V_{IL}	– 0.4	0.8	V	
	Input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
All except DD, DU; SX1, SX2	Output low voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
DD, DU	Output low voltage	V_{OL1}		0.45	V	I_{OL} = 7 mA
All except DD, DU; SX1, 2, A/BOUT	Output high voltage	V_{OH1}	2.4		V	I_{OH1} = 400 µA
			V_{DD} – 0.5		V	I_{OH1} = 100 µA
DD, DU	Output high voltage	V_{OH2}	3.5		V	I_{OH2} = 6 mA
All pins except SX1, 2; SR1,2; AIN, BIN, XIN	Input leakage current	I_{LI}		1	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Output leakage current	I_{LO}		1	µA	0 V ≤ V_{OUT} ≤ V_{DD}
	Input leakage current internal pull-up	I_{LIPU}	4	15 0	µA	V_{IN} = 2.5 V V_{IN} = V_{DD}
XIN	Input leakage current	I_L	-10	10	µA	0 V ≤ V_{IN} ≤ V_{DD}
AIN, BIN	Input leakage current	I_L	-25	700	µA	0 V ≤ V_{IN} ≤ V_{DD}
Relevant only when NTC-T functionality selected						
SX1, SX2	Absolute value of output pulse amplitude ($V_{SX2} - V_{SX1}$)	V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω R_L = 400 Ω
SX1, SX2	S-Transmitter output current	I_X	7.5	13.4	mA	R_L = 5.6 Ω
SX1, SX2	S-Transmitter output impedance	Z_X	10 0		kΩ Ω	inactive or during binary one (V_{DD} = 0 … 5 V) during binary zero R_L = 50 Ω
SR1, SR2	S-Receiver input impedance	Z_R	10 100		kΩ Ω	V_{DD} = 5 V V_{DD} = 0 V

U-Transceiver Characteristics

	Limit Values			Unit
	min.	typ.	max.	
Receive Path				
Signal / (noise + total harmonic distortion)	65			dB
DC-level at AD-output	46.5		53.5	%
Threshold of level detect	15		45	mV
Transmit Path				
Signal / (noise + total harmonic distortion)	65			dB
Output DC-level	2.05	2.375	2.6	dB
Offset between AOUT and BOUT			35	mV
Signal amplitude	3.10	3.20	3.30	V
Output impedance AOUT/BOUT: Power-up Power-down			 4 12	 Ω Ω

Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; f_C = 1 MHz

Pin	Parameter	Symbol	Limit Values		Unit
			min.	max.	
All pins except SX1,2, AOUT, BOUT	Pin capacitance	C_{IO}		5	pF
SX1,2	Output capacitance against V_{SS}	C_{OUT}		10	pF
AOUT, BOUT	Output capacitance against V_{SS}	C_{OUT}		27	pF

Power Supply

Supply voltages VDD_D 1-2 = + 5 V ± 0.25 V
VDD_A 1-3 = + 5 V ± 0.25 V

Maximum ripple on VDD_A 1-3 is 50 mV peak-to-peak (in power-up)

9.4 AC Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **Figure 90.**

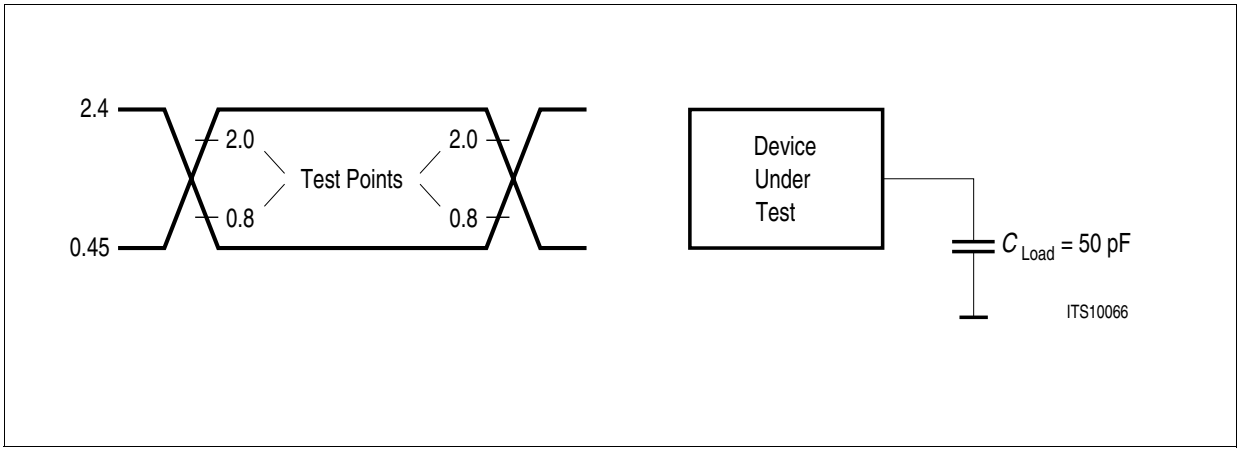


Figure 90 Input/Output Waveform for AC Tests

IOM-1 Interface

Relevant only when IEC-T functionality selected

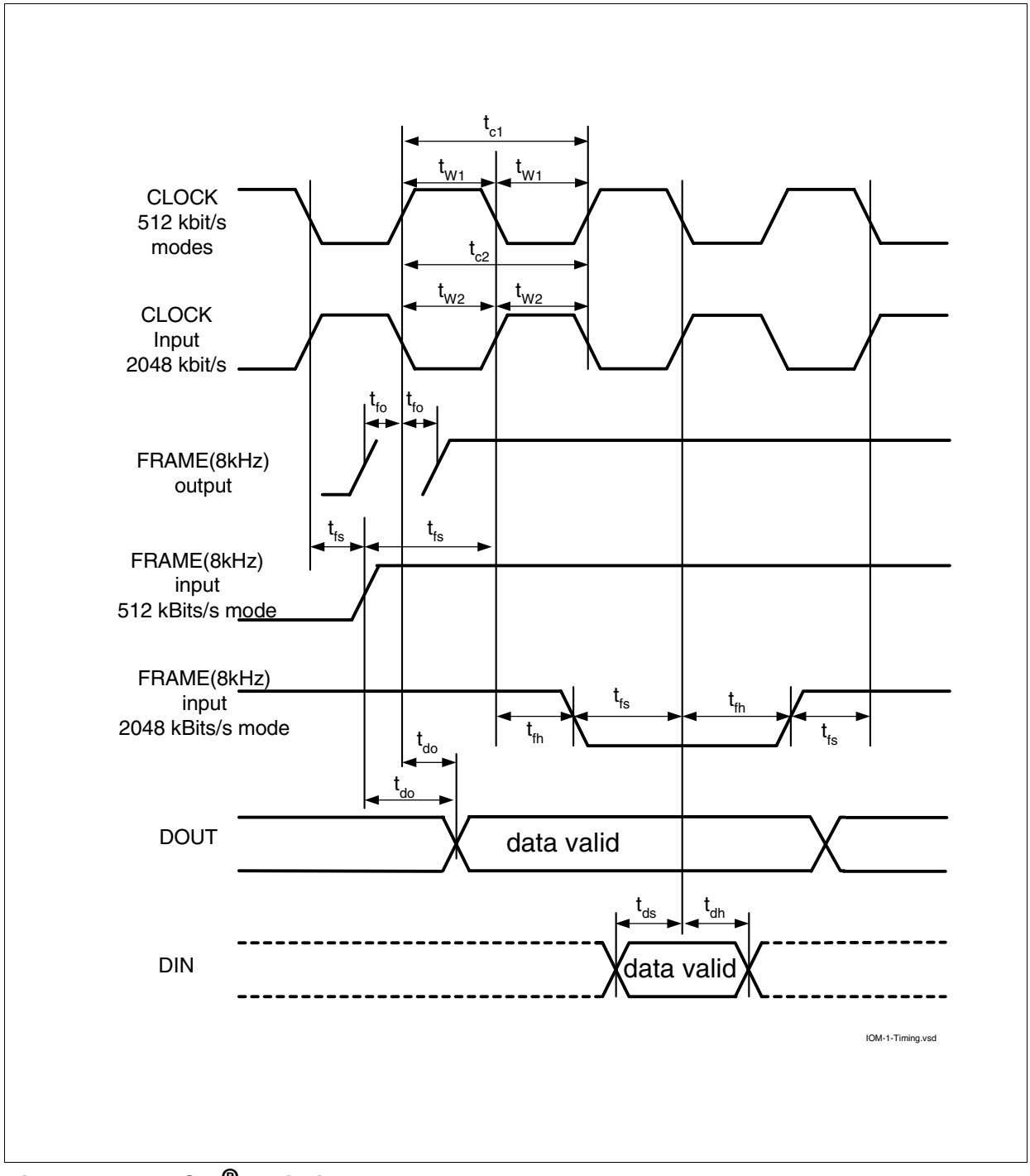


Figure 91 IOM®-1 Timing

Table 19 IOM®-1: Dynamic Input Characteristics

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Rise time	CLOCK, FRAME, DIN, MPF	t_{rise}			30	ns	
Fall time	CLOCK, FRAME, DIN, MPF	t_{fall}			30	ns	
Frame setup time	FRAME	t_{fs}	30			ns	
Frame hold time	FRAME	t_{fh}	30			ns	
Setup time	DIN, MPF	t_{ds}	30			ns	
Hold time	DIN, MPF	t_{dh}	30			ns	
CLOCK high	CLOCK	t_{w1}	100			ns	
CLOCK low	CLOCK	t_{w2}	100			ns	

Table 20 IOM®-1: Dynamic Output Characteristics

Signal	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CLOCK, FRAME, DISS, CLS, RD1, RD2	t_{rise}			30	ns	C = 25pF
CLOCK, FRAME, DISS, CLS, RD1, RD2	t_{fall}			30	ns	C = 25pF
DOUT	t_{fall}	0		200	ns	C = 150pF R = 1kΩ to V_{DD}
CLOCK 512kHz	t_{cl}	1875	1953	2035	ns	C = 25pF
CLOCK 512kHz	t_{w1}	880		1075	ns	C = 25pF
FRAME	t_{fo}	-30		30	ns	C = 25pF
DOUT (high-low transition)	t_{do}	0 0		200 150	ns	C = 150pF R = 1kΩ to V_{DD} C = 50pF R = 1kΩ to V_{DD}

IOM®-2 Interface Timing

Relevant only when NTC-T functionality selected

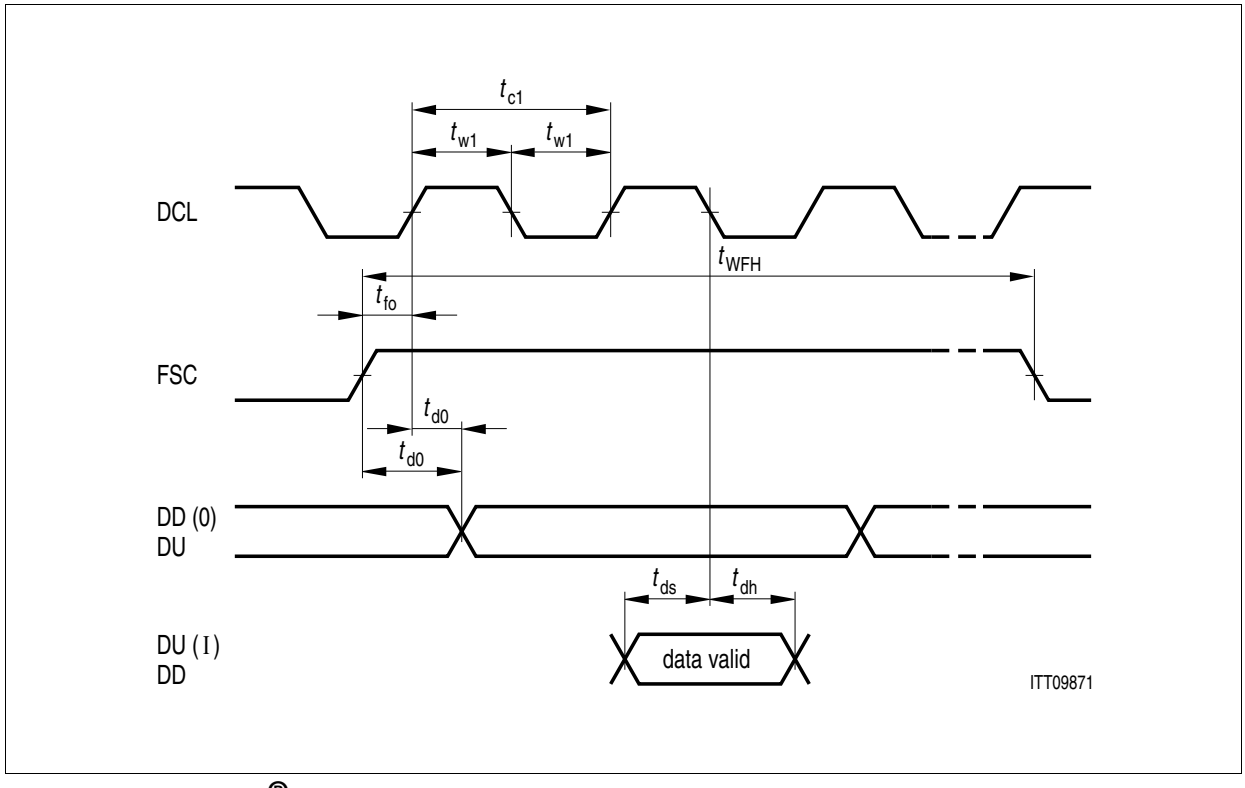


Figure 92 IOM®-2 Timing

Table 21 IOM®-2

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Clock period	DCL	t_{C1}	1875	1953	2035	ns	
Pulse width high/low		t_{w1}	880		1075	ns	
Frame width high	FSC	t_{wFH}		62.5		µs	
Frame advance		t_{f0}	-30	0	30	ns	
Data delay clock	DD/ DU	t_{d0}			100	ns	
Data setup	DU/ DD	t_{ds}	30			ns	
Data hold		t_{dh}	30			ns	

Auxiliary IOM®-2 Interface Timing

Relevant only when NTC-T functionality selected

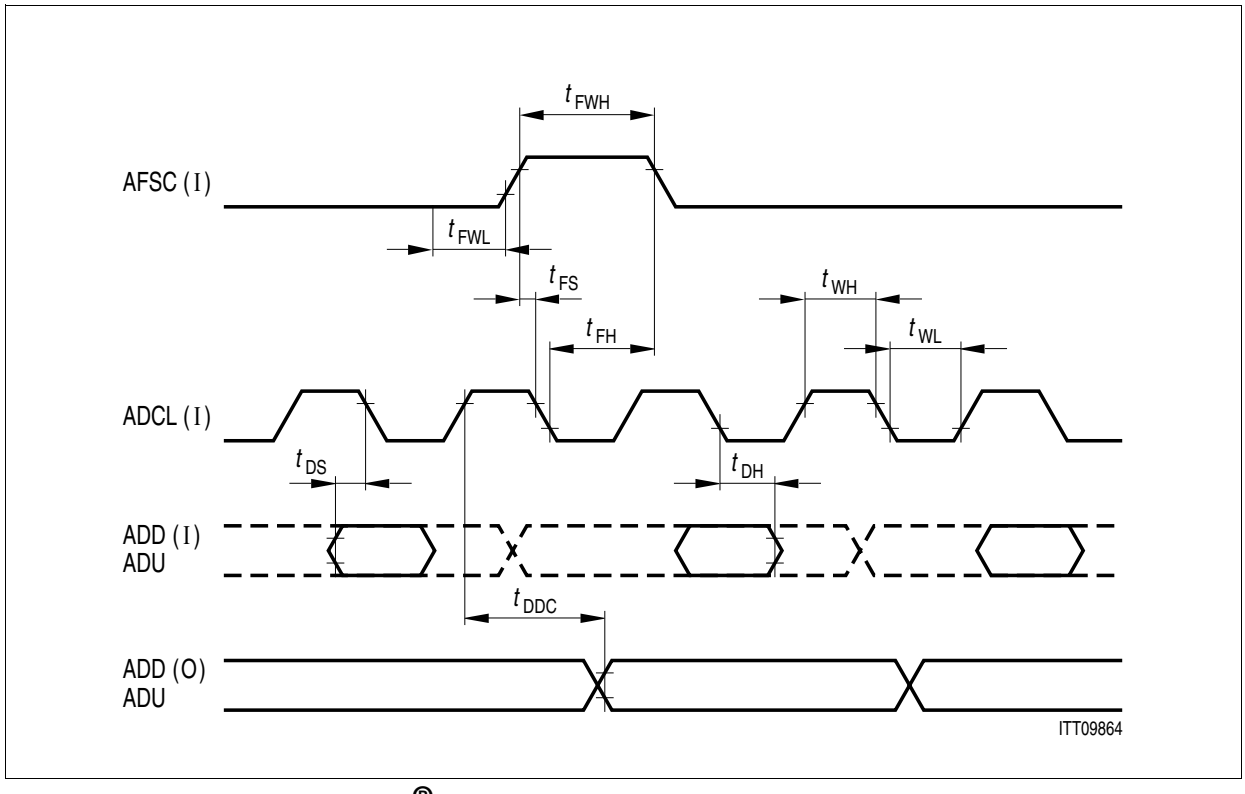


Figure 93 Auxiliary IOM®-2 Timing

Table 22 Auxiliary IOM®-2

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Pulse width high/low	ADCL	t_{WH}, t_{WL}	90			ns	
Frame width high	AFSC	t_{FWH}	130			ns	
Frame width low		t_{FWL}	t_{DCL}			ns	
Frame setup		t_{FS}	70			ns	
Frame hold		t_{FH}	30			ns	
Data delay to clock	ADU/ ADD	t_{DDC}			100	ns	
Data setup	ADD/ ADU	t_{DS}	20			ns	
Data hold		t_{DH}	50			ns	

External Reset Timing

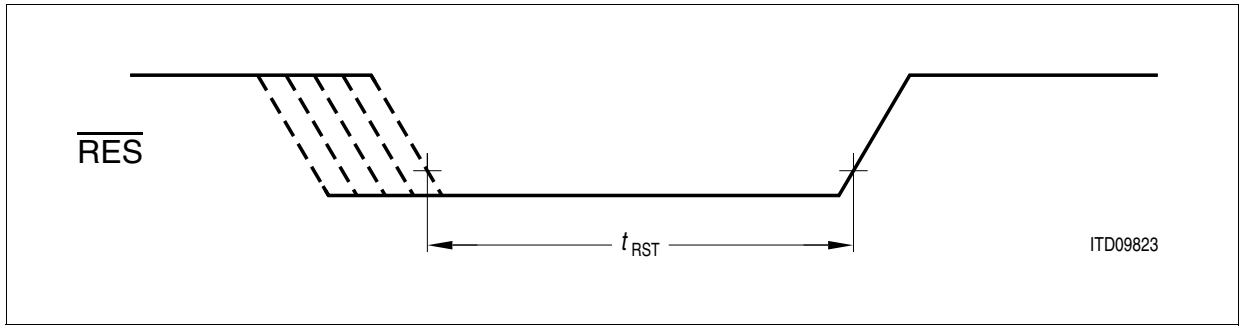


Figure 94 External Reset Timing

Table 23 External Reset Timing

Parameter	Symbol	Limit Values	Unit	Test Conditions
		min.		
Reset at pin $\overline{RES}$/ pin RESQ Active low state	t_{RST}	300	µs	

Undervoltage Detection

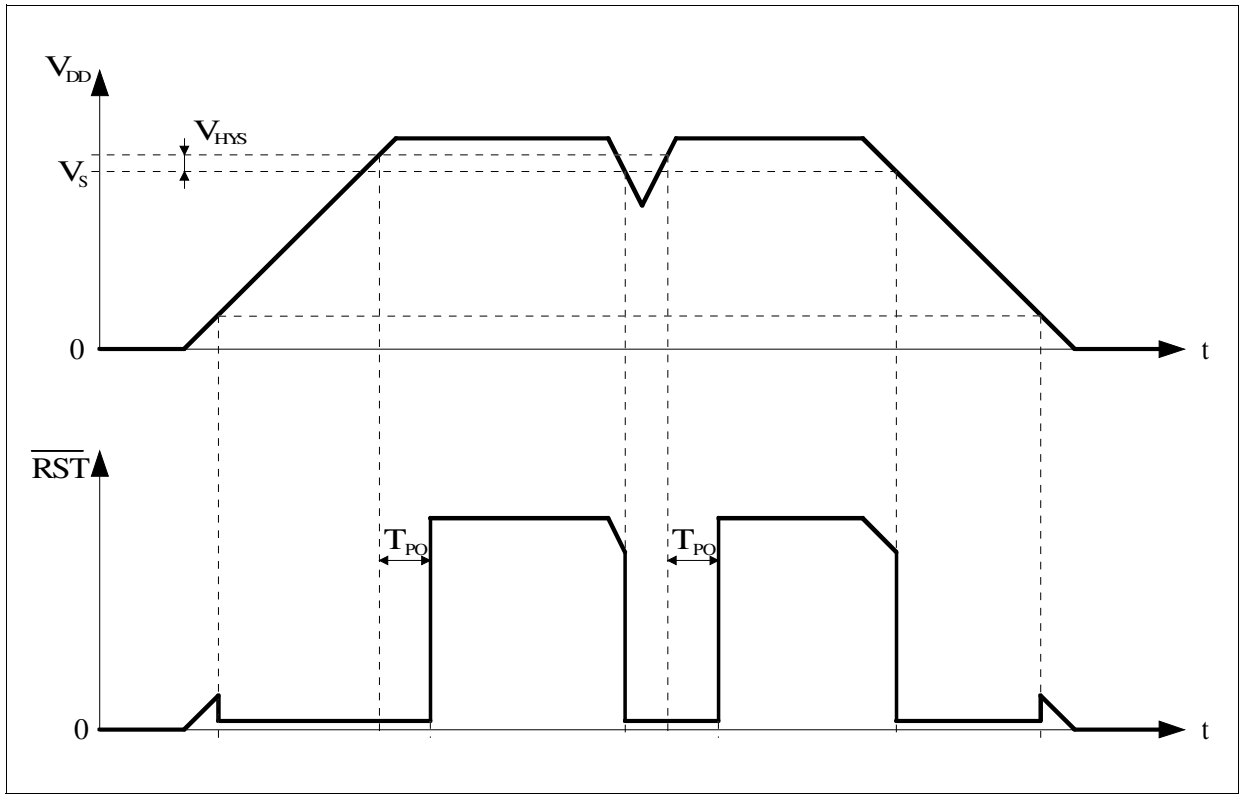


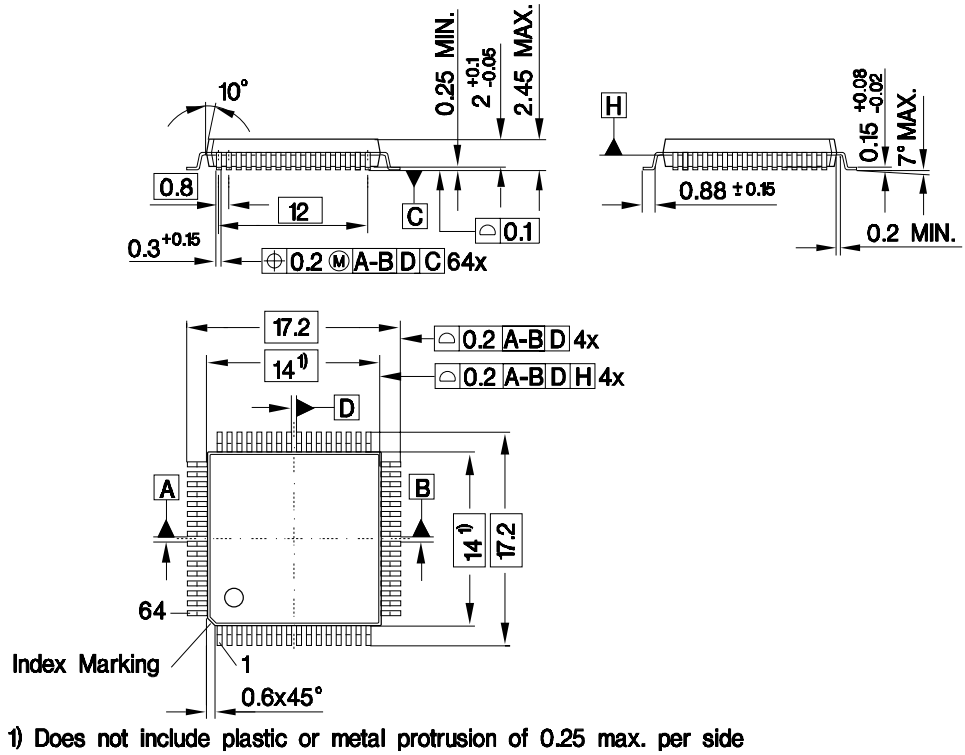
Figure 95 Undervoltage Detection

Table 24 Undervoltage Detection

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reset length	t_{PO}	300			µs	
Hysteresis width	V_{HYS}		65		mV	
Trigger level (V_{DD} falling)	V_S	3.8		4.5	V	

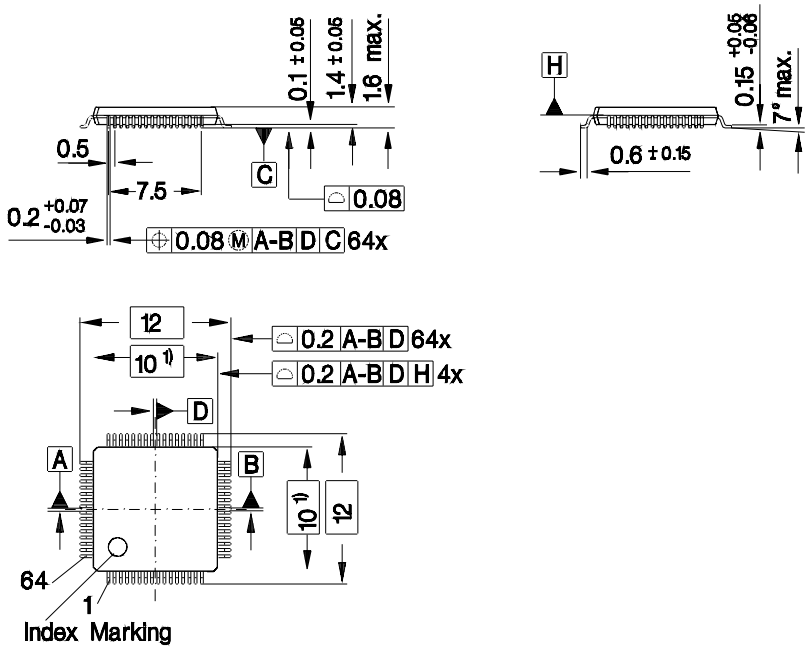
10 Part III 'Common': Package Outlines

Plastic Package, P-MQFP-64
(Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Plastic Package, P-TQFP-64
(Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.
SMD = Surface Mounted Device

Dimensions in mm

11 Part III 'Common': Power Consumption in the Application

Table 25 shows the typical power consumption of the NTC-T AM in an NT1 application. It can be seen how different test conditions such as the loop length of the U-line and the data pattern influence the power consumption of the device.

The lab measurements were done with specific, arbitrarily selected devices on the NT1 Evaluation Board SIPB80900. All measurements were performed at room temperature.

The first row shows the power consumption under typical conditions. Bold letters in the following rows indicate conditions that are different from those in the first row.

Table 25 Power Consumption in a Typical Application

U-Loop	Load on S/T Interface	Data Pattern	V_{DD}	IOM-interface enabled	Power Consumption in mW
ETSI Loop #2 [1]	50 Ω	50% Zeros	5.0 V	no	233
ETSI Loop #1 [2]	50 Ω	50% Zeros	5.0 V	no	246
150 Ω	50 Ω	50% Zeros	5.0 V	no	236
ETSI Loop #2	50 Ω	**100 % Ones**	5.0 V	no	220
ETSI Loop #2	50 Ω	**100 % Zeros**	5.0 V	no	245
ETSI Loop #2	50 Ω	50% Zeros	**4.75 V**	no	212
ETSI Loop #2	50 Ω	50% Zeros	**5.25 V**	no	254
ETSI Loop #2	50 Ω	50% Zeros	5.0 V	**yes [3]**	237

[1] 4400 m, 0.4 mm PE attenuation 35.7 dB
[2] 0kft cable
[3] No output load

12 Part III 'Common': External Component Sourcing

The following tables contain transformers and crystals recommended by different manufacturers for use with Siemens ICs. No manufacturer can be recommended over another.

Until date of print transformers marked with *) have been tested at Siemens Semiconductors and have shown positive test results.

This list is not complete. It contains a few examples of devices offered by different manufacturers. Most manufacturers offer a variety of components with different parameters. For latest information please contact the manufacturers directly or visit their web pages where available.

Note: There may also exist other manufacturers than those included in the list.

Table 26 U-Transformer Information

Part Number	Comments	Contacts (Phone)	Fax
APC			www.apcisdn.com
		EU: +44 1634 2905-88 SEA: +852 2410-2731 US: (201) 368 17-50	**-91** -2518 -04
PulseEngineering			www.pulseeng.com
PE-65578	2 kV, PTH	D: 089-963 046 EU: +44 14834-28877 SEA: +886 78-213141 US: (619) 674 8100	-966626 -16011 -419707 -8262
T4026			
S+MComponents			www.siemens.de/pr
B78386-A1126-A3	2 kV, RM6, SMD	EU: +49 89 636-24265 SEA: +65 744-7768 US: (908)-906 4300	-24112 -6992 -632 2830
B78388-P1310-A5	2 kV, RM8, PTH		
B78388-P1256-A5	4 kV, RM8, PTH		

Table 26 U-Transformer Information (cont'd)

Part Number	Comments	Contacts (Phone)	Fax
Vacuumschmelze			www.vaccorp.com
T6040 3-M6290-X045 *)	2 kV, RM8, PTH	EU: +49 6181-382673 SEA: +65 8404 880 US: (405) 943 9651	-382780
3-M6276-X005 *)	2 kV, RM6, SMD		
7-L5052-X106	2 kV, SMD, Module		
TDK			
		EU: +49 2192 487-0	
Valor			www.valorinc.com
		EU: +44 1727 8248-75 SEA: +852 2 953-1000 US: (619) 537-2500	-98 -1333 -2525
Vogt			www.vogt-electronic.com
544 02 009 00	2 kV, PTH	EU: +49 8591 17-0 SEA: +86 21 6251-2227 US: (914) 921-6900	-240 -4489 -6381
503 20 908 00	2 kV, SMD		

Table 27 S-Transformer Information

Part Number	Comments	Contacts (Phone)	Fax
APC			www.apcisdn.com
APC2040 S		see **Table 26**	
APC1020 S			
APC9018 D			
PulseEngineering			www.pulseeng.com
T5042	3.0 kV, SMD, Dual	see **Table 26**	
T5035	3.0 kV, PTH, Single		
T5015	1.5 kV, PTH, Module		
S+MComponents			www.siemens.de/pr
B78384-A1060-A3	1.5 kV, RM5, SMD	see **Table 26**	
B78384-A1111-A5	0.5 kV, RM5, PTH		
B78510-A1223-A5	2.0 kV, R10, SMD		
Vacuumschmelze			www.vaccorp.com
T6040 3-L5024-X028	1.5 kV, SMD	see **Table 26**	
3-L4097-X011 *)	3.0 kV, PTH		
7-L5052-X102 *)	2.0 kV, SMD, Module		
TDK			
		see **Table 26**	
Valor			www.valorinc.com
PT 5001		see **Table 26**	
PT 5069			
ST 5069			
Vogt			www.vogt-electronic.com

Table 27 S-Transformer Information (cont'd)

Part Number	Comments	Contacts (Phone)	Fax
503 10 009 00	1.5 kV, SMD	see Table 26	
503 20 019 00	4.0 kV, SMD		
503 75 002 00	2.0 kV, SMD, Module		

Table 28 Crystal Information

Part Number	Comments	Contacts (Phone)	Fax
FrischerElectronic			
		EU: +49 9131-33007	
KVG			
		EU: +49 7263 648-0	
Tele Quarz			
		EU: +49 7268 8010	

13 Part III 'Common': Glossary

A/D	Analog-to digital
ADC	Analog-to digital converter
AGC	Automatic gain control
AIN	Differential U-interface input
ARCOFI	Audio ringing codec filter
AOUT	Differential U-interface output
B	64-kbit/s voice and data transmission channel
BIN	Differential U-interface input
BOUT	Differential U-interface output
C/I	Command/Indicate (channel)
CCITT	Comité Consultatif International des Téléphones et Télégraph
D	16-kbit/s data and control transmission channel
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DCL	Data clock
DD	Data downstream
DU	Data upstream
EC	Echo canceller
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETSI	European Telephone Standards Institute
FSC	Frame synchronizing clock
GND	Ground
IEC-T	ISDN-echo cancellation circuit conforming to 4B3T-transmission code
IOM-2	ISDN-oriented modular 2nd generation
INFO	U- and S-interface signal as specified by ETSI
ISDN	Integrated services digital network
LSB	Least significant bit
LT	Line termination
MON	Monitor channel command
MSB	Most significant bit
NT	Network termination
OSI	Open systems interconnection
PLL	Phase locked loop
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up
RMS	Root mean square
RP	Repeater
S/T	Two-wire pair interface
SBCX	S/T-bus interface circuit extended

SICOFI	Signal processing codec filter
SLIC	Subscriber line interface circuit
SSP	Send single pulses (test mode)
TE	Terminal equipment
TP	Test pin
U	Single wire pair interface

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

http://www.infineon.com

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