



3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS, BUS-HOLD, 5V TOLERANT I/O

IDT74LVCH16901 ADVANCE INFORMATION

FEATURES:

- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.50mm pitch TSSOP package
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH16901:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

This 18-bit universal bus transceiver is built using advanced dual metal

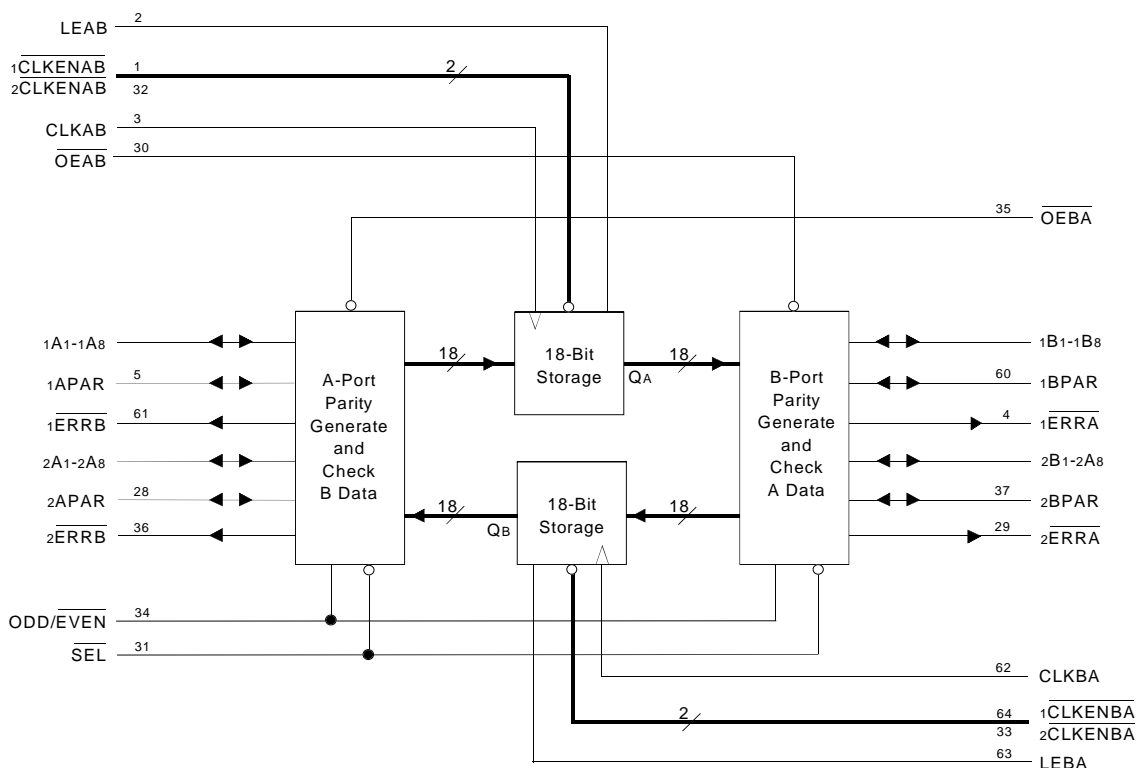
CMOS technology. The LVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

The LVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock enable ($\overline{CLKENAB}$ or $\overline{CLKENBA}$) inputs. It also provides parity-enable (\overline{SEL}) and parity-select (ODD/EVEN) inputs and separate error-signal (\overline{ERRA} and \overline{ERRB}) outputs for checking parity. The direction of data flow is controlled by \overline{OEAB} and \overline{OEBA} . When \overline{SEL} is low, the parity functions are enabled. When \overline{SEL} is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16901 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16901 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

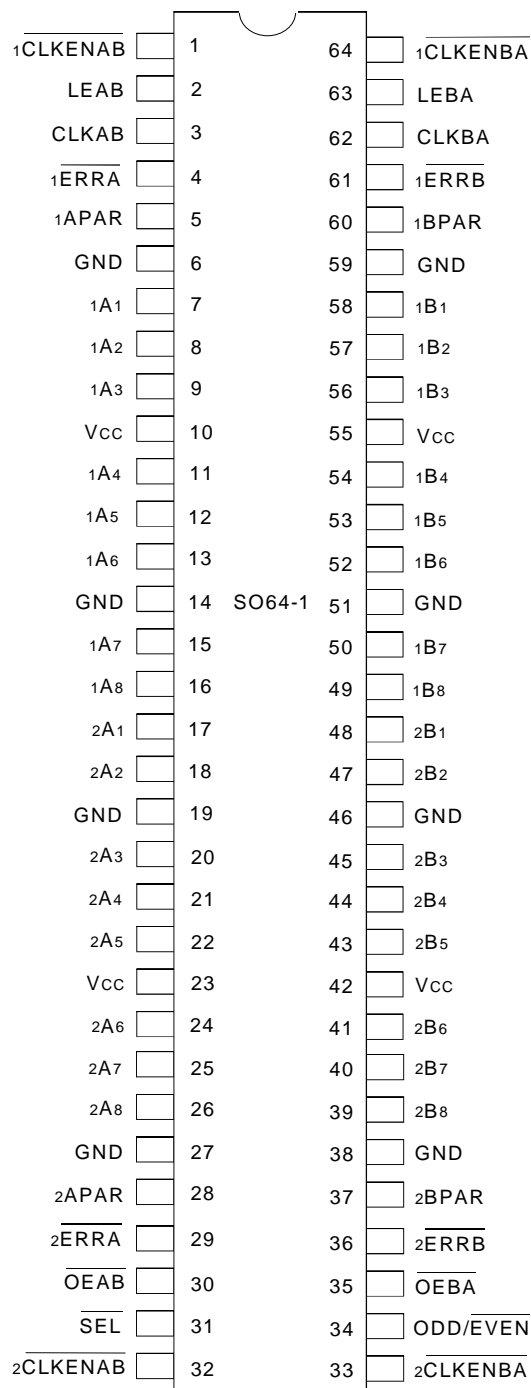
FUNCTIONAL BLOCK DIAGRAM



EXTENDED COMMERCIAL TEMPERATURE RANGE

OCTOBER 1999

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
IOUT	DC Output Current	- 50 to +50	mA
I _{IK}	Continuous Clamp Current, V _i < 0 or V _o < 0	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA

LVC Link

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

LVC Link

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{xCLKENAB}$	A-to-B 9-bit Clock Enables
$\overline{xCLKENBA}$	B-to-A 9-bit Clock Enables
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
\overline{xERRA}	A Error-Signal Outputs
\overline{xERRB}	B Error-Signal Outputs
xAPAR	A Port Parities
xBPAR	B Port Parities
$\overline{ODD/EVEN}$	Parity Select Input
SEL	Parity Enables
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (1,2)

Inputs					Outputs
CLKENAB	OEAB	LEAB	CLKAB	xAx	xBx
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ ⁽³⁾
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ ⁽³⁾
L	L	L	H	X	B ₀ ⁽⁴⁾

PARITY ENABLE

Inputs			Operation or Function	
SEL	OEBA	OEAB		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are disabled; device acts as a standard 18 bit registered transceiver.	QA data to B, QB data to A
H	L	H		QB data to A
H	H	L		QA data to B
H	H	H		Isolation

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKENBA.
2. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.

PARITY

Inputs							Outputs				
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1–A8 = H	Σ OF INPUTS B1–B8 = H	xAPAR	xBPAR	xAPAR	xERRA	xBPAR	xERRB
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	H	Z	H
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE(1)	Z	PE(1)	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO(2)	Z	PO(2)	Z

NOTES:

1. Parity output is set to the level so that the specific bus side is set to even parity.
2. Parity output is set to the level so that the specific bus side is set to odd parity.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V other inputs at V _{CC} or GND		—	—	500	μA

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NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHNO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

LVC Link

NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = - 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to +85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 1.8V	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	37	52	68	pF
CPD	Power Dissipation Capacitance Outputs disabled		16	22	28	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 1.8V	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Typical	Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		125	125	—	125	—	125	—	MHz
t _{PLH} t _{PHL}	Propagation Delay xAx to xBx or xBx to xAx	5.9	1	6.2	—	5.8	1	5.4	ns
t _{PLH} t _{PHL}	Propagation Delay xAx to xBPAR or xBx to xAPAR	12.7	2	9.9	—	8.6	2	7.7	ns
t _{PLH} t _{PHL}	Propagation Delay xAPAR to xBPAR or xBPAR to xAPAR	7	1	6.7	—	6.2	1	5.7	ns
t _{PLH} t _{PHL}	Propagation Delay xAPAR to \overline{xERRA} or xBPAR to \overline{xERRB}	13	2	10.7	—	9.7	2	8.5	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{ODD/EVEN}$ to \overline{xERRB} or \overline{xERRA}	9.9	1.5	9.7	—	8.9	1.5	7.8	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{ODD/EVEN}$ to xAPAR or xBPAR	10.4	1.5	9.3	—	8.6	1.5	7.5	ns
t _{PLH} t _{PHL}	Propagation Delay \overline{SEL} to xAPAR or xBPAR	6.9	1	7.1	—	6.9	1	6.1	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to xAx or LEAB to xBx	6.8	1	7	—	6.5	1	5.8	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to xAPAR or LEAB to xBPAR (parity feed through)	7.9	1.5	7.7	—	7	1.5	6.3	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to xAPAR or LEAB to xBPAR (parity generated)	13.6	2.5	10.8	—	9.3	2	8.4	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to \overline{xERRB} or LEAB to \overline{xERRA}	13.5	2.5	10.9	—	9.5	2	8.5	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to xAx or CLKAB to xBx	6.9	1	7.4	—	6.8	1	6.1	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to xAPAR or CLKAB to xBPAR (parity feed through)	8.5	1.5	8.1	—	7.3	1.5	6.6	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to xAPAR or CLKAB to xBPAR (parity generated)	14.1	2.5	11.2	—	9.7	2	8.7	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to \overline{xERRB} or CLKAB to \overline{xERRA}	14.3	2.5	11.5	—	9.9	2	8.9	ns

(CONTINUED ON NEXT PAGE)

SWITCHING CHARACTERISTICS (CONTINUED) ⁽¹⁾

Symbol	Parameter	V _{CC} = 1.8V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PZH} t _{PZL}	Output Enable Time \overline{OEAB} or \overline{OEBA} to xBx, xBPAR or xAx, xAPAR	—	6.8	1.4	7.3	—	7.1	1	6.3	ns
t _{PZH} t _{PZL}	Output Enable Time \overline{OEAB} or \overline{OEBA} to \overline{xERRA} or \overline{xERRB}	—	7.4	1.4	7.2	—	6.5	1	5.9	ns
t _{PZH} t _{PZL}	Output Enable Time \overline{SEL} to \overline{xERRA} or \overline{xERRB}	—	7.6	1.4	7.7	—	7.5	1	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OEAB} or \overline{OEBA} to xBx, xBPAR or xAx, xAPAR	—	6.9	1.3	7.1	—	6.2	1.5	5.9	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OEAB} or \overline{OEBA} to \overline{xERRA} or \overline{xERRB}	—	9.3	1.3	8.3	—	7.5	1	6.7	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{SEL} to \overline{xERRA} or \overline{xERRB}	—	7.8	1.3	7.4	—	6.4	1.5	5.9	ns
t _{SU}	Set-up Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR before CLK↑	4.7	—	2.7	—	2.8	—	2.5	—	ns
t _{SU}	Set-up Time, HIGH or LOW, $\overline{xCLKENAB}$ or $\overline{xCLKENBA}$ before CLK↑	4.5	—	2.9	—	2.9	—	2.5	—	ns
t _{SU}	Set-up Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR before LE↓	0	—	2.2	—	2.1	—	2	—	ns
t _H	Hold Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR after CLK↑	0	—	1.2	—	1.2	—	1.3	—	ns
t _H	Hold Time, HIGH or LOW, $\overline{xCLKENAB}$ or $\overline{xCLKENBA}$ after CLK↑	0	—	1.3	—	1.3	—	1.5	—	ns
t _H	Hold Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR after LE↓	1	—	1.7	—	1.9	—	1.7	—	ns
t _w	Pulse Width LEAB or LEBA HIGH	3	—	3	—	3	—	3	—	ns
t _w	Pulse Width CLKAB or CLKBA HIGH or LOW	4	—	3	—	3	—	3	—	ns
t _{sk(o)}	Output Skew ⁽²⁾	—	—	—	—	—	—	—	500	ps

NOTES:

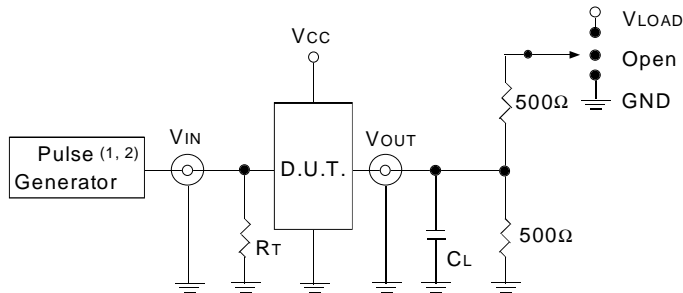
1. See test circuits and waveforms. T_A = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ± 0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

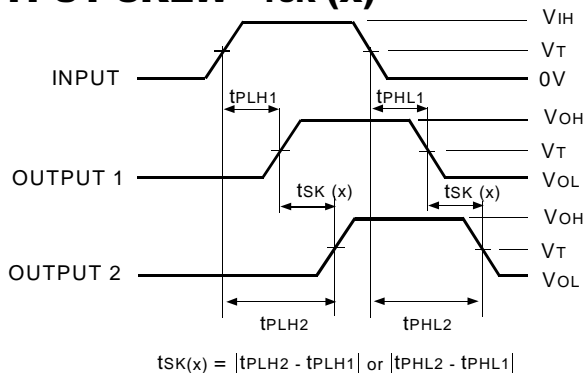
NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

OUTPUT SKEW - T_{SK} (x)

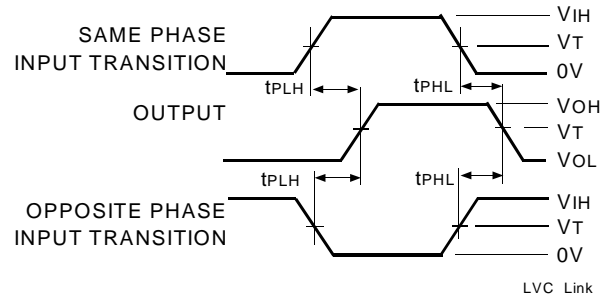


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

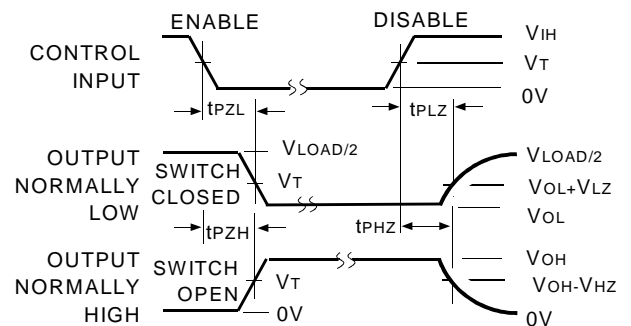
NOTES:

1. For t_{sk(o)} OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{sk(b)} OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



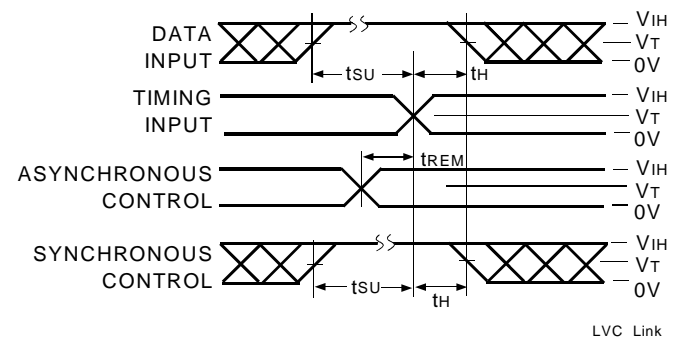
ENABLE AND DISABLE TIMES



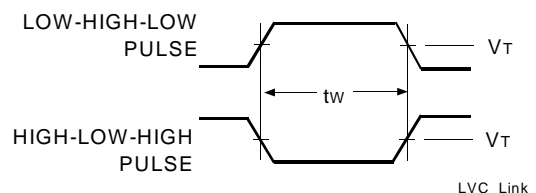
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



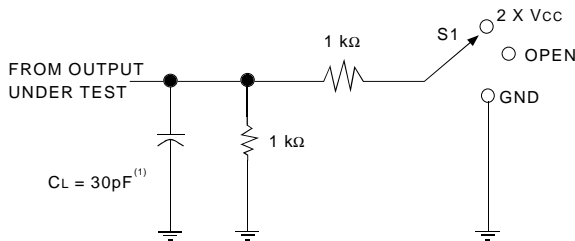
PULSE WIDTH



PARAMETER MEASUREMENT INFORMATION

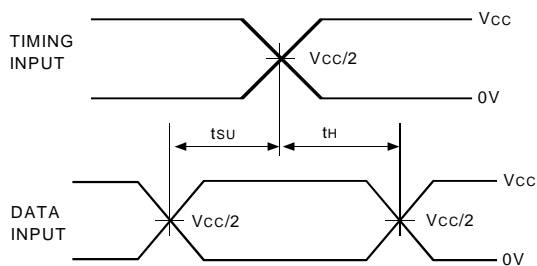
V_{CC} = 1.8V

LOAD CIRCUIT

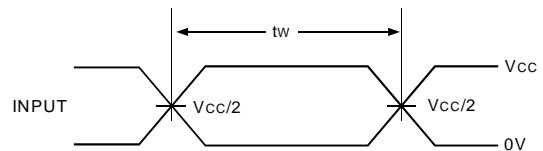


TEST	S1
t _{PD}	Open
t _{PLZ} /t _{PZL}	2 x V _{CC}
t _{PHZ} /t _{PZH}	GND

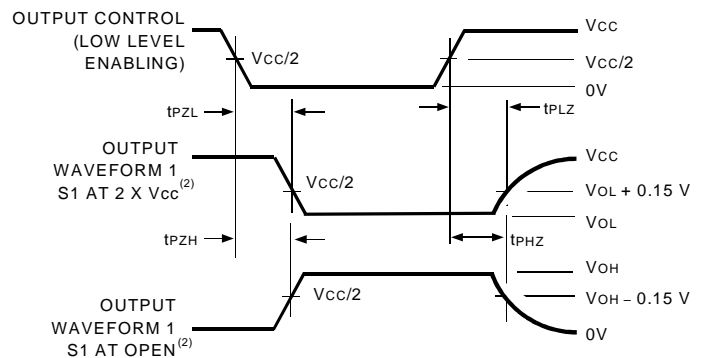
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



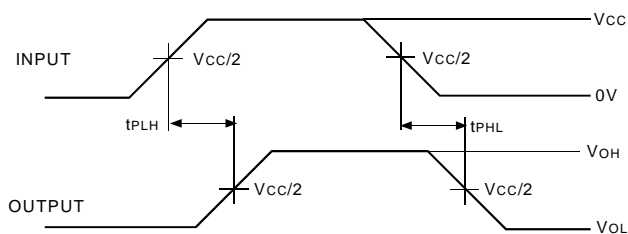
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



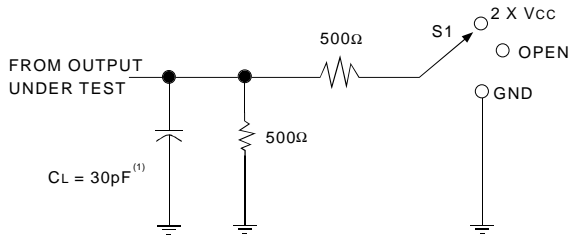
NOTES:

- CL includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_o = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{DIS}.
- t_{PZL} and t_{PZH} are the same as t_{EN}.
- t_{PLH} and t_{PHL} are the same as t_{PD}.

PARAMETER MEASUREMENT INFORMATION

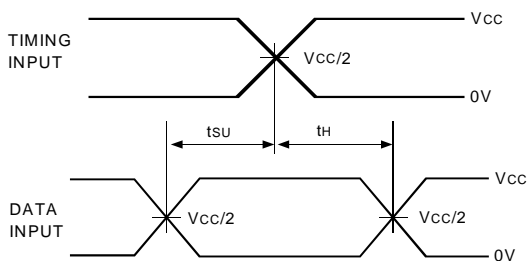
$V_{CC} = 2.5V \pm 0.2V$

LOAD CIRCUIT

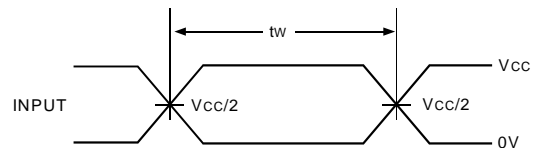


TEST	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

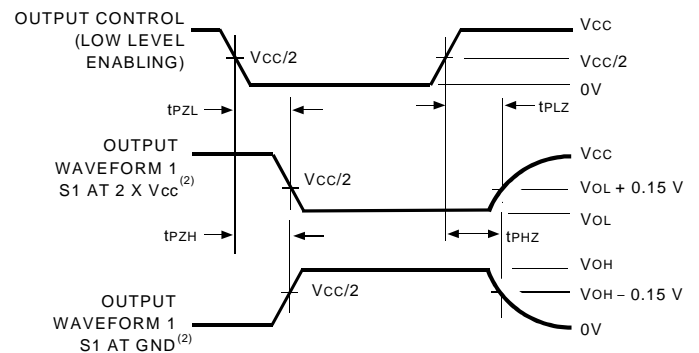
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



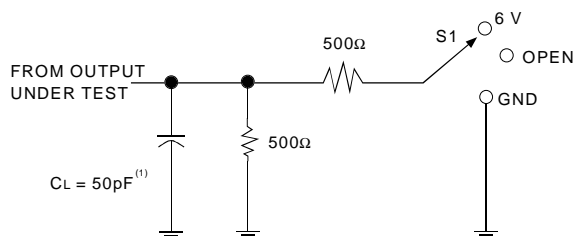
NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz$, $Z_o = 50\Omega$, $t_r \leq 2ns$, $t_f \leq 2ns$.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{DIS} .
6. t_{PZL} and t_{PZH} are the same as t_{EN} .
7. t_{PLH} and t_{PHL} are the same as t_{PD} .

PARAMETER MEASUREMENT INFORMATION

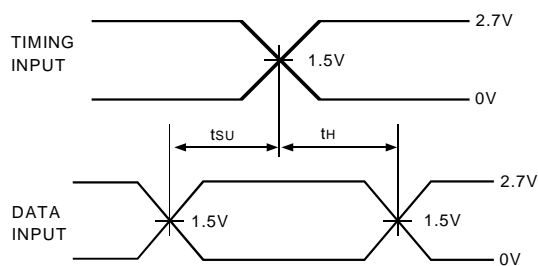
$V_{CC} = 2.7V$ and $3.3V \pm 0.3V$

LOAD CIRCUIT

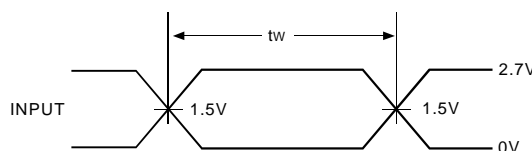


TEST	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

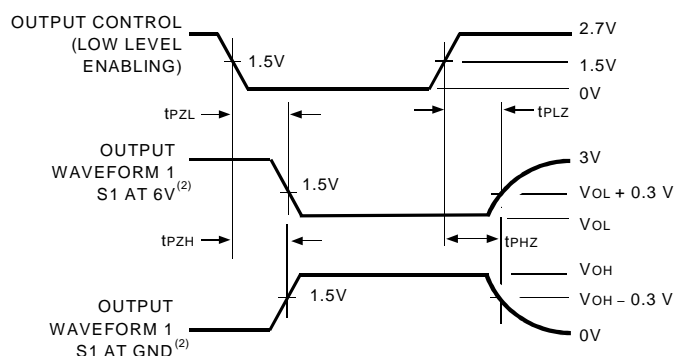
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



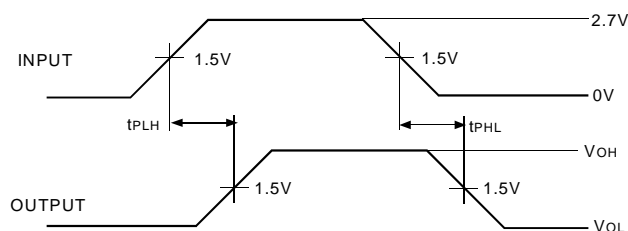
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



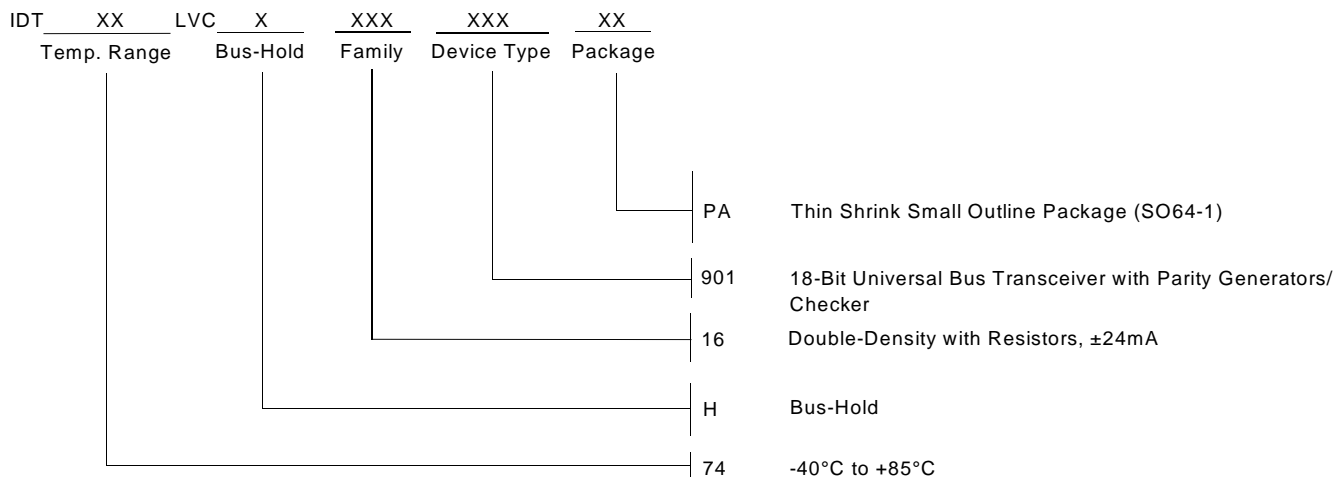
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



NOTES:

- CL includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz$, $Z_o = 50\Omega$, $t_r \leq 2ns$, $t_f \leq 2ns$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{DIS} .
- t_{PZL} and t_{PZH} are the same as t_{EN} .
- t_{PLH} and t_{PHL} are the same as t_{PD} .

ORDERING INFORMATION



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