Integrated Circuit Systems, Inc.

ICS9248-189

Advance Information

AMD - K7™ Clock Generator for Mobile System

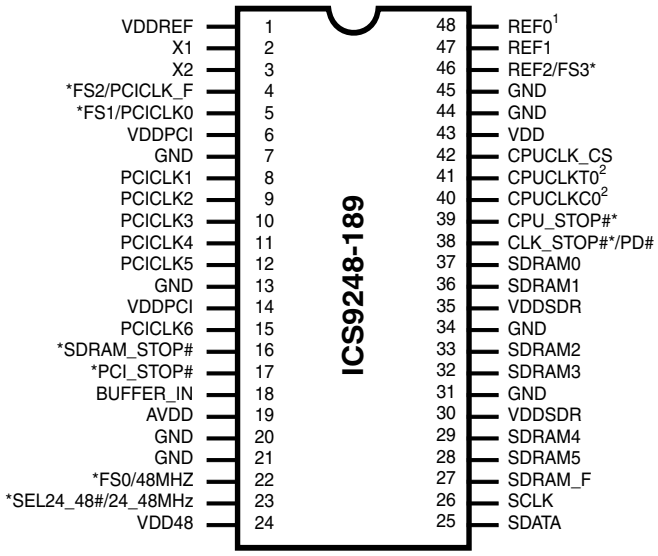
Recommended Application:
VIA K7/KN/KX-133 style chipset

Output Features:
- 1 - Differential pair open drain CPU clocks
- 1 - CPU clock @ 3.3V
- 7 - SDRAM @ 3.3V
- 8 - PCI @ 3.3V,
- 1 - 48MHz, @ 3.3V fixed
- 1 - 24/48MHz @ 3.3V
- 3 - REF @ 3.3V, 14.318MHz.

Features:
- Up to 166MHz frequency support
- Support power management via hardware select CPU stop, CLOCK stop, PCI stop, and SDRAM stop
- Support power management via I^2C programing
- Spread spectrum for EMI control (± 0.25% to ± 0.06% center, or 0 to -0.5% or -1.0% down spread)
- Uses external 14.318MHz crystal

Key Specifications:
- CPU - CPU Skew: <175ps
- CPU - SDRAM Skew: ±125ps
- CPU - PCI Skew: ±100ps
- PCI - PCI Skew: <500ps

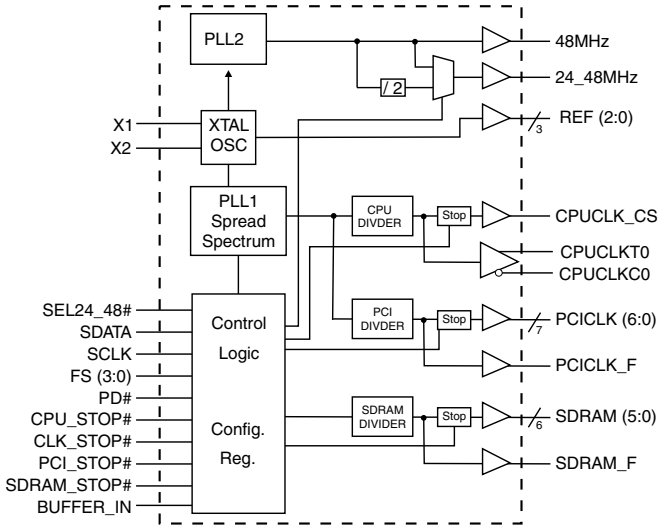
Pin Configuration



48-Pin 300mil SSOP & 240mil TSSOP

* Internal Pull-up Resistor of 120K to VDD
1 These outputs have double strength to drive 2 loads.
2 These outputs can be set to 1X or 1.5X strength through I^2C

Block Diagram



Functionality

FS2	FS1	FS0	CPU	PCI	Spread Percentage
0	0	0	100.00	33.33	+/- 0.35% Center Spread
0	0	1	133.33	33.33	+/- 0.35% Center Spread
0	1	0	100.00	33.33	0 to - 0.5% Down Spread
0	1	1	133.33	33.33	0 to - 0.5% Down Spread
1	0	0	100.00	33.33	+/- 0.6% Center Spread
1	0	1	133.33	33.33	+/- 0.6% Center Spread
1	1	0	100.00	33.33	No Spread
1	1	1	133.33	33.33	No Spread

Note: For a complete functionality table please see table in page 3.

Power Groups

VDD48 = 48MHz, Fixed PLL
VDDA = VDD for Core PLL
VDDREF = REF, Xtal

ICS9248-189

Advance Information

General Description

The **ICS9248-189** is a main clock synthesizer chip for AMD-K7 based note book systems with VIA style chipset. This provides all clocks required for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-189 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 6, 14, 24, 30, 35, 43	VDD	PWR	Power supply, nominal 3.3V
2	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2.
3	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (36pF).
4	FS2[1, 2]	IN	Frequency select pin, latched input
	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
5	FS1[1, 2]	IN	Frequency select pin, latched input
	PCICLK0	OUT	PCI clock output
7, 13, 21, 31, 34, 44, 45	GND	PWR	Ground
15, 12, 11, 10, 9, 8	PCICLK (6:1)	OUT	PCI clock outputs
16	SDRAM_STOP#[1]	IN	Stops all SDRAMs besides the SDRAM_F clocks at logic 0 level, when input low.
17	PCICLK_STOP#[1]	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low.
18	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
19	AVDD	PWR	Supply for core, & CPU 3.3V
20	AGND	PWR	Analog ground
22	FS0[1, 2]	IN	Frequency select pin, latched input
	48MHz	OUT	48MHz output clock
23	SEL24_48#[1, 2]	IN	Logic input to select 24 or 48MHz
	24_48MHz	OUT	24MHz/48MHz clock output
25	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
26	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
27	SDRAM_F	OUT	Free running SDRAM clock not affected by SDRAM_STOP# for power management.
28, 29, 32, 33, 36, 37	SDRAM (5:0)	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset).
38	CLK_STOP#[1]	IN	Powers down chip, active low except XTAL and CPUCLK_T0 & CPUCLKC0.
	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
39	CPU_STOP#[1,]	IN	Only stops CPUCLK_CS
40	CPUCLKC0	OUT	"Complementary" clock of differential pair CPU output. This open drain outputs needs an external 1.5V pull-up.
41	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
42	CPUCLK_CS	OUT	CPU clock to the chipset
46	REF2	OUT	14.318 Mhz reference clock
	FS3[1, 2]	IN	Frequency select pin, latched Input
47, 48	REF0 (1:0)	OUT	14.318 Mhz reference clock

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Serial Configuration Command Bitmap

Functionality and Frequency Select Register (default = 0)

Bit	Description								PWD
	Bit 2	Bit 1	Bit 6	Bit 5	Bit 4	CPUCLK (MHz)	PCICLK (MHz)	Spread Precentage	
Bit 2:1, Bit 6:4	0	0	0	0	0	166.00	41.6	OFF	Reserved 00101
	0	0	0	0	1	160.00	40.0	OFF	
	0	0	0	1	0	155.00	38.7	OFF	
	0	0	0	1	1	150.00	37.5	OFF	
	0	0	1	0	0	145.00	36.2	OFF	
	0	0	1	0	1	140.00	35.0	OFF	
	0	0	1	1	0	136.00	34.00	OFF	
	0	0	1	1	1	130.00	32.5	OFF	
	0	1	0	0	0	127.00	31.7	OFF	
	0	1	0	0	1	124.00	31.00	OFF	
	0	1	0	1	0	120.00	40.00	OFF	
	0	1	0	1	1	118.00	39.3	OFF	
	0	1	1	0	0	116.00	38.60	OFF	
	0	1	1	0	1	115.00	38.30	OFF	
	0	1	1	1	0	114.00	38.00	OFF	
	0	1	1	1	1	113.00	37.60	OFF	
	1	0	0	0	0	112.00	37.30	OFF	
	1	0	0	0	1	111.00	37.00	OFF	
	1	0	0	1	0	110.00	36.60	OFF	
	1	0	0	1	1	108.00	36.00	OFF	
	1	0	1	0	0	106.00	35.30	OFF	
	1	0	1	0	1	104.00	34.60	OFF	
	1	0	1	1	0	102.00	34.00	OFF	
	1	0	1	1	1	95.00	31.70	OFF	
	1	1	0	0	0	100.00	33.33	+/- 0.35% Center Spread	
	1	1	0	0	1	133.33	33.33	+/- 0.35% Center Spread	
	1	1	0	1	0	100.00	33.33	0 to - 0.50% Down Spread	
	1	1	0	1	1	133.33	33.33	0 to - 0.50% Down Spread	
	1	1	1	0	0	100.00	33.33	+/- 0.60% Center Spread	
	1	1	1	0	1	133.33	33.33	+/- 0.60% Center Spread	
	1	1	1	1	0	100.00	33.33	OFF	
	1	1	1	1	1	133.33	33.33	OFF	

Note: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Byte 0: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	38	0	CLK_STOP# (1 = PD#, 0 = CLK_STOP#)
Bit 6	4	0	FS2
Bit 5	5	0	FS1
Bit 4	22	0	FS0
Bit 3	-	0	Hardware / Software Frequency selection
Bit 2	-	1	Reserved
Bit 1	46	0	FS3
Bit 0	-	0	Reserved

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	40, 41	1	CPUCLKC0/T0 (1 = 1X, 0 = 1.5X)
Bit 2	42	1	CPUCLK_CS
Bit 1	41	1	CPUCLKT0
Bit 0	40	1	CPUCLKC0

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	15	1	PCICLK6
Bit 6	12	1	PCICLK5
Bit 5	11	1	PCICLK4
Bit 4	10	1	PCICLK3
Bit 3	9	1	PCICLK2
Bit 2	8	1	PCICLK1
Bit 1	5	1	PCICLK0
Bit 0	4	1	PCICLK_F

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	23	0	SEL24_48#
Bit 5	22	1	48MHz
Bit 4	23	1	24_48MHz
Bit 3	27	1	SDRAM_F
Bit 2	28, 29	1	SDRAM(5:4)
Bit 1	32, 33	1	SDRAM(3:2)
Bit 0	36, 37	1	SDRAM(1:0)

Byte 4: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	22	X	FS0 (readback)
Bit 6	5	X	FS1 (readback)
Bit 5	4	X	FS2 (readback)
Bit 4	46	X	FS3 (readback)
Bit 3	23	X	SEL24_48# (readback)
Bit 2	46	1	REF2
Bit 1	47	1	REF1
Bit 0	48	1	REF0

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

Note: Don't write into this register, writing into this register can cause malfunction

Byte 7: Peripheral , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

Absolute Maximum Ratings

Supply Voltage 5.5V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			180	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz				
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133MHz				
Input frequency	F_i	V_{DD} = 3.3 V;	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$t_{CPU-SDRAM}$	V_T = 50%	-125		125	ps
	$t_{CPU-PCI}$		-100		100	
	$t_{CPU-AGP}$		-500		500	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - USB or 48MHz, REF

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKT0/CPUCLKC0 (Open Drain)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$				Ω
Output High Voltage	V_{OH2B}	Termination to $V_{pull-up(external)}$	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to $V_{pull-up(external)}$			0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18			mA
Rise Time[1]	t_{r2B}	V_{OL} = 0.3 V, V_{OH} = 1.2 V			0.9	ns
Fall Time[1]	t_{f2B}	V_{OH} = 1.2 V, V_{OL} = 0.3 V			0.9	ns
Differential voltage-AC[1]	V_{DIF}	Note 2	0.4		$V_{pullup(external)}$ + 0.6	V
Differential voltage-DC[1]	V_{DIF}	Note 2	0.2		$V_{pullup(external)}$ + 0.6	V
Differential Crossover Voltage[1]	V_X	Note 3	550		1100	mV
Duty Cycle[1]	d_{t2B}	V_T = 50%	45		55	%
Skew[1]	t_{sk2B}	VT = 50%			200	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$			250	ps
Jitter, Absolute[1]	t_{jabs2B}	VT = 50%	-250		+250	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V_{DIF} specifies the minimum input differential voltages (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.

3 - $Vpullup_{(external)}$ = 1.5V, Min = $Vpullup_{(external)}$/2-150mV; Max=($Vpullup_{(external)}$/2)+150mV

Electrical Characteristics - CPUCLK_CS

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V			1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V			1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V			150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250		+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-16	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	19			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Skew[1] (window)	T_{sk}[1]	VT = 1.5V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_F

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	12			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Skew[1](window)	T_{sk}[1]	VT = 1.5V			200	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V			0.5	ns
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

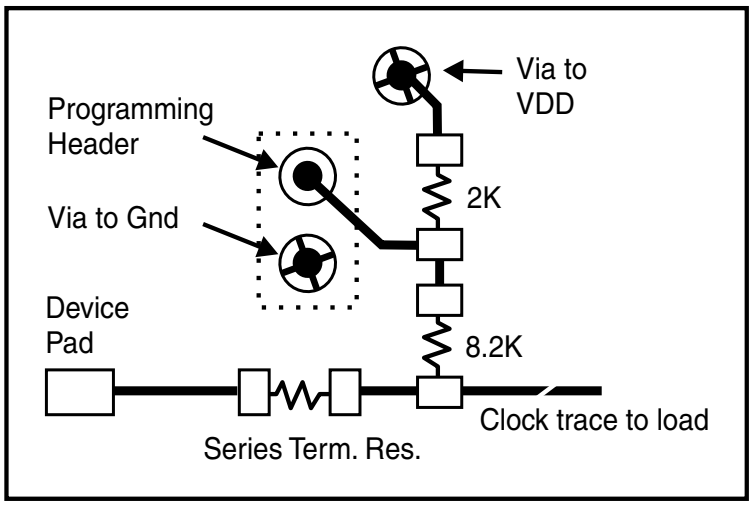
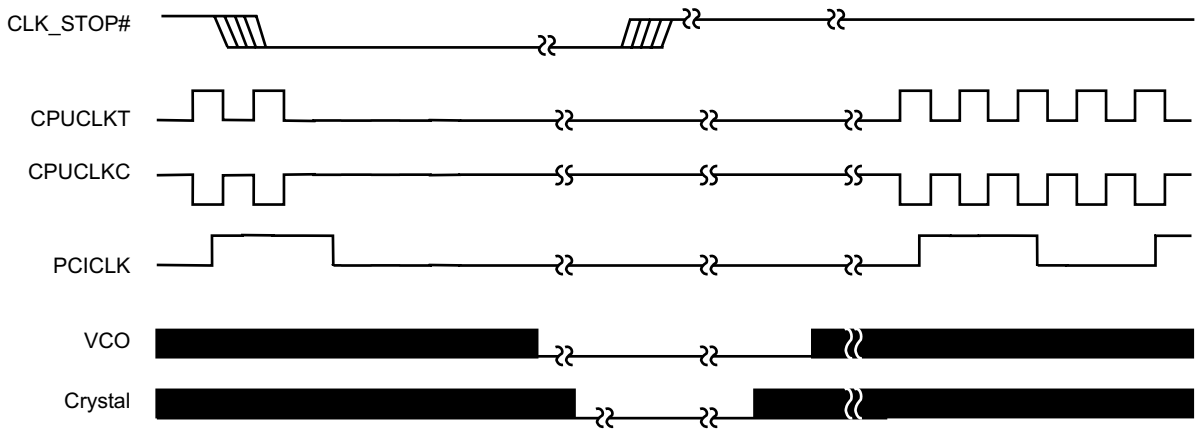


Fig. 1

CLK_STOP# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. CLK_STOP# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When CLK_STOP# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. CPU_STOP# is considered to be a don't care during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

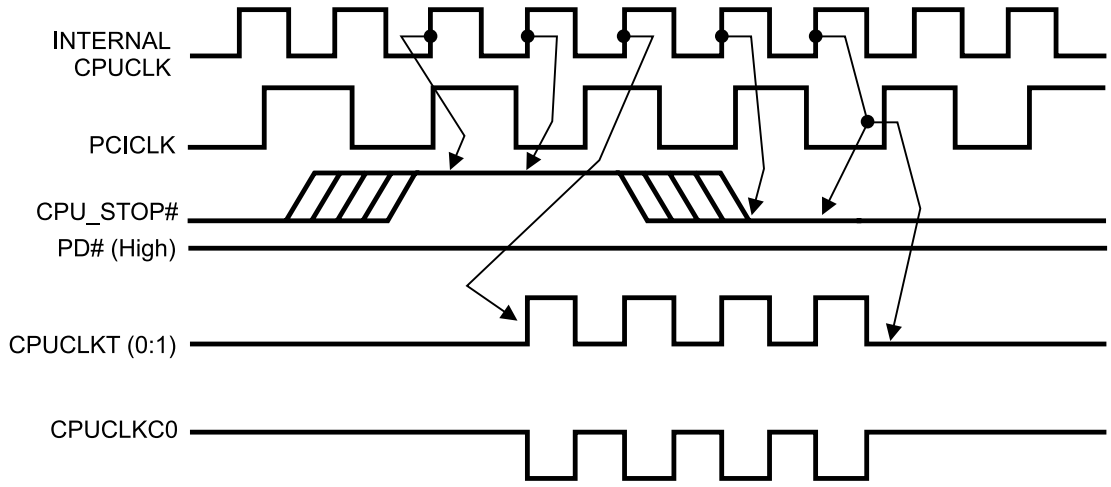


Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-189 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. CLK_STOP# is an input pin which stops all clocks, expcpt XTAL and CPUCLKT0/CPUCLKC0
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

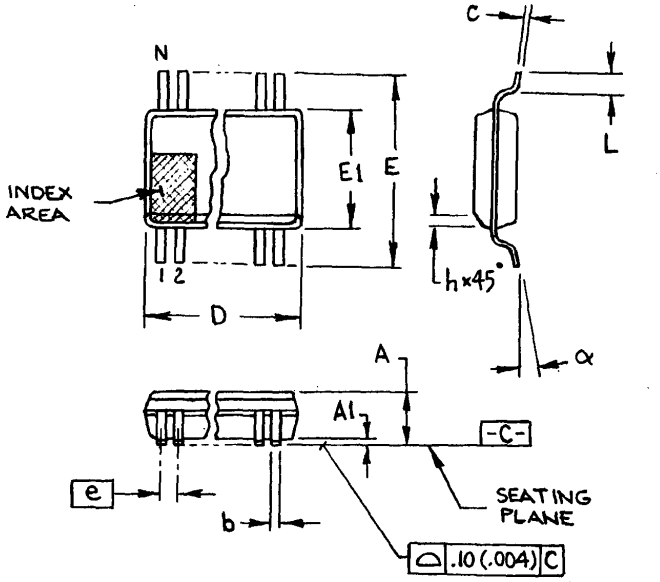
CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-189**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-189.
3. All other clocks continue to run undisturbed.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

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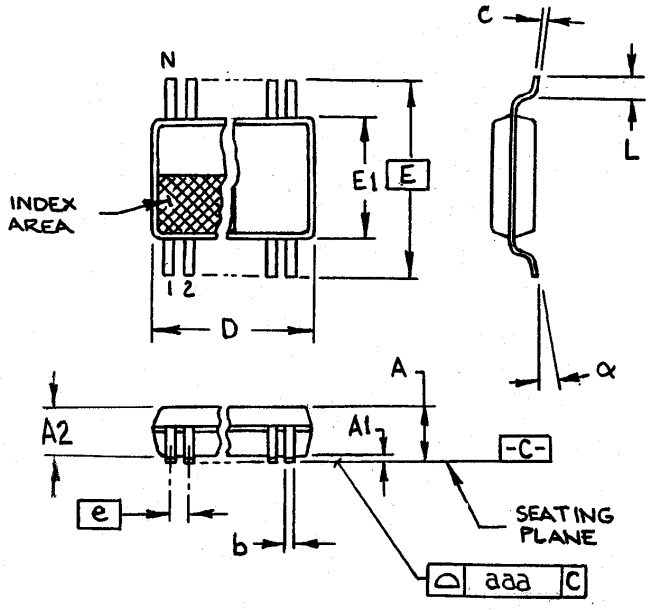
Ordering Information

ICS9248yF-189-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device



6.10 mm. Body, 0.50 mm. pitch TSSOP (240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.30
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

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Ordering Information

ICS9248yG-189-T

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device