



GENERAL DESCRIPTION

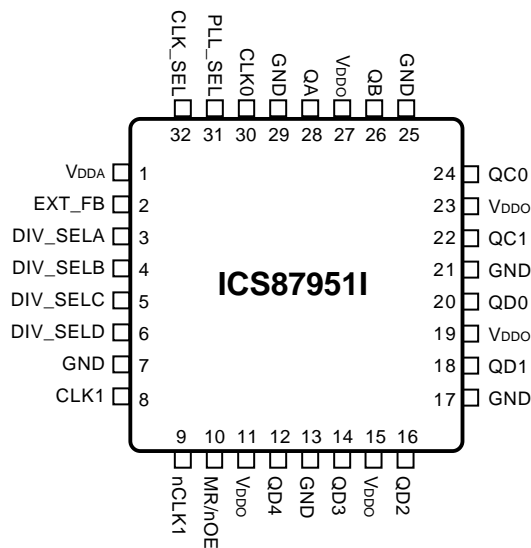


The ICS879511 is a low voltage, low skew 1-to-9 Differential-to-LVCMOS clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS879511 has two selectable clock inputs. The single ended clock input accepts LVCMOS or LVTTTL input levels. The CLK1, nCLK1 pair can accept most standard differential input levels. With output frequencies up to 180MHz, the ICS879511 is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS879511 contains frequency configurable outputs and an external feedback input for regenerating clocks with “zero delay”.

FEATURES

- Fully integrated PLL
- 9 single ended 3.3V LVCMOS outputs
- Selectable single ended CLK0 or differential CLK1, nCLK1 inputs
- The single ended CLK0 input can accept the following input levels: LVCMOS or LVTTTL input levels
- CLK1, nCLK1 supports the following input types: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Output frequency range: 25MHz to 180MHz
- VCO range: 200MHz to 480MHz
- External feedback for “zero delay” clock regeneration
- Cycle-to-cycle jitter: $\pm 100\text{ps}$ (typical)
- Output skew: 375ps (maximum)
- PLL reference zero delay: 350ps window (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Pin compatible with the MPC951

PIN ASSIGNMENT



32-Lead LQFP

7mm x 7mm x 1.4mm package body

Y package
Top View



BLOCK DIAGRAM

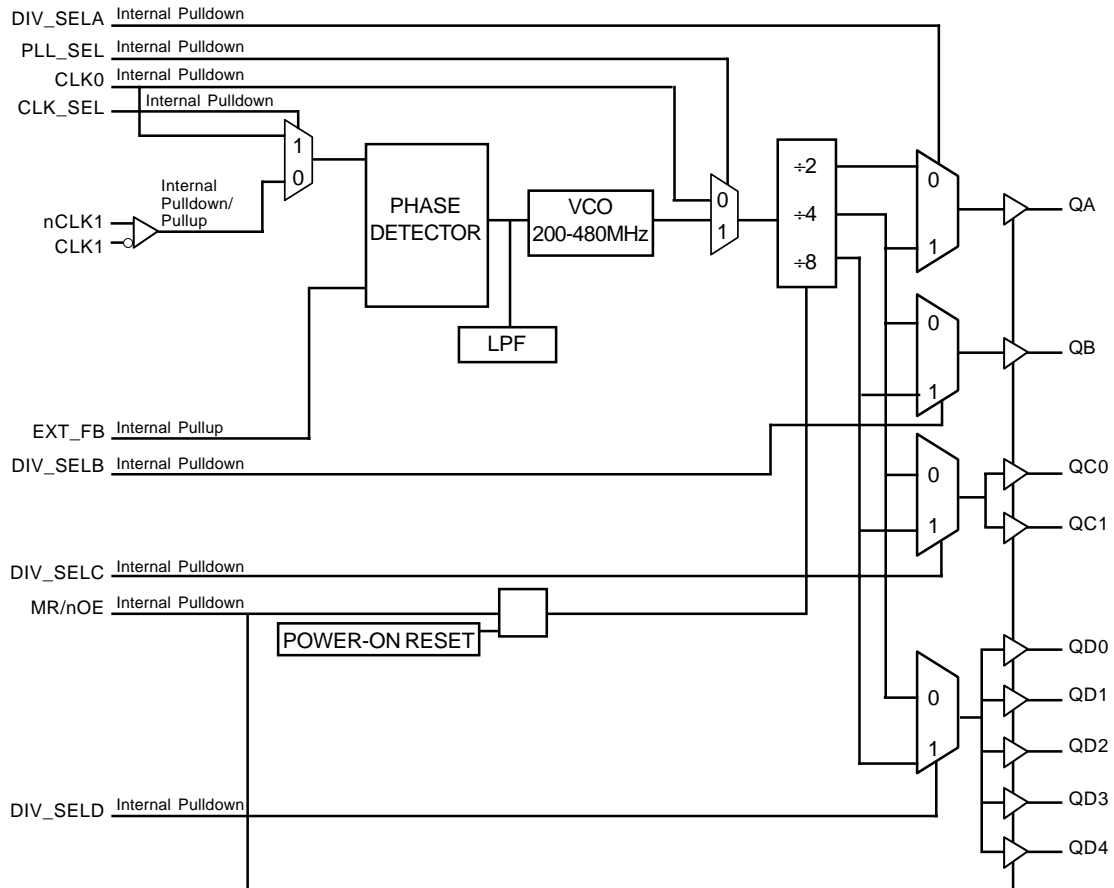




TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------------------------|----------------------------|--------|----------|--|
| 1 | V _{DDA} | Power | | Analog supply pin. |
| 2 | EXT_FB | Input | Pullup | Feedback input to phase detector for regenerating clocks with "zero delay". LVCMOS / LVTTTL interface levels. |
| 3 | DIV_SELA | Input | Pulldown | Selects divide value for Bank A output as described in Table 3D. LVCMOS / LVTTTL interface levels. |
| 4 | DIV_SELB | Input | Pulldown | Selects divide value for Bank B output as described in Table 3D. LVCMOS / LVTTTL interface levels. |
| 5 | DIV_SELC | Input | Pulldown | Selects divide value for Bank C outputs as described in Table 3D. LVCMOS / LVTTTL interface levels. |
| 6 | DIV_SELD | Input | Pulldown | Selects divide value for Bank D outputs as described in Table 3D. LVCMOS / LVTTTL interface levels. |
| 7, 13, 17, 21, 25, 29 | GND | Power | | Power supply ground. |
| 8 | CLK1 | Input | Pullup | Non-inverting differential clock input. |
| 9 | nCLK1 | Input | Pulldown | Inverting differential clock input. |
| 10 | MR/nOE | Input | Pulldown | Master reset and output enable. When LOW, outputs are enabled. When HIGH, outputs are disabled and dividers are reset. LVCMOS / LVTTTL interface levels. |
| 11, 15, 19, 23, 27 | V _{DDO} | Power | | Output supply pins. |
| 12, 14, 16, 18, 20 | QD4, QD3, QD2, QD1, QD0 | Output | | Bank D clock outputs. 7Ω typical output impedance. LVCMOS interface levels. |
| 22, 24 | QC1, QC0 | Output | | Bank C clock outputs. 7Ω typical output impedance. LVCMOS interface levels. |
| 26 | QB | Output | | Bank B clock output. 7Ω typical output impedance. LVCMOS interface levels. |
| 28 | QA | Output | | Bank A clock output. 7Ω typical output impedance. LVCMOS interface levels. |
| 30 | CLK0 | Input | Pulldown | LVCMOS / LVTTTL phase detector reference clock input. |
| 31 | PLL_SEL | Input | Pulldown | Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS / LVTTTL interface levels. |
| 32 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK0. When LOW, selects CLK1, nCLK1. LVCMOS / LVTTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--|---|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | | 4 | pF |
| C _{PD} | Power Dissipation Capacitance (per output) | V _{DDA} , V _{DDO} = 3.47V | | 25 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | KΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | KΩ |



TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

| Inputs | Outputs | | | | |
|--------|---------|---------|---------|----------|---------|
| | MR/nOE | QA | QB | QC0, QC1 | QD0:QD4 |
| 1 | HiZ | HiZ | HiZ | HiZ | HiZ |
| 0 | Enabled | Enabled | Enabled | Enabled | Enabled |

TABLE 3B. OPERATING MODE FUNCTION TABLE

| Inputs | Operating Mode |
|---------|----------------|
| PLL_SEL | |
| 0 | Bypass |
| 1 | PLL |

TABLE 3C. PLL INPUT FUNCTION TABLE

| Inputs | |
|---------|-------------|
| CLK_SEL | PLL Input |
| 0 | CLK1, nCLK1 |
| 1 | CLK0 |

TABLE 3D. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE

| Inputs | | | | Outputs | | | |
|----------|----------|----------|----------|---------|-------|-------|-------|
| DIV_SELA | DIV_SELB | DIV_SELC | DIV_SELD | QA | QB | QCx | QDx |
| 0 | 0 | 0 | 0 | VCO/2 | VCO/4 | VCO/4 | VCO/4 |
| 0 | 0 | 0 | 1 | VCO/2 | VCO/4 | VCO/4 | VCO/8 |
| 0 | 0 | 1 | 0 | VCO/2 | VCO/4 | VCO/8 | VCO/4 |
| 0 | 0 | 1 | 1 | VCO/2 | VCO/4 | VCO/8 | VCO/8 |
| 0 | 1 | 0 | 0 | VCO/2 | VCO/8 | VCO/4 | VCO/4 |
| 0 | 1 | 0 | 1 | VCO/2 | VCO/8 | VCO/4 | VCO/8 |
| 0 | 1 | 1 | 0 | VCO/2 | VCO/8 | VCO/8 | VCO/4 |
| 0 | 1 | 1 | 1 | VCO/2 | VCO/8 | VCO/8 | VCO/8 |
| 1 | 0 | 0 | 0 | VCO/4 | VCO/4 | VCO/4 | VCO/4 |
| 1 | 0 | 0 | 1 | VCO/4 | VCO/4 | VCO/4 | VCO/8 |
| 1 | 0 | 1 | 0 | VCO/4 | VCO/4 | VCO/8 | VCO/4 |
| 1 | 0 | 1 | 1 | VCO/4 | VCO/4 | VCO/8 | VCO/8 |
| 1 | 1 | 0 | 0 | VCO/4 | VCO/8 | VCO/4 | VCO/4 |
| 1 | 1 | 0 | 1 | VCO/4 | VCO/8 | VCO/4 | VCO/8 |
| 1 | 1 | 1 | 0 | VCO/4 | VCO/8 | VCO/8 | VCO/4 |
| 1 | 1 | 1 | 1 | VCO/4 | VCO/8 | VCO/8 | VCO/8 |



ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{DDx} | 4.6V |
| Inputs, V_i | -0.5V to $V_{DDA} + 0.5V$ |
| Outputs, V_o | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 42.1°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-------------------|---------|---------|---------|-------|
| V_{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DDO} | Power Supply Current | All V_{CC} pins | | | 115 | mA |
| I_{DDA} | Analog Supply Current | | | | 20 | mA |

TABLE 4B. DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|---------------------|-----------|---------|-----------------|---------|
| V_{IH} | Input High Voltage | LVCMOS/LVTTL Inputs | 2 | | 3.6 | V |
| V_{IL} | Input Low Voltage | LVCMOS/LVTTL Inputs | | | 0.8 | V |
| V_{PP} | Peak-to-Peak Input Voltage | CLK1, nCLK1 | 300 | | 1000 | mV |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | GND + 0.5 | | $V_{DD} - 0.85$ | V |
| V_{OH} | Output High Voltage | $I_{OH} = -40mA$ | 2.4 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 40mA$ | | | 0.5 | V |
| I_{IN} | Input Current | | | | ± 120 | μA |

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for CLK1 and nCLK1 is $V_{DDA} + 0.3V$.



TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---------------------------|-----------------|---------|---------|---------|-------|
| f_{REF} | Input Reference Frequency | | | | 100 | MHz |

TABLE 6. AC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------------|-------------------------------|---|----------------------------------|-----------|-----------------|----------|
| f_{MAX} | Output Frequency | QA \div 2 | | | 180 | MHz |
| | | QA/QB \div 4 | | | 120 | MHz |
| | | QB \div 8 | | | 60 | MHz |
| f_{VCO} | PLL VCO Lock Range | | 200 | | 480 | MHz |
| $t(\emptyset)$ | Static Phase Offset; NOTE 1,3 | CLK0 | fREF = 50MHz Feedback = VCO/8 | 15 | 165 | ps |
| | | CLK1, nCLK1 | | | -445 | -95 |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | Same Frequencies | | | 375 | ps |
| | | Different Frequencies QAf _{MAX} < 150MHz QAf _{MAX} > 150MHz | | | 500 750 | ps ps |
| $f_{jit(cc)}$ | Cycle-to-Cycle Jitter; NOTE 3 | | | ± 100 | | ps |
| t_{LOCK} | PLL Lock Time; NOTE 3 | | | | 10 | mS |
| t_R | Output Rise Time | 0.8 to 2V | 0.1 | | 1.0 | ns |
| t_F | Output Fall Time | 0.8 to 2V | 0.1 | | 1.0 | ns |
| t_{PW} | Output Pulse Width | | tcycle/2 - 1000 | | tcycle/2 + 1000 | ps |
| t_{PZL} | Output Enable Time | | | | 6 | ns |
| t_{PLZ}, t_{PHZ} | Output Disable Time | | | | 7 | ns |

All parameters measured at f_{MAX} unless noted otherwise.

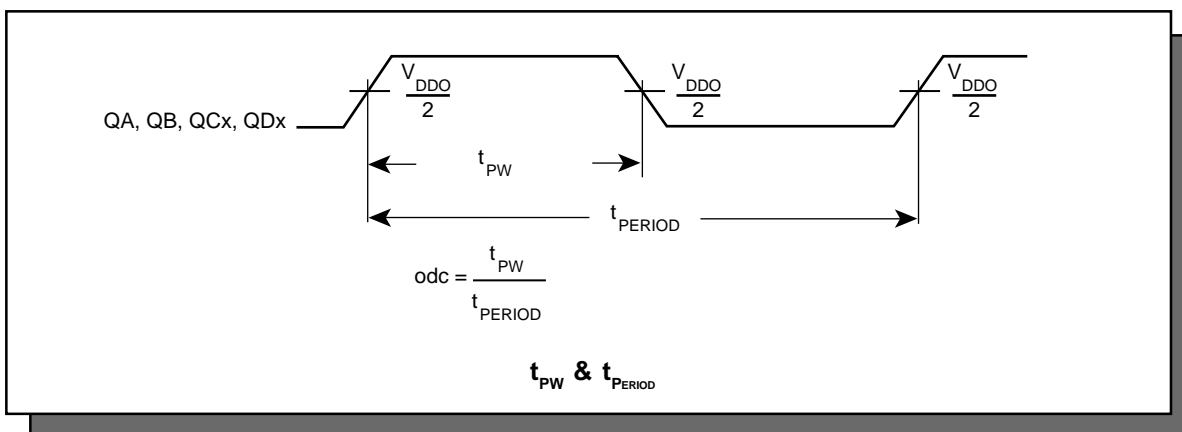
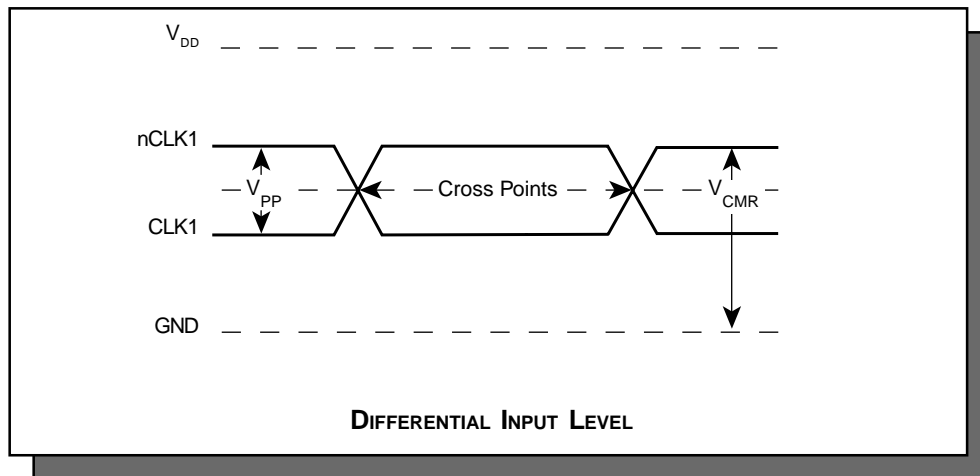
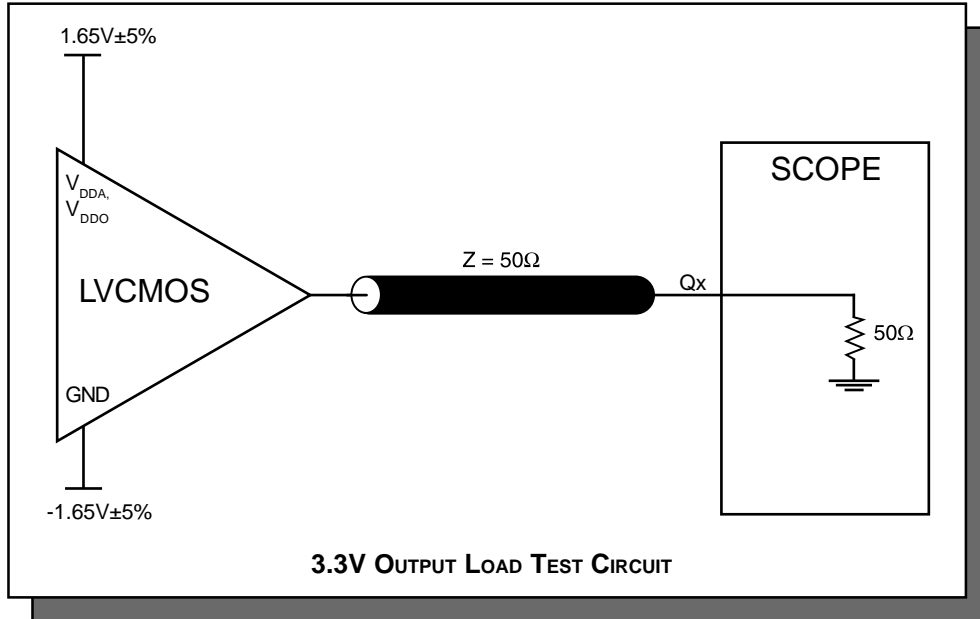
NOTE 1: Defined as the time difference between the input reference clock and the averaged feedback input signal, when the PLL is locked and the input reference frequency is stable.

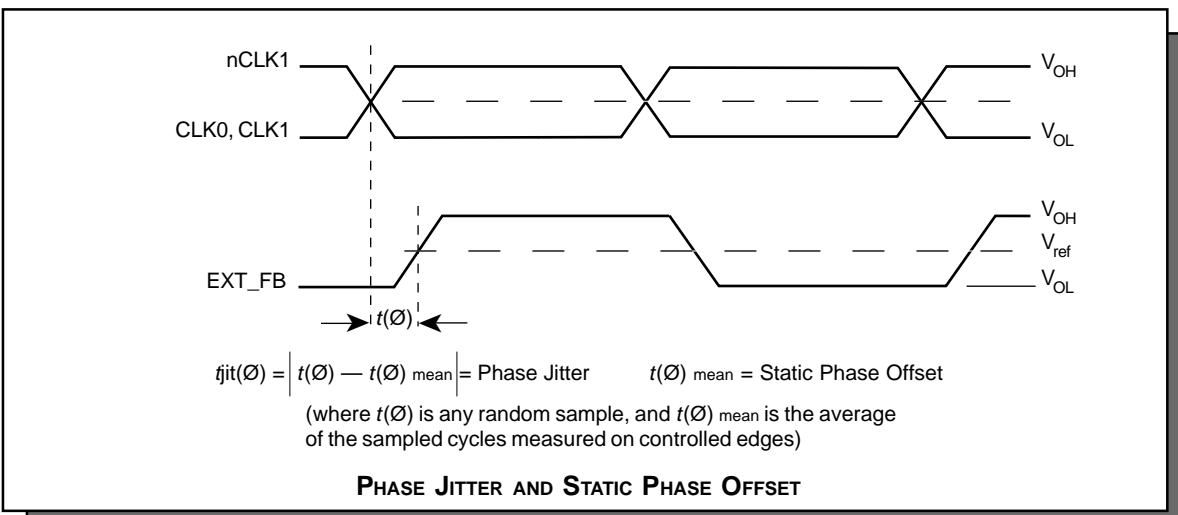
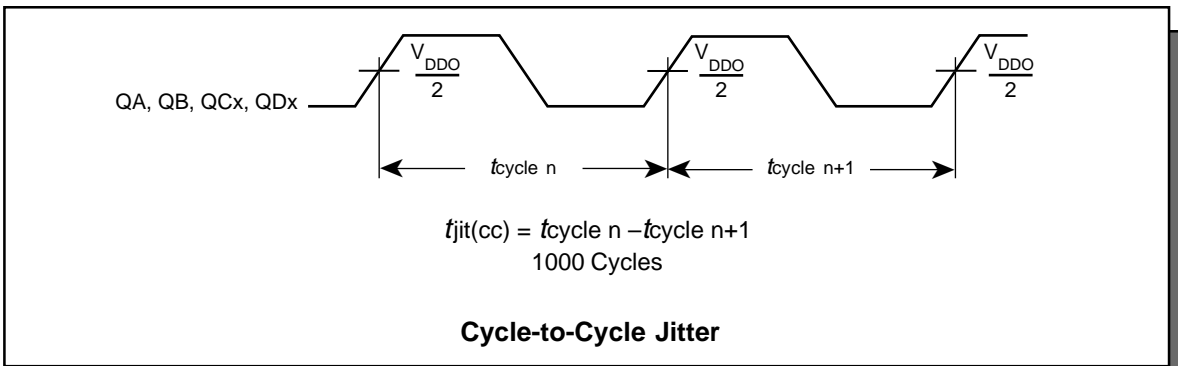
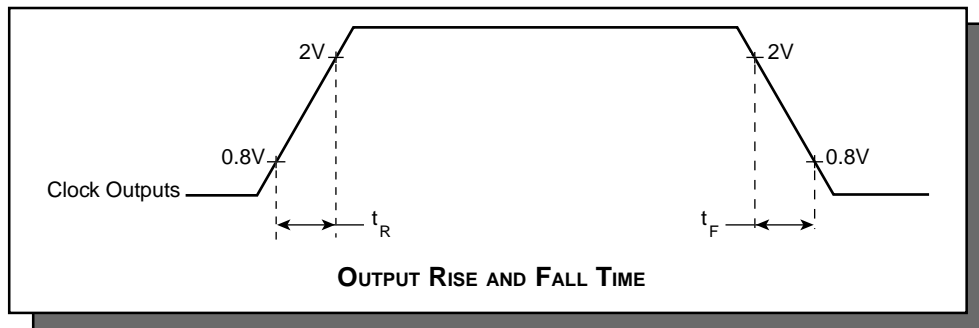
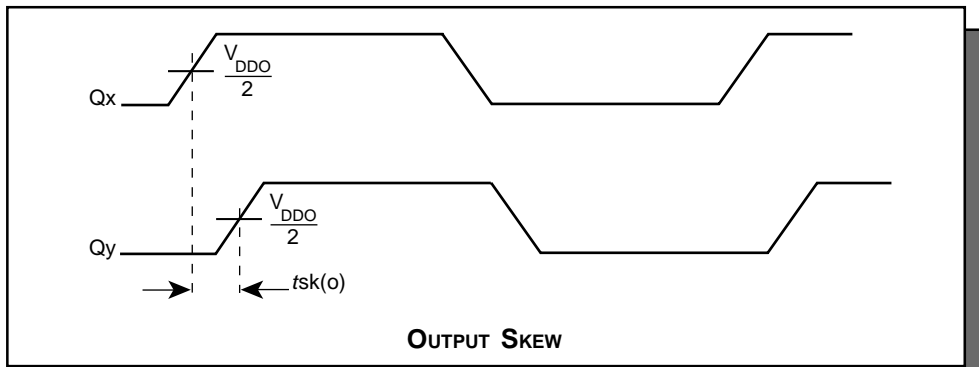
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



PARAMETER MEASUREMENT INFORMATION



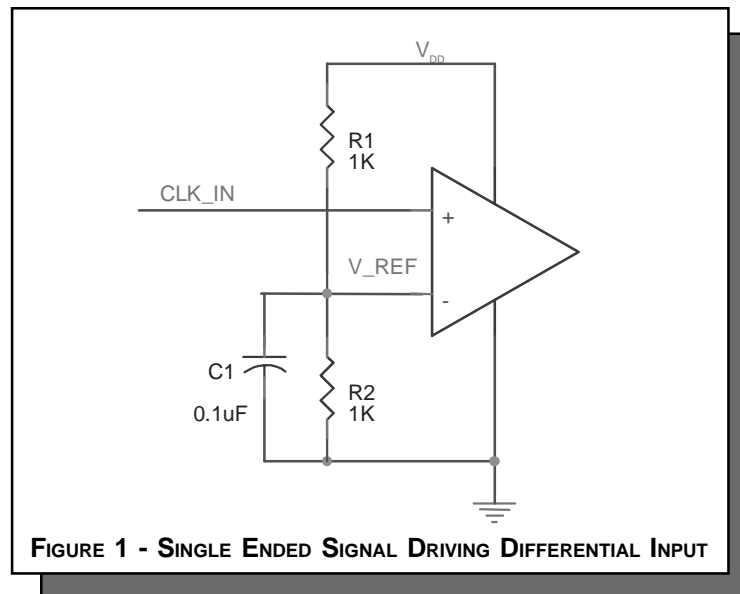




APPLICATION INFORMATION

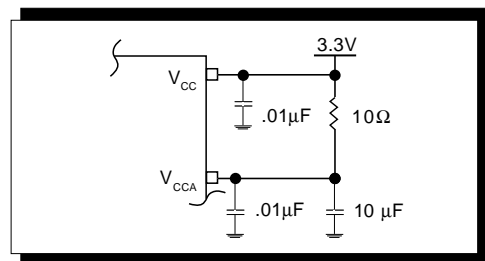
WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} \approx V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.



POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87951I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. Figure 2 illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{DDA} pin.





RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87951I is: 2674



PACKAGE OUTLINE - Y SUFFIX

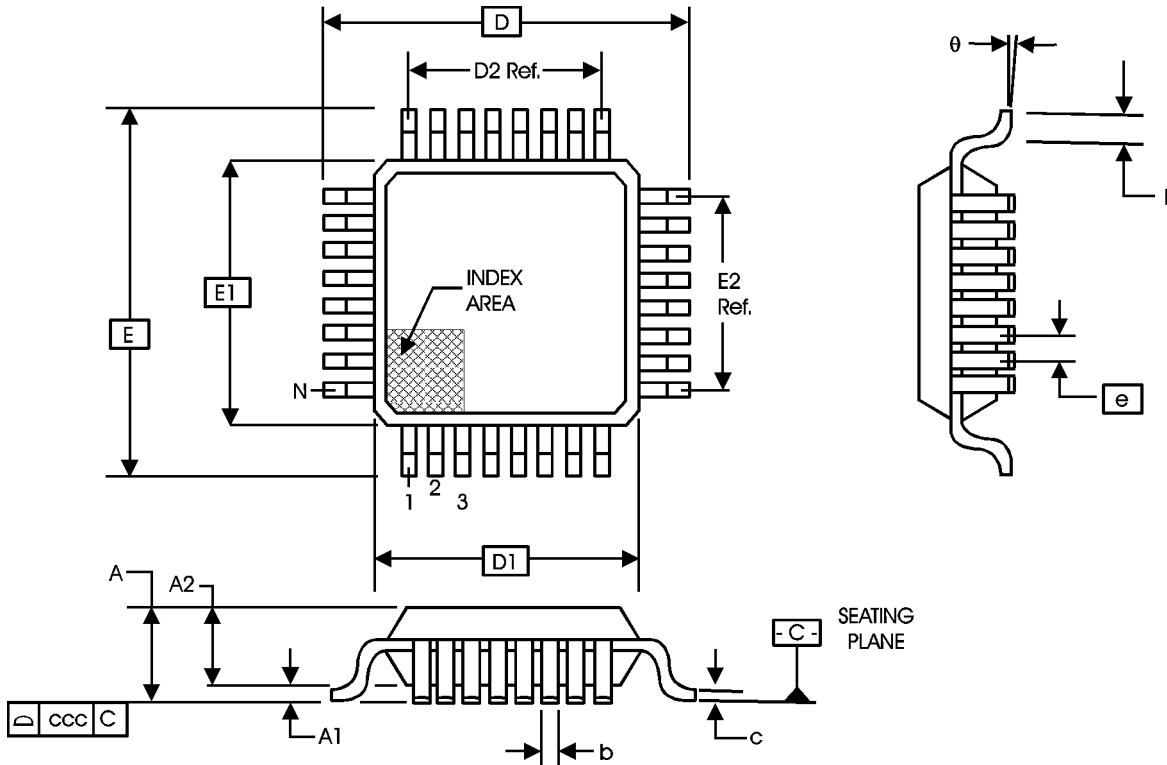


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|------------|---------|---------|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| theta | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS87951I
LOW SKEW, 1-TO-9
DIFFERENTIAL-TO-LVCMOS ZERO DELAY BUFFER

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|--------------------------|----------------|-------------------------------|--------------|--------------------|
| ICS87951AYI | ICS87951AYI | 32 Lead LQFP | 250 per tray | -40°C to 85°C |
| ICS87951AYIT | ICS87951AYI | 32 Lead LQFP on Tape and Reel | 1000 | -40°C to 85°C |

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.