PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8731-01

LOW SKEW, 1-TO-11 DIFFERENTIAL-TO-3.3V LVPECL CLOCK MULTIPLIER / ZERO DELAY BUFFER

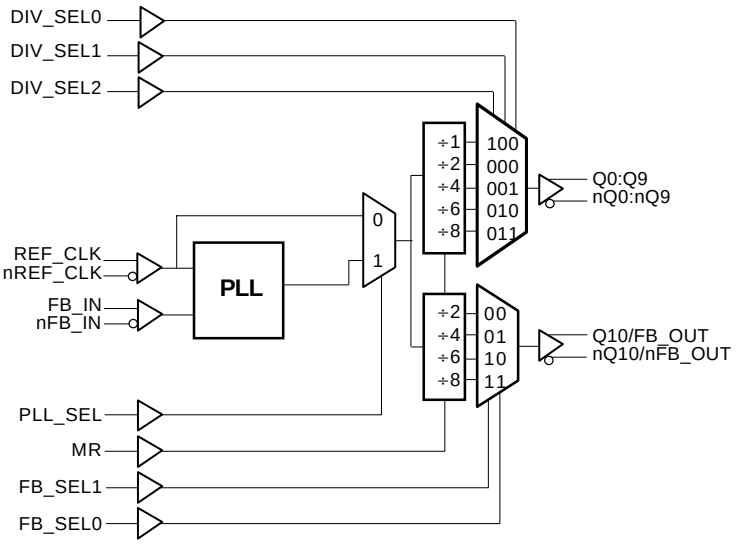
GENERAL DESCRIPTION

The ICS8731-01 is a low voltage, low skew, 1-to-11 Differential-to-3.3V LVPECL Clock Multiplier/Zero Delay Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. With output frequencies up to 650MHz the ICS8731-01 is targeted at high performance clock applications. Along with a fully integrated PLL the ICS8731-01 contains frequency configurable, differential outputs and external feedback inputs for multiplying clock frequencies and regenerating clocks with “zero delay”. Frequency multiplication is achieved by utilizing the seperate feedback and clock output dividers. The value of the multiplier is determined by the ratio of the feedback divider, M, to the output divider, N. For multiplier values greater than 1, M must be greater than N. For multiplier values less than 1, M must be less than N. The zero delay mode is achieved with M and N at equal values. The divide values of the clock and feedback outputs are controlled by the DIV_SEL0:2 and FB_SEL0:1 inputs, respectively. The ICS8731-01 accepts any differential signal and translates it to differential 3.3V LVPECL output levels.

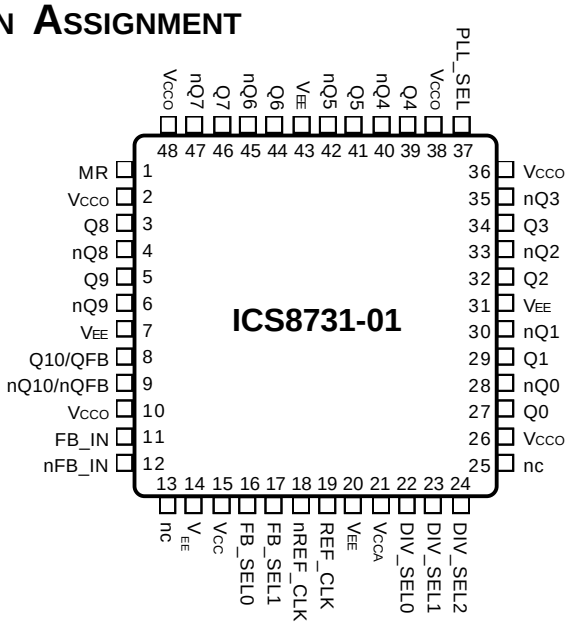
FEATURES

- 11 differential 3.3V LVPECL outputs
- Differential reference clock input pair
- REF_CLK, nREF_CLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Output frequency up to 650MHz
- Maximum reference clock input frequency: 250MHz
- Accepts any single-ended input signal with a resistor bias on nCLK input
- External feedback for zero delay capabilitiy
- Output skew: 200ps (maximum)
- Cycle-to-cycle jitter: 50ps (typical)
- Full 3.3V operating supply
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR	Input	Pulldown	Master Reset. Resets the output divider. LVCMOS / LVTTL interface levels.
2, 10, 26, 36, 38, 48	V_{CCO}	Power		Output supply pins.
3, 4, 5, 6	Q8, nQ8, Q9, nQ9	Output		Differential output pair.
7, 14, 20, 31, 43	V_{EE}	Power		Negative supply pins.
8, 9	Q10/QFB, nQ10/nQFB	Output		Differential clock outputs.
11, 12	FB_IN, nFB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay".
15	V_{CC}	Power		Positive supply pin.
16	FB_SEL0	Input	Pulldown	Determines output divider for Q10 outputs (see Table 3). LVCMOS / LVTTL interface levels.
17	FB_SEL1	Input	Pulldown	Determines output divider for Q10 outputs (see Table 3). LVCMOS / LVTTL interface levels.
18	nREF_CLK	Input	Pullup	Inverting differential clock input.
19	REF_CLK	Input	Pulldown	Non-inverting differential clock input.
21	V_{CCA}	Power		Analog supply pin.
22	DIV_SEL0,	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
23	DIV_SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
24	DIV_SEL2	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
13, 25	nc	Unused		No connect.
27, 28 29, 30	Q0, nQ0, Q1, nQ1	Output		Differential output pairs.
32, 33, 34, 35	Q2, nQ2, Q3, nQ3	Output		Differential output pairs.
37	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS / LVTTL interface levels.
39, 40, 41, 42	Q4, nQ4, Q5, nQ5	Output		Differential output pairs.
44, 45, 46, 47	Q6, nQ6, Q7, nQ7	Output		Differential output pairs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE FOR Q0:Q9 OUTPUTS

Inputs					Outputs
MR	**PLL_SEL**	**DIV_SEL2**	**DIV_SEL1**	**DIV_SEL0**	**Q0:Q9, nQ0:nQ9**
1	X	X	X	X	Low
0	1	1	0	0	fVCO/1
0	1	0	0	0	fVCO/2
0	1	0	0	1	fVCO/4
0	1	0	1	0	fVCO/6
0	1	0	1	1	fVCO/8
0	0	1	0	0	fREF_CLK/1
0	0	0	0	0	fREF_CLK/2
0	0	0	0	1	fREF_CLK/4
0	0	0	1	0	fREF_CLK/6
0	0	0	1	1	fREF_CLK/8

TABLE 3B. CONTROL INPUT FUNCTION TABLE FOR Q10/FB

Inputs				Outputs
MR	**PLL_SEL**	**FB_SEL1**	**FB_SEL0**	**Q10, nQ10**
1	X	X	X	Low
0	1	0	0	fVCO/2
0	1	0	1	fVCO/4
0	1	1	0	fVCO/6
0	1	1	1	fVCO/8
0	0	0	0	fREF_CLK/2
0	0	0	1	fREF_CLK/4
0	0	1	0	fREF_CLK/6
0	0	1	1	fREF_CLK/8

TABLE 4. QX OUTPUT FREQUENCY W/FB_IN = Q10/FB

Inputs						fVCO
FB_IN	**FB_SEL1**	**FB_SEL0**	**Q10/FB Output Divider Mode**	**REF_CLK (MHz)**		**(NOTE 1)**
				Minimum	**Maximum**	
Q10/FB	0	0	÷2	162.5	250 (NOTE 2)	fREF_CLK x 2
Q10/FB	0	1	÷4	81.25	162.5	fREF_CLK x 4
Q10/FB	1	0	÷6	54.16	108.33	fREF_CLK x 6
Q10/FB	1	1	÷8	40.63	81.25	fREF_CLK x 8

NOTE 1: NOTE 1: VCO frequency range is 325MHz to 650MHz.
NOTE 2: The maximum input frequency that the phase defector can accept is 250MHz.

TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency				250	MHz

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CCx}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CCO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 6A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				130	mA
I_{CCA}	Analog Supply Current					mA

TABLE 6B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	PLL_SEL, DIV_SEL0, DIV_SEL1, DIV_SEL2, FB_SEL0, FB_SEL1, MR		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	PLL_SEL, DIV_SEL0, DIV_SEL1, DIV_SEL2, FB_SEL0, FB_SEL1, MR		-0.3		0.8	V
I_{IH}	Input High Current	DIV_SEL0, DIV_SEL1, DIV_SEL2, MR, FB_SEL0, FB_SEL1	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		PLL_SEL	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SEL0, DIV_SEL1, DIV_SEL2, MR, FB_SEL0, FB_SEL1	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 6C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	REF_CLK, FB_IN	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nREF_CLK, nFB_IN	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	REF_CLK, FB_IN	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nREF_CLK, nFB_IN	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for REF_CLK, nREF_CLK and FB_IN, nFB_IN is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 6D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

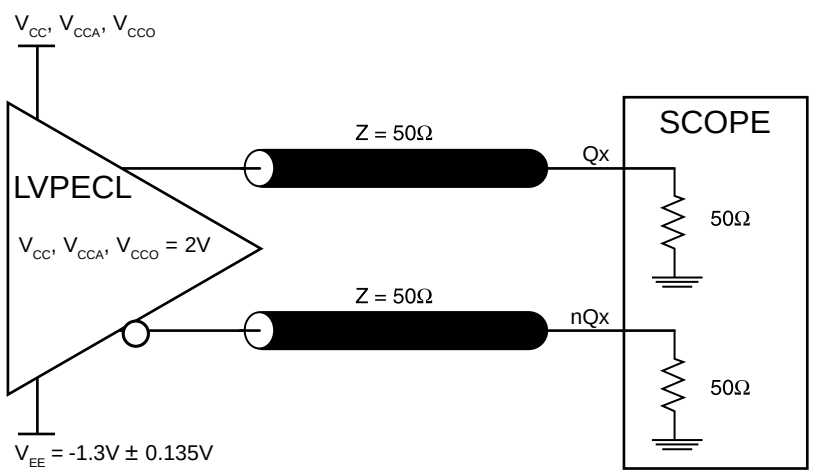
NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 7. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

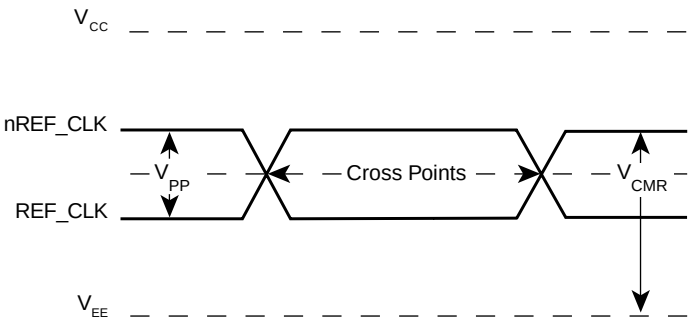
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					650	MHz
t_{PD}	Propagation Delay; NOTE 1		PLL_SEL = 0V, f ≤ 650MHz	3.63		4.25	ns
t(Ø)	Static Phase Offset; NOTE 2	REF_CLK	PLL_SEL = 3.3V, f_{REF} = TBD, f_{VCO} = TBD		TBD		ps
		nREF_CLK			TBD		ps
*t*sk(o)	Output Skew; NOTE 3, 5		Measured on rising edge at differential cross point			200	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 5		Measured on rising edge at differential cross point				ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5				50		ps
t_L	PLL Lock Time					1	ms
t_R	Output Rise Time		20% to 80%	200		700	ps
t_F	Output Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle			48	50	52	%

All parameters measured at fMAX unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

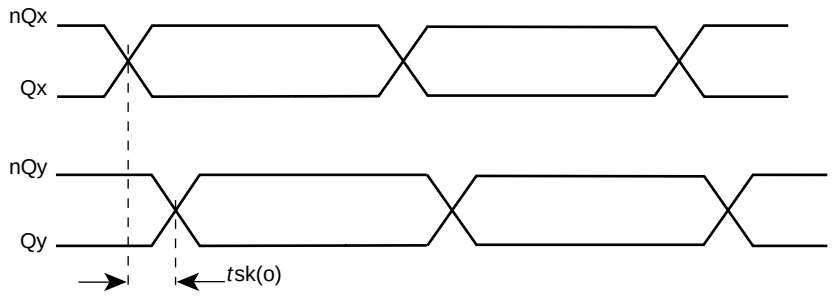
PARAMETER MEASUREMENT INFORMATION



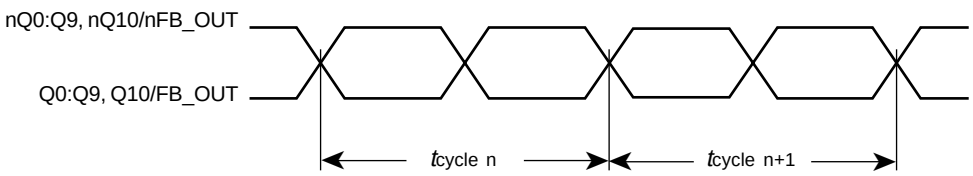
OUTPUT LOAD TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL



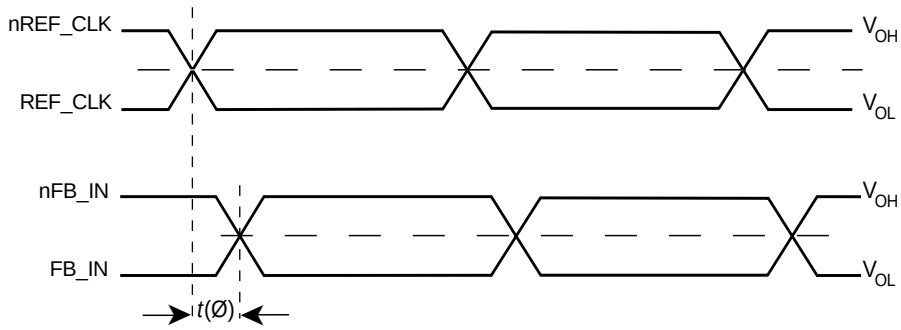
OUTPUT SKEW



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

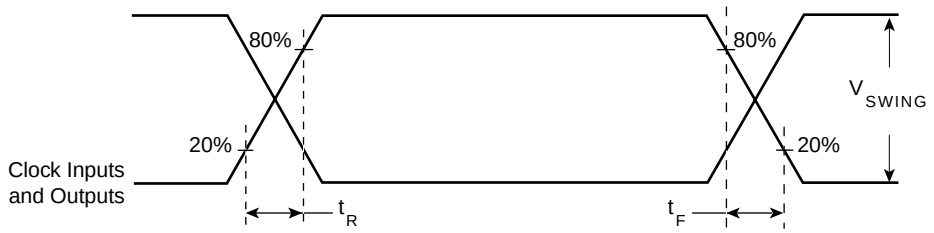
Cycle-to-Cycle Jitter



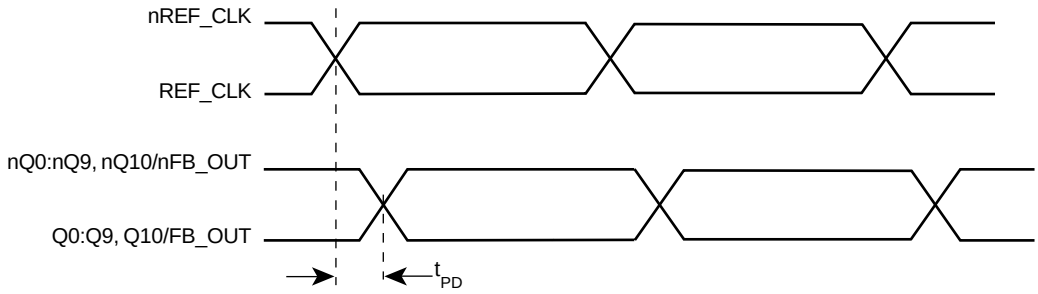
$t_{jit}(Ø) = \left| t(Ø) - t(Ø)_{mean} \right|$ = Phase Jitter $\quad t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

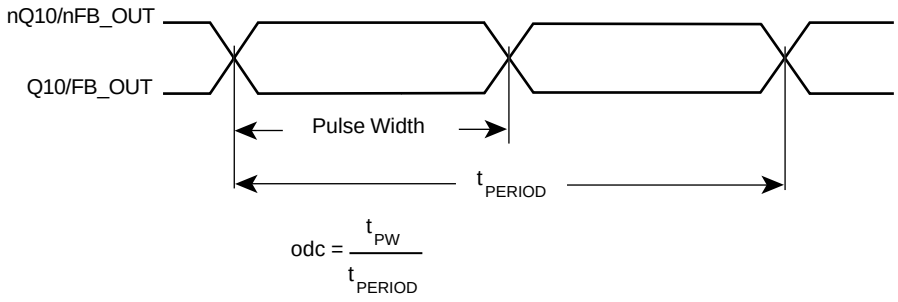
PHASE JITTER AND STATIC PHASE OFFSET



INPUT AND OUTPUT RISE AND FALL TIME



PROPAGATION DELAY



odc & t_{PERIOD}

APPLICATION INFORMATION

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

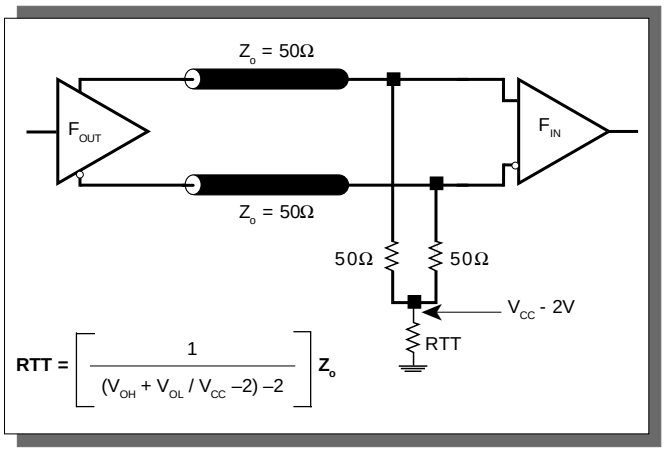


FIGURE 1A - LVPECL OUTPUT TERMINATION

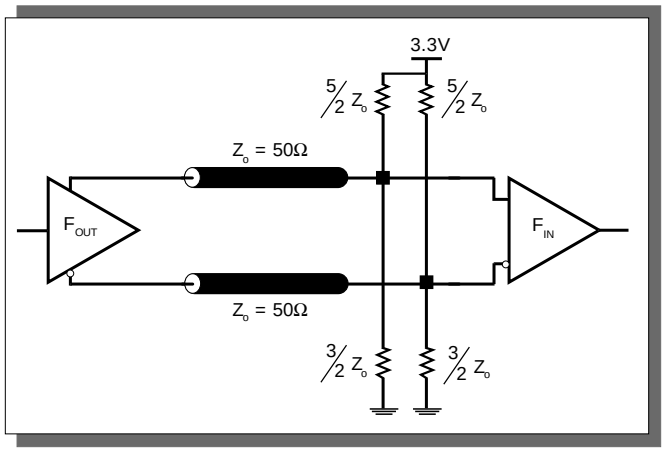


FIGURE 1B - LVPECL OUTPUT TERMINATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8731-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

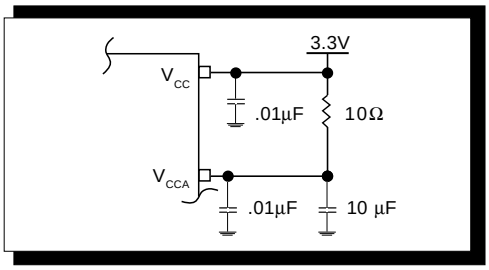


FIGURE 2 - POWER SUPPLY FILTERING

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8731-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8731-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 130mA = **450.5mW**
- Power $(outputs)_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 11 * 30.2mW = **332.2mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 450.5mW + 332.2mW = **782.7mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.783W * 42.1°C/W = 103°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 3.*

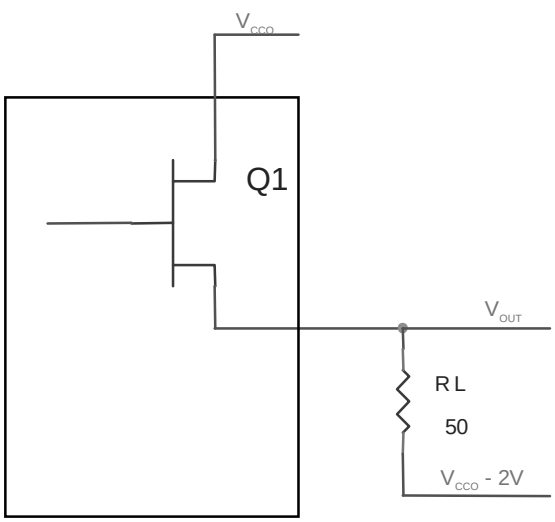


FIGURE 3 - LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 1.0V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC} - V_{OH\_MAX}))/R_L] * (V_{CC} - V_{OH\_MAX}) =$
$[(2V - 1V)/50Ω] * 1V =$ **20.0mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC} - V_{OL\_MAX}))/R_L] * (V_{CC} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 9. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8731-01 is: 2883

PACKAGE OUTLINE - Y SUFFIX

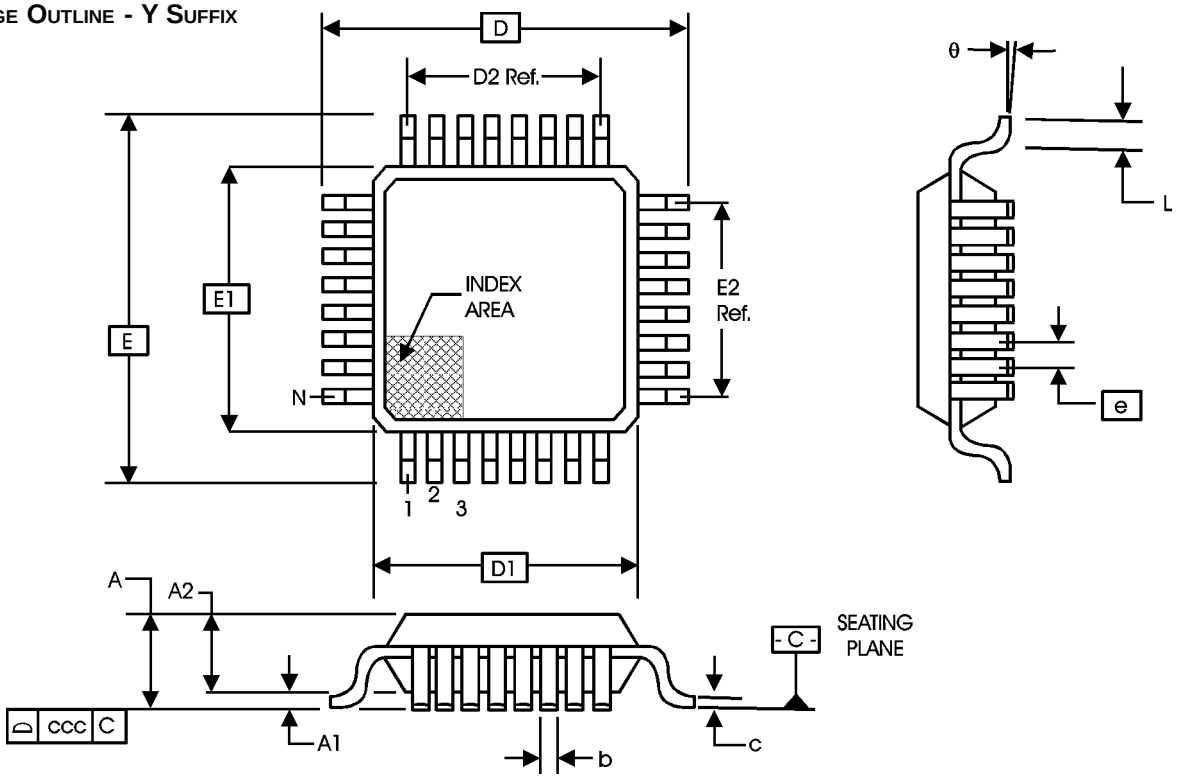


TABLE 10. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8731CY-01	ICS8731CY-01	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8731CY-01T	ICS8731CY-01	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C

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