ICS1531

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Triple 8-bit MSPS A/D Converters with Line-Locked Clock Generator

General Description

The ICS1531 is a high-performance, cost-effective, 3-channel, 8-bit analog-to-digital converter with an integrated line-locked clock generator. It is part of a family of chips intended for high-resolution video applications that use analog inputs, such as LCD monitors, LCD projectors, plasma displays, and projection TVs. Using ICS's low-voltage CMOS mixed-signal technology, the ICS1531 is an effective data-capture solution for resolutions from VGA to UXGA.

The ICS1531 offers analog-to-digital data conversion and synchronized pixel clock generation at speeds of 100, 140, or 165 MHz (or mega samples per second, MSPS). The Dynamic Phase Adjust (DPA) circuitry allows end-user control over the pixel clock phase, relative to the recovered sync signal and analog pixel data. Either the internal pixel clock can be used as a capture clock input to the analog-to-digital converters or an external clock input can be used. The ICS1531 provides either one or two 24-bit pixels per clock. An ADCSYNC output pin provides recovered HSYNC from the pixel clock phase-locked-loop (PLL) divider chain output, which can be used to synchronize display enable output.

A clamp signal can be generated internally or provided through the CLAMP pin. A high-bandwidth video amplifier with adjustable gain allows fine tuning of the analog signal. The advanced PLL uses an internal programmable feedback divider. Two additional, independent programmable PLLs, each with spread-spectrum functionality, support memory and panel clock requirements.

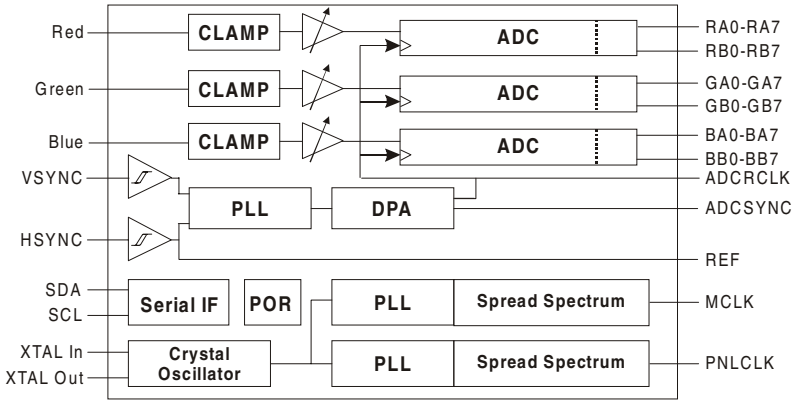
Features

- 3-channel 8-bit analog-to-digital conversion up to 165 MHz
- Direct connection to analog input data (no external pre-amplifier circuit needed)
- Video amplifier: 500-MHz analog bandwidth, software-adjustable gain
- Dynamic Phase Adjust (DPA) for software-adjustable analog sample points
- Software selectable: One pixel per clock (for 24-bit pixels) or two pixels per clock (for a total of 48 bits)
- Internal clamp circuit. Very low jitter.
- Low-voltage TTL clock outputs, synchronized with digital pixel data outputs
- Independent software reset for PLLs and DPA
- Double-buffered PLL and DPA control registers
- Two additional PLLs with spread spectrum for memory and panel clock
- External/internal loop-filter selection with software
- Automatic Power-On Reset (POR) detection
- Uses 3.3 VDC. Digital inputs are 5-V tolerant.
- Industry-standard 2-wire serial bus interface speeds: low (100 kHz), high (400 kHz), or ultra (800 kHz)
- Lock detection available in hardware and software
- 144-pin low-profile quad flat pack (LQFP) package

Applications

- LCD displays, LCD projectors, plasma displays, and projection TVs

ICS1531 Functional Block Diagram



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Chapter 1 Abbreviations and Acronyms

Table 1-1 lists and interprets the abbreviations and acronyms used throughout this data sheet.

Table 1-1. Abbreviations and Acronyms

Abbreviation / Acronym	Interpretation
ADC	analog-to-digital converter
ASIC	application-specific integrated circuit
BNC	Type of connector, named for (“**B**ayonet”) Paul **N**eill and Carl **C**oncelman
CMOS	complimentary metal-oxide semiconductor
DAC	digital-to-analog converter
DPA	Dynamic Phase Adjust
EMI	electro-magnetic interference
FCC	(United States) Federal Communications Commission
IF	interface
LCD	liquid crystal display
LQFP	low-profile quad flat pack
LSB	least-significant bit
LVTTL	low-voltage digital transistor-transistor logic
Max.	maximum
Min.	minimum
MSB	most-significant bit
MSPS	mega samples per second
MUX	multiplexer
N/A	Not Applicable
PC	personal computer
PFD	phase/frequency detector
PLL	phase-locked loop
POR	power-on reset
Reg	register
RGB	red, green, blue
R/W	read/write
SXGA	super XGA
TTL	transistor-transistor logic
Typ.	typical
UXGA	ultra XGA
VCO	voltage-controlled oscillator
VESA	Video Electronics Standards Association
VGA	video graphics array
XGA	eXtended graphics array

Chapter 2 Summary

2.1 Overview

The ICS1531 addresses stringent display system line-locked applications by providing clock signals and digitized pixel data through internal high-performance analog-to-digital converters (ADCs). The ICS1531 is a complete solution for capturing analog red, green, and blue (RGB) signals from personal computers and workstations. It supports data capture for resolutions from VGA (640 × 480) to UXGA (1600 × 1200). The ICS1531 features are described in the following sections.

2.2 Clamp, Video Amplifier, and Analog-to-Digital Circuits (Condition RGB Inputs)

For the following circuits, see Figure 4-3.

2.2.1 Clamp Circuits (Adjust RGB Inputs to ADC Range)

To properly digitize incoming RGB analog signals, the ICS1531 must adjust the signals to the range of the ADC. This adjustment is done by clamping the signal, which both (1) establishes a bottom voltage limit and (2) offsets the signal to align the black level of the incoming signal with the bottom voltage limit. Then the signal is amplified to adjust the top limit to the upper range of the ADC.

The ICS1531 incorporates an internal clamping circuit to generate a clamping signal. Optionally, the CLAMP pin can be used to input an externally generated clamp signal (Reg 30:2). In either case, the polarity of the signal to a clamp can be programmed (Reg 30:3). Typically, the clamp signal is generated by ADCSYNC (the recovered HSYNC timing pulse). The clamp signal is generated during a non-display region of time, when most PC display controllers output a black signal.

2.2.2 Video Amplifier Circuits (Amplify RGB Inputs)

The ICS1531's video amplifier circuit can directly accept analog RGB input signals from a PC display controller (that is, no external pre-amplifier is required). The video amplifier circuit has three independent 500-MHz video amplifiers for the RGB inputs. To adjust the top level of the signal, this video amplifier circuit can be programmed for a gain of 1.0, 1.2, 1.4, or 1.6 (Regs 31:1-0, 32:1-0, and 33:1-0). As a result, the video amplifier circuit can improve low-amplitude signals and adjust analog input signals for the optimum sampling range of the ADC circuit.

2.2.3 Analog-to-Digital Circuits (Digitize RGB Inputs)

The ICS1531 has high-performance analog-to-digital converters (ADCs) to capture and digitize analog RGB data (Reg 30:7). Low-power CMOS technology is used to create 8-bit ADCs, which are calibrated to align the capture event between (1) the 3 analog input channels and (2) either 3 or 6 digital output channels. The ADC can provide (through Reg 30:6) one of the following:

- Two 24-bit pixels aligned to a half-rate pixel clock (two-pixels-per-clock mode), which can be used for 48-bit interface panels and image-scaling chips
- One 24-bit pixel aligned to a full-rate pixel clock (one-pixel-per-clock mode), which can be used for 24-bit-per-pixel applications

In addition, programmable digital-to-analog converters for the R, G, and B inputs fine-tune VRTR, VRTG, and VRTB, the individual R, G, and B maximum reference 'top' voltages (Regs 34-36).

2.3 Phase-Locked Loop (Generates Pixel Clock from Input HSYNC)

The ICS1531 uses a phase-locked loop (PLL) to generate its pixel clock output frequency. A PLL is a closed-loop feedback system that locks an output signal's phase and frequency to that of a reference input signal's phase and frequency. In the case of the ICS1531, when its PLL is locked it locks a pixel clock output to that of an HSYNC signal from input video.For a block diagram of the ICS1531 PLL, see Figure 4-1 and Figure 4-2.

2.3.1 Phase/Frequency Detector (Compares Two Input Signals)

The first section of the PLL is the Phase/Frequency Detector (PFD). To use the PLL, first the PFD must be enabled either through hardware control (with a signal from the PDEN pin) or software control (Reg 00:1-0). Once the PFD is enabled, the PFD compares both the phase and frequency of the following two input signals.

- **PFD Input Signal 1:** External HSYNC Signal or Internal Oscillator Signal

  The first input to the PFD can be selected from either the external HSYNC signal or the ICS1531 internal crystal oscillator signal (Reg 00:5).

  – External HSYNC signal

    Typically, one of the input signals to the PFD comes from the HSYNC of a PC display controller. This input HSYNC signal can have a transition time of tens of nanoseconds. Furthermore, if the input HSYNC signal is from a remote source, its pulses can degrade.

    A high-performance Schmitt trigger (Reg 00:7-6) conditions the HSYNC pulse before it is input to the PFD. The polarity of this input pulse can be programmed (Reg 00:2). The result of this conditioning is REF, a clean reference clock signal that in comparison to the input HSYNC signal has a short transition time. [For more information on adjusting the HSYNC signal, see Section 2.6, "Dynamic Phase Adjust (Positions Pixel Clock on Sub-Pixel Basis)".]

  – Internal crystal oscillator

    Alternatively, one of the input signals to the PFD can be from the ICS1531 internal crystal oscillator (Regs 07:7-0 and 2C:6-4).

- **PFD Input Signal 2:** Signal from Feedback Loop

  The second input to the PFD comes from the output of the PLL feedback loop, which results from the processing that takes place with the charge pump, filter, voltage-controlled oscillator, post-scaler divider, and feedback divider. That is, the PLL output (the signal from the feedback loop) also appears as one of the two inputs to the PFD.

As a result of the comparison of the two input signals, the PFD processes the inputs so there is the proper ratio between them. Then the PFD uses the output to drive a charge pump.

2.3.2 Charge Pump (Boosts Voltage Gain of Signal from PFD)

The charge pump, which is a current-source and current-sink pair, boosts the voltage gain of the signal from the PFD. This PFD signal gain is programmable over a 7-bit range up to 128 µA (Reg 01:2-0).

2.3.3 Loop Filter (Filters Output from Charge Pump)

The loop filter, which is a capacitance and resistance in series, acts as a low-bandpass filter for the frequency output from the charge pump. The ICS1531 can select between either an external loop filter, or more typically, an internal loop filter (Reg 08:0). The advantage of the internal filter is that it can be used for all Video Electronics Standards Association (VESA) timing modes, for ease in manufacturing.

Note: VESA establishes standard timing specifications for the personal-computer industry. Although many computer manufacturers require that display controllers adhere to the VESA timing specifications, there is no enforcement. As a result, not all display controllers conform precisely to the VESA timing specifications.

2.3.4 Voltage-Controlled Oscillator (Matches Input Signals to PFD)

The voltage level resulting from the output signals from the combined processing by the PFD, charge pump, and loop filter drives the voltage-controlled oscillator (VCO). The VCO uses the level of this input voltage to proportionally adjust its frequency output. This signal is compared to the input to the PFD so that both inputs to the PFD match in both phase and frequency. The VCO can operate up to nearly 600 MHz with a fixed gain. Consequently, the ICS1531 can be optimized for the best performance at all operating frequencies. (For more information on the VCO, see Chapter 11, "VCO Transfer Characteristics".)

2.3.5 Post-Scaler Divider (Sets Ratio of VCO and Pixel Clock Frequencies)

Using the frequency output from the VCO, the programmable Post-Scaler Divider (PSD) can set the ratio of VCO frequency-to-pixel clock frequency at 2:1, 4:1, 8:1, or 16:1 (Reg 01:5-4). The maximum pixel clock output frequency is therefore 300 MHz. However, for practical applications, the analog-to-digital converter limits this output frequency to either 100, 140, or 165 MHz.

2.3.6 Feedback Divider (Controls Number of Pixel Clocks per HSYNC)

The ICS1531's internal 12-bit pixel Feedback Divider (Regs 02 and 03) controls the total number of pixel clocks per line (that is, between successive HSYNCs). The total number of pixels per line includes both displayed and non-displayed pixels.

Reg 06:2 can delay the recovered HYSNC signal (that is, ADCSYNC) by one input clock period. This delay has the effect of moving channel 'A' data to the 'B' channel output pins and the channel 'B' data to the 'A' channel output pins.

Note:

1. As a starting point to capture analog RGB input from VESA-compliant sources, ICS recommends certain register settings for the software "***.ics files**" that come with the ICS1531 Register Tool. However, the Register Tool register settings are only a guide. (For more information on the ICS1531 Register Tool and its ***.ics.files**, see the ICS1531 Demo Board Guide.)
2. The display manufacturer must provide a way to optimize the display for the particular display controller in use.
3. If the ICS1531 internal pixel PLL Feedback Divider is not set correctly, it can create visible errors on the display.
4. To adjust the ICS1531 on a sub-pixel basis, see Section 2.6, "Dynamic Phase Adjust (Positions Pixel Clock on Sub-Pixel Basis)".

2.4 Analog-to-Digital Converter (Synchronizes Data Capture)

By using the internal 3-channel analog-to-digital converter (ADC), the ICS1531 internally provides the pixel clock needed to synchronize data capture. The pixel clock can be further processed by the Dynamic Phase Adjust. [For more information on the ADC, see Section 2.2.3, "Analog-to-Digital Circuits (Digitize RGB Inputs)" and Figure 4-3.] For the pixel clock to appear on the CLK pin, the pixel clock output must be enabled (Reg 06:6).

2.5 Additional PLLs, with Spread Spectrum (Drive Memory and Panel Data Clocks)

Besides the pixel clock PLL, the ICS1531 has two other independent PLLs for use as needed. Typically, one of the PLLs is used to drive memory clocks (Regs 26–2B and 2D) and the other PLL is used to drive panel data clocks (Regs 20–25 and 2D). Both of these additional PLLs are tailored for the required frequency ranges. Each supports software-controlled spread-spectrum clock dithering to reduce measured electro-magnetic interference (EMI).

2.6 Dynamic Phase Adjust (Positions Pixel Clock on Sub-Pixel Basis)

Most display controllers provide an HSYNC signal that can be used as a reference signal for the pixel clock. However, when this HSYNC signal is used as an input, frequently it has significant jitter that impacts data capture. Furthermore, the analog data stream from the display controller to the ICS1531 has no pixel-rate reference clock.

So that analog pixel data inputs can be properly sampled and digitized, the ICS1531's pixel PLL tracks the input HSYNC signal and the line-to-line jitter. To provide a properly aligned sampling clock (ADCSYNC) to the ADC blocks, the ICS1531's Dynamic Phase Adjust (DPA) circuitry can add delays to the pixel clock position. The delay, which occurs in relation to the edge of ADCSYNC (the recovered HSYNC signal), is added in sub-pixel time increments.

Regs 04:5-0, 05:1-0 and 06 are used to program the ICS1531 DPA for a value representing incremental sub-pixel delay units. By choosing the proper value, pixel data to the ICS1531 can be sampled at the optimum time for proper digitization and the best-looking display. Typically, a system's microcontroller presets this value, based on either a table or proprietary algorithms. The end user can change the value through the system's on-screen display controls.

Table 2-1 lists the number of possible delay element units that can be used to program to add a delay of up to one pixel clock period, in increments of either 16, 32, or 64 (Reg 04:5-0 and Reg 5:1-0).

Table 2-1. Increments for Delay Element Units

Number of Delay Element Units	Pixel Clock Range, MHz
16	55 – 260
32	27 – 130
64	14 – 64

Note: To adjust the ICS1531 on a pixel-by-pixel basis, see Section 2.3.6, "Feedback Divider (Controls Number of Pixel Clocks per HSYNC)".

2.7 Automatic Power-On Reset Detection (Automatically Resets ICS1531)

The ICS1531 automatically detects power-on resets. As a result, the ICS1531 resets itself if the supply voltage drops below threshold values. No external connection to a reset signal is required.

2.8 Logic Inputs and Outputs

- **Inputs.** The ICS1531 uses both of the following inputs:
  - Analog inputs
  - Digital inputs. The digital inputs are low-voltage TTL (LVTTL) inputs that operate at 3.3 V. These LVTTL inputs are also 5-V tolerant. (For inputs that are 5-V tolerant, see Section 3.2.3.10, "List of 5-V Tolerant Pins".)
- **Outputs.** The ICS1531 has high-speed LVTTL clock outputs.

2.9 Industry-Standard 2-Wire Serial Interface

To access all its registers, the ICS1531 uses an industry-standard 2-wire serial interface that operates at one of the following speeds:

- A low speed of 100 kHz
- A high speed of 400 kHz
- An ultra speed of 800 kHz

For use with the 2-wire serial interface, the ICS1531 has 5 V-tolerant inputs. The ICS1531 can use either of two unique, alternative sets of addresses. Table 2-2 lists the addresses that can be used, depending on the state of the SBADR pin.

Table 2-2. ICS1531 Address Sets

Addresses in Address Set	Address Set 1. (SBADR Pin Is Low)	Address Set 2. (SBADR Pin Is High)
7-bit device address	24h	25h
8-bit read address	49h	4Bh
8-bit write address	48h	4Ah

2.10 Programmable Outputs

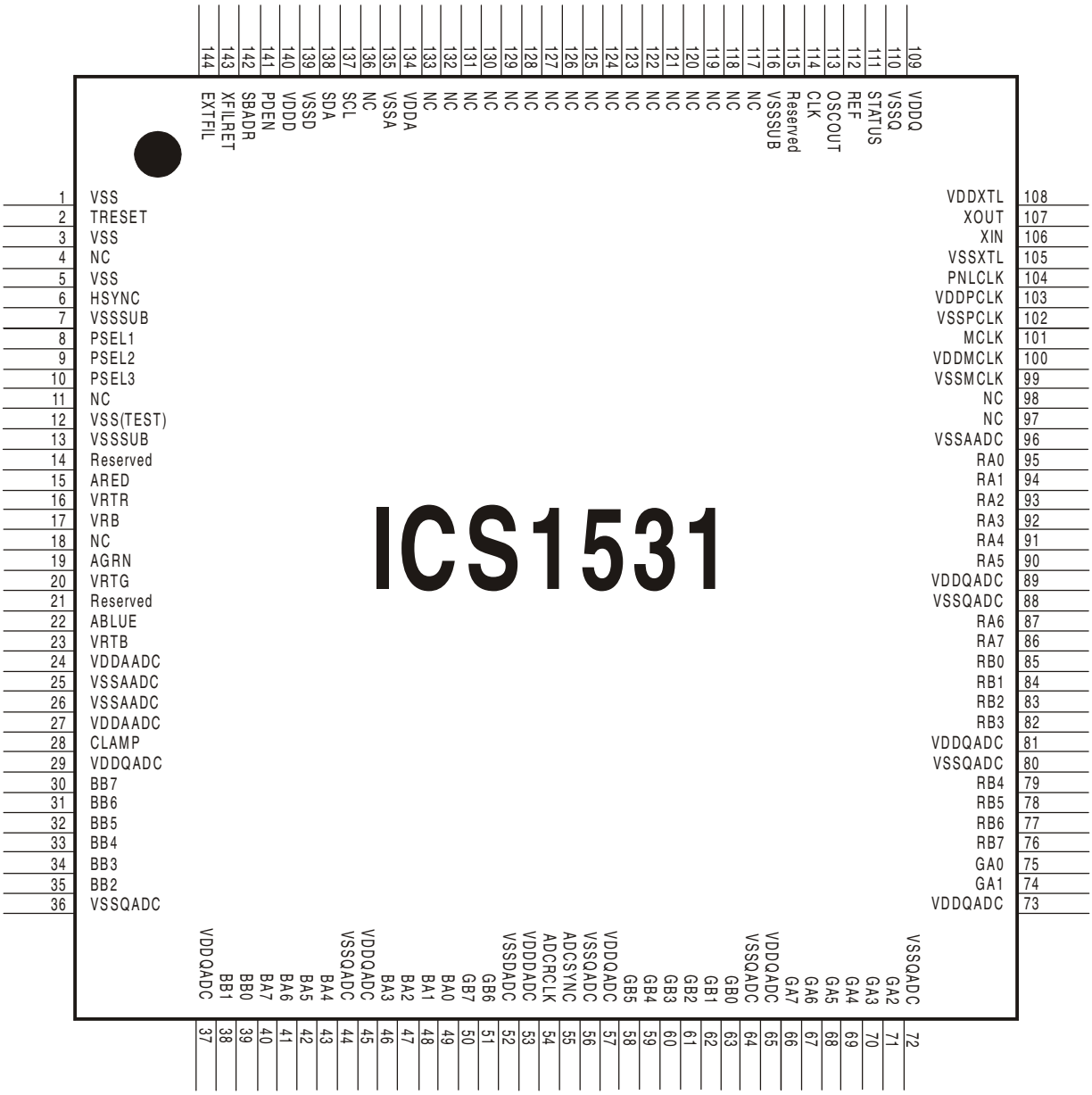
For general-purpose outputs, the ICS1531 provides three programmable pins, PSEL3, PSEL2, PSEL1 (Reg 37:2-0).

Chapter 3 Pin Diagram and Listings

3.1 Pin Diagram for ICS1531

Figure 3-1 shows the pin diagram for the ICS1531, which is packaged in a 144-pin low-profile quad flat pack (LQFP).

Figure 3-1. Pin Diagram



3.2 Pin Listings

Note:

1. The TRESET pin (pin 2) was formerly a Reserved pin.
2. The following pins, formerly 'Reserved', are now NC (No Connect): 4, 11, 18, 97–98, 117–133, 136
3. The (active-low) STATUS pin (pin 111) was formerly called 'LOCK'

3.2.1 Pin Listing by Pin Number

Table 3-1. ICS1531 Pins, by Pin Number

Pin No.	Pin Name
1	VSS
2	TRESET
3	VSS
4	NC
5	VSS
6	HSYNC
7	VSSSUB
8	PSEL1
9	PSEL2
10	PSEL3
11	NC
12	VSS(TEST)
13	VSSSUB
14	Reserved
15	ARED
16	VRTR
17	VRB
18	NC
19	AGRN
20	VRTG
21	Reserved
22	ABLUE
23	VRTB
24	VDDAADC
25	VSSAADC
26	VSSAADC
27	VDDAADC
28	CLAMP
29	VDDQADC
30	BB7
31	BB6
32	BB5
33	BB4
34	BB3
35	BB2
36	VSSQADC

Pin No.	Pin Name
37	VDDQADC
38	BB1
39	BB0
40	BA7
41	BA6
42	BA5
43	BA4
44	VSSQADC
45	VDDQADC
46	BA3
47	BA2
48	BA1
49	BA0
50	GB7
51	GB6
52	VSSDADC
53	VDDDADC
54	ADCRCLK
55	ADCSYNC
56	VSSQADC
57	VDDQADC
58	GB5
59	GB4
60	GB3
61	GB2
62	GB1
63	GB0
64	VSSQADC
65	VDDQADC
66	GA7
67	GA6
68	GA5
69	GA4
70	GA3
71	GA2
72	VSSQADC

Pin No.	Pin Name
73	VDDQADC
74	GA1
75	GA0
76	RB7
77	RB6
78	RB5
79	RB4
80	VSSQADC
81	VDDQADC
82	RB3
83	RB2
84	RB1
85	RB0
86	RA7
87	RA6
88	VSSQADC
89	VDDQADC
90	RA5
91	RA4
92	RA3
93	RA2
94	RA1
95	RA0
96	VSSAADC
97	NC
98	NC
99	VSSMCLK
100	VDDMCLK
101	MCLK
102	VSSPCLK
103	VDDPCLK
104	PNLCLK
105	VSSXTL
106	XIN
107	XOUT
108	VDDXTL

Pin No.	Pin Name
109	VDDQ
110	VSSQ
111	STATUS
112	REF
113	OSCOUT
114	CLK
115	Reserved
116	VSSSUB
117	NC
118	NC
119	NC
120	NC
121	NC
122	NC
123	NC
124	NC
125	NC
126	NC
127	NC
128	NC
129	NC
130	NC
131	NC
132	NC
133	NC
134	VDDA
135	VSSA
136	NC
137	SCL
138	SDA
139	VSSD
140	VDDD
141	PDEN
142	SBADR
143	XFILRET
144	EXTFIL

3.2.2 Pin Listing by Alphabetical Pin Name

Note:

1. The TRESET pin was formerly a Reserved pin.
2. The following pins, formerly 'Reserved', are now NC (No Connect): 4, 11, 18, 97–98, 117–133, 136
3. The (active-low) STATUS pin was formerly called 'LOCK'.

Table 3-2. ICS1531 Pins, by Alphabetical Pin Name

Pin Name	Pin No.
ABLUE	22
ADCRCLK	54
ADCSYNC	55
AGRN	19
ARED	15
BA0	49
BA1	48
BA2	47
BA3	46
BA4	43
BA5	42
BA6	41
BA7	40
BB0	39
BB1	38
BB2	35
BB3	34
BB4	33
BB5	32
BB6	31
BB7	30
CLAMP	28
CLK	114
EXTFIL	144
GA0	75
GA1	74
GA2	71
GA3	70
GA4	69
GA5	68
GA6	67
GA7	66
GB0	63
GB1	62
GB2	61

Pin Name	Pin No.
GB3	60
GB4	59
GB5	58
GB6	51
GB7	50
HSYNC	6
MCLK	101
NC	4, 11, 18, 97–98, 117–133, 136
OSCOUT	113
PDEN	141
PNLCLK	104
PSEL1	8
PSEL2	9
PSEL3	10
RA0	95
RA1	94
RA2	93
RA3	92
RA4	91
RA5	90
RA6	87
RA7	86
RB0	85
RB1	84
RB2	83
RB3	82
RB4	79
RB5	78
RB6	77
RB7	76
REF	112
Reserved	14, 21, 115
SBADR	142
SCL	137

Pin Name	Pin No.
SDA	138
STATUS	111
TRESET	2
VDDA	134
VDDAADC	24, 27
VDDD	140
VDDDADC	53
VDDMCLK	100
VDDPCLK	103
VDDQ	109
VDDQADC	29, 37, 45, 57, 65, 73, 81, 89
VDDXTL	108
VRB	17
VRTB	23
VRTG	20
VRTR	16
VSS	1, 3, 5
VSSA	135
VSSAADC	25, 26, 96
VSSD	139
VSSDADC	52
VSSMCLK	99
VSSPCLK	102
VSSQ	110
VSSQADC	36, 44, 56, 64, 72, 80, 88
VSSSUB	7, 13, 116
VSS(TEST)	12
VSSXTL	105
XFILRET	143
XIN	106
XOUT	107

3.2.3 Pin Listing by Functional Grouping

3.2.3.1 Clock Pins

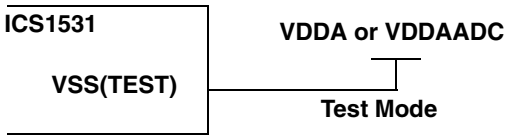
For more information on the clock pins, see Figure 4-2 and Figure 4-3.)

Table 3-3. Clock Pins

Pin Name	Pin Type	Pin Description
ADCRCLK	Input or Output	**Analog-to-Digital Converter Reference Clock.** • This pin outputs a half-rate pixel clock for latching digital output pixel data. • Typically, this pin connects to an LCD panel controller/scaler. • In this table, see also CLK.
ADCSYNC	Input or Output	**Analog-to-Digital Converter Sync.** • This pin provides a recovered HSYNC signal (that is, an HSYNC signal conditioned by a Schmitt trigger) that aligns to ADCRCLK. • For some previous ICS chips, the ADCSYNC pin is called FUNC.
CLK	Output	**Clock.** • This pin outputs the full-rate pixel clock for latching digital output pixel data. • In this table, see also ADCRCLK.
HSYNC	Input	**Horizontal Sync.** (See Table 3-6.)
MCLK	Output	**Memory Clock.** • This pin provides an independent user-programmable clock source. • Typically, this pin is used by LCD panel controller/scaler chips or microcontrollers.
OSCOUT	Output	**Oscillator Output.** • This output from this pin is from a crystal oscillator. • The output frequency is one of the following: – The same frequency as the input frequency to the crystal oscillator – The frequency that results when the input frequency is divided by a programmable value
PNLCLK	Output	**Panel Clock.** • This pin provides an independent user-programmable clock source. • Typically, this pin is used by LCD panel controller/scaler chips or microcontrollers.
REF	Output	**Reference.** This pin provides various reference line clock sync signals.
SCL	Input	**Serial Clock.** (See Table 3-7.)
XIN	Input	**Crystal Input.** This pin accepts input from one of the following: • A 14.31818-MHz crystal • An external clock source
XOUT	Output	**Crystal Output.** Do one of the following with this pin: • Connect it to a 14.31818-MHz crystal. • Leave it open for an external clock source.

3.2.3.2 Control Pins

Table 3-4. Control Pins

Pin Name	Pin Type	Pin Description
CLAMP	Input	**Clamp.** This pin accepts an external signal that is provided as an alternative to the ICS1531's internally generated clamp signal.
PSEL1, PSEL2, PSEL3	Output	**Programmable Select 1, 2, 3.** These pins are used as general-purpose programmable output pins.
TRESET	Input	**Test Reset.** When the ICS1531: • Is not in Test mode, this pin has no effect. • Is placed into Test mode: – This pin acts as a reset that sets the ICS1531 to an initial known state. – For information about the Test mode, in this table see VSS(TEST).
VSS(TEST)	Input	**Ground (Normal Mode) or Test Mode.** • Normal Mode. For the VSS(TEST) pin's Normal-mode function, see Table 3-4. • Test Mode. – When this pin is connected to either VDDA or VDDAADC, the ICS1531 is in Test mode. As a result, the ICS1531 is set to an initial known state. – The Test mode overrides whatever the bit setting of Reg 37:3 is, so that the Calibration Regs 38h to 3Ch are automatically enabled. – The Test mode bits are intended for use only by ICS.  **In Test mode, Test-mode bits are enabled and Calibration Regs 38h to 3Ch are automatically enabled.**

3.2.3.3 Pixel Data Pins

Table 3-5. Pixel Data Pins

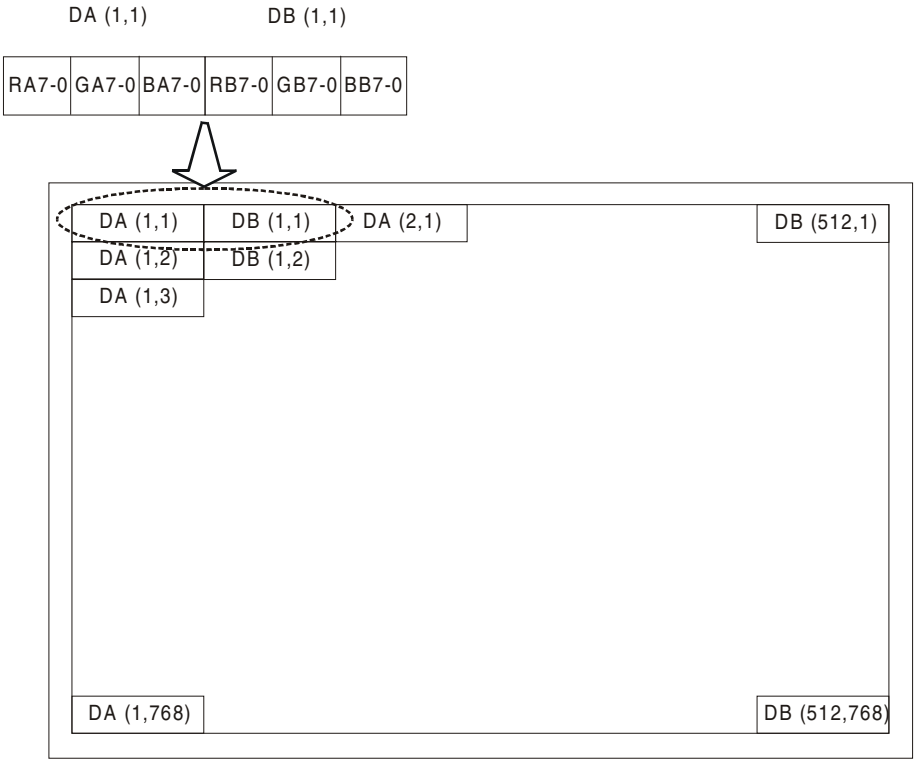
Pin Name	Pin Type	Pin Description
ABLUE, AGRN, ARED	Input	**Analog Blue, Analog Green, Analog Red.** • These pins accept analog data for the ADC blue, green, and red channels. • Typically, the data for these pins comes from a PC display controller.
BA7 – BA0, GA7 – GA0, RA7 – RA0	Output	**Blue ('A channel') A7 – A0, Green ('A channel') A7 – A0, Red ('A channel') A7 – A0.** • These pins output first blue, green, and red pixel data, respectively. • A7 pins reflect most-significant data bits. A0 pins reflect least-significant data bits.
BB7 – BB0, GB7 – GB0, RB7 – RB0	Output	**Blue ('B channel') B7 – B0, Green ('B channel') B7 – B0, Red ('B channel') B7 – B0.** • These pins output second blue, green, and red pixel data, respectively. • B7 pins reflect most-significant data bits. B0 pins reflect least-significant data bits.

Figure 3-2 shows the following:

- The relationship of:
  - Outputs from the ICS1531 ADC
  - To inputs of a 1024 × 768 LCD panel that samples 2 pixels of data with either a 36- or 48-bit data signal.
- DA indicates 'A channel' pixels, and DB indicates 'B channel' pixels.)

For timing information, see Chapter 10, "Timing Diagrams".

Figure 3-2. Relationship of Outputs from an ICS1531's ADC to Inputs of 1024 × 768 LCD Panel



3.2.3.4 Phase-Locked Loop Pins

Table 3-6 lists the pins for the phase-locked loop circuitry. For a block diagram that shows the function of these pins, see Figure 4-1.

Table 3-6. Phase-Locked Loop Pins

Pin Name	Pin Type	Pin Description
EXTFIL	Input	**External Filter.** This pin works with XFILRET (in this table, see XFILRET) and other components as part of an optional external filter for the pixel phase-locked loop.
HSYNC	Input	**Horizontal Sync.** • This 5-V tolerant pin is the clock input for the pixel PLL. • Typically this pin is connected to the HSYNC from a PC display controller. • In this data sheet, this HSYNC signal is also called 'input HSYNC'.
LOCK	Output	In this table, see the 'STATUS' pin name.
PDEN	Input	**Phase-Detector Enable.** This pin is the input for the Phase/Frequency Detector enable that can suspend the charge pump activity. It is 5-V tolerant. (For more information, see Reg 00:1-0 in Section 6.5.1, "Register 00h: Input Control Register".)
STATUS	Output	**Status (Formerly called 'Lock').** This active-low pin works with Reg 2C:1-0 and Reg 12:3-2. The signal on this pin is: • Low when a lock condition occurs for one of the PLLs selected by Reg 2C:1-0 or 12:3-2. • High when no lock condition occurs for one of the PLLs selected by Reg 2C:1-0 or 12:3-2.
XFILRET	Input	**External Filter Return.** This pin works with EXTFIL (in this table, see EXTFIL) and other components as part of an optional external filter for the pixel phase-locked loop.

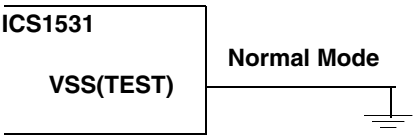
3.2.3.5 Industry-Standard 2-Wire Serial Bus Pins

Table 3-7. Industry-Standard 2-Wire Serial Bus Pins

Pin Name	Pin Type	Pin Description
SBADR	Input	**Serial Bus Address.** This pin determines the address for the ICS1531 industry-standard 2-wire serial bus. • When the signal on this pin is: – Low, the pixel bit address is 49h for read operations and 48h for write operations. – High, the pixel bit address is 4Bh for read operations and 4Ah for write operations. • For more information on this pin, see Section 2.9, "Industry-Standard 2-Wire Serial Interface".
SCL	Input	**Serial Clock.** This 5-V tolerant pin is the clock for the interface to an industry-standard 2-wire serial bus.
SDA	Input/ Output	**Serial Data.** This 5-V tolerant pin connects to the data pin for an industry-standard 2-wire serial bus.

3.2.3.6 Ground Pins

Table 3-8. Ground Pins

Pin Name	Pin Description
VSS	**Ground for (Analog Inputs for Digital Pixel PLL Circuitry).** • These pins are used to ground digital portions of the pixel PLL circuitry that receive analog inputs. • The VSSD pin must also be connected to these pins.
VSSA	**Ground for Analog (Pixel PLL Circuitry).** This pin is used to ground the analog portions of the pixel PLL circuitry.
VSSAADC	**Ground for Analog ADC (Circuitry).** These pins are used to ground the analog portions of the ADC.
VSSD	**Ground for Digital (Pixel PLL and Circuitry for Industry-Standard 2-Wire Serial Interface).** This pin is used to ground the digital portions of the pixel PLL circuitry and the circuitry for an industry-standard 2-wire serial interface.
VSSDADC	**Ground for Digital ADC (Circuitry).** This pin is used to ground the digital portions of the ADC.
VSSMCLK	**Ground for Memory Clock (Circuitry).** This pin is used to ground the circuitry for the memory clock PPL (that is, MCLK).
VSSPCLK	**Ground for Panel Clock (Circuitry).** This pin is used to ground the circuitry for the panel clock PLL (that is, PNLCLK).
VSSQ	**Ground for Output Drivers.** This pin is used to ground output drivers for the pixel PLL circuitry.
VSSQADC	**Ground for Output Drivers for ADC.** These pins are used to ground the pixel data output drivers for the analog-to-digital converter.
VSSSUB	**Ground for Substrate.** These pins are used to provide ground for the chip substrate.
VSS(TEST)	**Ground (Normal Mode) or Test Mode.** • Normal Mode. – Typically, this pin must be connected to ground (the Normal mode). – When the ICS1531 is in Normal mode, the Calibration registers 38h to 3Ch can be enabled by using Reg 37:3. (See Section 6.5.39, “Register 37h: PSEL”.)  **In Normal mode, use Reg 37:3 to enable Calibration Regs 38h to 3Ch.** • Test Mode. For the VSS(TEST) pin’s Test-mode function, see Table 3-4.
VSSXTL	**Ground for Crystal Oscillator.** This pin is used to ground the internal crystal oscillator circuitry.

3.2.3.7 Power Pins

Table 3-9. Power Pins

Pin Name	Pin Description
VDDA	**(3.3 V) Supply for Analog (Pixel PLL Circuitry).** This pin supplies 3.3 V to the analog portions of the pixel PLL circuitry.
VDDAADC	**(3.3 V) Supply for Analog ADC (Circuitry).** These pins supply 3.3 V to the analog portions of the ADC.
VDDD	**(3.3 V) Supply for Digital (Pixel PLL and Industry-Standard 2-Wire Serial Bus) Circuitry.** This pin supplies 3.3 V to the digital pixel PLL and circuitry for an industry-standard 2-wire serial bus interface.
VDDDADC	**(3.3 V) Supply for Digital ADC (Circuitry).** This pin supplies 3.3 V to digital portions of the ADC.
VDDMCLK	**(3.3 V) Supply for Memory Clock.** This pin supplies 3.3 V to the memory clock PLL circuitry.
VDDPCLK	**(3.3 V) Supply for Panel Clock.** This pin supplies 3.3 V to the panel clock PLL circuitry.
VDDQ	**(3.3 V) Supply for Output Drivers.** This pin supplies 3.3 V to the output driver circuitry for the pixel PLL.
VDDQADC	**(3.3 V) Supply for Output Drivers for Analog-to-Digital Converter.** These pins supply 3.3 V to the pixel data output drivers of the ADC.
VDDXTL	**(3.3V) Supply for Crystal Oscillator.** This pin supplies 3.3 V to the internal crystal oscillator circuitry.
VRB	**Voltage Reference Bottom.** The ADC uses this pin as a bottom reference voltage. Typically, this pin is grounded.
VRTB, VRTG, VRTR	**Voltage Reference Top Blue, Green, Red** • The ADC uses these pins as an alternative to the blue, green, and red top reference voltages from the internal DACs. • Each of these pins must connect to its own separate bypass capacitor.

3.2.3.8 No-Connect Pins

Table 3-10. No-Connect Pins

Pin Name	Pin Description
NC	**No Connect.** Do not connect these pins. **Caution:** Do not connect or use No-Connect pins. Connecting them can affect the performance and operation of the ICS1531 and future members of the ICS153X family.

3.2.3.9 Reserved Pins

Table 3-11. Reserved Pins

Pin Name	Pin Type	Pin Description
Reserved	–	**Reserved.** These pins are always reserved for use by ICS. **Caution:** Do not connect or use Reserved pins. Connecting them can affect the performance and operation of the ICS1531 and future members of the ICS153X family.

3.2.3.10 List of 5-V Tolerant Pins

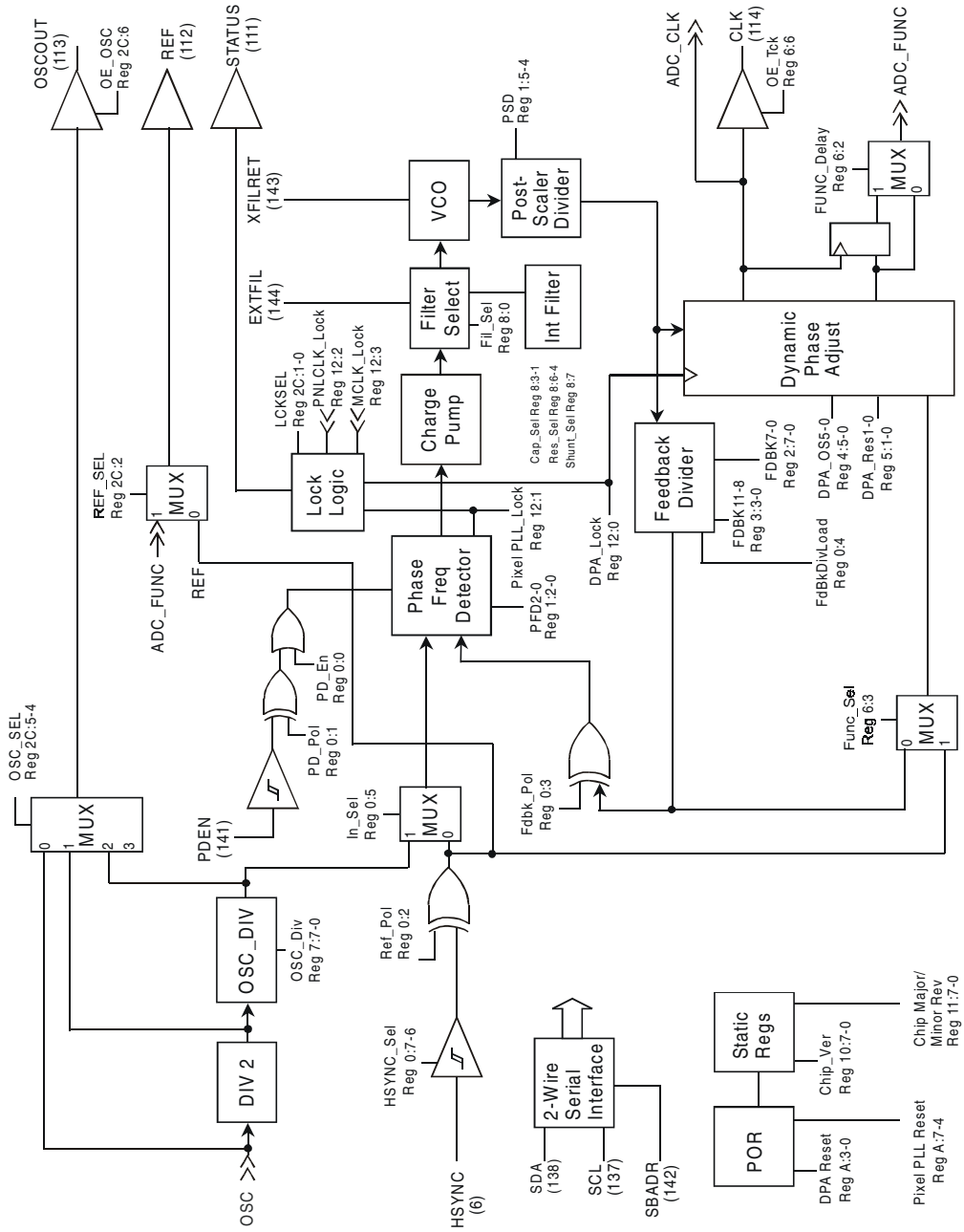
The following pins are 5-V tolerant:

- HSYNC (Table 3-6)
- PDEN (Table 3-6)
- SCL (Table 3-7)
- SDA (Table 3-7)
- TRESET (Table 3-4)

Chapter 4 Functional Blocks

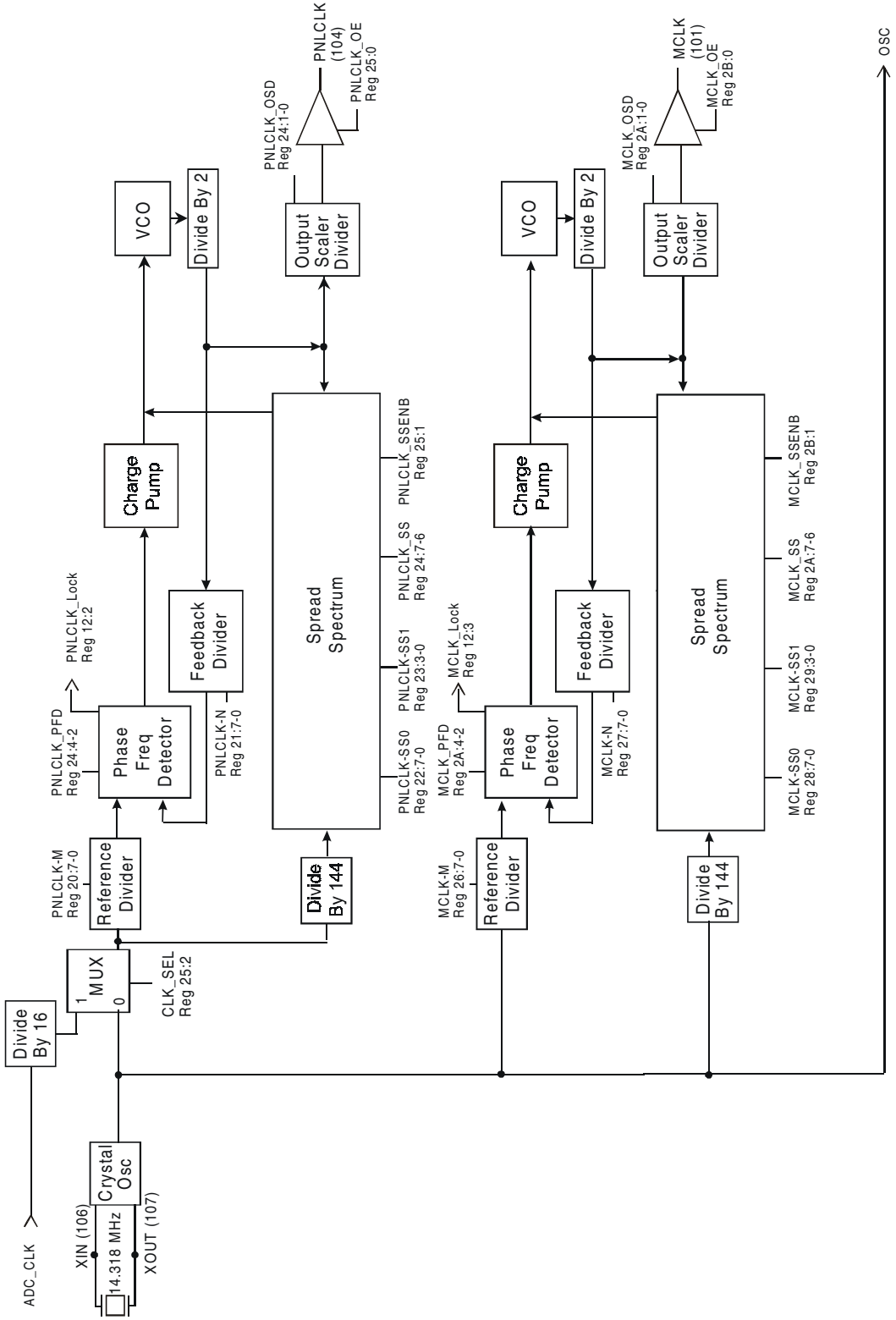
4.1 Pixel PLL Functional Block

Figure 4-1. Pixel PLL Block Diagram



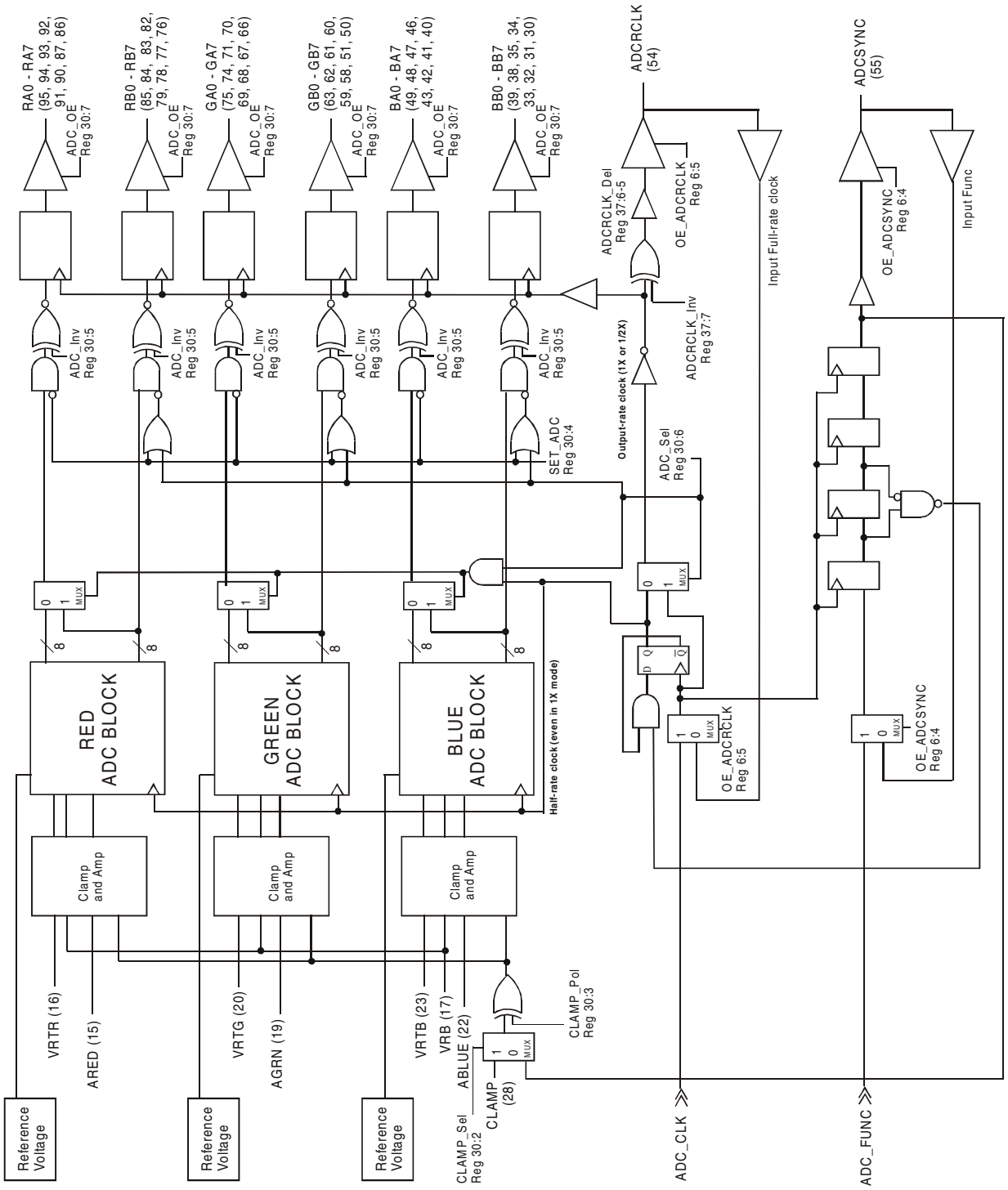
4.2 CLK Functional Block

Figure 4-2. CLK Block Diagram



4.3 ADC Functional Block

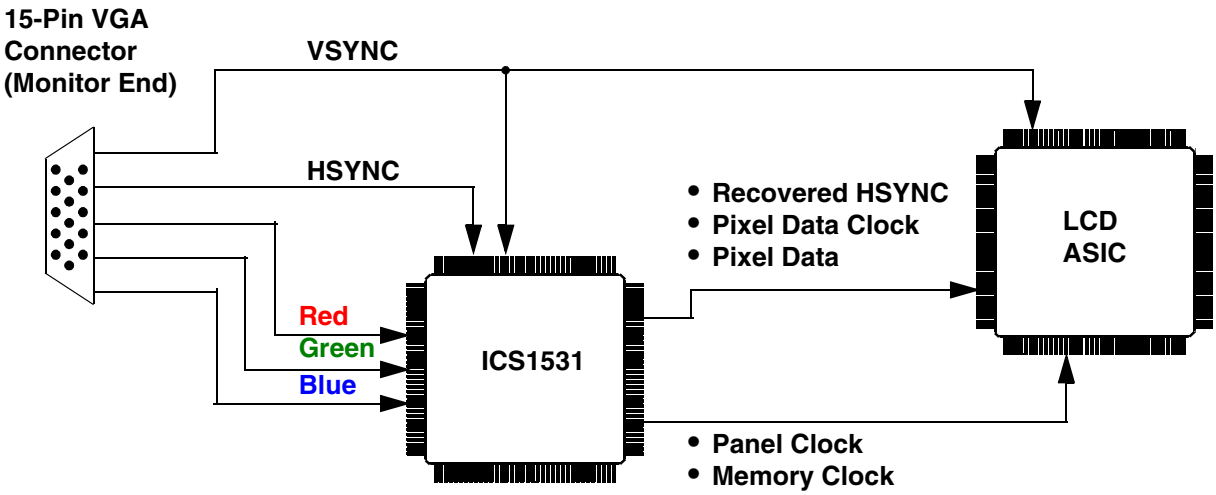
Figure 4-3. ADC Block Diagram



Chapter 5 Application Overview

Figure 5-1 shows a basic application for the ICS1531.

Figure 5-1. ICS1531 Application



Chapter 6 Register Set

The tables in this chapter detail the functionality of the bits in the ICS1531 Register Set. The tables include the register locations, the bit positions, names, and definitions, along with their read/write access, reset values, and any special functions or capabilities.

6.1 Reserved Bits

The ICS1531 has a number of reserved bits throughout the Register Set. These bits provide enhanced test functions (intended for use only by ICS manufacturing) and calibration functions (intended for use in production environments).

Important: The customer must not change the value of reserved bits. If the customer changes the default values of these reserved bits, normal operation of the ICS1531 can be affected.

6.2 Register Set Conventions

Register Set conventions include the following:

- Bits are listed in the order of most-significant bit (MSB) to least-significant bit (LSB).
- Unless otherwise indicated, bit settings are listed in terms of digital (and not hexadecimal) values.
- When a bit definition includes word(s) in parentheses, the word in parenthesis is not part of the bit name, but is given to explain the origin of the bit's name.

6.3 Register Set Abbreviations and Acronyms

Table 6-1 lists and defines abbreviations and acronyms used specifically in this chapter. (Table 1-1 lists other abbreviations and acronyms used throughout this data sheet.)

Table 6-1. Register Set Abbreviations and Acronyms

Abbreviation or Acronym	Definition
D-DPA	**Double-Buffered / Dynamic Phase Adjust.** Indicates double-buffered registers for which working registers load during a software Dynamic Phase Adjust reset.
D-MK	**Double-Buffered / Memory Clock.** Indicates double-buffered registers for which working registers load during a software MCLK reset.
D-PK	**Double-Buffered / Panel Clock.** Indicates double-buffered registers for which working registers load during a software PNLCLK reset.
D-PLL	**Double-Buffered / Phase-Locked Loop.** Indicates double-buffered registers for which working registers load during a software pixel PLL reset.
IN-A	**Increment All.** Indicates a value that increments with each all-layer revision of the ICS1531.
Reg	**Register**
R/W	**Read/Write**
Spec. Func.	**Special Function.** Indicates a special function, such as the following (listed in this table): D-DPA, D-MK, D-PK, D-PLL

6.4 Register Set Outline

Table 6-2 outlines the ICS1531 Register Set.

Note:

1. For the reserved bits, see Section 6.1, “Reserved Bits”.
2. For abbreviations and acronyms, see Section 6.3, “Register Set Abbreviations and Acronyms”.

Table 6-2. Register Set Outline

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
00h	Input Control	R/W	7-6	HSYNC_Sel	Select a Schmitt trigger	0
			5	In_Sel	Select input	1
			4	Fdbk Div Load	Select load for Feedback Divider	0
			3	Fdbk_Pol	Select polarity of feedback to Phase/Frequency Detector	0
			2	Ref_Pol	Select polarity of external reference	0
			1	PD_Pol	Select polarity of PDEN to Phase/Frequency Detector	0
			0	PD_En	Enable Phase/Frequency Detector	1
01h	Loop Control	R/W. D-PLL.	7-6	Reserved	Reserved	0
			5-4	PSD	Select value for Post-Scaler Divider	0
			3	Reserved	Reserved	0
			2-0	PFD	Select Phase/Frequency Detector gain	0
02h	Fdbk Div 0	R/W. D-PLL.	7-0	FDBK [7-0]	Select value for Feedback Divider LSBs bits 7-0	FF
03h	Fdbk Div 1	R/W. D-PLL.	7-4	Reserved	Reserved	–
			3-0	FDBK [11-8]	Select value for Feedback Divider MSBs bits 11-8	0
04h	DPA Offset	R/W	7-6	Reserved	Reserved	0
			5-0	DPA_OS	Select offset for Dynamic Phase Adjust	0
05h	DPA Control	R/W. D-DPA.	7-2	Reserved	Reserved	–
			1-0	DPA_Res	Select resolution for Dynamic Phase Adjust	0
06h	Output Enables	R/W	7	Reserved	Reserved	0
			6	OE_Tck	Enable clock output to ADC	0
			5	OE_ADCRCLK	Enable clock output from ADC	0
			4	OE_ADCSYNC	Enable output for delayed ADCSYNC	0
			3	FUNC_Sel	Select signal source for ADC_FUNC signal	0
			2	FUNC_Delay	Select delay for ADC_FUNC signal	0
			1-0	Reserved	Reserved	0
07h	OSC Divider	R/W	7-0	OSC_Div	Specify value for oscillator divider	0
08h	Internal Filter	R/W	7	Shunt_Sel	Select internal filter shunt capacitor size	1
			6-4	Res_Sel	Select internal filter resistor size	7
			3-1	Cap_Sel	Select internal filter capacitor size	7
			0	Fil_Sel	Select type of loop filter	1
09h	Reserved					N/A
0Ah	Pixel PLL Reset/ DPA Reset	Write	7-4	Pixel PLL Reset	Writing 5xh resets pixel PLL and loads working Regs 1h through 3h	N/A
			3-0	DPA Reset	Writing xAh resets DPA and loads working Reg 5h	N/A
0Bh-0Fh	Reserved					N/A

Table 6-2. Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
10h	Chip Ver	Read	7-0	Chip Ver	Read chip version 31 decimal (1F hex) as in 1531	1F
11h	Chip Rev	Read. IN-A.	7-4	Chip Major Rev	Read initial value 00h. +Value increments with chip revision.	00+
			3-0	Chip Minor Rev	Read initial value 01h. +Value increments with chip revision.	01+
12h	Rd_Reg	Read	7-4	Reserved	Reserved	N/A
			3	PNLCLK_Lock	Read PNLCLK lock status	N/A
			2	MCLK_Lock	Read MCLK lock status	N/A
			1	Pixel PLL_Lock	Read pixel PLL lock status	N/A
			0	DPA_Lock	Read DPA lock status	N/A
13h-1Fh	Reserved					N/A
20h	PNLCLK-M	R/W. D-PK.	7-0	PNLCLK_M	Select value for PNLCLK M Reference Divider	0
21h	PNLCLK-N	R/W. D-PK.	7-0	PNLCLK_N	Select value for PNLCLK N Feedback Divider	0
22h	PNLCLK-SS0	R/W. D-PK.	7-0	PNLCLK_SS0	Select value for PNLCLK spread-spectrum counter LSBs bits 7-0	0
23h	PNLCLK-SS1	R/W. D-PK.	7-4	Reserved	Reserved	0
			3-0	PNLCLK_SS1	Select value for PNLCLK spread-spectrum counter MSBs bits 11-8	0
24h	PNLCLK-SSOE	R/W. D-PK.	7-6	PNLCLK_SS	Select PNLCLK spread-spectrum gain	0
			5	Reserved	Reserved	0
			4-2	PNLCLK_PFD	Select PNLCLK Phase/Frequency Detector gain	0
			1-0	PNLCLK_OSD	Select value for PNLCLK Output Scaler Divider	0
25h	PNLCLK-OE	R/W	7-3	Reserved	Reserved	0
			2	CLK_SEL	Select input for PNLCLK PLL	0
			1	PNLCLK_SSENB	Enable PNLCLK spread-spectrum	0
			0	PNLCLK_OE	Enable PNLCLK output	0
26h	MCLK-M	R/W. D-MK.	7-0	MCLK_M	Select value for MCLK M Reference Divider	0
27h	MCLK-N	R/W. D-MK.	7-0	MCLK_N	Select value for MCLK N Feedback Divider	0
28h	MCLK-SS0	R/W. D-MK.	7-0	MCLK_SS0	Select MCLK spread-spectrum counter LSBs bits 7-0	0
29h	MCLK-SS1	R/W. D-MK.	7-4	Reserved	Reserved	0
			3-0	MCLK_SS1	Select MCLK spread-spectrum counter MSBs bits 11-8	0
2Ah	MCLK-SSOE	R/W. D-MK.	7-6	MCLK_SS	Select MCLK spread-spectrum gain	0
			5	Reserved	Reserved	0
			4-2	MCLK_PFD	Select MCLK Phase/Frequency Detector gain	0
			1-0	MCLK_OSD	Select value for MCLK Output Scaler Divider	0
2Bh	MCLK-OE	R/W	7-2	Reserved	Reserved	0
			1	MCLK_SSENB	Enable MCLK spread-spectrum	0
			0	MCLK_OE	Enable MCLK output	0

Table 6-2. Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
2Ch	OUTPUT MUX	R/W	7	High_Drive	Select drive strength for all ADC outputs	0
			6	OE_OSC	Enable OSCOUT output	1
			5-4	OSC_Sel	Select output from 4-way MUX to OSCOUT	0
			3	Reserved	Reserved	0
			2	REFSEL	Select REF status	0
			1-0	LCKSEL	Select PLL lock status	1
2Dh	PLL Reset	Write	7-4	MCLK_Reset	Writing 5xh resets MCLK PLL and loads working Regs 26h to 2Bh.	N/A
			3-0	PNLCLK_Reset	Writing xAh resets PNLCLK PLL and loads working Regs 20h to 25h.	N/A
2Eh-2Fh	Reserved					N/A
30h	ADC CTRL	R/W	7	ADC_OE	Enable ADC output	0
			6	ADC_Sel	Select ADC capture	0
			5	ADC_Inv	Invert ADC outputs	1
			4	Force_ADC	Force all ADC output buffers off	0
			3	CLAMP_Pol	Select polarity of signal to a clamp	0
			2	CLAMP_Sel	Select source to a clamp	0
			1	VA_Disable	Disable video amplifier	0
			0	FA_Disable	Disable fine adjust	0
31h	R_COARSE	R/W	7-6	Reserved	Reserved	0
			5	Reserved	Reserved	1
			4-2	Reserved	Reserved	0
			1-0	R_Coarse_Adj	Adjust video amplifier gain to red channel of ADC	0
32h	G_COARSE	R/W	7-6	Reserved	Reserved	0
			5	Reserved	Reserved	1
			4-2	Reserved	Reserved	0
			1-0	G_Coarse_Adj	Adjust video amplifier gain to green channel of ADC	0
33h	B_COARSE	R/W	7-6	Reserved	Reserved	0
			5	Reserved	Reserved	1
			4-2	Reserved	Reserved	0
			1-0	B_Coarse_Adj	Adjust video amplifier gain to blue channel of ADC	0
34h	R_FINE	R/W	7-0	R_Fine_Adj	Adjust VRT for red channel of ADC	20
35h	G_FINE	R/W	7-0	G_Fine_Adj	Adjust VRT for green channel of ADC	20
36h	B_FINE	R/W	7-0	B_Fine_Adj	Adjust VRT for red channel of ADC	20
37h	PSEL	R/W	7	ADCRCLK_Inv	Invert ADCRCLK signal	1
			6-5	ADCRCLK_Del	Delay ADCRCLK signal	2
			4	Reserved	Reserved	0
			3	Cal_Access	Select access to Calibration/Test Regs	0
			2	PSEL3	Select general-purpose programmable output 3	0
			1	PSEL2	Select general-purpose programmable output 2	0
			0	PSEL1	Select general-purpose programmable output 1	0
38h	R_COMP_OFF	R/W	7-4	R_C_O_B	Select red comparator offset, ‘B’ channel	7
			3-0	R_C_O_A	Select red comparator offset, ‘A’ channel	7
39h	G_COMP_OFF	R/W	7-4	G_C_O_B	Select green comparator offset, ‘B’ channel	7
			3-0	G_C_O_A	Select green comparator offset, ‘A’ channel	7

Table 6-2. Register Set Outline (*Continued*)

Register Index	Register Name	Register Access	Bit #	Bit Name	Brief Description	Reset Value
3Ah	B_COMP_OFF	R/W	7-4	B_C_O_B	Select blue comparator offset, 'B' channel	7
			3-0	B_C_O_A	Select blue comparator offset, 'A' channel	7
3Bh	CAL_1	R/W	7	Reserved	Reserved	0
			6	ADC_DD	Select delay for all RGB data from ADC (LSB, bit 0)	0
			5-3	G_CD	Select clock delay for green channel	5
			2-0	R_CD	Select clock delay for red channel	5
3Ch	CAL_2	R/W	7-5	Bandgap_CAL	Calibrate bandgap voltage	5
			4-3	ADC_DD	Select delay for all RGB data from ADC (MSB bits 2-1)	0
			2-0	B_CD	Select clock delay for blue channel	5

6.5 Register Definitions

The tables in this section specify for each register bit the reset value, if one exists. After a reset, the ICS1531 sets all register bits to their default values.

Note:

1. For the reserved bits, see Section 6.1, “Reserved Bits”.
2. For Register Set conventions, see Section 6.2, “Register Set Conventions”.
3. For acronyms used in this table, see Section 6.3, “Register Set Abbreviations and Acronyms”.

6.5.1 Register 00h: Input Control Register

The Input Control Register is used to select inputs that control the pixel PLL Phase/Frequency Detector.

Table 6-3. Input Control Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
00:7-00:6	HSYNC_Sel [1-0]	**Horizontal Sync Select [1-0].** These multiplexed bits select one of possible four Schmitt triggers that connect to the input HSYNC pin. • 0 = Schmitt trigger 0 • 1 = Schmitt trigger 1 • 2 = Schmitt trigger 2. (Recommended setting.) • 3 = Schmitt trigger 3	–	–	0
00:5	In_Sel	**Input Select.** This bit selects an input to the Phase/Frequency Detector. • 0 = The input is HSYNC. • 1 = The input is OSC (default).	–	–	1
00:4	Fdbk Div Load	**Feedback Divider Load Control.** This bit selects a load for the internal feedback divider. • 0 = The load is on the pixel PLL reset. • 1 = The load is on the next scan line.	R/W	–	0
00:3	Fdbk_Pol	**Feedback Polarity.** This bit selects the polarity of the feedback signal to the Phase/ Frequency Detector. • 0 = The polarity is positive edge. • 1 = The polarity is negative edge.	R/W	–	0
00:2	Ref_Pol	**(External) Reference Polarity.** This bit selects the polarity of REF, the reference signal provided by the input HSYNC to the Phase/Frequency Detector. • 0 = The polarity is positive edge. • 1 = The polarity is negative edge.	R/W	–	0
00:1	PD_Pol	**Phase/(Frequency) Detector Polarity.** This bit selects the polarity of the PDEN signal to the Phase/Frequency Detector. • 0 = The signal from the PDEN pin is active high. • 1 = The signal from the PDEN pin is active low. **Note:** This bit is disabled when Reg 00:0 = 1.	R/W	–	0

Table 6-3. Input Control Register (*Continued*)

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
00:0	PD_En	**Phase/(Frequency) Detector Enable.** This bit is used to enable the Phase/Frequency Detector. Typically, the signal for this bit is from the source of the VSYNC signal to a display. • 0 = The Phase/Frequency Detector is disabled temporarily and 'coasts' (that is, it continues to be disabled) as long as the signal from the PDEN pin is in an active state. (See Reg 00:1). • 1 = The Phase/Frequency Detector is enabled regardless of the PDEN pin state. (This state overrides Reg 00:1.)	R/W	–	1

6.5.2 Register 01h: Loop Control Register

The Loop Control Register is used to control the pixel PLL.

Table 6-4. Loop Control Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
01:7-01:6	Reserved	**Reserved.** • See Section 6.1, "Reserved Bits". • These bits can be programmed to '0'.	–	–	0
01:5-01:4	PSD [1-0]	**Post-Scaler Divider [1-0].** • These bits select the division value for the Post-Scaler Divider (PSD). • By dividing the frequency output from the voltage-controlled oscillator (VCO), the PSD can set the ratio of the VCO frequency output to the pixel clock frequency as follows. – 0 = Division is by 2, so the ratio is 2:1. – 1 = Division is by 4, so the ratio is 4:1. – 2 = Division is by 8, so the ratio is 8:1. – 3 = Division is by 16, so the ratio is 16:1.	R/W	D-PLL	0
01:3	Reserved	**Reserved.** • See Section 6.1, "Reserved Bits". • This bit can be programmed to '0'.	–	–	0
01:2-01:0	PFD [2-0]	**Phase/Frequency Detector (Gain) [2-0].** These bits select the gain (that is, µA/2πrad) for the Phase/Frequency Detector. • 0 = PFD gain selected is 1 µA. • 1 = PFD gain selected is 2 µA. • 2 = PFD gain selected is 4 µA. • 3 = PFD gain selected is 8 µA. • 4 = PFD gain selected is 16 µA. • 5 = PFD gain selected is 32 µA. • 6 = PFD gain selected is 64 µA. • 7 = PFD gain selected is 128 µA.	R/W	D-PLL	0

6.5.3 Register 02h: Fdbk Div 0 Register

The Fdbk Div 0 (Feedback Divider 0) Register, in combination with Fdbk Div 1 Register, sets the value of the internal feedback divider for the pixel PLL. It adjusts the number of pixel clocks by using the horizontal total, where:

Horizontal Total = [(Number of displayed pixels) + (Horizontal blanking interval)] per HSYNC

Table 6-5. Fdbk Div 0 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
02:7-02:0	FDBK [7–0]	**(Pixel PLL) Feedback Divider [7-0].** • These bits are the least-significant bits [7-0] for the internal pixel PLL Feedback Divider. (See Table 6-6 and Figure 6-1, the Feedback Divider Modulus.) • When bit 0 is: – 0 = The total number of pixels is even. – 1 = The total number of pixels is odd.	R/W	D-PLL	FF

6.5.4 Register 03h: Fdbk Div 1 Register

The Fdbk Div 1 (Feedback Divider 1) Register is used in combination with Fdbk Div 0 Register.

Table 6-6. Fdbk Div 1 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
03:7-03:4	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	–
03:3-03:0	FDBK [11-8]	**(Pixel PLL) Feedback Divider [11-8].** • These bits are the most-significant bits [11-8] for the internal pixel PLL Feedback Divider. (See Table 6-5.) • For the total number of clock periods that the ICS1531 generates between successive HSYNCs, do the following: – See Figure 6-1. – Obtain the Feedback Divider Modulus value as follows: 1. Program the Feedback Divider 0 and Feedback Divider 1 registers with the total number of horizontal pixels per line. 2. Add 8. **Note:** The ICS1531 generates 8 more clocks than what is programmed in these bits.	R/W	D-PLL	0

Figure 6-1. Feedback Divider Modulus

Feedback Divider Modulus =

Fdbk Div 1 (Reg 3)				Fdbk Div 0 (Reg 2)							
3	2	1	0	7	6	5	4	3	2	1	0

+ 8

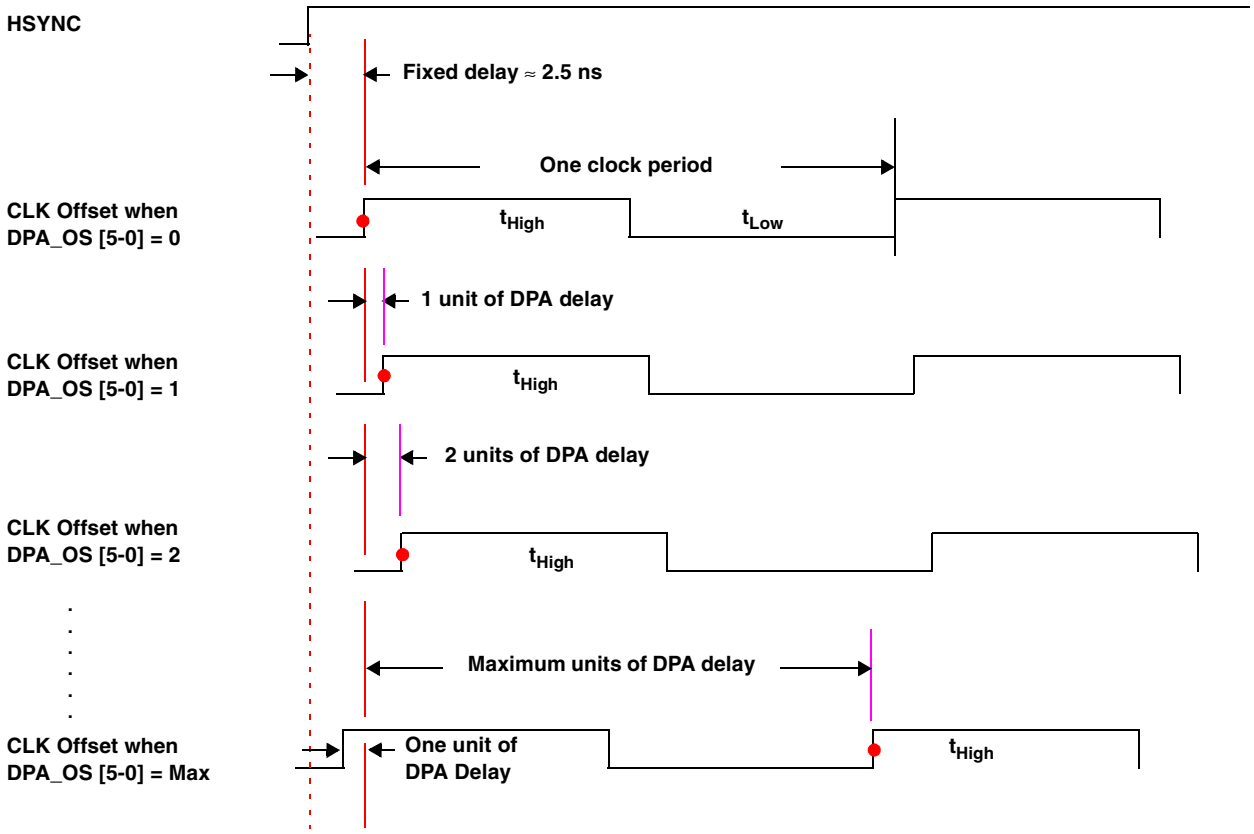
6.5.5 Register 04h: DPA Offset

The DPA Offset (Dynamic Phase Adjust Offset) Register is used to select the clock edge offset.

Table 6-7. DPA Offset Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
04:7-04:6	Reserved	**Reserved.** • See Section 6.1, "Reserved Bits". • These bits can be programmed to '0'.	–	–	0
04:5-04:0	DPA_OS [5-0]	**Dynamic Phase Adjust Offset [5-0].** As Figure 6-2 shows, these bits control the amount of offset between the rising edge of the **recovered** HSYNC and the rising edge of CLK. • The offset is in discrete steps from 0 clock periods up to 1 clock period, minus one unit of a DPA delay. • The unit of the DPA delay depends on both the pixel clock output frequency and the number of delay element units (as selected by Reg 05:1-0).	R/W	–	0

Figure 6-2. DPA Offset (As Determined by Regs 04 and 05)



6.5.6 Register 05h: DPA Control

The DPA Control (Dynamic Phase Adjust Control) Register is used to select the resolution of the Dynamic Phase Adjust circuitry, used to adjust the pixel clock on a sub-pixel basis.

Table 6-8. DPA Control Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
05:7-05:2	Reserved	**Reserved.** • See Section 6.1, "Reserved Bits". • These bits can be programmed to '0'.	–	–	–
05:1-05:0	DPA_Res [1-0]	**Dynamic Phase Adjust Resolution [1-0].** These bits select the resolution of (that is, the number of delay element units) for the Dynamic Phase Adjust Offset of Reg 04:5-0. Table 6-9 lists, for the Reg 05 bit settings: 1. The resulting (decimal) number of delay element units • 0 = The resolution is for 16 delay element units. • 1 = The resolution is for 32 delay element units. • 2 = Reserved. • 3 = The resolution is for 64 delay element units. 2. The corresponding maximum values for Reg 04 DPA offset 3. The corresponding pixel clock output frequency ranges. **Important:** (ICS does not recommend using the DPA above 260 MHz.)	R/W	D-DPA	0

Table 6-9. DPA Control

Reg 05:1-0		(1) Number of Delay Element Units (Decimal)	(2) Reg 04:5-0 Max. Value (Hex)	(3) Pixel Clock Range (MHz)
Bit 1	Bit 0			
0	0	16	0F	55 – 260
0	1	32	1F	27 – 130
1	0	Reserved	Reserved	
1	1	64	3F	14 – 64

6.5.7 Register 06h: Output Enables

The Output Enables Register is used to select and enable various outputs.

Note: Table 6-10 refers to ADC_FUNC, an internally generated signal that is delayed so it is in the same domain as the internal ADC_CLK signal (that is, the pixel clock). Functionally, depending on the setting of Reg 06:3, ADC_FUNC is equivalent to either ADCSYNC (which provides recovered HSYNC) or the input HSYNC.

Table 6-10. Output Enables Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
06:7	Reserved	**Reserved.** • See Section 6.1, "Reserved Bits". • This bit can be programmed to '0'.	–	–	0
06:6	OE_Tck	**Output Enable Clock.** This bit enables the pixel clock output on the CLK pin. • 0 = The pixel clock output is disabled (high- impedance). • 1 = The pixel clock output is enabled.	–	–	0
06:5	OE_ADCRCLK	**Output Enable for ADCRCLK.** This bit enables the clock output for ADCRCLK. When this bit is: • 0 = The following are both true: – The clock output for the ADC is disabled (that is, high-impedance). – Because the clock source for the ADC is accepted from the ADCRCLK pin, an external clock can be provided to the ADC. • 1 = The following are both true: – The clock output for the ADC is enabled. – The input multiplexer selects the internal pixel clock.	–	–	0
06:4	OE_ADCSYNC	**Output Enable for ADCSYNC.** This bit enables the output for ADCSYNC. When this bit is: • 0 = The following are both true: – The output for the ADCSYNC signal is disabled (high-impedance). – An external sync signal for the ADC is accepted from the ADCSYNC pin. • 1 = The following are both true: – The output for the ADCSYNC signal is enabled. – The input multiplexer selects the internal sync signal.	R/W	–	0
06:3	FUNC_Sel	**FUNC Select.** This bit selects the source of the signal to ADC_FUNC. (See the note at the first of this table.) • 0 = The source is recovered HSYNC. • 1 = The source is REF, the input HYSNC signal that is conditioned before it goes to the phase-locked loop block.	–	–	0

Table 6-10. Output Enables Register (*Continued*)

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
06:2	FUNC_Delay	**FUNC Delay.** This bit selects the delay for the ADC_FUNC signal. (See the note at the first of this table.) • 0 = The ADC_FUNC signal is delayed by 0 cycles. • 1 = The ADC_FUNC signal is delayed by 1 cycle, which has the effect of moving the channel ‘A” data to the ‘B’ channel output pins and the reverse.	R/W	–	0
06:1-06:0	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0

6.5.8 Register 07h: OSC Divider

Table 6-11. OSC Divider Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
07:7-07:0	OSC_Div [7-0]	**Oscillator Divider [7-0].** After the signal from the internal crystal oscillator is divided by 2 (see Figure 4-1), these bits select the value by which the resulting signal is divided. • 0 = This divide-down value is reserved. • 1 = Divide by 1. • 2 = Divide by 2, and so forth.	R/W	–	0

6.5.9 Register 08h: Internal Filter

The Internal Filter Register is used to select values for the internal loop filter.

Table 6-12. Internal Filter Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
08:7	Shunt_Sel	**Shunt (Capacitor) Select.** This bit selects the size of the internal filter's shunt capacitor. • 0 = Selects an alternate-size shunt capacitor • 1 = Select the default-size shunt capacitor	R/W	–	1
08:6-08:4	Res_Sel [2-0]	**Resistor Select [2-0].** These bits are used to select the size of the internal filter's resistor as follows: Resistor value $\approx$ {(Value of Res_Sel [2-0] bits) $\times$ 4kΩ} + 3kΩ	R/W	–	7
08:3-08:1	Cap_Sel [2-0]	**Capacitor Select [2-0].** These bits are used to select the size of the internal filter's capacitor as follows: Capacitor value: $\approx$ {(Value of Cap_Sel [2-0] bits) + 1} $\times$ 236 pF	R/W	–	7
08:0	Fil_Sel	**(Loop) Filter Select.** This bit selects the type of loop filter. • 0 = The loop filter is external. • 1 = The loop filter is internal (default).	R/W	–	1

6.5.10 Register 09h: Reserved

This register is reserved. (See Section 6.1, "Reserved Bits".)

6.5.11 Register 0Ah: Pixel PLL/DPA Reset

The Pixel PLL/DPA Reset Register is used to reset the pixel PLL and DPA circuits.

Table 6-13. Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
0A:7-0A:4	Pixel PLL Reset [3-0]	**Pixel Phase-Locked Loop Reset [3-0].** Writing 5xh to these bits does the following: • Resets the pixel phase-locked loop. • Loads working Regs 01 to 03.	Write	–	N/A
0A:3-0A:0	DPA Reset [3-0]	**Dynamic Phase Adjust Reset [3-0].** Writing xAh to these bits does the following: • Resets the Dynamic Phase Adjust. • Loads working Reg 05.	Write	–	N/A

6.5.12 Register 0Bh-0Fh: Reserved

These registers are reserved. (See Section 6.1, "Reserved Bits".)

6.5.13 Register 10h: Chip Ver

The Chip Ver (Chip Version) Register is used to read the version number of the ICS1531.

Table 6-14. Chip Ver Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
10:7-10:0	Chip Ver [7-0]	**Chip Version [7-0].** • This register indicates the version number of the ICS chip. • For the ICS1531, these bits have a value of 31 decimal (that is, 1F hex), as in 1531.	Read	–	1F

6.5.14 Register 11h: Chip Rev

The Chip Rev (Chip Revision) Register is used to read the revision level of the ICS1531 chip.

Table 6-15. Chip Rev Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
11:7-11:4	Chip Major Rev [3-0]	**Chip Major Revision [3-0].** The value of these bits: • Indicate a ICS1531 major revision. • Increment (+) with each all-layer revision. • Have an initial (reset) value of 00h.	Read	IN-A	00+
11:3-11:0	Chip Minor Rev [3-0]	**Chip Minor Revision [3-0].** The value of these bits: • Indicate a ICS1531 minor revision. • Increment (+) with each all-layer revision. • Have an initial (reset) value of 01h.	Read	IN-A	01+

6.5.15 Register 12h: Rd_Reg

The Rd_Reg (Read Register) is used to read the lock status of the four PLLs on the ICS1531.

Table 6-16. Rd_Reg Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
12:7-12:4	Reserved	**Reserved.** Because these bits are read-only: • These bits cannot be programmed. • Information on these bits can be ignored.	Read	–	N/A
12:3	PNLCLK_Lock	**PNLCLK Lock (Status).** • 0 = The PNLCLK is 'unlocked'. • 1 = The PNLCLK is 'locked'.	Read	–	N/A
12:2	MCLK_Lock	**MCLK Lock (Status).** • 0 = The MCLK is 'unlocked'. • 1 = The MCLK is 'locked'.	Read	–	N/A
12:1	Pixel PLL_Lock	**Pixel Phase-Locked Loop Lock (Status).** • 0 = The pixel PLL is 'unlocked'. • 1 = The pixel PLL is 'locked'.	Read	–	N/A
12:0	DPA_Lock	**Dynamic Phase Adjust Lock (Status).** • 0 = The DPA is 'unlocked'. • 1 = The DPA is 'locked'.	Read	–	N/A

6.5.16 Register 13h-1Fh: Reserved

These registers are reserved. (See Section 6.1, "Reserved Bits".)

6.5.17 Register 20h: PNLCLK-M

The PNLCLK-M Register is used to divide the reference frequency provided to the PNLCLK PLL. The 'M' value is used to determine the output frequency of the PLL as specified in the equation given in Section 6.5.18, "Register 21h: PNLCLK-N".

Table 6-17. PNLCLK-M Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
20:7-20:0	PNLCLK_M [7-0]	**PNLCLK_M (Reference Divider) [7-0].** • This register includes bits for the PNLCLK Reference Divider. • The value in this register is used as the variable 'M' in the frequency equation given in Section 6.5.18, "Register 21h: PNLCLK-N".	R/W	D-PK	0

6.5.18 Register 21h: PNLCLK-N

The PNLCLK-N Register is used to determine the output frequency of the PNLCLK.

Table 6-18. PNLCLK-N Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
21:7-21:0	PNLCLK_N [7-0]	**PNLCLK_N (Feedback Divider) [7-0].** • This register includes bits for the PNLCLK Feedback Divider. • The value in this register is used as the variable 'N' in the frequency equation for the PNLCLK.	R/W	D-PK	0

To determine the PNLCLK frequency (which is in units of MHz), use the following equation:

$$F_{PNLCLK} = \frac{OSC \times (N + 8)}{(M + 2)}$$

6.5.19 Register 22h: PNLCLK-SS0

The PNLCLK-SS0 (PNLCLK Spread-Spectrum Counter 0) Register is used in combination with the PNLCLK-SS1 Register to specify the amount of clock spread. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-19. PNLCLK-SS0 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
22:7-22:0	PNLCLK_SS0 [7-0]	**PNLCLK Spread-Spectrum (Counter) 0 [7-0].** These bits are the least-significant bits [7-0] for the PNLCLK spread-spectrum counter.	R/W	D-PK	0

6.5.20 Register 23h: PNLCLK-SS1

The PNLCLK-SS1 (PNLCLK Spread-Spectrum Counter 1) Register is used in combination with the PNLCLK-SS0 Register. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-20. PNLCLK-SS1 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
23:7-23:4	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
23:3-23:0	PNLCLK_SS1 [3-0]	**PNLCLK Spread-Spectrum (Counter) 1 [3-0].** These bits are the most-significant bits [11-8] for the PNLCLK spread-spectrum counter.	R/W	D-PK	0

6.5.21 Register 24h: PNLCLK-SSOE

The PNLCLK-SSOE (PNLCLK Spread-Spectrum Output Enable) Register is used to control the gain of the PNLCLK PFD and spread spectrum. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-21. PNLCLK-SSOE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
24:7-24:6	PNLCLK_SS [1-0]	**PNLCLK Spread-Spectrum (Gain Select) [1-0].** These bits determine the PNLCLK spread-spectrum gain. • 0 = The gain is 1. • 1 = The gain is 2. • 2 = The gain is 4. • 3 = The gain is 8.	R/W	D-PK	0
24:5	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • This bit can be programmed to ‘0’.	–	–	0
24:4-24:2	PNLCLK_PFD [2-0]	**PNLCLK Phase/Frequency Detector (Gain Select) [2-0].** These bits determine the PNLCLK Phase/Frequency Detector gain. • 0 = The gain is 1. • 1 = The gain is 2. • 2 = The gain is 4. • 3 = The gain is 8. • 4 = The gain is 16, and so forth.	R/W	D-PK	0
24:1-24:0	PNLCLK_OSD [1-0]	**PNLCLK Output Scaler Divider (Value) [1-0].** These bits determine the value for dividing the PNLCLK output scaler as follows: • 0 = Division is by 1. • 1 = Division is by 2. • 2 = Division is by 4. • 3 = Division is by 8.	R/W	D-PK	0

6.5.22 Register 25h: PNLCLK-OE

The PNLCLK-OE (PNLCLK Output Enable) Register is used to enable the PNLCLK output and spread-spectrum functionality. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-22. PNLCLK-OE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
25:7-25:3	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
25:2	CLK_SEL	**Clock Selection.** This bit selects the input to the PNLCLK phase-lock loop. • 0 = Frequency input is from a crystal. • 1 = Frequency input is from ADC_CLK, divided by 16.	R/W	–	0
25:1	PNLCLK_SSENB	**PNLCLK Spread-Spectrum Enable.** • 0 = Disable PNLCLK spread-spectrum functionality. • 1 = Enable PNLCLK spread-spectrum functionality.	R/W	–	0
25:0	PNLCLK_OE	**PNLCLK Output Enable.** • 0 = Disable PNLCLK output. • 1 = Enable PNLCLK output.	R/W	–	0

6.5.23 Register 26h: MCLK-M

The MCLK-M Register is used to divide the reference frequency provided to the MCLK PLL. The 'M' value is used to determine the output frequency of the PLL as specified in the equation given in Section 6.5.24, "Register 27h: MCLK-N".

Table 6-23. MCLK-M Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
26:7-26:0	MCLK_M [7-0]	**MCLK M (Reference Divider) [7-0].** • This register includes bits for the MCLK Reference Divider. • The value in this register is used as the variable 'M' in the frequency equation given in Section 6.5.24, "Register 27h: MCLK-N".	R/W	D-MK	0

6.5.24 Register 27h: MCLK-N

The MCLK-N Register is used to determine the output frequency of the MCLK.

Table 6-24. MCLK-N Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
27:7-27:0	MCLK_N [7-0]	**MCLK N (Feedback Divider) [7-0].** • This register includes bits for the MCLK Feedback Divider. • The value in this register is used as the variable 'N' in the frequency equation for the MCLK.	R/W	D-MK	0

To determine the MCLK frequency (which is in units of MHz), use the following equation:

$$F_{MCLK} = \frac{OSC \times (N + 8)}{(M + 2)}$$

6.5.25 Register 28h: MCLK-SS0

The MCLK-SS0 (MCLK Spread-Spectrum Counter 0) Register is used in combination with the MCLK-SS1 Register to specify the amount of clock spread. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-25. MCLK-SS0 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
28:7-28:0	MCLK_SS0 [7-0]	**MCLK Spread-Spectrum (Counter) 0 [7-0].** These bits are the least-significant bits [7-0] for the MCLK spread-spectrum counter.	R/W	D-MK	0

6.5.26 Register 29h: MCLK-SS1

The MCLK-SS1 (MCLK Spread-Spectrum Counter 1) Register is used in combination with the MCLK-SS0 Register. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-26. MCLK-SS1 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
29:7-29:4	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
29:3-29:0	MCLK_SS1 [3-0]	**MCLK Spread-Spectrum (Counter) 1 [3-0].** These bits are the most-significant bits [11-8] for the MCLK spread-spectrum counter.	R/W	D-MK	0

6.5.27 Register 2Ah: MCLK-SSOE

The MCLK-SSOE (MCLK Spread Spectrum Output Enable) Register is used to control the gain of the MCLK PFD and spread spectrum. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-27. MCLK-SSOE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
2A:7-2A:6	MCLK_SS [1-0]	**MCLK Spread-Spectrum (Gain Select) [1-0].** • 0 = The gain is 1. • 1 = The gain is 2. • 2 = The gain is 4. • 3 = The gain is 8.	R/W	D-MK	0
2A:5	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • This bit can be programmed to ‘0’.	–	–	0
2A:4-2A:2	MCLK_PFD [2-0]	**MCLK Phase/Frequency Detector (Gain Select) [2-0].** These bits determine the gain for the MCLK Phase/Frequency Detector. • 0 = The gain is 1. • 1 = The gain is 2. • 2 = The gain is 4. • 3 = The gain is 8. • 4 = The gain is 16, and so forth.	R/W	D-MK	0
2A:1-2A:0	MCLK_OSD [1-0]	**MCLK Output Scaler Divider [1-0].** These bits determine the value for dividing the MCLK output scaler. • 0 = Division is by 1. • 1 = Division is by 2. • 2 = Division is by 4. • 3 = Division is by 8.	R/W	D-MK	0

6.5.28 Register 2Bh: MCLK-OE

The MCLK-OE (MCLK Output Enable) Register is used to enable the MCLK output and spread-spectrum functionality. (To select values, see Section 7.3, “Programming Spread Spectrum”.)

Table 6-28. MCLK-OE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
2B:7-2B:2	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
2B:1	MCLK_SSENB	**MCLK Spread-Spectrum Enable.** • 0 = Disable MCLK spread-spectrum functionality. • 1 = Enable MCLK spread-spectrum functionality.	R/W	–	0
2B:0	MCLK_OE	**MCLK Output Enable.** • 0 = Disable MCLK output. • 1 = Enable MCLK output.	R/W	–	0

6.5.29 Register 2Ch: OUTPUT MUX

The OUTPUT MUX Register is used to select the source for the REF pin and STATUS pin (an active-low pin formerly called 'LOCK').

Table 6-29 refers to ADC_FUNC, an internally generated signal that is delayed so it is in the same domain as the internal ADC_CLK signal. Functionally, depending on the setting of Reg 06:3, ADC_FUNC is equivalent to either ADCSYNC (which provides recovered HSYNC) or the input HSYNC.

Table 6-29. OUTPUT MUX Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
2C:7	High_Drive	**High Drive.** This bit selects a drive strength for all analog-to-digital converter outputs. • 0 = Drive strength is normal strength. • 1 = Drive strength is doubled.	–	–	0
2C:6	OE_OSC	**Output Enable for OSCOUT.** • 0 = Disable OSCOUT output. • 1 = Enable OSCOUT output.	R/W	–	1
2C:5-2C:4	OSC_Sel [1-0]	**OSCOUT (Multiplexer) Select [1-0].** These bits select the output from a 4-way multiplexer (MUX) to the OSCOUT pin. • 0 = The OSCOUT source is OSC. • 1 = The OSCOUT source is OSC/2. • 2 = The OSCOUT source is OSCDIVIDER. • 3 = The OSCOUT source is a reserved value.	R/W	–	0
2C:3	Reserved	**Reserved.** • See Section 6.1, "Reserved Bits". • This bit must be programmed to '0'.	–	–	0
2C:2	REF_Sel	**REF (Status) Select.** This bit selects the REF pin reference output as follows: • 0 = The REF output source is from the input to the pixel PLL PDINPUT (the Phase/Frequency Detector Input). • 1 = The REF output source is from ADC_FUNC. (For more information on ADC_FUNC, see Section 6.5.7, "Register 06h: Output Enables".)	R/W	–	0
2C:1-2C:0	LCKSEL [1-0]	**(PLL) Lock (Status) Select [1-0].** These bits select the lock status output for the active-low STATUS pin (formerly called 'LOCK'.) • 0 = The lock status output is for the pixel PLL. • 1 = The lock status output is for the Dynamic Phase Adjust. • 2 = The lock status output is for PNLCLK. • 3 = The lock status output is for MCLK.	R/W	–	1

6.5.30 Register 2Dh: PLL Reset

The PLL Reset (Phase-Locked Loop Reset) Register is used to reset the MCLK and PNLCLK PLLs.

Table 6-30. PLL Reset Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
2D:7-2D:4	MCLK_Reset [3-0]	**MCLK Reset [3-0].** Writing 5xh to these bits: • Resets MCLK PLL. • Loads working Regs 26h to 2Bh.	Write	–	N/A
2D:3-2D:0	PNLCLK_Reset [3-0]	**PNLCLK Reset [3-0].** Writing xAh to these bits: • Resets PNLCLK PLL. • Loads working Regs 20h to 25h.	Write	–	N/A

6.5.31 Register 2Eh-2Fh: Reserved

These registers are reserved. (See Section 6.1, “Reserved Bits”.)

6.5.32 Register 30h: ADC CTRL

The ADC CTRL (Analog-to-Digital Converter Control) Register is used to control the ADC.

Table 6-31. ADC CTRL Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
30:7	ADC_OE	**Analog-to-Digital Converter (Digital) Outputs Enable.** This bit enables the ADC digital outputs. • 0 = The ADC digital outputs are disabled. (The ICS1531 output pads are high-impedance.) • 1 = The ADC digital outputs are enabled. (The polarity is controlled by Reg 30:5.)	R/W	–	0
30:6	ADC_Sel	**Analog-to-Digital Converter (Capture) Select.** This bit selects a mode for the ADC. • 0 = – The clock rate is 2 pixels per clock (half-rate clock). – Both the 'A' and 'B' channels each provide 24-bit pixels (48 bits total). • 1 = – The clock rate is 1 pixel per clock (full-rate clock). – The 'A' channel provides 24-bit pixels (24 bits total). – The 'B' channel is driven either high or low, depending on the value of Reg 30:5 (ADC_INV).	R/W	–	0
30:5	ADC_Inv	**Analog-to-Digital Converter (Output) Invert (Disable).** This bit disables the inversion of the ADC outputs. • 0 = The ADC outputs are inverted. • 1 = The ADC outputs are not inverted (default).	R/W	–	1
30:4	Force_ADC	**Force Analog-to-Digital Converter (Outputs).** This bit forces to 'off' all output buffers for the ADC pin. • 0 = Normal operation • 1 = Force all ADC output buffers low or high as follows: – Reg 30:5 = 0 to force buffers low – Reg 30:5 = 1 to force buffers high	R/W	–	0
30:3	CLAMP_Pol	**Clamp Polarity.** This bit selects the polarity of the signal to a clamp. • 0 = The polarity of the signal to a clamp is positive. • 1 = The polarity of the signal to a clamp is negative.	R/W	–	0
30:2	CLAMP_Sel	**Clamp (Source) Select.** This bit selects the source of the signal to a clamp. • 0 = The source of the signal is internally generated. • 1 = The source of the signal is from the CLAMP pin.	R/W	–	0
30:1	VA_Disable	**Video Amplifier Disable.** • 0 = Video amplifier is enabled (default). • 1 = Video amplifier is disabled to conserve power.	–	–	0
30:0	FA_Disable	**Fine Adjust Disable.** • 0 = The DACs are enabled and they drive the VRTR, VRTG, and VRTB pins internally. • 1 = The DACs are disabled and the VRTR, VRTG, and VRTB pins must be driven externally with ADC top reference voltage.	R/W	–	0

6.5.33 Register 31h: R_COARSE

The R_COARSE Register is the first adjustment for the red channel of the ADC. It is used to coarsely adjust the analog signal used by the ADC. (See also Section 6.5.36, “Register 34h: R_FINE”.)

Table 6-32. R_COARSE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
31:7-31:6	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
31:5	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • This bit must be programmed to ‘1’.	–	–	1
31:4-31:2	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
31:1-31:0	R_Coarse_ADJ [1-0]	**Red Coarse (Gain) Adjust [1-0].** These bits adjust the red channel of the ADC by adjusting the gain of the video amplifier for the analog signal used by the ADC. • 0 = The gain is 1.0 (default). • 1 = The gain is 1.2. • 2 = The gain is 1.4 (typical). • 3 = The gain is 1.6.	R/W	–	0

6.5.34 Register 32h: G_COARSE

The G_COARSE Register is the first adjustment for the green channel of the ADC. It is used to coarsely adjust the analog signal used by the ADC. (See also Section 6.5.37, “Register 35h: G_FINE”.)

Table 6-33. G_COARSE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
32:7-32:6	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
32:5	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • This bit must be programmed to ‘1’.	–	–	1
32:4-32:2	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
32:1-32:0	G_Coarse_ADJ [1-0]	**Green Coarse (Gain) Adjust [1-0].** These bits adjust the green channel of the ADC by adjusting the gain of the video amplifier for the analog signal used by the ADC. • 0 = The gain is 1.0 (default). • 1 = The gain is 1.2. • 2 = The gain is 1.4 (typical). • 3 = The gain is 1.6.	R/W	–	0

6.5.35 Register 33h: B_COARSE

The B_COARSE Register is the first adjustment for the blue channel of the ADC. It is used to coarsely adjust the analog signal used by the ADC. (See also Section 6.5.38, “Register 36h: B_FINE”.)

Table 6-34. B_COARSE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
33:7-33:6	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
33:5	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • This bit must be programmed to ‘1’.	–	–	1
33:4-33:2	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • These bits can be programmed to ‘0’.	–	–	0
33:1-33:0	B_Coarse_ADJ [1-0]	**Blue Coarse (Gain) Adjust [1-0].** These bits adjust the blue channel of the ADC by adjusting the gain of the video amplifier for the analog signal used by the ADC. • 0 = The gain is 1.0 (default). • 1 = The gain is 1.2. • 2 = The gain is 1.4 (typical). • 3 = The gain is 1.6.	R/W	–	0

6.5.36 Register 34h: R_FINE

The R_FINE Register is the second adjustment for the red channel of the ADC. It is used to fine tune the top reference used by the ADC. (See also Section 6.5.33, “Register 31h: R_COARSE”.)

Table 6-35. R_FINE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
34:7-34:0	R_Fine_ADJ [7-0]	**Red Fine Adjust [7-0].** These bits adjust the amount of voltage to the top reference of the red channel of the ADC. • 0 = Lowest-voltage value • 255 = Highest-voltage value	R/W	–	20

6.5.37 Register 35h: G_FINE

The G_FINE Register is the second adjustment for the green channel of the ADC. It is used to fine tune the top reference used by the ADC. (See also Section 6.5.34, “Register 32h: G_COARSE”.)

Table 6-36. G_FINE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
35:7-35:0	G_Fine_ADJ [7-0]	**Green Fine Adjust [7-0].** These bits adjust the amount of voltage to the top reference of the green channel of the ADC. • 0 = Lowest-voltage value • 255 = Highest-voltage value	R/W	–	20

6.5.38 Register 36h: B_FINE

The B_FINE Register is the second adjustment for the blue channel of the ADC. It is used to fine tune the top reference used by the ADC. (See also Section 6.5.35, “Register 33h: B_COARSE”.)

Table 6-37. B_FINE Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
36:7-36:0	B_Fine_ADJ [7-0]	**Blue Fine Adjust [7-0].** These bits adjust the amount of voltage to the top reference of the blue channel of the ADC. • 0 = Lowest-voltage value • 255 = Highest-voltage value	R/W	–	20

6.5.39 Register 37h: PSEL

The PSEL Register is used to program the general-purpose pins, PSEL1 through PSEL3.

Table 6-38. PSEL Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
37:7	ADCRCLK_Inv	**ADCRCLK Invert.** This bit inverts the ADCRCLK signal. • 0 = Do not invert the ADCRCLK signal. • 1 = Invert the ADCRCLK signal (default).	–	–	1
37:6-37:5	ADCRCLK_Del	**ADCRCLK Delay.** These bits delay the ADCRCLK signal, relative to data, in 0.5-ns increments. • 0 = 0-ns delay of ADCRCLK • 1 = 0.5-ns delay of ADCRCLK • 2 = 1.0-ns delay of ADCRCLK (default) • 3 = 1.5-ns delay of ADCRCLK	–	–	2
37:4	Reserved	**Reserved.** • See Section 6.1, “Reserved Bits”. • This bit must be programmed to ‘0’.	–	–	0
37:3	Cal_Access	**Calibration Access.** Depending on the state of the VSS(TEST) pin (see Section 3.2.3.6, “Ground Pins”), this bit performs in either the Normal mode or the Test mode. • **Normal mode.** When the ICS1531 is in Normal mode and this bit = – 0, Calibration Regs cannot be accessed. – 1, Calibration Regs 38h to 3Ch can be accessed. • **Test mode.** – When the ICS1531 is in Test mode, Calibration Regs 38h to 3Ch can be accessed, regardless of the setting of Reg 37:3. – The Test mode is intended for use only by ICS.	R/W	–	0
37:2	PSEL3	**Programmable Select 3.** This bit is used to program general-purpose pin PSEL3.	R/W	–	0
37:1	PSEL2	**Programmable Select 2.** This bit is used to program general-purpose pin PSEL2.	R/W	–	0
37:0	PSEL1	**Programmable Select 1.** This bit is used to program general-purpose pin PSEL1.	R/W	–	0

6.5.40 Calibration Registers

The registers in this section can be used to calibrate the ICS1531. Typically, the Calibration registers do not need to be adjusted. However, access is provided so that production-line calibrations can be made as necessary.

Note: For information on how to enable the Calibration Regs, see Reg 37:3.

6.5.40.1 Register 38h: R_COMP_OFF

The R_COMP_OFF Register is used to adjust as necessary the comparator offset for the red ‘B’ and ‘A’ channels.

Table 6-39. R_COMP_OFF

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
38:7 38:4	R_C_O_B	**Red Comparator Offset (B Channel).** Reserved.	See Reg 37:3	–	7
38:3-38:0	R_C_O_A	**Red Comparator Offset (A Channel).** Reserved.	See Reg 37:3	–	7

6.5.40.2 Register 39h: G_COMP_OFF

The G_COMP_OFF Register is used to adjust as necessary the comparator offset for the green ‘B’ and ‘A’ channels.

Table 6-40. G_COMP_OFF Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
39:7 39:4	G_C_O_B	**Green Comparator Offset (B Channel).** Reserved.	See Reg 37:3	–	7
39:3-39:0	G_C_O_A	**Green Comparator Offset (A Channel).** Reserved.	See Reg 37:3	–	7

6.5.40.3 Register 3Ah: B_COMP_OFF

The B_COMP_OFF Register i is used to adjust as necessary the comparator offset for the blue ‘B’ and ‘A’ channels.

Table 6-41. B_COMP_OFF Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
3A:7 3A:4	B_C_O_B	**Blue Comparator Offset (B Channel).** Reserved.	See Reg 37:3	–	7
3A:3-3A:0	B_C_O_A	**Blue Comparator Offset (A Channel).** Reserved.	See Reg 37:3	–	7

6.5.40.4 Register 3Bh: CAL_1

The CAL_1 Register is used to select (1) delays to calibrate the ADC data delay and (2) the clock delay for the green and red channels.

Table 6-42. CAL1 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
3B:7	Reserved	**Reserved.** • See Section 6.1, "Reserved Bits". • This bit can be programmed to '0'.	–	–	0
3B:6	ADC_DD [0]	**Analog-to-Digital Converter Data (Global) Delay [0].** • This bit works with Regs 3C:4 and 3C:3 for a global delay of all RGB data output from the ADC. • This bit is the least-significant bit.	See Reg 37:3	–	0
3B:5-3B:3	G_CD	**Green (Channel) Clock Delay.** These bits select a delay (that is, an offset) for use in calibrating the clock for the green channel. (An acknowledge of these bits occurs only when the Calibration Regs are enabled.) When these bits are: • 0, the clock delay calibration offset is 0. • 1 or above, the clock delay calibration offset increases.	R/W See Reg 37:3	–	5
3B:2 3B:0	R_CD	**Red (Channel) Clock Delay.** These bits select a delay (that is, an offset) for use in calibrating the clock for the red channel. (An acknowledge of these bits occurs only when the Calibration Regs are enabled.) When these bits are: • 0, the clock delay calibration offset is 0. • 1 or above, the clock delay calibration offset increases.	R/W See Reg 37:3	–	5

6.5.40.5 Register 3Ch: CAL_2

The CAL_2 Register is used to select (1) delays to calibrate the ADC data delay and (2) the clock delay for blue channel.

Table 6-43. CAL2 Register

Bit	Bit Name	Bit Definition	Access	Spec. Func.	Reset
3C:7-3C:5	Bandgap_CAL	**Bandgap Calibration.** To calibrate the ICS1531 bandgap voltage, these bits adjust the current to VRTR, VRTG, and VRTB. (An acknowledge occurs only when the Test mode is enabled.)	R/W	–	5
3C:4-3C:3	ADC_DD [2-1]	**Analog-to-Digital Converter Data (Global) Delay [2-1].** • These bits work with Reg 3B:6 for a global delay of all RGB data output from the ADC. • These bits are the most-significant bits.	See Reg 37:3	–	0
3C:2-3C:0	B_CD	**Blue (Channel) Clock Delay.** These bits select a delay (that is, an offset) for use in calibrating the clock for the blue channel. (An acknowledge of these bits occurs only when the Calibration Regs are enabled.) When these bits are: • 0, the clock delay calibration offset is 0. • 1 or above, the clock delay calibration offset increases.	R/W See Reg 37:3	–	5

Chapter 7 Programming

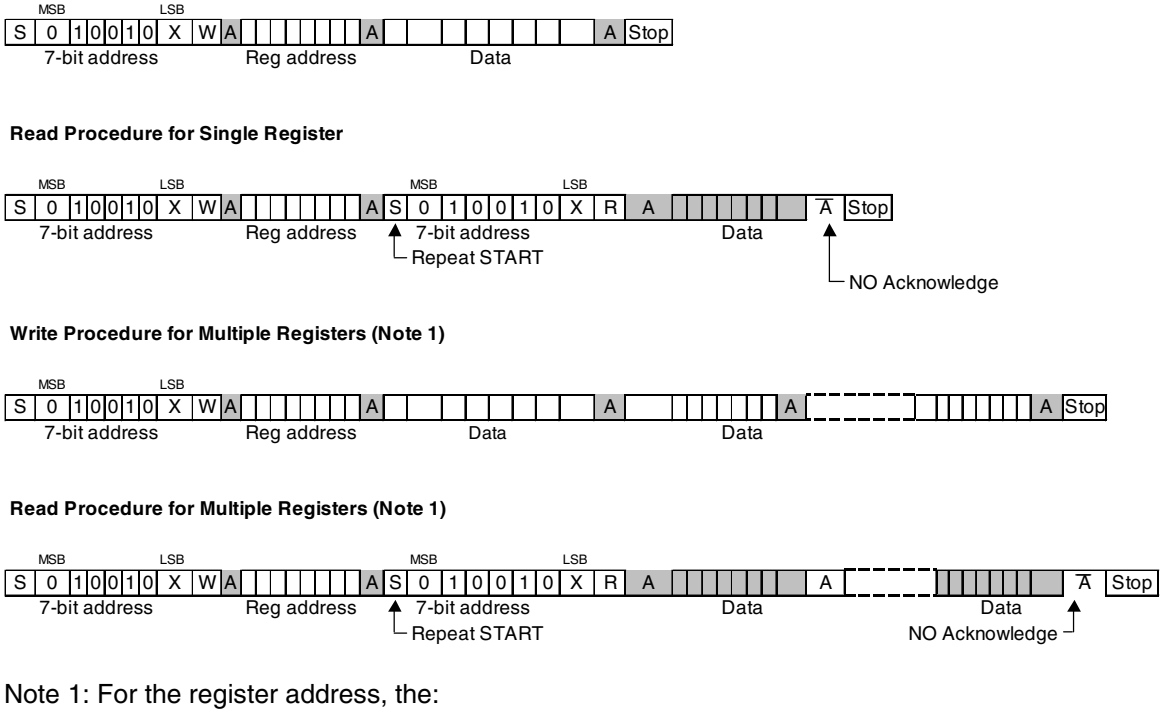
7.1 Industry-Standard 2-Wire Serial Bus: Data Format

Figure 7-1 shows the data format for an industry-standard 2-wire serial bus.

Note:

1. All values are transmitted with the most-significant bit (MSB) first and the least-significant bit (LSB) last.
2. A dashed line – — — – means multiple transactions.
3. A = ACK = Acknowledge
4. R = Read = 1
5. S = Start
6. W = Write = 0
7. X = Bit value that equals the logic state of the SBADR pin.
8. Direction:
   - ☐ Master device drives signal to ICS1531
   - ▒ ICS1531 drives signal to master device

Figure 7-1. ICS1531 Data Format for Industry-Standard 2-Wire Serial Bus

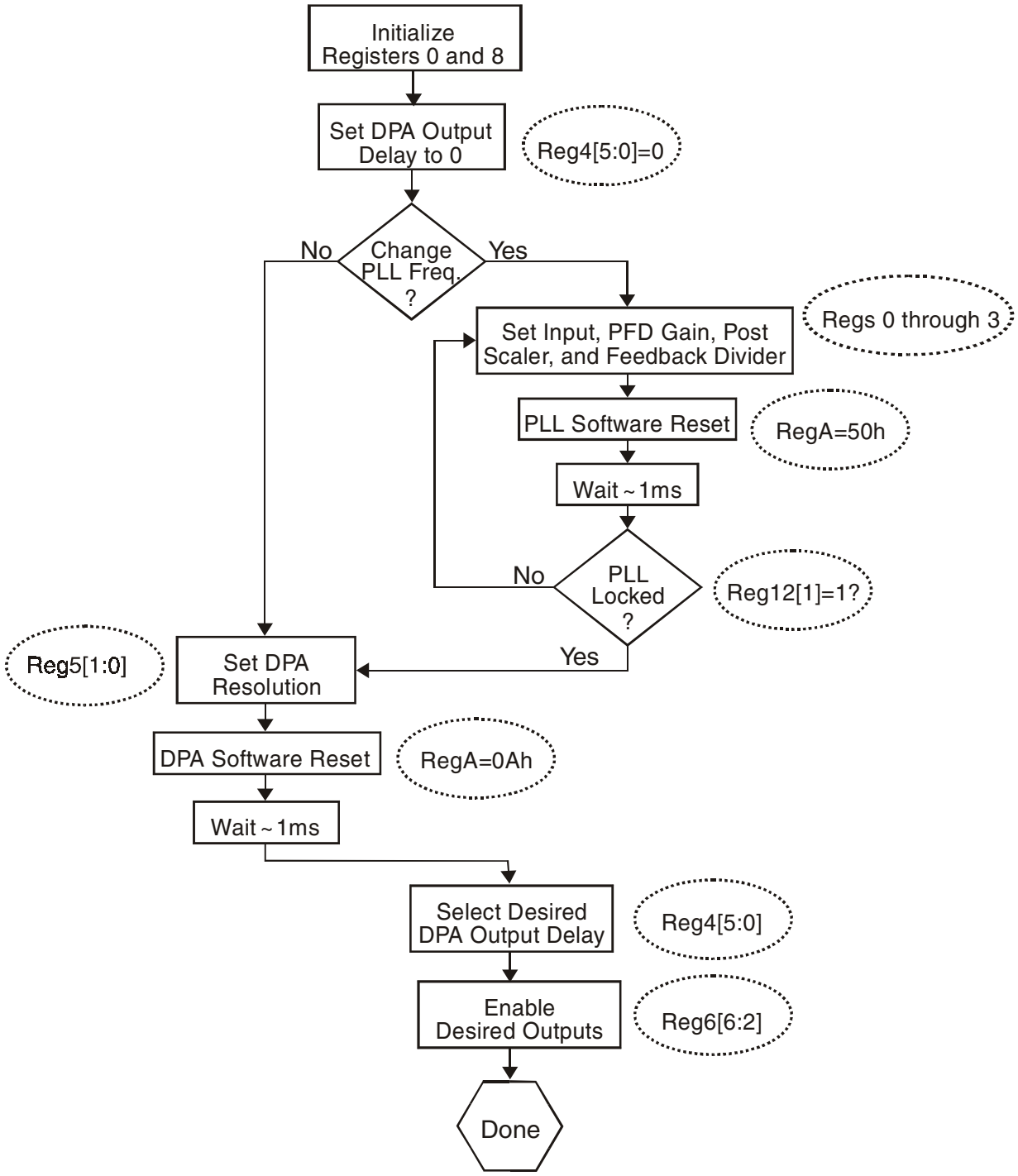


Note 1: For the register address, the:

- Lower nibble automatically increments after each successive data byte is written to or read from the ICS1531.
- Upper nibble does not automatically increment, and the software must explicitly re-address the ICS1531. As a result, to write or read all the ICS1531 registers, the software:
  - Must not index 0 and then do 64 one-byte transactions.
  - Must break the transactions into four separate bus transactions:
    (1) 00 to 0F (2) 10 to 1F (3) 20 to 2F (4) 30 to 3F

7.2 Programming Flow for Modifying PLL and DPA Settings

Figure 7-2. ICS1531 Flow for Capture/Input Clock PLL



7.3 Programming Spread Spectrum

7.3.1 Spread Spectrum Definition and Purpose

Spread spectrum is a process for distributing (or 'spreading') the energy of a single-frequency signal over a wider frequency spectrum so that it reduces the peak radiated energy on any single frequency.

The need for spread-spectrum technology results from the increase in speeds of PCs and the subsequent increase in operating resolutions. That is, there has been an increase both in the speed of (1) pixel clocks for cathode-ray tube displays and (2) panel clocks for LCD displays.

Accompanying these increases has been an increase in generated electro-magnetic interference (EMI). In some cases, EMI emissions of the fundamental frequency can be too high to pass a country's communications regulations [such as those from the American government agency, the Federal Communications Commission (FCC)].

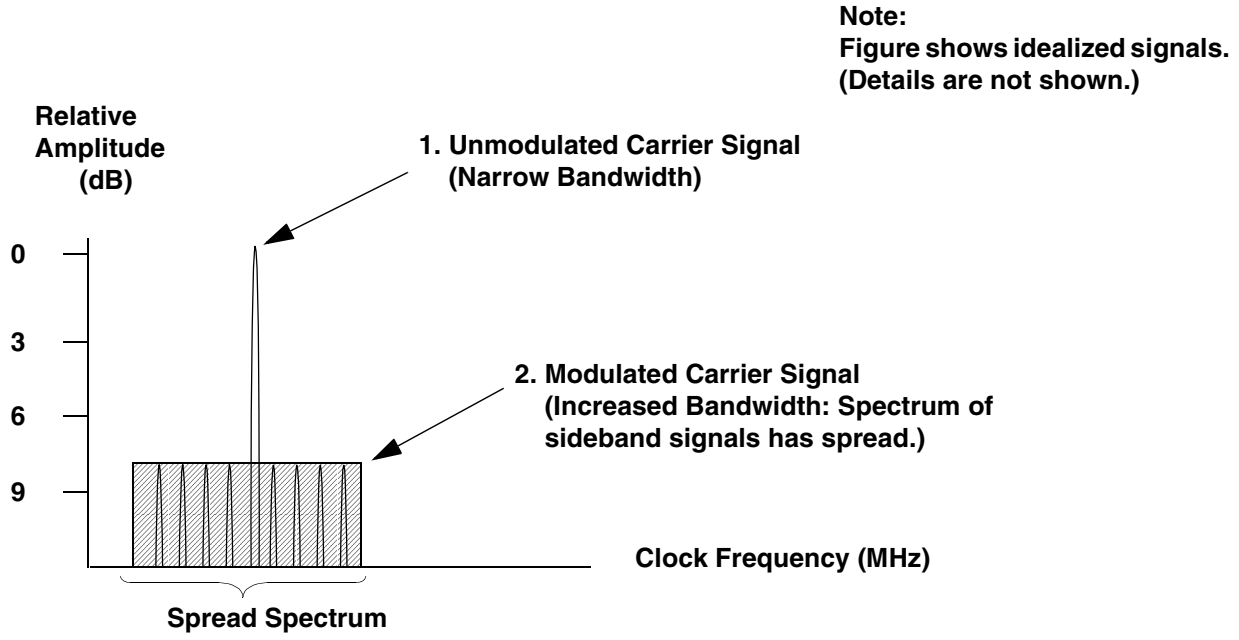
Figure 7-3 shows an idealized (1) unmodulated carrier signal and (2) modulated signal resulting from spread-spectrum technology. (Both of the actual signals have a fundamental frequency and more variable peaks and sidebands than what this figure shows.)

1. In this example, the unmodulated carrier signal has a frequency whose peak amplitude creates EMI emissions that are too high to pass FCC requirements.
2. To reduce EMI, the ICS1531 use spread-spectrum technology to modulate the carrier frequency of the input timing signals from either the memory clock, or the panel clock, or both. Figure 7-3 shows how the energy of the unmodulated signal can be redistributed as sidebands of a modulated signal.

   The peak amplitude of the composite single-frequency carrier signal is thereby attenuated. As a result, the EMI peak decreases, while the total signal energy is maintained. This attenuation occurs without increasing cycle-to-cycle jitter. Consequently, system design costs can be reduced by decreasing the need to design shielding for the ICS1531.

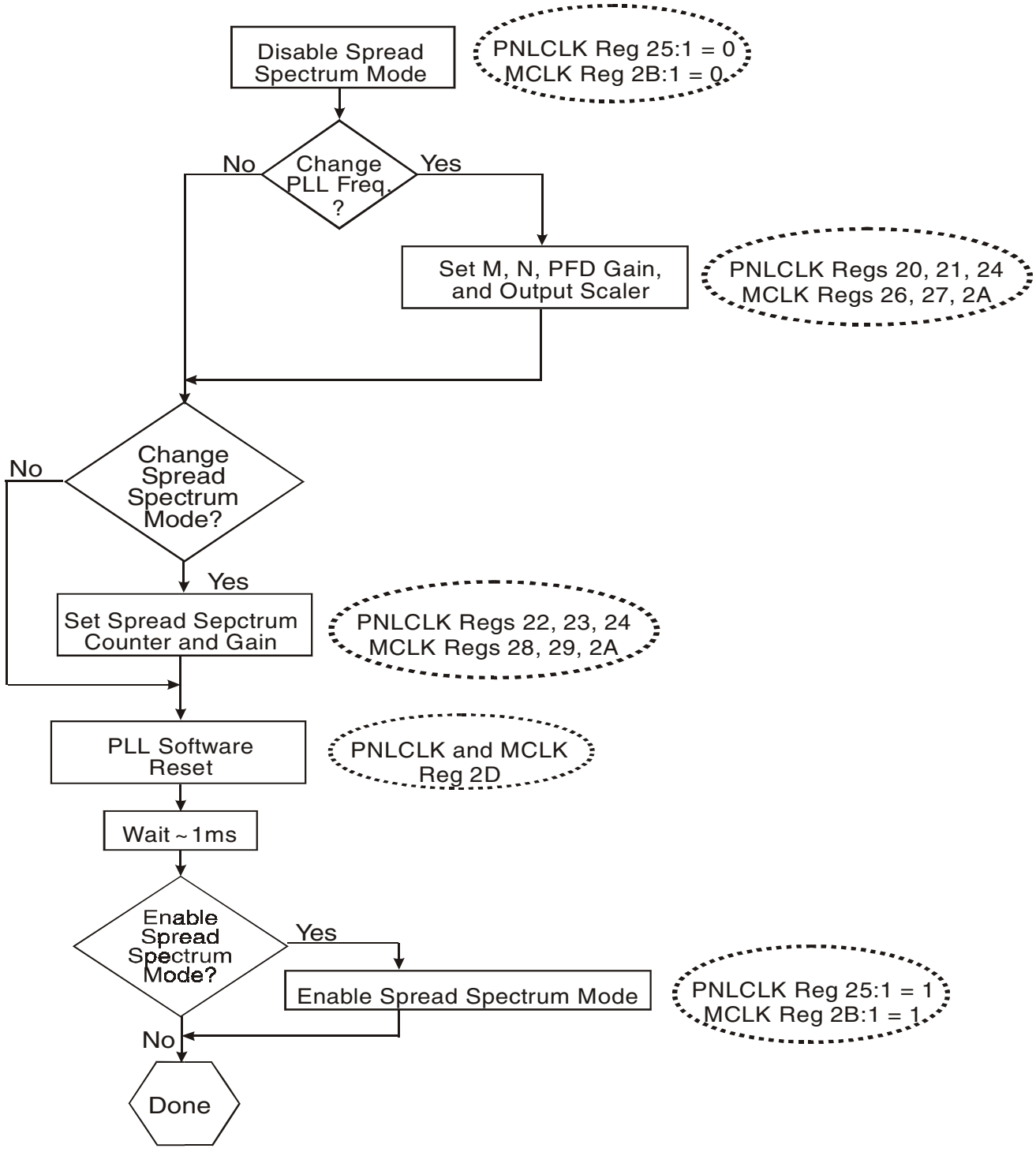
Note: Both the MCLK and PNLCLK PLLs use spread-spectrum technology. (The pixel PLL does not.) For information on how to achieve specific spread-spectrum results, see ICS1531 application notes.

Figure 7-3. Signal Characteristics (1) Before and (2) After Applying Spread-Spectrum Circuitry



7.3.2 Programming Flow for Modifying Settings for Spread Spectrum

Figure 7-4. ICS1531 Flow for PNLCLK and MCLK PLL Spread-Spectrum Settings



Chapter 8 Layout and Power Considerations

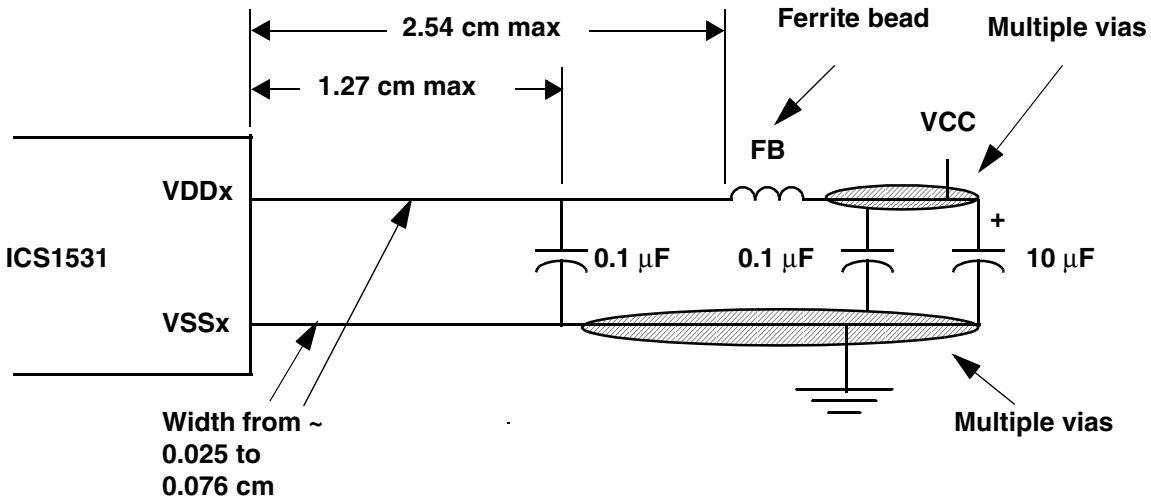
8.1 Layout Considerations

8.1.1 General Guidelines for Printed Circuit Board Layout

To lay out a printed circuit board that uses the ICS1531, see Figure 8-1 and use the following general guidelines.

- Use a printed circuit board with at least the following four planes:
  - One power plane
  - One ground plane. (No special cutouts required.)
  - Two signal planes
- Power supply voltages:
  - Provide all supply voltages from a common source.
  - Ensure that all supply voltages ramp together.
  - Bypass each power supply pin with a 0.1-µF capacitor.
- When using capacitors for filtering or decoupling, use either tantalum or ceramic capacitors with good high-frequency characteristics. (Do not use electrolytic capacitors.) Place the capacitors as close as possible to the ICS1531 pins that are being filtered or decoupled.
- Trace widths:
  - Use nominal trace widths of approximately 0.020 to 0.025 cm.
  - Use a maximum trace width of approximately 0.076 cm.
- As Figure 8-1 indicates, connect the appropriate VDDx and VSSx pins to the appropriate plane, using multiple surface-etched vias.
- Ensure that the area of the printed circuit board where the ICS1531 is placed is free of contaminants. (Flux and other board-surface debris can degrade the performance of the external loop filter.)

Figure 8-1. General Decoupling Circuit for ICS1531



8.1.2 Specific Guidelines for Printed Circuit Board Layout

8.1.2.1 Digital Inputs

The ICS1531 digital inputs are designed to work with either 3.3-V and 5-V signals. No extra components are required.

8.1.2.2 Analog Inputs

To reduce noise, minimize traces for the ICS1531 analog red, green, and blue input pins by placing the ICS1531 as close as possible to the board's input connector. Input connectors can include any of the following:

- 15-pin D connector
- BNC connector
- Digital Visual Interface connector (from the Digital Display Working Group)
- 'P&D', the 'Plug and Display' connector (from VESA)

8.1.2.3 External Loop Filter

The ICS1531 has software that allows for the selection of components for an internal loop filter for the pixel clock PLL. (The internal loop filter has the advantage of not requiring any extra components.)

The ICS1531 also allows for the selection of components for an external loop filter for the pixel clock PLL. If the external loop-filter option is used, do the following:

1. Place loop filter components as close as possible to the EXTFIL and XFILRET pins.
2. For loop filter components, typical values are as follows:
   a. 6.8K Ω for the series resistor
   b. 3300 pF RF-type capacitor for the series capacitor
   c. 33 pF for the shunt capacitor

8.2 Power Considerations

8.2.1 Power-On Reset

The ICS1531 incorporates special internal power-on reset circuitry that requires no external reset signal connections.

- During normal operations, the VDD supply voltage for the ICS1531 must remain within the recommended operating conditions. (See Section 9.2, “Recommended Operating Conditions”.)
- To reset the ICS1531, do the following:
  - Reduce the level of the VDD supply voltage to the ICS1531 (and the voltage seen on all ICS1531 pins) so that it is below V_{th}, the threshold voltage for time t1. (For a typical threshold voltage V_{th}, see Section 10.2, “Power-On Reset Timing”.)
  - Keep the supply voltage below that threshold voltage for time t1, such that power-conditioning capacitors for the printed circuit board are drained and the proper reset state is latched. (For a typical time t1, see Section 10.2, “Power-On Reset Timing”.)
- A successful power-on reset results in all the ICS1531 registers having the appropriate reset values as stated in the tables in Chapter 6, “Register Set”.

8.2.2 Power Conservation

For information on how to conserve power, see the ICS1531 application notes.

8.2.3 Layout for Power Supply Voltages

See Section 8.1.1, “General Guidelines for Printed Circuit Board Layout”.

Chapter 9 AC/DC Operating Conditions

Warning: The values in this chapter are preliminary and subject to change.

9.1 Absolute Maximum Ratings

Table 9-1 lists absolute maximum ratings for the ICS1531. Stresses above these ratings can cause permanent damage to the ICS1531. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the ICS1531 at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 9-1. ICS1531 Absolute Maximum Ratings

Item	Rating
VDD, VDDQ (measured with respect to VSS)	4.3 V
Digital Inputs	VSS -0.3 V to +5.5 V
Digital Outputs	VSSQ -0.3 V to VDDQ +0.3 V
Analog Inputs	VSS -0.3 V to +5.5 V
Analog Outputs	VSSA -0.3 V to VDDA +0.3 V
Storage Temperature	-65 to +150° C
Junction Temperature	175° C
Soldering Temperature	260° C
Power Dissipation	See Section 9.3, “Power Values”

9.2 Recommended Operating Conditions

Table 9-2. ICS1531 Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Ambient Operating Temperature	0	–	+70	° C
Power Supply Voltage (measured with respect to VSS)	+3.0	+3.3	+3.6	V

9.3 Power Values

Table 9-3. ICS1531 Power Values

Item	Conditions	Typical	
Power Dissipation, Active	3.3 V	ICS1531 (100 MHz):	800 mW
		ICS1531 (140 MHz):	850 mW
		ICS1531 (160 MHz):	900 mW
Power Dissipation, Standby	3.3 V	~250 mW	

9.4 AC Operating Characteristics

Table 9-4. AC Operating Characteristics for ICS1531 Inputs

Parameter	Symbol	Min.	Max.	Units
Input HSYNC: Input Frequency	f_{HSYNC}	12	120	kHz
PDEN: Input Frequency	f_{PDEN}	30	120	Hz

9.5 DC Operating Characteristics

This section lists the DC operating characteristics for the ICS1531.

9.5.1 DC Operating Characteristics for Supply Current.

Note: All VDD measurements are taken with respect to VSS (which equals 0 V).

Table 9-5. DC Operating Characteristics for Supply Current to ICS1531

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Current, Digital †	IDDD	VDDD = 3.3 V, 100 MHz	–	135	150	mA
Supply Current, Analog †	IDDA	VDDA = 3.3 V, 100 MHz	–	125	135	mA

9.5.2 DC Operating Characteristics for Digital Inputs

Table 9-6 lists DC operating characteristics for the following ICS1531 TTL input pins:

- HSYNC
- PDEN
- SBADR
- SCL
- SDA (Input mode only. For output mode, see Table 9-7.)

Note: All VDD measurements are taken with respect to the VSS pin (which equals 0 V).

Table 9-6. DC Operating Characteristics for TTL Inputs

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	–	2.4	–	–	V
Input Low Voltage	V_{IL}	–	–	–	0.8	V
Input High Current	I_{IH}	V_{IH} = VDD	–	–	±10	µA
Input Low Current	I_{IL}	V_{IL} = 0	±10	–	–	µA
Input Capacitance (Note 1)	C_{in}	–	–	10	–	pF

Note 1. Typically guaranteed by design.

9.5.3 DC Operating Characteristics for SDA Digital Pin, in Output Mode

Table 9-7 lists DC characteristics for the SDA pin output mode. (For input mode, see Table 9-6.)

Table 9-7. DC Operating Characteristics for ICS1531 SDA Pin, Output Mode

Parameter	Symbol	Conditions	Min.	Max.	Units
Output Low Voltage	V_{OL}	I_{OUT} = 3 mA	–	0.4	V

Chapter 10 Timing Diagrams

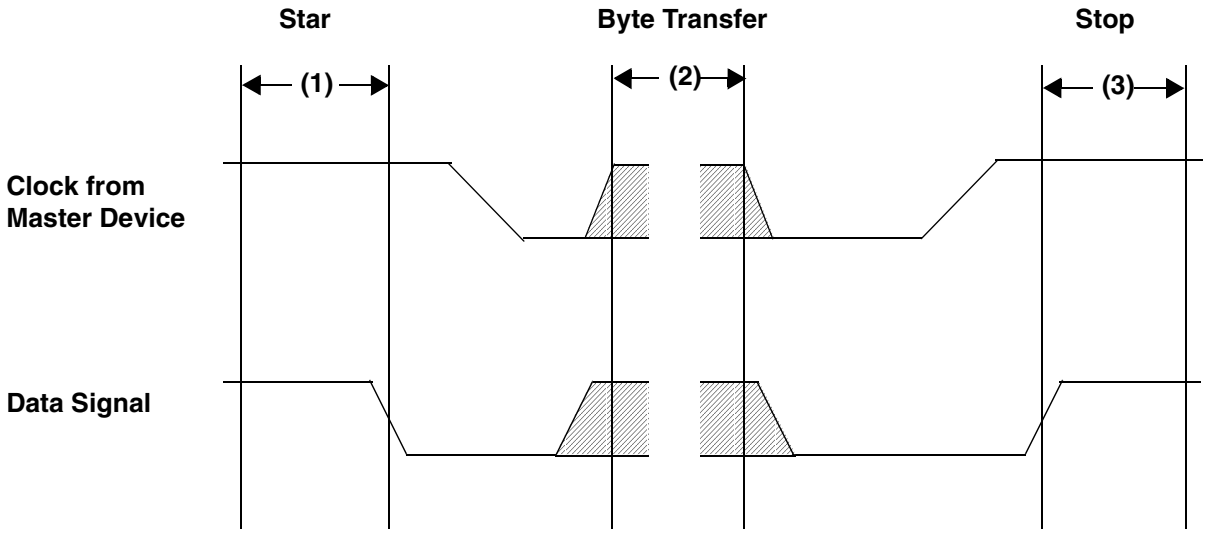
10.1 Industry-Standard 2-Wire Serial Bus Timing Diagrams

10.1.1 Start and Stop Conditions

Figure 10-1 shows in general terms how start and stop conditions work when transferring bits on an industry-standard 2-wire serial bus. All bus transactions begin with a start and end with a stop.

- To start a bus transfer (1), the clock signal from a master device (typically a microcontroller) is allowed to float high while the data signal driven by the master device transitions from high to low.
- The bytes transfer (2) from the master device to/from the ICS1531. (For details, see Section 10.1.2, “Transfer of Data Bytes”.)
- To stop a bus transfer (3), while the clock signal is high, the data signal transitions from low to high.

Figure 10-1. Start and Stop Conditions



10.1.2 Transfer of Data Bytes

Table 10-1 lists significant time periods for signals on SDA and SCL pins during the transfer of data bytes.

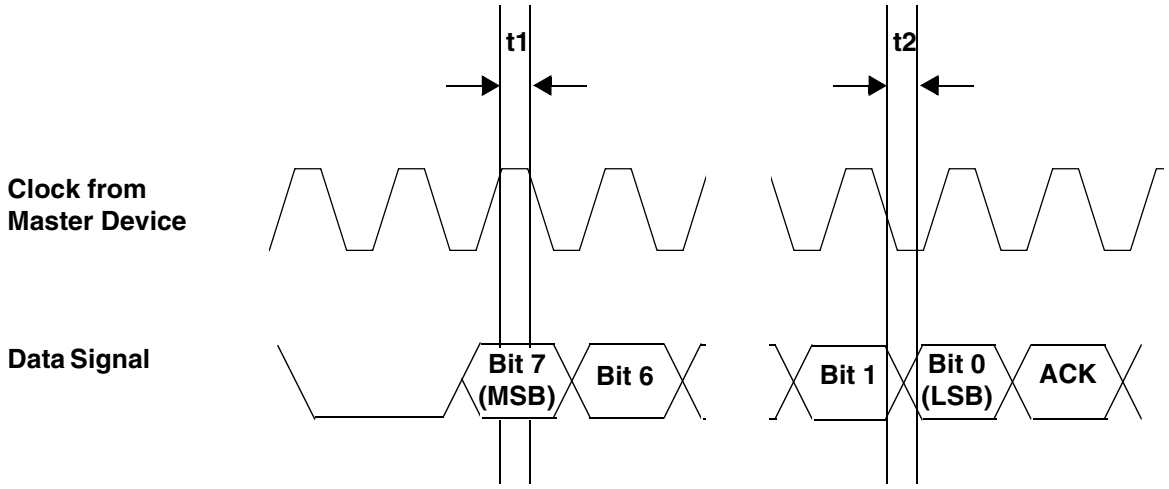
Table 10-1. ICS1531 Byte Transfer

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	Data Held Valid	–	2.5	–	10	µs
t2	Change of Data Allowed	–	2.5	–	10	µs

Figure 10-2 shows how bits are transferred on an industry-standard 2-wire serial bus.

- For start and stop conditions, see Section 10.1.1, “Start and Stop Conditions”.
- When there is a transfer of valid data (t1), the bits that transfer are Bits 7 through 0.
  - These first 8 bits are either data or address bits that are output sequentially.
  - Bit 7, the most-significant bit of these 8 bits, is output first.
  - Bit 0, the least-significant bit of these 8 bits, is output last.
- After each bit transfer, a change of data occurs (t2).
- For details on the ACK signal, see Chapter 10.1.3, “Acknowledge Conditions”.

Figure 10-2. Byte Transfer on Industry-Standard 2-Wire Serial Bus

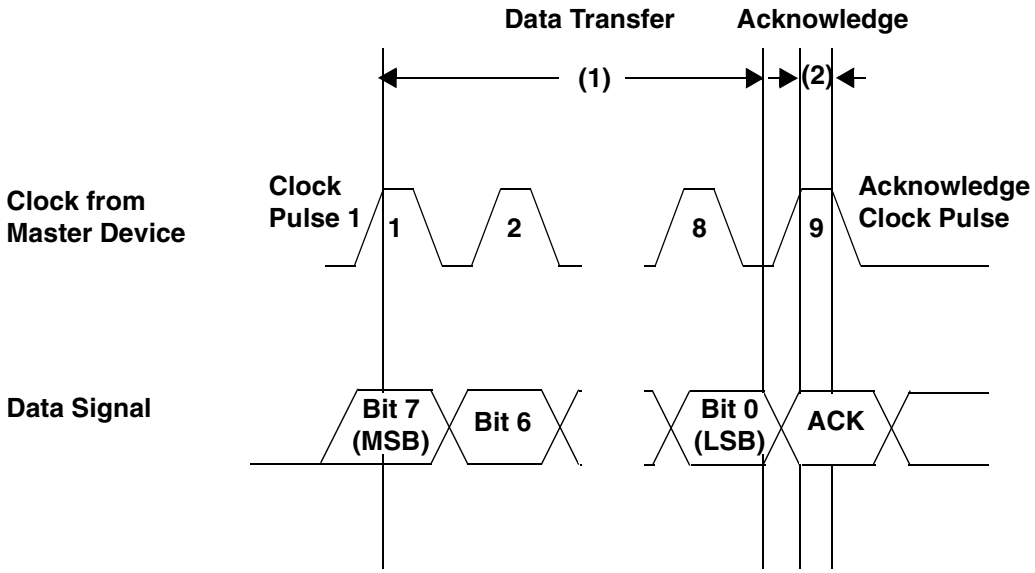


10.1.3 Acknowledge Conditions

Figure 10-3 shows in general how an acknowledge works on an industry-standard 2-wire serial bus.

- For start and stop conditions, see Section 10.1.1, “Start and Stop Conditions”.
- The data transfers (1). (For details, see Section 10.1.2, “Transfer of Data Bytes”.) If there is a:
  - Data read, the ICS1531 drives the data, and the master (typically, a microcontroller) drives the ACK.
  - Data write, the master drives the data, and the ICS1531 drives the ACK.
- The acknowledge bit (ACK) is the ninth (and last) bit output.
  - The ACK bit is a read-write bit that indicates whether the first 8 bits are either:
    - Read from the ICS1531 by a master device (typically, a microcontroller), or
    - Written to the ICS1531 by a master device
  - For an acknowledge (2) to occur, you must do the following:
    - Address the ICS1531 properly
    - Write a valid register index
    - Read/write the specified data

Figure 10-3. Acknowledge on Industry-Standard 2-Wire Serial Bus



10.2 Power-On Reset Timing

Table 10-2 lists typical ICS1531 power-on reset (POR) timing measures and Figure 10-4 shows the POR timing relationships. (For information on how the ICS1531 POR circuitry operates, see Section 8.2, "Power Considerations".)

Table 10-2. Typical ICS1531 POR Transition Times

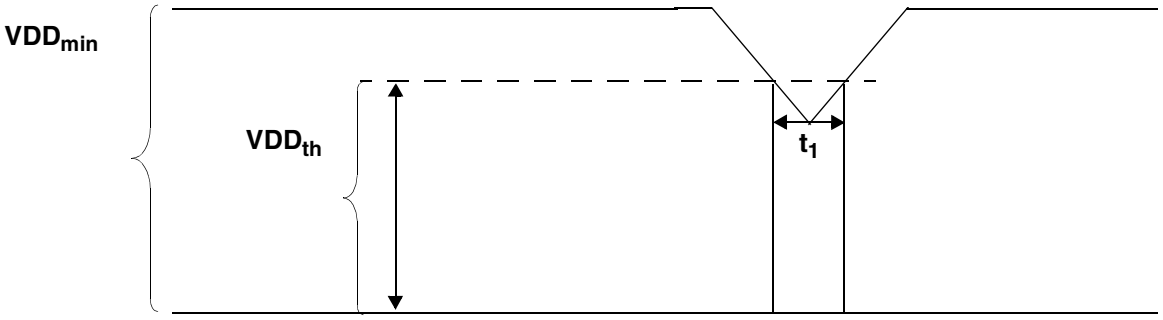
Symbol	Timing Description	Min	Typ	Max	Units
VDD	Supply Voltage ('On' State)	3.0	3.3	3.6	V
VDD_{th}	Threshold Supply Voltage	–	1.8	–	V
t_1	Hold Time for Reset State	–	10	–	ms

If a reset:

- Is desired, reduce the VDD supply voltage (and the voltage on all ICS1531 pins) so that it is below the threshold voltage (VDD_{th}) of the POR circuit for the period t1. (A time of 10 ms is sufficient.)
- Is not desired, ensure either one or both of the following conditions:
  - Ensure the VDD supply voltage (and the voltage on all ICS1531 pins) is not reduced below V_{min}.
  - If the VDD supply voltage (and the voltage on all ICS1531 pins) is reduced below V_{th}, then ensure that it is at this level for less than the period t1.

Note: The POR signal is an internal signal. It is generated regardless of the ICS1531 mode.

Figure 10-4. Power-On Reset Condition for ICS1531



10.3 AC Timing Diagrams

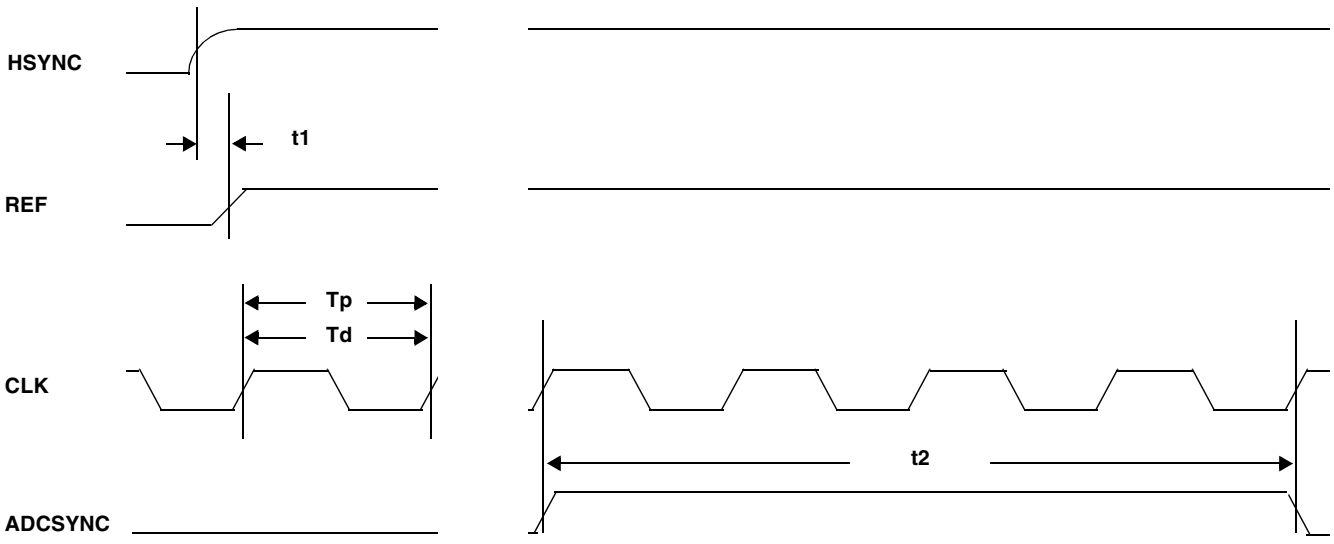
10.3.1 Phase-Locked-Loop Timing for Digital Setup and Hold

The input HSYNC signal is used to generate the REF output signal. In the Phase/Frequency Detector, the REF signal is compared with ADCSYNC (which provides the recovered HSYNC signal). Table 10-3 gives the timing for these signals, and Figure 10-5 shows timing characteristics.

Table 10-3. Phase-Locked-Loop Timing

Time Period	Timing Description	Min	Typ	Max	Units
t1	Input HSYNC Rise Time to REF Rise Time	TBD	7	TBD	ns
Tp	Clock Period		$Tp = \frac{\text{Input HSYNC Frequency}}{\text{Result from: Section 6.5.3, “Register 02h: Fdbk Div 0 Register” and Section 6.5.4, “Register 03h: Fdbk Div 1 Register”}}$		ns
Td	Clock Duty Cycle	45-55	50-50	55-45	%
t2	ADCSYNC Active Time		4 × Tp		ns

Figure 10-5. Timing for Phase-Locked Loop



10.3.2 Two-Pixels-per-Clock Mode Timing

For 2-pixels-per-clock mode, Reg 30:6 must be cleared to '0'. Table 10-4 lists pixel characteristics for this mode, as determined by Reg 2:0. (Both 'A' and 'B' channel pixels are pipelined and aligned with the rising edge of the ADCRCLK.) Table 10-5 lists time measures for this mode, and Figure 10-6 shows timing characteristics.

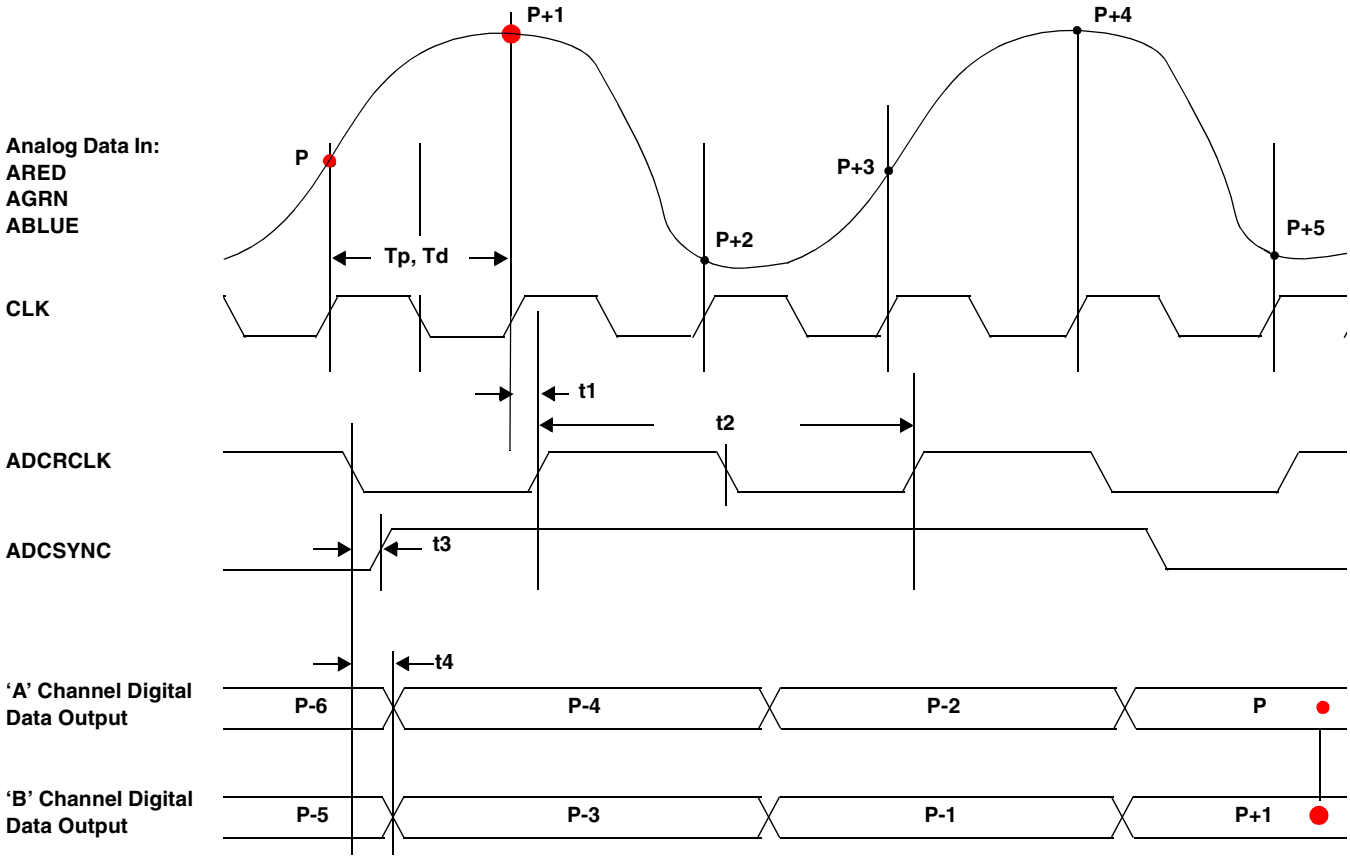
Table 10-4. Pixel Characteristics for 2-Pixels-per-Clock Mode

Reg 2:0 Setting	Pixel Characteristics When Reg 30:6 is Cleared to '0'		
	Total Number of Pixels	Pixel Output	What the Pixels Represent
0	Total number is even.	Output is on Channel 'A'.	Samples taken on half-rate ADCRCLK's rising edge.
1	Total number is odd.	Output is on Channel 'B'.	Samples taken on half-rate ADCRCLK's falling edge.

Table 10-5. Timing for 2-Pixels-per-Clock Mode

Time Period	Timing Description	Min	Typ	Max	Units
Tp, Td	CLK Period, CLK Duty Cycle	–	See Table 10-3.	–	ns
t1	CLK Rise Time to ADCRCLK Rise Time	–	2.6	–	ns
t2	ACDRCLK Period	–	t2 = 2 × Tp	–	ns
t3	ACDRCLK Fall Time to ADCSYNC Rise Time	–	TBD	–	ns
t4	Digital Data Transition	3.8	5	TBD	ns

Figure 10-6. AC Timing for 2-Pixels-per-Clock Mode



10.3.3 One-Pixel-per-Clock Mode Timing

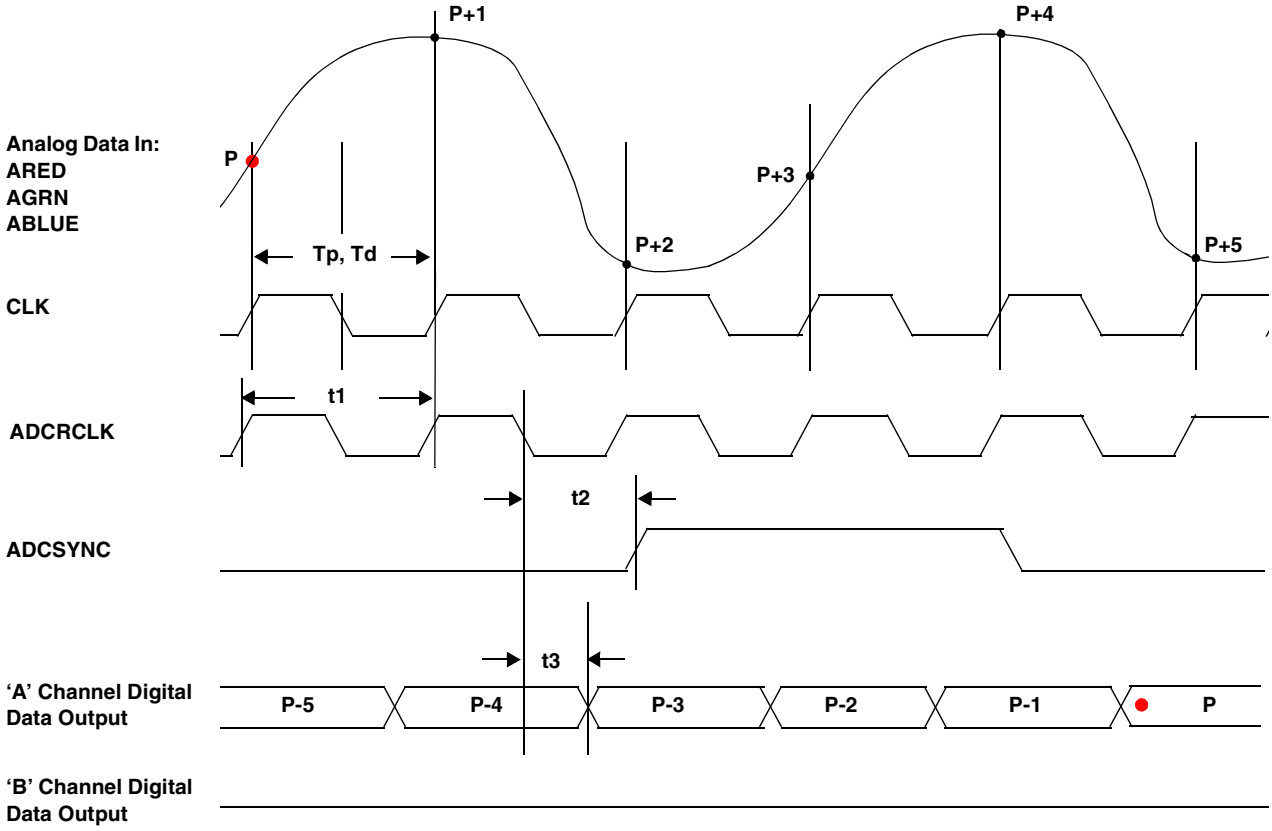
For 1-pixel-per-clock mode, Reg 30:6 must be set to '1'. Table 10-6 lists time measures for this mode, and Figure 10-5 shows timing characteristics.

Note: For the 1-pixel-per-clock mode, the 'B' channel data outputs are always at ground level.

Table 10-6. Timing for 1-Pixel-per-Clock Mode

Time Period	Timing Description	Min	Typ	Max	Units
Tp, Td	CLK Period, CLK Duty Cycle	–	See Table 10-3.	–	ns
t1	ADCRCLK Period	–	t1 = Tp	–	ns
t2	ADCRCLK Fall Time to ADCSYNC Rise Time	–	TBD	–	ns
t3	Digital Data Transition	0	2.0	2.5	ns

Figure 10-7. AC Timing for 1-Pixel-per-Clock Mode



Chapter 11 VCO Transfer Characteristics

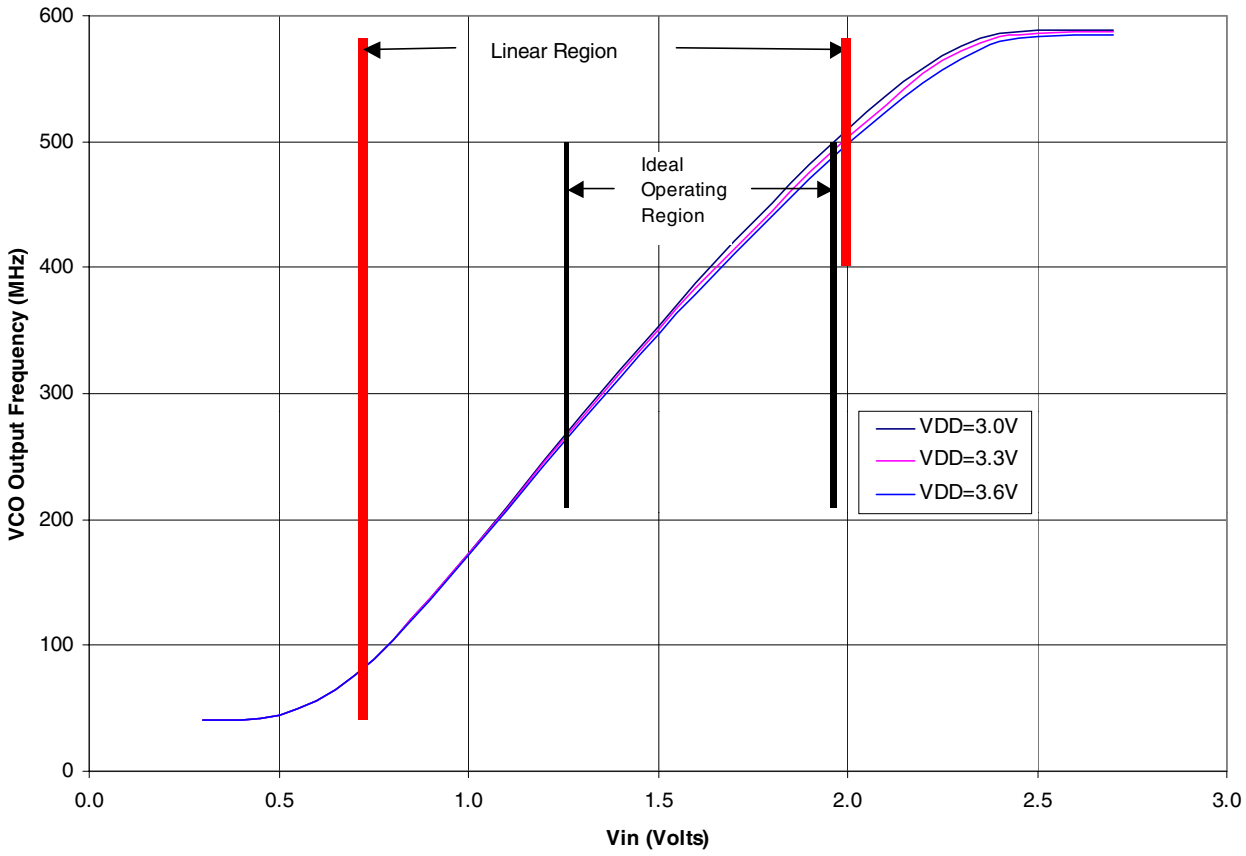
Figure 11-1 shows the VCO output frequency as a function of both Vin (that is, the VCO control voltage) and VDD under the following conditions:

- Temperature is ‘ambient’.
- The Phase/Frequency Detector is disabled.
- The external filter is selected, and Vin is applied between the EXTFIL pin and XFILRET pin.

The VCO gain, shown as the slope of the linear region, is approximately 300 MHz/V. ICS recommends that ideally, the ICS1531 is operated in a region from 250 to 500 MHz.

Important: If both the HSYNC and ADCSYNC signals are first measured at 0° C and then the ADCSYNC signal is measured at 70° C, the drift (that is, the difference between the two ADCSYNC measurements) is 400 ps.

Figure 11-1. Relationship of VCO Voltage and VCO Output Frequency



Chapter 12 Package Dimensions

This section gives the physical dimensions for the package for the ICS1531, which is a 144-pin LQFP.

- The lead count (N) for the package is 144 leads.
- The nominal footprint (that is the body) for the package is 20 mm × 20 mm × 1.4 mm.

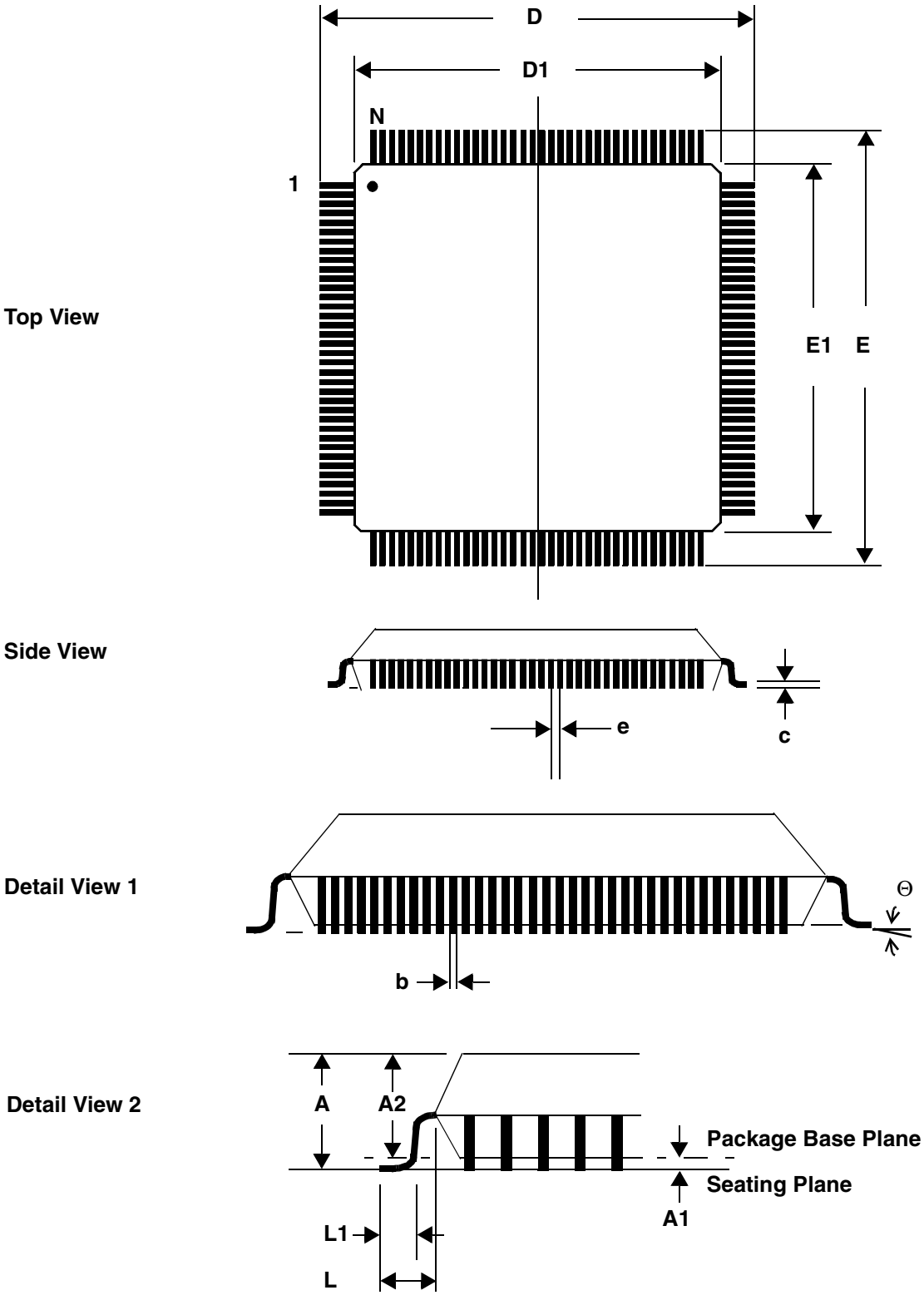
Note:

1. For full mechanical specifications, see JEDEC drawing number MS-026 Rev A.
2. Table 12-1 lists the ICS1531 physical dimensions. These dimensions are:
   a. For planning purposes only.
   b. Subject to change.
   c. Shown in Figure 12-1.

Table 12-1. Physical Dimensions for ICS1531

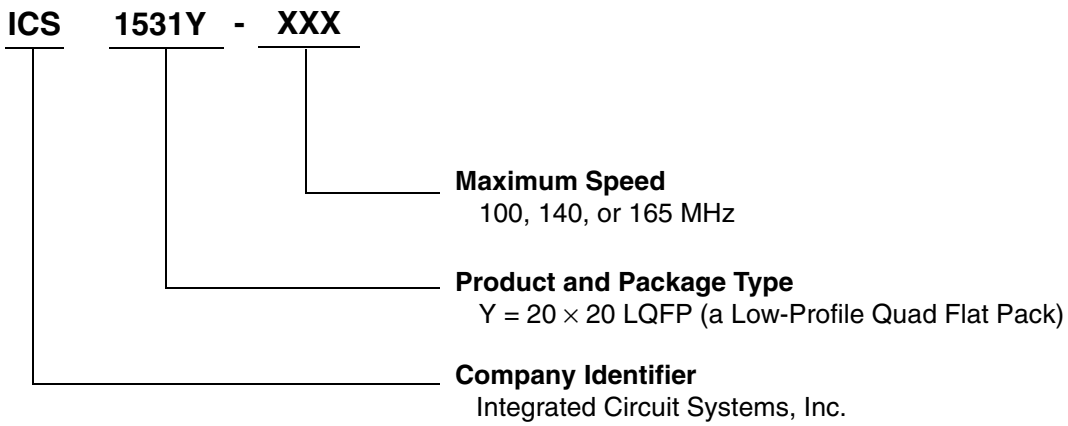
Symbol	Description	Min.	Nominal	Max.	Unit
A	Full Package Height	–	–	1.60	mm
A1	Package Body Standoff	0.05	–	0.15	mm
A2	Package Body Thickness	1.35	1.40	1.45	mm
b	Lead Width	0.17	0.22	0.27	mm
c	Lead Thickness	0.09	–	0.20	mm
D	Tip-to-Tip Dimension	21.8	22.0	22.2	mm
D1	Package Body Dimension	19.9	20.0	20.1	mm
e	Lead Pitch	–	0.50	–	mm
E	Tip-to-Tip Dimension	21.8	22.0	22.2	mm
E1	Package Body Dimension	19.9	20.0	20.1	mm
L	Lead Length, Entire Length	–	1.0	–	mm
L1	Lead Length, Segment 1 (Lead Tip Length)	0.45	0.60	0.75	mm
Θ	Lead Tip Angle	0	–	7	degrees

Figure 12-1. Physical Dimensions for ICS1531



Chapter 13 Ordering Information

Figure 13-1. ICS1531 Ordering Information



Notes

Revision History

Changes are not tracked for advance and preliminary copies.

Rev A was an advance copy dated 7/16/98.

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