DATA SHEET

CBTD16211

24-bit level shifting bus exchange switch with 12-bit output enables

Product data

2001 Jun 13

Philips Semiconductors

PHILIPS

24-bit level shifting bus exchange switch with 12-bit output enables

CBTD16211

FEATURES

- 5Ω switch connection between two ports
- TTL compatible control input levels
- Designed to be used in level shifting applications
- Package options include shrink small outline (SSOP) and thin shrink small outline (TSSOP)
- ESD protection exceeds 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

The CBTD16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

A diode to V_{CC} is integrated in the circuit to allow for level shifting between 5 V inputs and 3.3 V outputs.

The device is organized as a dual 12-bit bus switch with separate output-enable ($\overline{OE}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and a high-impedance state exists between the ports.

The CBTD16211 is characterized for operation from –40 to +85 °C.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50 pF; V_{CC} = 5 V	0.25	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4.3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0 V or V_{CC}	6.9	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5 V	3.0	µA

ORDERING INFORMATION

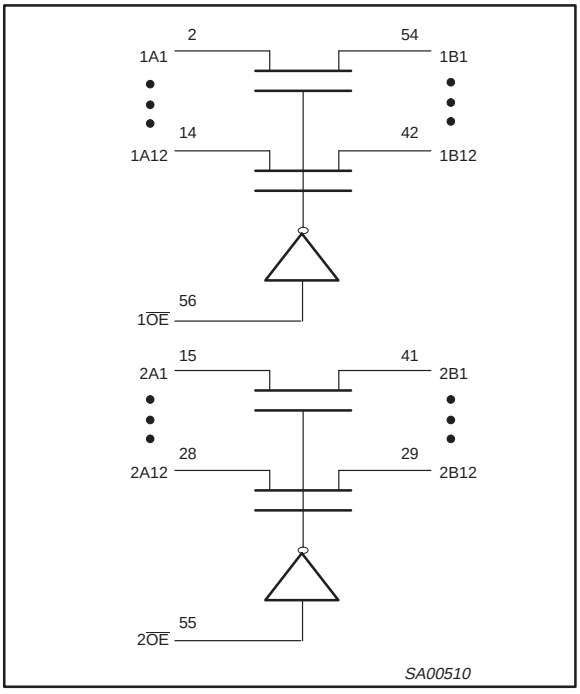
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP Type III	–40 to +85 °C	CBTD16211DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40 to +85 °C	CBTD16211DGG	SOT364-1

FUNCTION TABLE

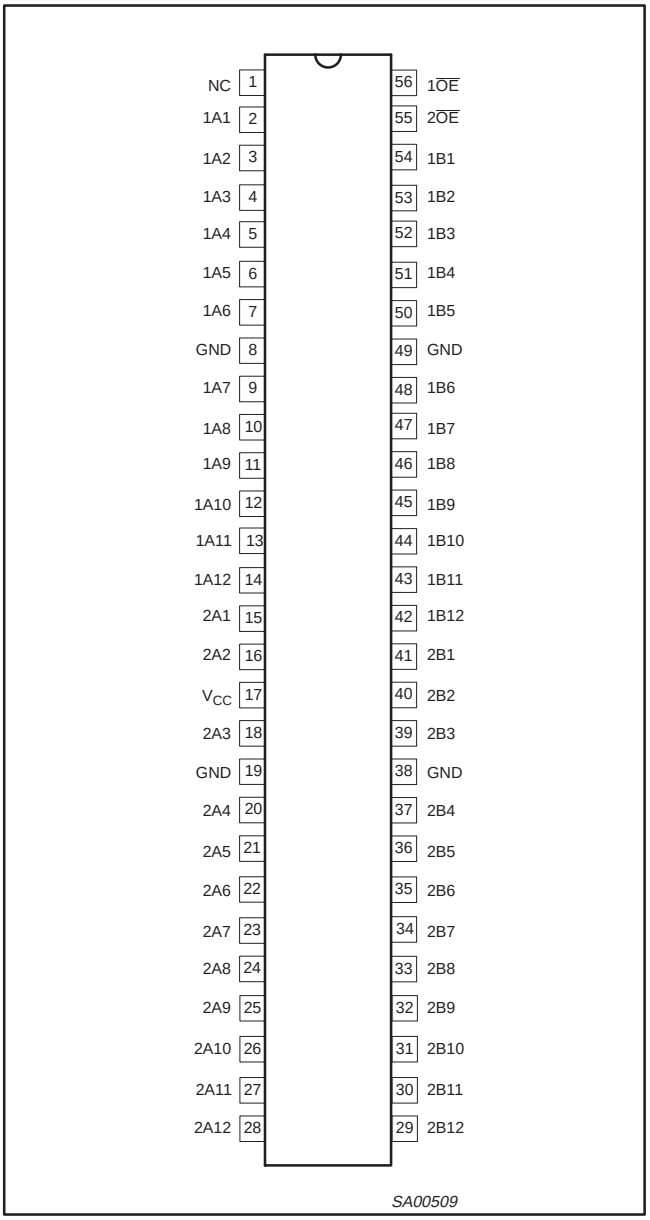
INPUTS		OUTPUTS	
$1\overline{OE}$	$2\overline{OE}$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance “off” state

LOGIC SYMBOL



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	NC	No internal connection
56, 55	$1\overline{OE}$, $2\overline{OE}$	Output enables
2, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14	1A1-1A12	Inputs
54, 53, 52, 51, 50, 48, 47, 46, 45, 44, 43, 42	1B1-1B12	Outputs
15, 16, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28	2A1-2A12	Inputs
41, 40, 39, 37, 36, 35, 34, 33, 32, 31, 30, 29	2B1-2B12	Outputs
8, 19, 38, 49	GND	Ground (0 V)
17	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.0	—	V
V_{IL}	Low-level Input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = –40 to +85 °C			
			Min	Typ[1]	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_I = –18 mA	—	—	–1.2	V
V_{OH}	Output high pass voltage	See Figure 1	—	—		V
I_I	Input leakage current	V_{CC} = 0 V; V_I = 5.5 V	—	—	10	µA
		V_{CC} = 5.5 V; V_I = GND or 5.5 V	—	—	±1	
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V; I_O = 0, V_I = V_{CC} or GND; $1\overline{OE}$=$2\overline{OE}$=GND	—	—	1.5	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	—	—	2.5	mA
C_I	Control pins	V_I = 3 V or 0	—	4.5	—	pF
$C_{I(OFF)}$	Port OFF capacitance	V_O = 3 V or 0, $\overline{OE}$ = V_{CC}	—	8	—	pF
r_{on}[3]		V_{CC} = 4.5 V; V_1 = 0 V; I_I = 64 mA	—	5	7	Ω
		V_{CC} = 4.5 V; V_1 = 0 V; I_I = 30 mA	—	5	7	
		V_{CC} = 4.5 V; V_1 = 2.4 V; I_I = –15 mA	—	35	50	

NOTES:
1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

GND = 0 V; $t_{R;}$ C_L = 50 pF

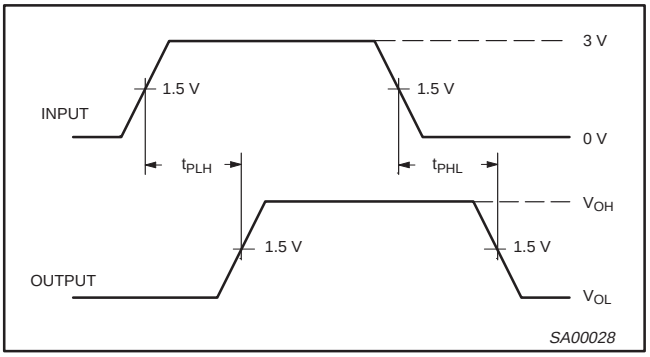
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5.0 V ±0.5 V		UNIT
				Min	Max	
t_{pd}	Propagation delay[1]	A or B	B or A	—	0.25	ns
t_{en}	Output enable time to High and Low level	$\overline{OE}$	A or B	1.5	8.5	ns
t_{dis}	Output disable time from High and Low level	$\overline{OE}$	A or B	1.5	7	ns

NOTE:

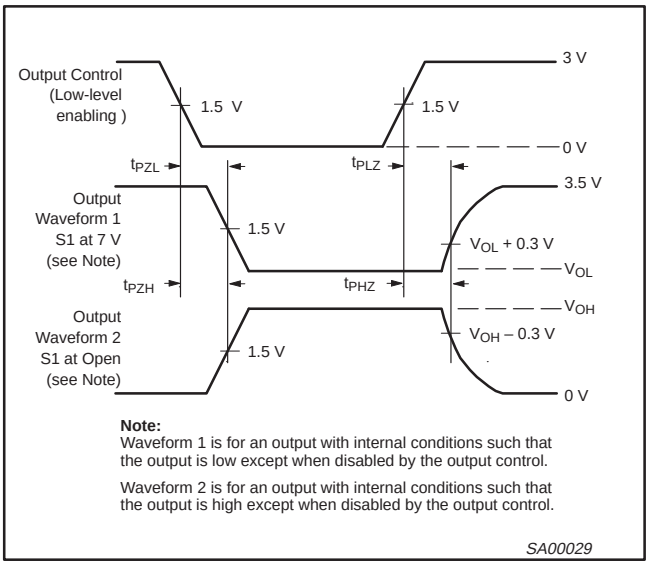
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V



Waveform 1. Input (An) to Output (Yn) Propagation Delays

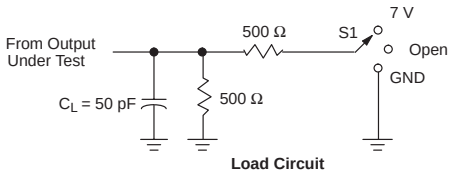


Note:
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Load Circuit

TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

TYPICAL CHARACTERISTICS

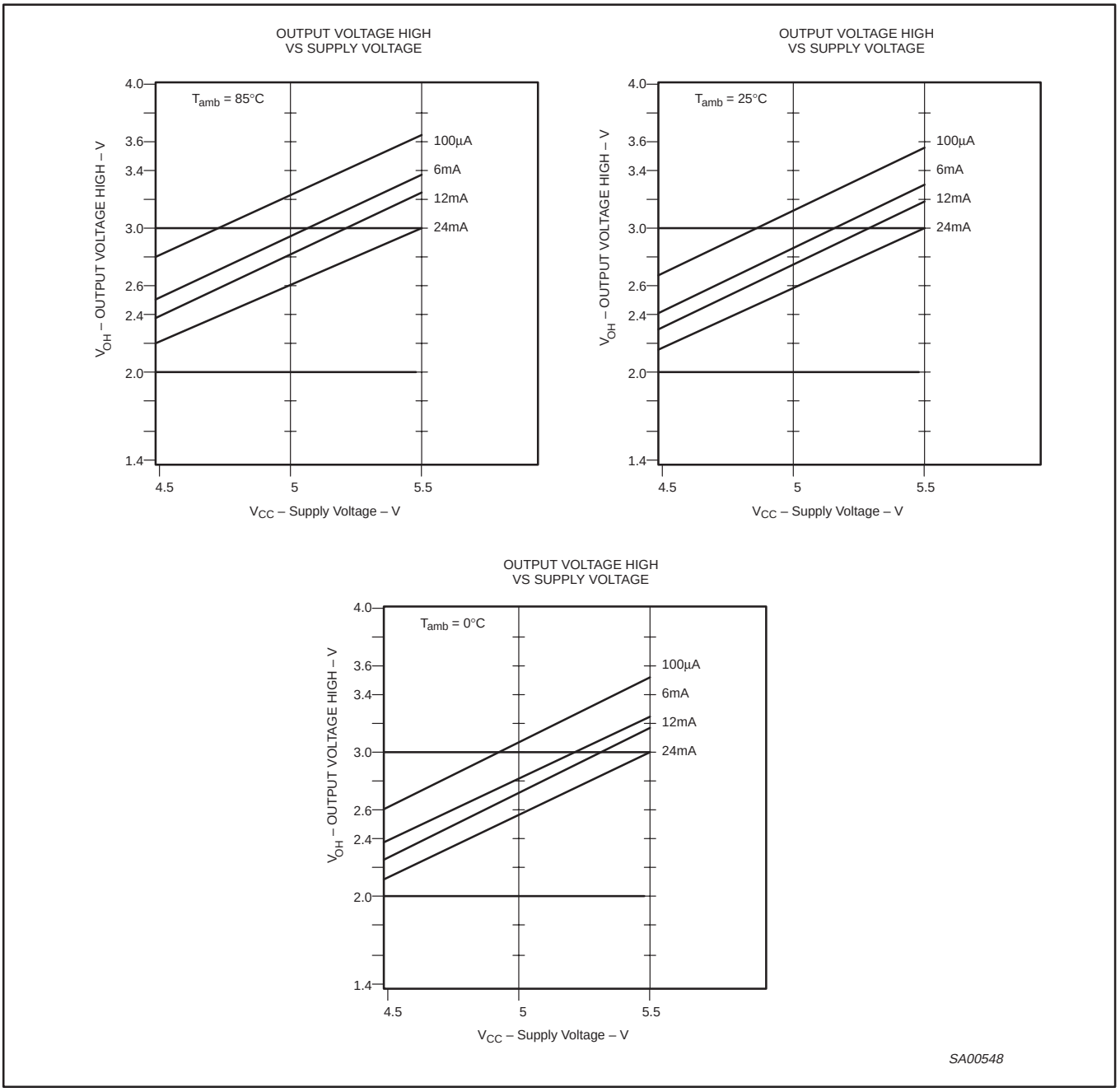
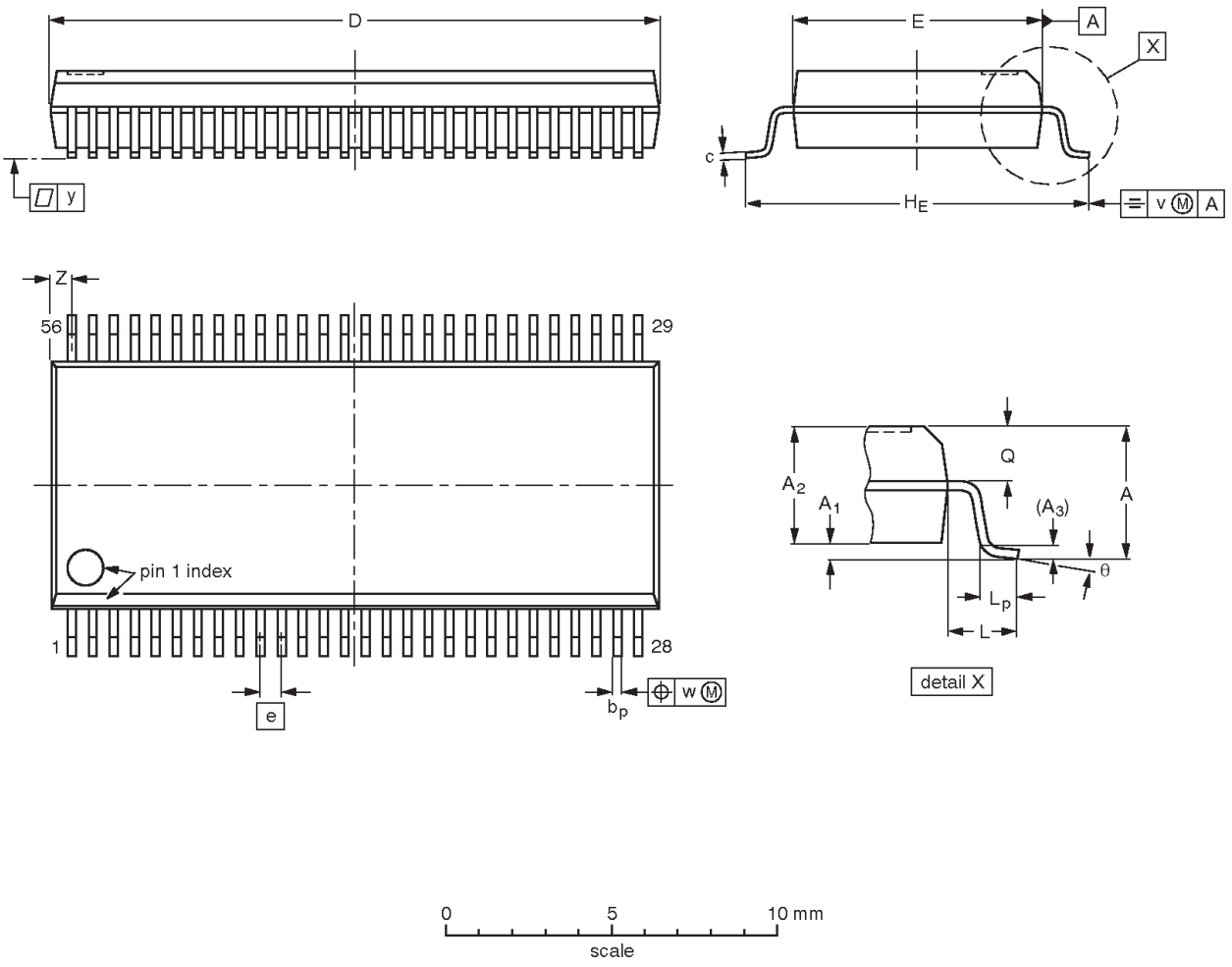


Figure 1. V_{OH} values (V_{in} = V_{CC})

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

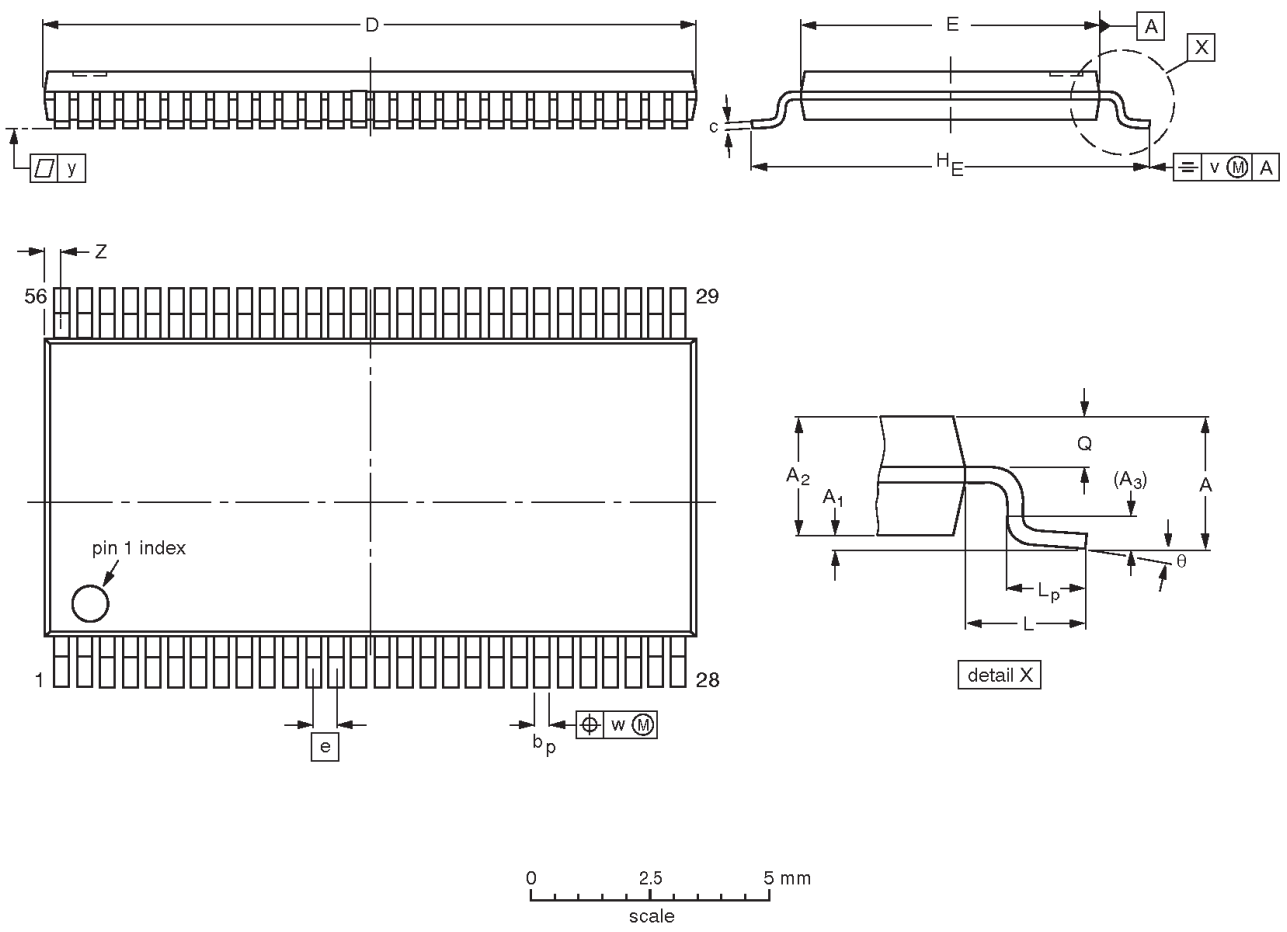
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				~~95-02-04~~ 99-12-27

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153					~~95-02-10~~ 99-12-27

24-bit level shifting bus exchange switch with 12-bit output enables

CBTD16211

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued datasheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

Date of release: 06-01

Document order number: 9793 750 08482

Let's make things better.

Philips Semiconductors

PHILIPS