Integrated Circuit Systems, Inc.

Product Brief

M2006-02/-12

VCSO Based FEC Clock PLL / Hitless Switching Option

General Description

The M2006-02 and -12 are VCSO (Voltage Controlled SAW Oscillator) based clock generator PLLs designed for clock frequency translation and jitter attenuation. They support both forward and inverse FEC (Forward Error Correction) clock multiplication ratios, which are pin-selected from pre-programming look-up tables.

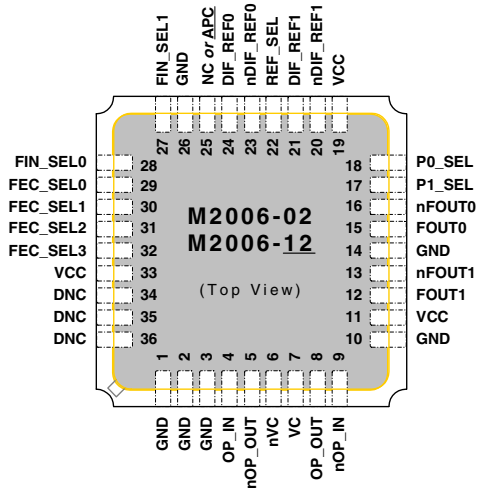
The M2006-12 adds Hitless Switching and Phase Build-out to enable SONET (GR-253) / SDH (G.813) MTIE and TDEV compliance during reference clock reselection. Hitless Switching (HS) engages when a 4ns or greater clock phase change is detected.

This phase-change triggered implementation of HS is not recommended when using an unstable reference (more than 1ns jitter pk-to-pk) or when the resulting phase detector frequency is less than 5MHz. Refer to full product data sheet for more information.

Features

- Pin-selectable PLL divider ratios support forward and inverse FEC ratio translation, including:
  - 255/238 (OTU1) Mapping and 238/255 De-mapping
  - 255/237 (OTU2) Mapping and 237/255 De-mapping
  - 255/236 (OTU3) Mapping and 236/255 De-mapping
- Supports input reference and VCSO frequencies up to 700MHz, supports loop timing modes (Specify VCSO frequency at time of order)
- Low phase jitter < 0.5 ps rms typical (12kHz to 20MHz or 50kHz to 80MHz)
- M2006-12 includes APC pin for Phase Build-out function (for absorption of the input phase change)
- Commercial and Industrial temperature grades
- Single 3.3V power supply
- Small 9 x 9 mm SMT (surface mount) package

Pin Assignment (9 x 9 mm SMT)



Example I/O Clock Frequency Combinations Using M2006-02/-12-622.0800 and Inverse FEC Ratios

FEC PLL Ratio Mfec / Rfec	Base Input Rate [1] (MHz)	Output Clock (either output) MHz
1/1	622.0800	622.08 or 155.52
238/255	666.5143	
237/255	669.3266	
236/255	672.1627	

Note 1: Input reference clock can be the base frequency shown divided by "Mfin", as shown in the following table.

Mfin Divider and Example Input Frequencies

FIN_SEL1:0	Mfin Value	For Base Input Rate of 622.0800 Sample Ref. Freq. (MHz)
1 1	1	622.08
1 0	4	155.52
0 1	8	77.76
0 0	32	19.44

Simplified Block Diagram