

Features

- 256K x 36 or 512K x 18 organization
- CMOS technology
- Double-data-rate (DDR) and single-data-rate (SDR) synchronous mode of operation
- Pipeline mode of operation
- Self-timed late write with full data coherence
- Single differential high-speed transceiver logic (HSTL) clock with HSTL input and output levels
- 2.5V power supply, 1.8V V_{DDQ}
- Registered addresses, controls, and data-ins
- Burst mode of operation
- Common I/O
- Asynchronous output enable
- Boundary scan using a limited set of JTAG 1149.1 functions
- 9 x 17 bump ball grid array package with SRAM JEDEC standard pinout and boundary SCAN order
- Programmable impedance output driver

Description

The IBM04368CBLBC and IBM04188CBLBC 8Mb SRAMs are synchronous pipeline-mode, high-performance CMOS static random-access memories that have wide I/O and achieve 2.5ns cycle times. Single differential CK clocks are used to initialize the read/write operation; all internal operations are self-timed. At the rising edge of the CK clock, addresses

and controls are registered internally. Data-outs are updated from output registers on the next rising and falling edges of the CK clock, hence the double data rate. Internal write buffers allow write data to follow one cycle after addresses and controls. The SRAM is operated with a single 2.5V power supply and is compatible with HSTL I/O interfaces.



x36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7	8	9
A	V _{SS}	V _{DDQ}	SA13	SA11	ZQ	SA10	SA8	V _{DDQ}	V _{SS}
B	DQ23	DQ20	SA14	V _{SS}	B1	V _{SS}	SA7	DQ15	DQ12
C	V _{SS}	V _{DDQ}	SA15	SA12	\bar{G}	SA9	SA6	V _{DDQ}	V _{SS}
D	DQ24	DQ21	NC	V _{SS}	V _{DD}	V _{SS}	SA5	DQ14	DQ11
E	V _{SS}	V _{DDQ}	V _{SS}	V _{DD}	V _{REF}	V _{DD}	V _{SS}	V _{DDQ}	V _{SS}
F	DQ25	CQ	DQ18	V _{DD}	V _{DD}	V _{DD}	DQ17	CQ	DQ10
G	V _{SS}	V _{DDQ}	V _{SS}	V _{SS}	CK	V _{SS}	V _{SS}	V _{DDQ}	V _{SS}
H	DQ26	DQ22	DQ19	V _{DD}	\bar{CK}	V _{DD}	DQ16	DQ13	DQ9
J	V _{SS}	V _{DDQ}	V _{SS}	V _{DD}	V _{DD}	V _{DD}	V _{SS}	V _{DDQ}	V _{SS}
K	DQ27	DQ31	DQ34	V _{SS}	B2	V _{SS}	DQ1	DQ4	DQ8
L	V _{SS}	V _{DDQ}	V _{SS}	\bar{LBO}	B3	MODE ¹	V _{SS}	V _{DDQ}	V _{SS}
M	DQ28	\bar{CQ}	DQ35	V _{DD}	V _{DD}	V _{DD}	DQ0	\bar{CQ}	DQ7
N	V _{SS}	V _{DDQ}	V _{SS}	V _{DD}	V _{REF}	V _{DD}	V _{SS}	V _{DDQ}	V _{SS}
P	DQ29	DQ32	NC	V _{SS}	V _{DD}	V _{SS}	SA4	DQ3	DQ6
R	V _{SS}	V _{DDQ}	V _{DD}	SA17	SA1	SA2	V _{DD}	V _{DDQ}	V _{SS}
T	DQ30	DQ33	SA16	V _{SS}	SA0	V _{SS}	SA3	DQ2	DQ5
U	V _{SS}	V _{DDQ}	TMS	TDI	TCK	TDO	NC ²	V _{DDQ}	V _{SS}

1. The MODE pin must be connected to V_{SS} or floated. The MODE pin has a very small pull-down, less than 5μA current at the V_{DD} input.
2. ESD protection diodes reside on this NC bump.

x18 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7	8	9
A	V _{SS}	V _{DDQ}	SA13	SA11	ZQ	SA10	SA8	V _{DDQ}	V _{SS}
B	NC	DQ10	SA14	V _{SS}	B1	V _{SS}	SA7	NC	DQ5
C	V _{SS}	V _{DDQ}	SA15	SA12	\bar{G}	SA9	SA6	V _{DDQ}	V _{SS}
D	DQ11	NC	NC	V _{SS}	V _{DD}	V _{SS}	SA5	DQ7	NC
E	V _{SS}	V _{DDQ}	V _{SS}	V _{DD}	V _{REF}	V _{DD}	V _{SS}	V _{DDQ}	V _{SS}
F	NC	CQ	NC	V _{DD}	V _{DD}	V _{DD}	DQ8	NC	DQ4
G	V _{SS}	V _{DDQ}	V _{SS}	V _{SS}	CK	V _{SS}	V _{SS}	V _{DDQ}	V _{SS}
H	DQ12	NC	DQ9	V _{DD}	\bar{CK}	V _{DD}	NC	DQ6	NC
J	V _{SS}	V _{DDQ}	V _{SS}	V _{DD}	V _{DD}	V _{DD}	V _{SS}	V _{DDQ}	V _{SS}
K	NC	DQ15	NC	V _{SS}	B2	V _{SS}	DQ0	NC	DQ3
L	V _{SS}	V _{DDQ}	V _{SS}	\bar{LBO}	B3	MODE ¹	V _{SS}	V _{DDQ}	V _{SS}
M	DQ13	NC	DQ17	V _{DD}	V _{DD}	V _{DD}	NC	\bar{CQ}	NC
N	V _{SS}	V _{DDQ}	V _{SS}	V _{DD}	V _{REF}	V _{DD}	V _{SS}	V _{DDQ}	V _{SS}
P	NC	DQ16	SA18	V _{SS}	V _{DD}	V _{SS}	SA4	NC	DQ2
R	V _{SS}	V _{DDQ}	V _{DD}	SA17	SA1	SA2	V _{DD}	V _{DDQ}	V _{SS}
T	DQ14	NC	SA16	V _{SS}	SA0	V _{SS}	SA3	DQ1	NC
U	V _{SS}	V _{DDQ}	TMS	TDI	TCK	TDO	NC ²	V _{DDQ}	V _{SS}

1. The MODE pin must be connected to V_{SS} or floated. The MODE pin has a very small pull down, less than 5μA current at the V_{DD} input.
2. ESD protection diodes reside on this NC bump.



Pin Description

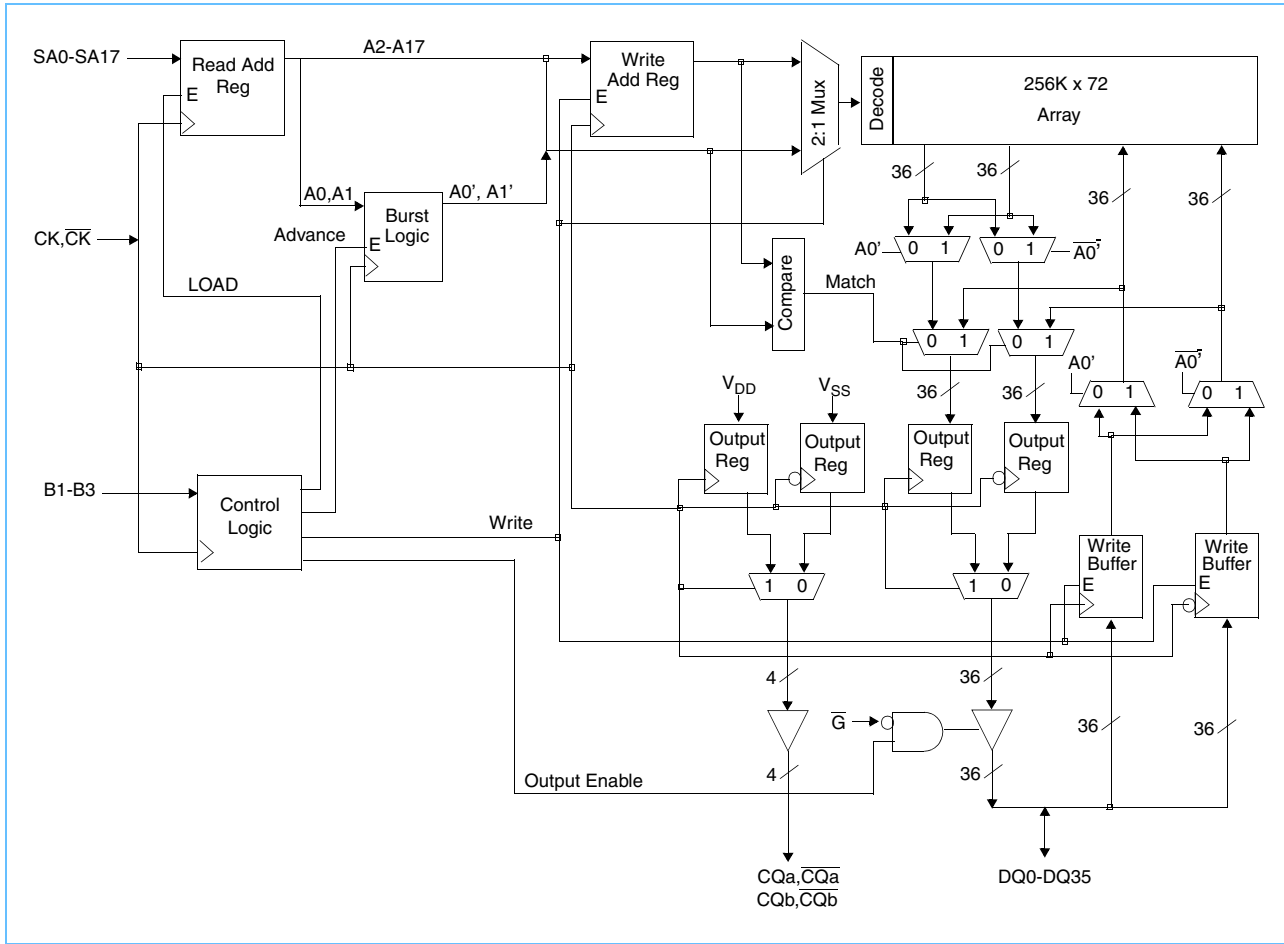
SA0-SA18	Address Input (SA0-SA1 burst-control starting addresses)	TDO	IEEE 1149.1 Test Output (LVTTTL level)
DQ0-DQ35	Data I/O	\overline{G}	Asynchronous Output Enable
CQ, \overline{CQ}	Differential Echo Clocks	MODE	Mode Pin must be connected to V_{SS}
CK, \overline{CK}	Differential Input Register Clocks	V_{REF}	HSTL Input Reference Voltage
B1	B1 = 0 initiates a Load operation	V_{DD}	Power Supply (+2.5V)
B2	B2 = 0 initiates a Write operation	V_{SS}	Ground
B3	B3 = 0 Double Data Rate, B3 = 1 Single Data Rate	V_{DDQ}	Output Power Supply
\overline{LBO}	Linear Burst Order ($\overline{LBO} = 1$, interleave mode; $\overline{LBO} = 0$, linear mode)	ZQ	Output Driver Impedance Control
TMS, TDI, TCK	IEEE® 1149.1 Test Inputs (LVTTTL levels)	NC	No Connect

Ordering Information

Part Number	Organization	Cycle Time (ns)	Package
IBM04368CBLBC-25	256K x 36	2.5	9 x 17 BGA
IBM04368CBLBC-28	256K x 36	2.8	9 x 17 BGA
IBM04368CBLBC-30	256K x 36	3.0	9 x 17 BGA
IBM04368CBLBC-35	256K x 36	3.5	9 x 17 BGA
IBM04188CBLBC-25	512K x 18	2.5	9 x 17 BGA
IBM04188CBLBC-28	512K x 18	2.8	9 x 17 BGA
IBM04188CBLBC-30	512K x 18	3.0	9 x 17 BGA
IBM04188CBLBC-35	512K x 18	3.5	9 x 17 BGA



Block Diagram (x36 Double-Data-Rate Mode)



SRAM Features

DDR and SDR Modes

Timing Diagram: Double-Data-Rate and Single-Data-Rate Modes on page 6 shows input and output data placements for both DDR and SDR modes. In DDR read mode, two sets of data-outs are generated from the second rising and falling edges of the CK clock, assuming the first rising edge of the CK clock samples the base address. The first of the two data-out sets (DOUT-A) is generated from the sampled base address (Base-A). The second data-out set (DOUT-A') is generated from the next burst order address, according to the burst order definition. Similarly, a DDR write requires data-in placement on the second rising and falling CK edges. In SDR read mode, only one set of data-outs is generated from the second rising CK edge. In SDR write mode, one set of data-ins is sampled on the second rising CK edge. The user can switch from DDR to SDR mode (or from SDR to DDR mode) during any LOAD (B1 = 0) operation.

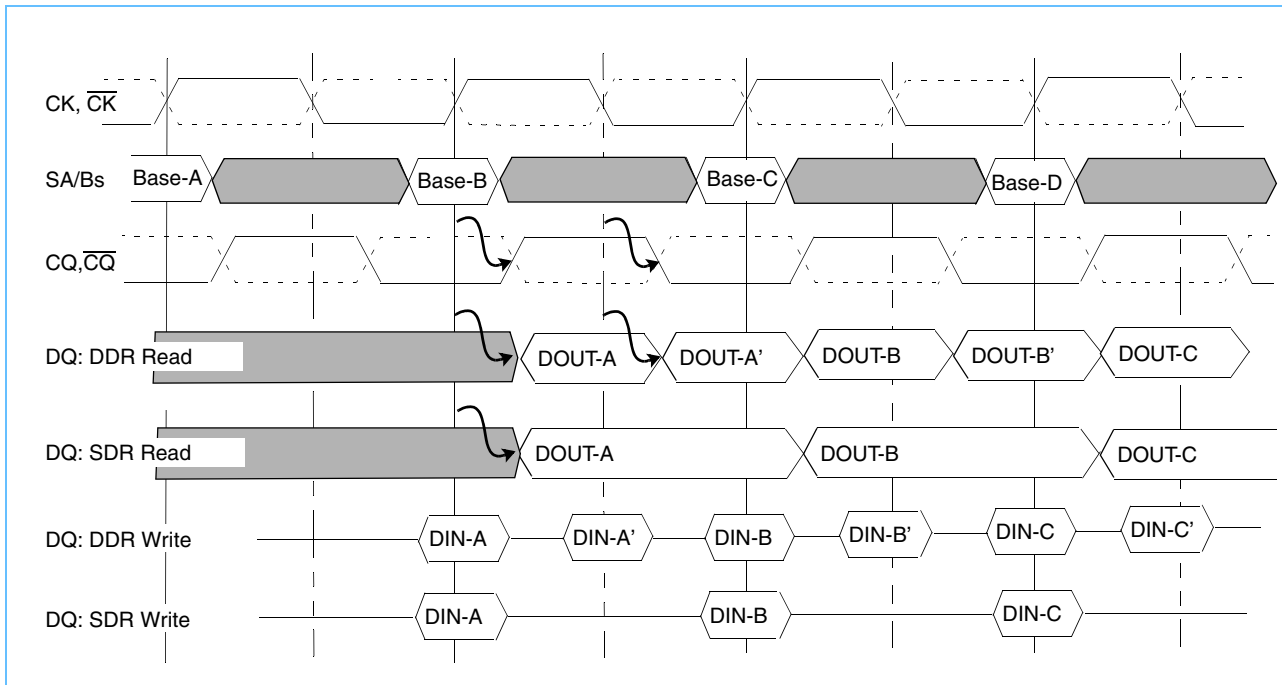
Late Write

The late-write function allows write data to be registered one cycle after addresses and controls. This feature eliminates one of two bus-turnaround cycles normally required when going from a read to a write operation. Late write is accomplished by buffering write addresses and data. The SRAM array update occurs during the third write cycle. Read-cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. Full data coherency is maintained for both DDR and SDR operations. As a result, NOP (write buffer flush) operations are not required going from write cycles to read cycles.

Echo Clocks

Echo clocks CQ and \overline{CQ} are generated from rising and falling edges of the CK clock, with access times representative of the data-outs. Echo clocks keep running during write and NOP operations. Echo-clock operation is identical for both DDR and SDR operations. The close tracking of echo clocks and data-out timings allows the echo clocks to be used as capture clocks for the data-outs by the receiving device.

Timing Diagram: Double-Data-Rate and Single-Data-Rate Modes



Programmable Impedance and Power-Up Requirements

An external resistor, R_Q , must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of R_Q must be five times the value of the intended line impedance driven by the SRAM. The allowable range of R_Q to guarantee impedance matching with a tolerance of 15% is between 175 Ω and 350 Ω . Periodic readjustment of the output driver impedance is necessary because the impedance is affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles; each evaluation can move the output driver impedance level one step at a time toward the optimum level. The output driver has 64 discrete binary weighted steps. Impedance updates for zeros occur whenever the SRAM is driving ones; impedance updates for ones occur whenever the SRAM is driving zeros. Updates of both zeros and ones occur when the SRAM is in High-Z. Furthermore, to guarantee the output driver impedance, the SRAM requires 2048 clock cycles and a Read '0' and Read '1' or a Read '1' and a Read '0' across all outputs. The RC time constant of the loaded R_Q trace must be less than 3 ns.

Power-Up and Power-Down Sequence

The power supplies must be powered up in the following sequence:

V_{DD} , V_{DDQ} , V_{REF} , followed by inputs

The power-down sequence must be in the reverse order. V_{DDQ} must not exceed V_{DD} .



Function Control

The function control is dependent on the state of the three function control pins (B1, B2 and B3), captured when CK transitions from low to high, as described in the following table (“n” refers to the current cycle and “n-1” refers to the previous SRAM cycle):

B1 (n-1)	B2 (n-1)	B3 (n-1)	B1 (n)	B2 (n)	B3 (n)	Function (n)
X	X	X	0	0	0	Load New Address, DDR Write
X	X	X	0	0	1	Load New Address, SDR Write
X	X	X	0	1	0	Load New Address, DDR Read
X	X	X	0	1	1	Load New Address, SDR Read
0	0	0	1	1	X	Continue Burst, DDR Write
0	0	1	1	1	X	Continue Burst, SDR Write
0	1	0	1	1	X	Continue Burst, DDR Read
0	1	1	1	1	X	Continue Burst, SDR Read
X	X	X	1	0	X	NOP (High-Z cycle n+1)
1	0	X	1	X	X	NOP (High-Z cycle n+2)

Burst Order Definition

The DC state of the $\overline{\text{LBO}}$ pin determines the burst order of the addresses, given the starting address in a Load operation (B1 = 0). The following table defines the order of addresses for the two different states of $\overline{\text{LBO}}$.

Address Sequence when $\overline{\text{LBO}} = V_{DD}$ (Interleave Burst)

	SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Starting address	0	0	0	1	1	0	1	1
Second address	0	1	0	0	1	1	1	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	1	0	0	1	0	0

Address Sequence when $\overline{\text{LBO}} = V_{SS}$ (Linear Burst)

	SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Starting address	0	0	0	1	1	0	1	1
Second address	0	1	1	0	1	1	0	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	0	0	0	1	1	0



Clock Truth Table

CK	B1 (n)	B2 (n)	B3 (n)	DQ (n)	DQ (n+1)	DQ (n+1.5)	Mode
L→H	L	H	H	X	D _{OUT} 0-35	Previous Data Held	Read Cycle SDR
L→H	L	H	L	X	D _{OUT} 0-35a	D _{OUT} 0-35b	Read Cycle DDR
L→H	L	L	H	X	D _{IN} 0-35	X	Write Cycle SDR
L→H	L	L	L	X	D _{IN} 0-35a	D _{IN} 0-35b	Write Cycle DDR
L→H	H	L	X	X	High-Z	High-Z	NOP (Deselect) Cycle
L→H	H	H	X				Continue Burst Operation

Output Enable Truth Table

Operation (n, n+1)	\overline{G} (n)	\overline{G} (n+1)	DQ (n)	DQ (n+1)
Read	L	L	X	D _{OUT} 0-35
Read	H	H	High-Z	High-Z
Write	L	L	X	High-Z
NOP	L	L	X	High-Z

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V _{DD}	Power Supply Voltage	-0.5 to 2.825	V	1
V _{IN}	Input Voltage	-0.5 to 3.0	V	1
V _{OUT}	Output Voltage	-0.5 to 2.825	V	1
T _A	Operating Temperature	0 to +85	°C	1
T _J	Junction Temperature	0 to +110	°C	
T _{STG}	Storage Temperature	-55 to +125	°C	1
I _{OUT}	Short Circuit Output Current	25	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect reliability.



Recommended DC Operating Conditions (T_A = 0 to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V _{DD}	Supply Voltage	2.5V - 5%	2.5	2.5V + 5%	V	1
V _{DDQ}	Output Driver Supply Voltage	1.4	1.8	1.9	V	1
V _{IH}	Input High Voltage	V _{REF} + 0.1		V _{DDQ} + 0.3	V	1, 2
V _{IL}	Input Low Voltage	-0.3		V _{REF} - 0.1	V	1, 3
V _{REF}	Input Reference Voltage	0.68	.9	1.0	V	1, 6
V _{IN-CLK}	Clocks Signal Voltage	-0.3		V _{DDQ} + 0.3	V	1, 4
V _{DIF-CLK}	Differential Clocks Signal Voltage	0.1		V _{DDQ} + 0.6	V	1, 5
V _{CM-CLK}	Clocks Common Mode Voltage	0.55		0.9	V	1

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ} and V_{SS} pins must be connected.
 2. V_{IH}(Max) DC = V_{DDQ} + 0.3V, V_{IH}(Max) AC = V_{DDQ} + 0.85 (pulse width ≤ 2ns).
 3. V_{IL}(Min) DC = -0.3V, V_{IL}(Min) AC = -1.5V (pulse width ≤ 2ns).
 4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (CK, \overline{CK}).
 5. V_{DIF-CLK} specifies the minimum clock differential voltage required for switching.
 6. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V ±5%)

Symbol	Parameter	Min.	Max.	Units	Notes	
I _{DD}	Average Power Supply Operating Current (I _{OUT} = 0, V _{IN} = V _{IH} or V _{IL})	x36	-25	750	mA	1
			-30	640		
			-40	510		
		x18	-25	540	mA	1
			-30	470		
			-40	390		
I _{SB}	Power Supply Standby Current SS = VIH, all other inputs = V _{IH} or V _{IL} , I _{OUT} = 0		150	mA	1	
I _{LI}	Input Leakage Current, any input (V _{IN} = V _{SS} or V _{DDQ})	-2	+2	μA		
I _{LO}	Output Leakage Current (V _{OUT} = V _{SS} or V _{DDQ} , DQ in High-Z)	-5	+5	μA		
V _{OH}	Output "High" Level Voltage (I _{OH} = -6mA)		V _{DDQ} - 0.4	V _{DDQ}	V	2
V _{OL}	Output "Low" Level Voltage (I _{OL} = +6mA)		V _{SS}	V _{SS} + 0.4	V	2
I _{LIJTAG}	JTAG Leakage Current (V _{IN} = V _{SS} or V _{DD})		-70	+10	μA	3

1. I_{OUT} = Device Output Current.
 2. Minimum Impedance Output Driver.
 3. For JTAG Inputs only.

Programmable Impedance Output Driver DC Electrical Characteristics

($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 2.5\text{V} \pm 5\%$)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OH}	Output High Voltage	$V_{DDQ} / 2$	V_{DDQ}	V	1, 3
V_{OL}	Output Low Voltage	V_{SS}	$V_{DDQ} / 2$	V	2, 3

- $I_{OH} = (V_{DDQ} / 2) / (R_Q / 5) \pm 15\%$ @ $V_{OH} = V_{DDQ} / 2$ (for: $175\Omega \leq R_Q \leq 350\Omega$)
- $I_{OL} = (V_{DDQ} / 2) / (R_Q / 5) \pm 15\%$ @ $V_{OL} = V_{DDQ} / 2$ (for: $175\Omega \leq R_Q \leq 350\Omega$)
- Parameter tested with $R_Q = 250\Omega$ and $V_{DDQ} = 1.8\text{V}$

PBGA Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.6	$^\circ\text{C/W}$

Capacitance ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 2.5\text{V} \pm 5\%$, $f = 1\text{MHz}$)

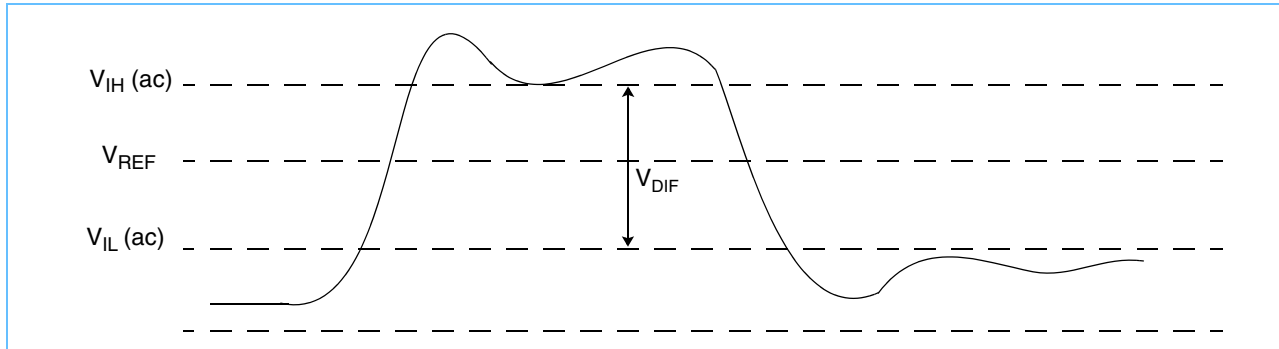
Symbol	Parameter	Test Condition	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4	pF
C_{OUT}	Data I/O Capacitance (DQ0–DQ35)	$V_{OUT} = 0\text{V}$	5	pF

AC Input Characteristics ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 2.5\text{V} \pm 5\%$)

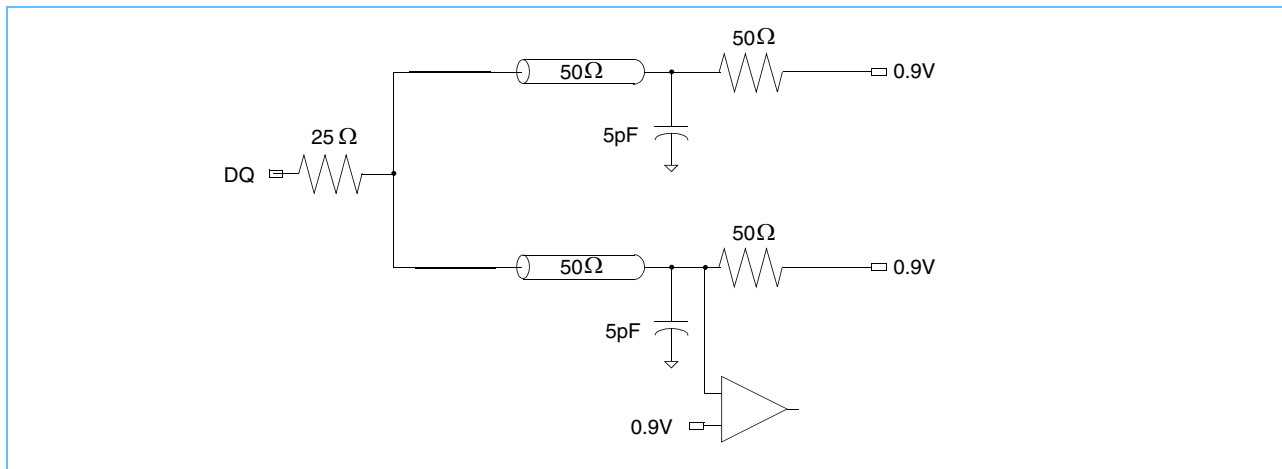
Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH(ac)}$	AC Input Logic High	$V_{REF} + 400$		mV	3, 4
$V_{IL(ac)}$	AC Input Logic Low		$V_{REF} - 400$	mV	3, 4
$V_{DIF(ac)}$	Clock Input Differential Voltage	800		mV	2, 3
$V_{REF(ac)}$	V_{REF} Peak-to-Peak AC Voltage		$5\% V_{REF}$ (DC)	mV	1

- The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF} .
- SRAM performance is a function of clock input differential voltage (V_{DIF}).
- To guarantee AC characteristics; V_{IH} , V_{IL} , T_{rise} and T_{fall} of the inputs and clocks must be within 20% of each other. If these conditions are not met then:
 - Setup time is measured from clock crossing to inputs at their switched V_{IHAC} and V_{ILAC} levels.
 - Hold time is measured from clock crossing to inputs switching out of their valid V_{IHAC} and V_{ILAC} levels.
- See *AC Input Definition* on page 11.

AC Input Definition



AC Test Loading



AC Test Conditions ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 2.5\text{V} \pm 5\%$, $V_{DDQ} = 1.8\text{V}$)

Symbol	Parameter	Conditions	Units	Notes
V_{IH}	Input High Level	1.5	V	
V_{IL}	Input Low Level	0.3	V	
V_{REF}	Input Reference Voltage	0.9	V	
$V_{DIF-CLK}$	Differential Clocks Voltage	1.2	V	
V_{CM-CLK}	Clocks Common Mode Voltage	0.9	V	
t_R	Input Rise Time	0.5	ns	
t_F	Input Fall Time	0.5	ns	
	I/O Signals Reference Level (except CK clocks)	0.9	V	
	Clocks Reference Level	Differential Cross Point	V	
	Output Load Conditions			1

1. See AC Test Loading

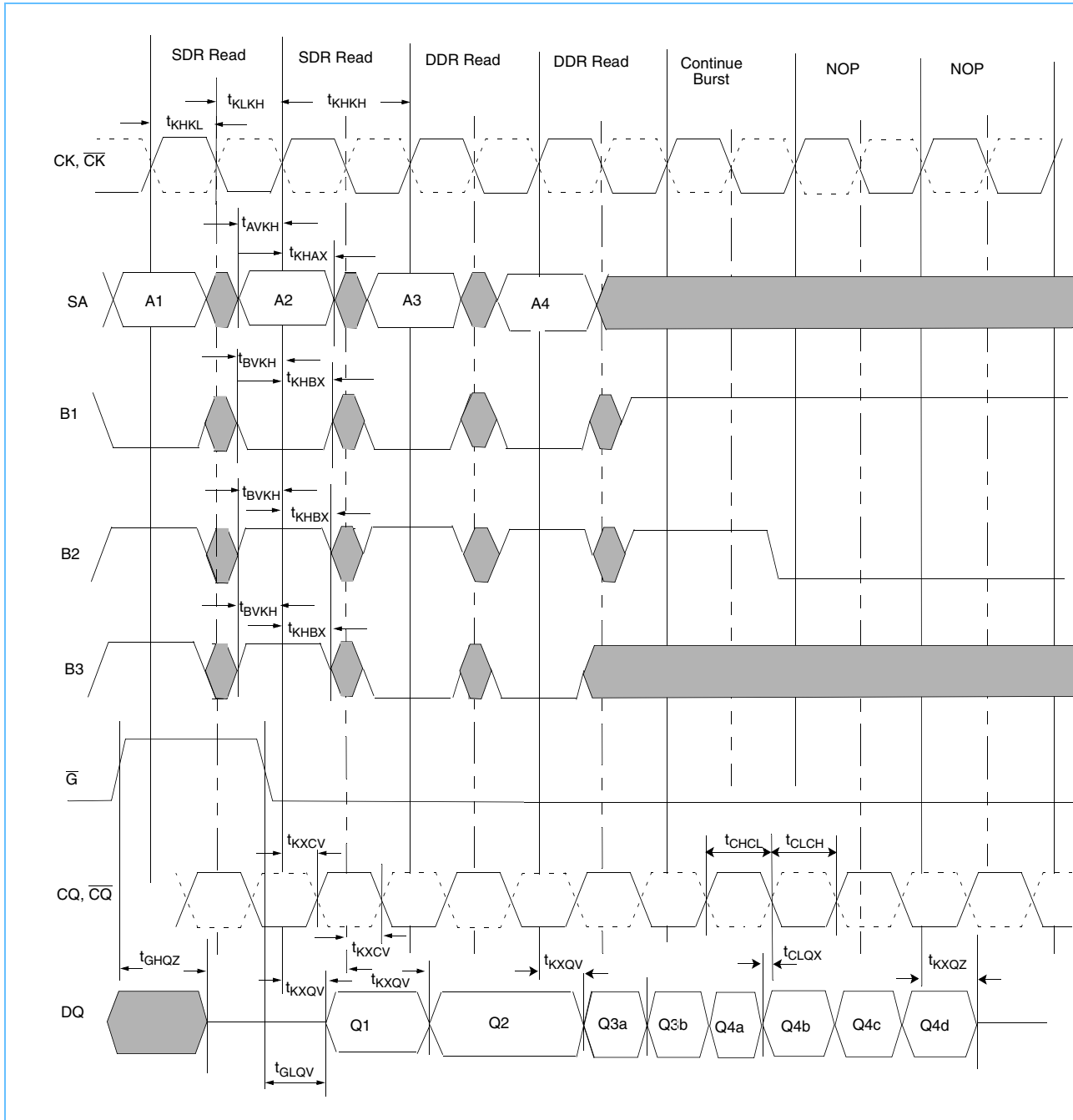


AC Characteristics ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 2.5\text{V} \pm 5\%$)

Symbol	Parameter	-25		-28		-30		-35		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{KHKL}	Cycle Time	2.5		2.8		3.0		3.5		ns	
t_{KHL}	Clock High Pulse Width	1.2		1.2		1.4		1.6		ns	
t_{KLKH}	Clock Low Pulse Width	1.2		1.2		1.4		1.6		ns	
t_{AVKH}	Address Setup Time	0.4		0.4		0.5		0.5		ns	1, 2,
t_{KHAX}	Address Hold Time	0.4		0.4		0.5		0.5		ns	1, 2, 6
t_{BVKH}	Function Control (B1, B2, B3) Setup Time	0.4		0.4		0.5		0.5		ns	1, 2, 6
t_{KHBX}	Function Control (B1, B2, B3) Hold Time	0.4		0.4		0.5		0.5		ns	1, 2, 6
t_{DVKH}	Data In Setup Time	0.21		0.25		0.25		0.3		ns	1, 2, 3, 6
t_{KHDX}	Data In Hold Time	0.21		0.25		0.25		0.3		ns	1, 2, 3, 6
t_{INPW}	Input Pulse Width	1.0		1.0		1.2		1.6			7
t_{CHCL}	Echo Clock (CQ) High Pulse Width	t_{KHKL} -0.1	t_{KHKL} +0.1	t_{KHKL} -0.1	t_{KHKL} +0.1	t_{KHKL} -0.1	t_{KHKL} +0.1	t_{KHKL} -0.1	t_{KHKL} +0.1	ns	1, 3, 6
t_{CLCH}	Echo Clock (CQ) Low Pulse Width	t_{KLKH} -0.1	t_{KLKH} +0.1	t_{KLKH} -0.1	t_{KLKH} +0.1	t_{KLKH} -0.1	t_{KLKH} +0.1	t_{KLKH} -0.1	t_{KLKH} +0.1	ns	1, 3, 6
t_{KXCV}	Clock (CK) crossing to Echo clock (CQ) Valid - slow corner	0.8	1.8	0.8	1.8	0.8	1.7	0.8	1.8	ns	1, 4, 6
t_{KXQV}	Clock (CK) crossing to Output Valid	0.8	1.8	0.8	1.8	0.8	1.7	0.8	1.8	ns	1, 6
t_{KXQZ}	Clock (CK) crossing to Output High-Z	0.8	1.8	0.8	1.8	0.8	1.7	0.8	1.8	ns	1, 6
t_{KXQLZ}	Clock (CK) crossing to Output Active	0.8	1.8	0.8	1.8	0.8	1.7	0.8	1.8	ns	1, 6
t_{QVTRK}	Echo Clock (CQ) Valid to Output Valid Tracking ($t_{KXCV} - t_{KXQV}$)	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	ns	1, 3, 5, 6
t_{QZTRK}	Echo Clock (CQ) Valid to Output High-Z Tracking ($t_{KXCV} - t_{KXQZ}$)	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	ns	1, 3, 5, 6
$t_{QLZ-TRK}$	Echo Clock (CQ) Valid to Output Active Tracking ($t_{KXCV} - t_{KXQLZ}$)	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	ns	1, 3, 5, 6
t_{GHQZ}	Output Enable (\overline{G}) High to High-Z		1.7	—	1.7		2.0		2.0	ns	3
t_{GLQV}	Output Enable (\overline{G}) Low to Output Valid		1.7	0.5	1.7		2.0		2.0	ns	3

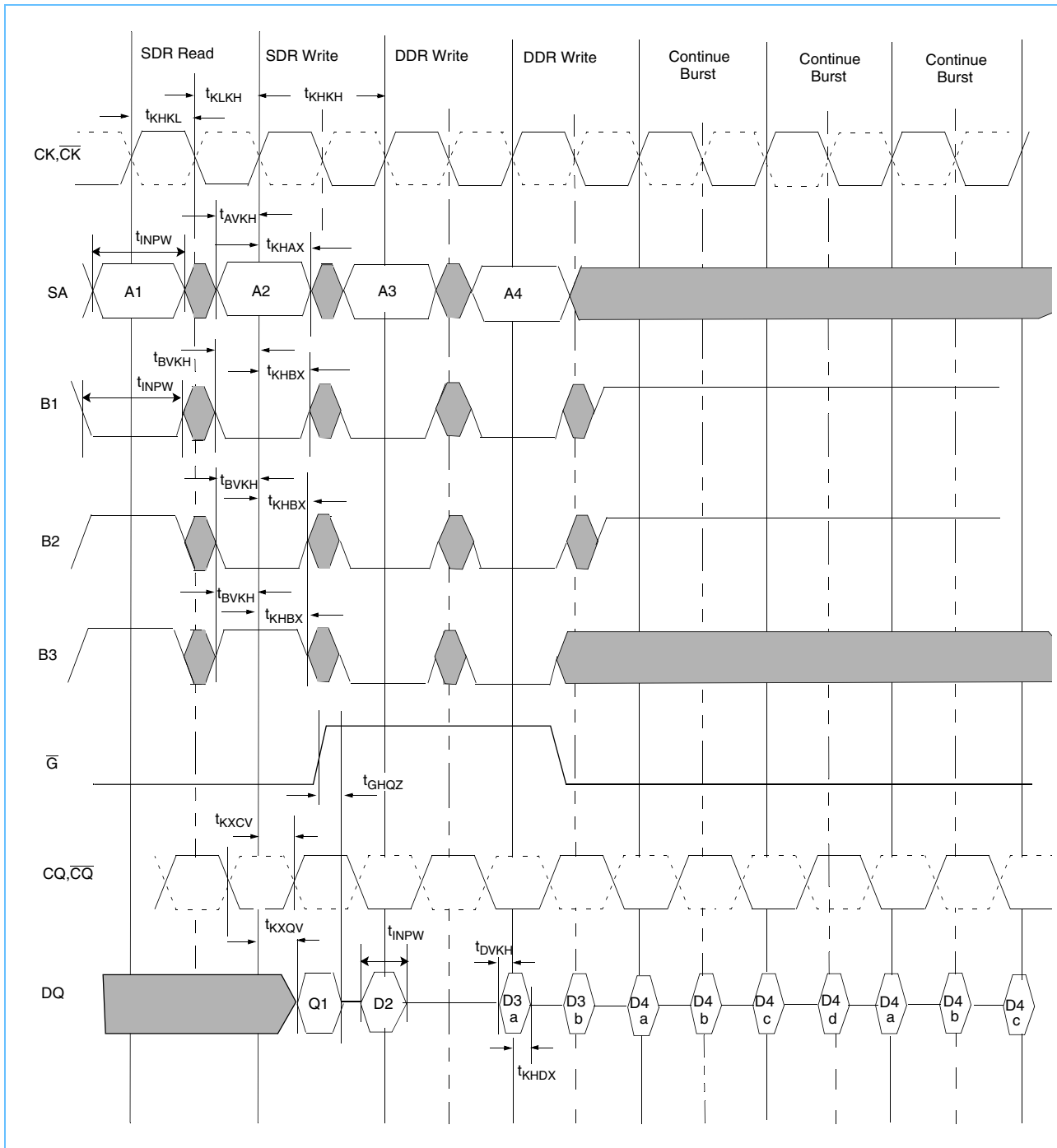
1. See *AC Test Loading* on page 11. To guarantee AC timing specifications, AC test conditions must be met.
2. To guarantee AC characteristics; V_{IH} , V_{IL} , T_{rise} , and T_{fall} of inputs and clocks must be within 20% of each other. If these conditions are not met, then setup time is measured from clock crossing to inputs at their switched V_{IHAC} , V_{ILAC} levels, and hold time is measured from clock crossing to inputs switching out of their valid V_{IHAC} , V_{ILAC} levels.
3. These parameters may not be tested at the values shown in this table, and may only be guaranteed by design.
4. Echo clock (CQ) Valid refers to CQ and \overline{CQ} rising and falling edges.
5. The tracking between echo-clock access times and DQ access times is across all cycle boundaries for any given SRAM address and function pattern.
6. CK and \overline{CK} clocks must be used differentially in order to meet specification.
7. Can not have an input pulse width that consists of $t_{minimum\ setup\ time} + t_{minimum\ hold\ time}$.

Timing Diagram (Read and NOP Cycles)





Timing Diagram (Read, Write Cycles)



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit-board traces or other components. There is no multiplexer in the path from the I/O pins to the RAM core.

In conformance with IEEE standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, a TRST signal is not required.

Signal List:

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

JTAG Recommended DC Operating Conditions ($T_A = 0$ to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH1}	JTAG Input High Voltage	2.0	—	$V_{DD} + 0.3V$	V	
V_{IL1}	JTAG Input Low Voltage	-0.3	—	0.8	V	
V_{OH1}	JTAG Output High Level	2.1	—	—	V	1
V_{OL1}	JTAG Output Low Level	—	—	0.2	V	2

1. OH1 = -2mA at 2.1V
 2. OL1 = +2mA at 0.2V

JTAG AC Test Conditions ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 2.5V \pm 5\%$)

Symbol	Parameter	Conditions	Units	Notes
V_{IH1}	Input Pulse High Level	2.0	V	
V_{IL1}	Input Pulse Low Level	0.0	V	
t_{R1}	Input Rise Time	2.0	ns	
t_{F1}	Input Fall Time	2.0	ns	
	Input and Output Timing Reference Level	1.0	V	1

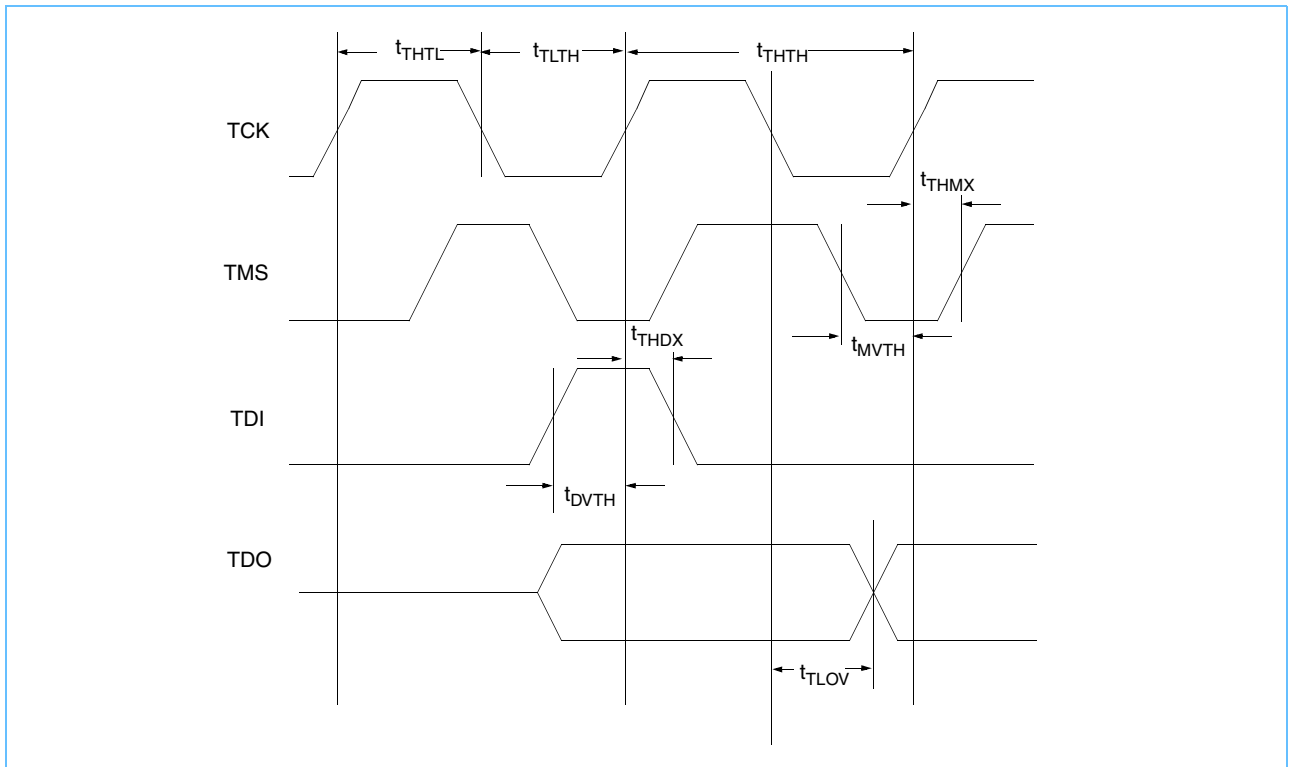
1. See *AC Test Loading* on page 11.

JTAG AC Characteristics ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 2.5\text{V} \pm 5\%$)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{THTH}	TCK Cycle Time	20		ns	
t_{HTL}	TCK High Pulse Width	7		ns	
t_{LTH}	TCK Low Pulse Width	7		ns	
t_{MVTH}	TMS Setup	4		ns	
t_{THMX}	TMS Hold	4		ns	
t_{DVTH}	TDI Setup	4		ns	
t_{THDX}	TDI Hold	4		ns	
t_{TLOV}	TCK Low to Valid Data		7	ns	1

1. See AC Test Loading on page 11.

JTAG Timing Diagram





Scan Register Definition

Register Name	Bit Size x18	Bit Size x36	Notes
Instruction	3	3	
Bypass	1	1	
ID	32	32	
Boundary Scan	49	68	1, 2

- The boundary-scan chain consists of the following bits:
 - 36 or 18 bits for data inputs depending on x36 or x18 configuration
 - 19 bits for SA0–SA18 for x36, 20 bits for SA0–SA19 for x18
 - 4 or 2 bits for CQ and \overline{CQ} clocks depending on x36 or x18 configuration
 - 9 bits for CK, \overline{CK} , ZQ, \overline{LBO} , B1, B2, B3, MODE and \overline{G}
- CK and \overline{CK} clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for boundary-scan sampling. CQ and \overline{CQ} clocks are sampled from the CK and \overline{CK} boundary scan register inputs.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit(0)
512K x 18	xxxx ¹	1011110011	101101	000101001001	1
256K x 36	xxxx ¹	1011010100	101101	000101001001	1

1. For IBM internal use.



Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	2
010	SAMPLE-Z	1
011	PRIVATE	5
100	SAMPLE	4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initialized to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. PRIVATE is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

This part has not been designed to comply with the following sections of IEEE 1149.1:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d



Boundary Scan Order (x36)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	SA1	5R	24	CQ	8F	47	CQ	2F
2	SA0	5T	25	DQ	9D	48	DQ	1F
3	SA	6R	26	DQ	7F	49	DQ	3H
4	SA	7T	27	DQ	8D	50	DQ	2H
5	SA	7P	28	DQ	9B	51	DQ	1H
6	DQ	8T	29	DQ	8B	52	ZQ	5A
7	DQ	9T	30	SA(8Mb)	7D	53	B1	5B
8	DQ	8P	31	SA	7C	54	B2	5K
9	DQ	7M	32	SA	7B	55	B3	5L
10	DQ	9P	33	SA	7A	56	$\overline{\text{LBO}}$	4L
11	$\overline{\text{CQ}}$	8M	34	SA	6C	57	DQ	1K
12	DQ	9M	35	SA	6A	58	DQ	2K
13	DQ	7K	36	SA	4A	59	DQ	3K
14	DQ	8K	37	SA	4C	60	DQ	1M
15	DQ	9K	38	SA	3A	61	$\overline{\text{CQ}}$	2M
16	MODE ³	6L	39	SA	3B	62	DQ	1P
17	$\overline{\text{CK}}$	5H	40	SA	3C	63	DQ	3M
18	CK	5G	41	PH ¹ (16Mb) ²	3D	64	DQ	2P
19	$\overline{\text{G}}$	5C	42	DQ	2B	65	DQ	1T
20	DQ	9H	43	DQ	1B	66	DQ	2T
21	DQ	8H	44	DQ	2D	67	SA	3T
22	DQ	7H	45	DQ	3F	68	SA	4R
23	DQ	9F	46	DQ	1D			

1. PH pins are place holders. BGA bump is a NC (no connect). PH pins are forced to V_{DD} .
2. Reserved address bit for 16Mb density.
3. MODE will scan out value placed on Mode pin or, if Mode pin is floated, Mode will scan V_{SS} .

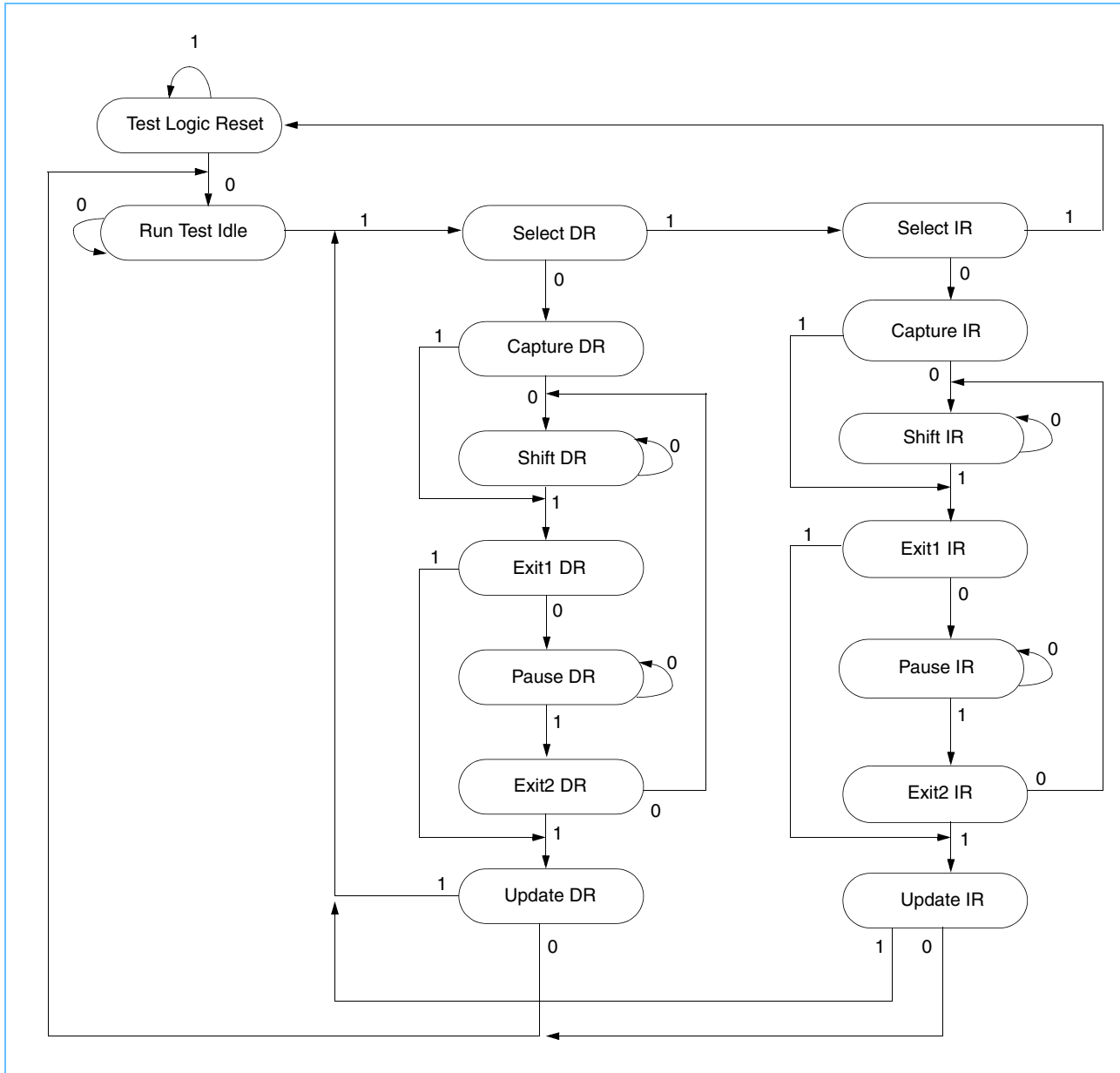


Boundary Scan Order (x18)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	SA1	5R	26	SA	4A
2	SA0	5T	27	SA	4C
3	SA	6R	28	SA	3A
4	SA	7T	29	SA	3B
5	SA	7P	30	SA	3C
6	DQ	8T	31	PH ¹ (16Mb) ²	3D
7	DQ	9P	32	DQ	2B
8	\overline{CQ}	8M	33	DQ	1D
9	DQ	7K	34	CQ	2F
10	DQ	9K	35	DQ	3H
11	MODE ³	6L	36	DQ	1H
12	\overline{CK}	5H	37	ZQ	5A
13	CK	5G	38	B1	5B
14	\overline{G}	5C	39	B2	5K
15	DQ	8H	40	B3	5L
16	DQ	9F	41	\overline{LBO}	4L
17	DQ	7F	42	DQ	2K
18	DQ	8D	43	DQ	1M
19	DQ	9B	44	DQ	3M
20	SA	7D	45	DQ	2P
21	SA	7C	46	DQ	1T
22	SA	7B	47	SA	3P
23	SA	7A	48	SA	3T
24	SA	6C	49	SA	4R
25	SA	6A			

1. PH pins are place holders. BGA bump is a NC (no connect). PH pins are forced to V_{DD}.
2. Reserved address bit for 16Mb density.
3. MODE will scan out value placed on Mode pin or, if Mode pin is floated, Mode will scan V_{SS}.

TAP Controller State Machine





Revision Log

Rev	Contents of Modification
June 7, 2002	Initial release (00).



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Printed in the United States of America June 2002

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June 7, 2002