HD74LV4040A

12-stage Binary Counter

HITACHI

ADE-205-282 (Z)
1st Edition
April 1999

Description

The HD74LV4040A is a 12 stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.3 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)

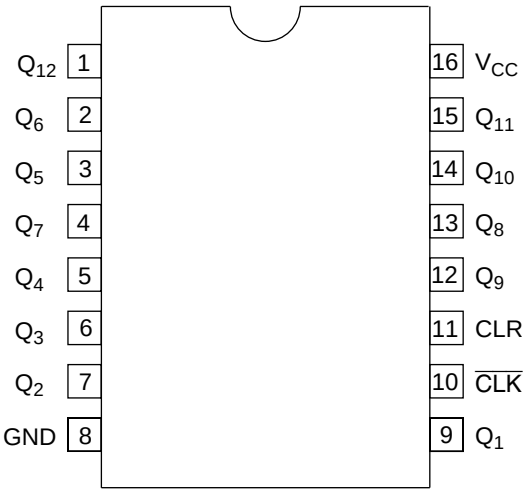
Function Table

Inputs		**Output**
$\overline{\textbf{CLK}}$	**CLR**	$\mathbf{Q_n}$
↑	L	Remains unchanged
↓	L	Changed
X	H	All outputs low

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition

Hitachi semiconductor

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		V_{CC}: OFF
Input clamp current	I_{IK}	–20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air)*[3]	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

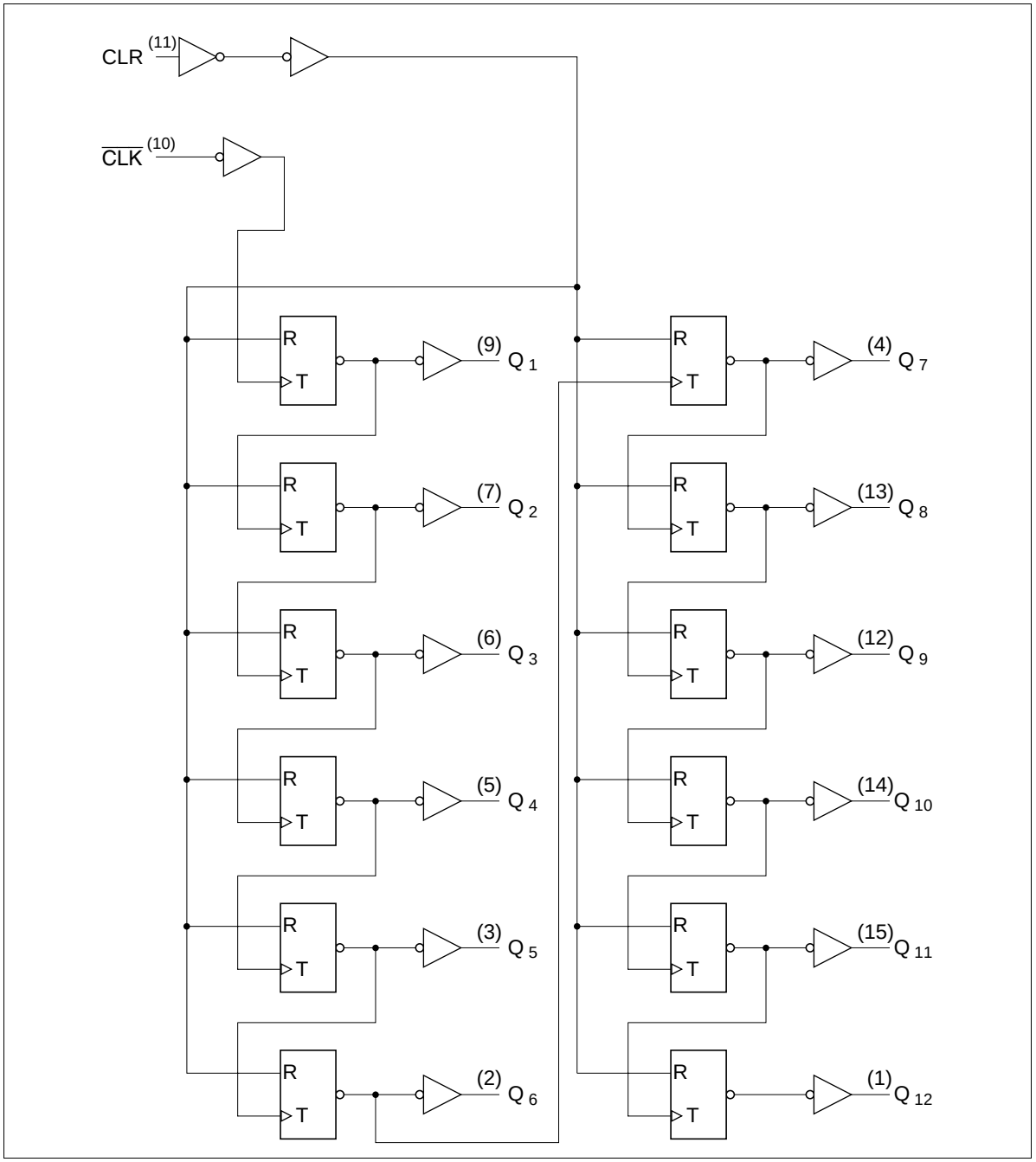
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

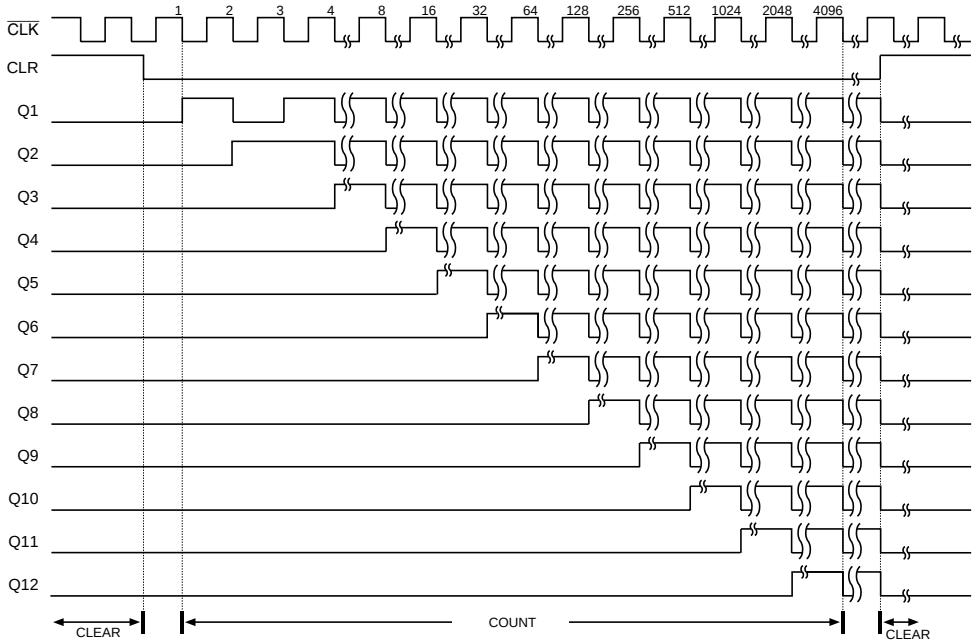
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	–50	µA	V_{CC} = 2.0 V
		—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	–6		V_{CC} = 3.0 to 3.6 V
		—	–12		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	50	µA	V_{CC} = 2.0 V
		—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	6		V_{CC} = 3.0 to 3.6 V
		—	12		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	100		V_{CC} = 3.0 to 3.6 V
		0	20		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

- **Ta = –40 to 85°C**

Item	Symbol	V_{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OH} = –50 µA
		2.3	2.0	—	—		I_{OH} = –2 mA
		3.0	2.48	—	—		I_{OH} = –6 mA
		4.5	3.8	—	—		I_{OH} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 6 mA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	µA	V_{IN} = V_{CC} or GND, I_O = 0
Output leakage current	I_{OFF}	0	—	—	5	µA	V_I or V_O = 0 to 5.5 V
Input capacitance	C_{IN}	3.3	—	3.7	—	pF	V_I = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C Min	Typ	Max	Ta = –40 to 85°C Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Maximum clock frequency	f_{max}	50	90	—	40	—	MHz	C_L = 15 pF		
		30	60	—	25	—		C_L = 50 pF		
Propagation delay time	t_{PLH}/t_{PHL}	—	10.0	16.0	1.0	18.3	ns	C_L = 15 pF	$\overline{CLK}$	Q_1
		—	12.7	19.6	1.0	22.2		C_L = 50 pF		
	t_{PHL}	—	9.9	15.4	1.0	17.5		C_L = 15 pF	CLR	
		—	11.8	18.0	1.0	20.4		C_L = 50 pF		
Propagation delay time skew	Δt_{pd}	—	3.0	5.5	—	6.3	ns	C_L = 50 pF	Q_n	Q_n + 1
Setup time	t_{SU}	7.0	—	—	7.0	—	ns		CLR inactive before $\overline{CLK}$ ↓	
Pulse width	t_w	7.0	—	—	7.0	—	ns		$\overline{CLK}$ high or low	
		7.0	—	—	7.0	—			CLR high	

Switching Characteristics (cont)

- **V_{CC} = 3.3 ± 0.3 V**

		Ta = 25°C			Ta = –40 to 85°C					
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**FROM (Input)**	**TO (Output)**
Maximum	f_{max}	75	140	—	70	—	MHz	C_L = 15 pF		
clock frequency		55	80	—	50	—		C_L = 50 pF		
Propagation	t_{PLH}/t_{PHL}	—	7.5	11.9	1.0	14.0	ns	C_L = 15 pF	$\overline{CLK}$	Q_1
delay time		—	10.0	15.4	1.0	17.5		C_L = 50 pF		
	t_{PHL}	—	8.3	12.8	1.0	15.0		C_L = 15 pF	CLR	
		—	10.8	16.3	1.0	18.5		C_L = 50 pF		
Propagation delay time skew	Δt_{pd}	—	2.4	4.4	—	5.0	ns	C_L = 50 pF	Q_n	Q_n + 1
Setup time	t_{SU}	5.0	—	—	5.0	—	ns		CLR inactive before $\overline{CLK}$ ↓	
Pulse width	t_w	5.0	—	—	5.0	—	ns		$\overline{CLK}$ high or low	
		5.0	—	—	5.0	—			CLR high	

Switching Characteristics (cont)

- **V_{CC} = 5.0 ± 0.5 V**

		Ta = 25°C			Ta = –40 to 85°C					
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**FROM (Input)**	**TO (Output)**
Maximum	f_{max}	150	210	—	125	—	MHz	C_L = 15 pF		
clock frequency		95	125	—	80	—		C_L = 50 pF		
Propagation	t_{PLH}/t_{PHL}	—	4.8	7.3	1.0	8.5	ns	C_L = 15 pF	$\overline{CLK}$	Q_1
delay time		—	6.3	9.3	1.0	10.5		C_L = 50 pF		
	t_{PHL}	—	5.6	8.6	1.0	10.0		C_L = 15 pF	CLR	
		—	7.1	10.6	1.0	12.0		C_L = 50 pF		
Propagation delay time skew	Δt_{pd}	—	1.6	3.1	—	3.5	ns	C_L = 50 pF	Q_n	Q_n + 1
Setup time	t_{SU}	5.0	—	—	5.0	—	ns		CLR inactive before $\overline{CLK}$ ↓	
Pulse width	t_w	5.0	—	—	5.0	—	ns		$\overline{CLK}$ high or low	
		5.0	—	—	5.0	—			CLR high	

Operating Characteristics

- **C_L = 50 pF**

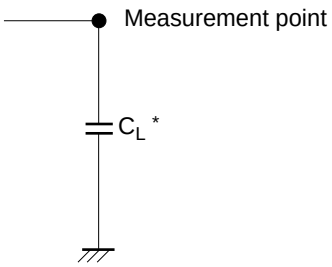
			Ta = 25°C				
Item	**Symbol**	**V_{cc} = (V)**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Power dissipation capacitance	C_{PD}	3.3	—	17.3	—	pF	f = 10 MHz
		5.0	—	19.0	—		

Noise Characteristics

- **C_L = 50 pF**

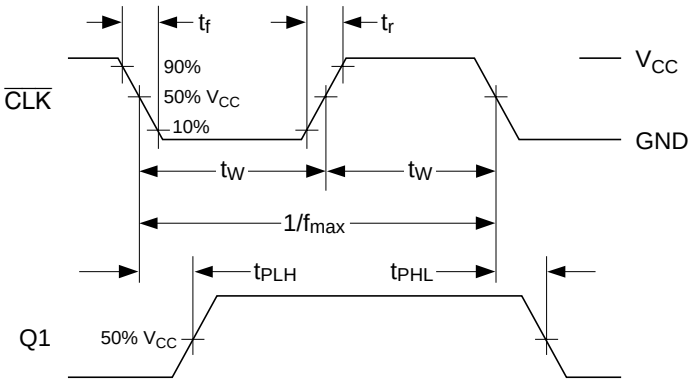
			Ta = 25°C				
Item	**Symbol**	**V_{cc} = (V)**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Quiet output, maximum dynamic V_{OL}	$V_{OL (P)}$	3.3	—	0.4	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL (V)}$	3.3	—	–0.5	-0.8		
Quiet output, minimum dynamic V_{OH}	$V_{OH (V)}$	3.3	—	3.0	—		
High-level dynamic input voltage	$V_{IH (D)}$	3.3	2.31	—	—		
Low-level dynamic input voltage	$V_{IL (D)}$	3.3	—	—	0.99		

Test Circuit

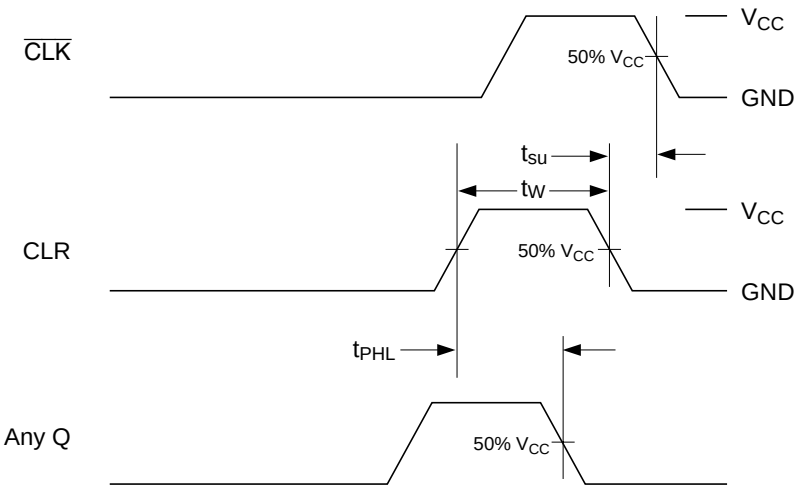


Note: C_L includes the probe and jig capacitance.

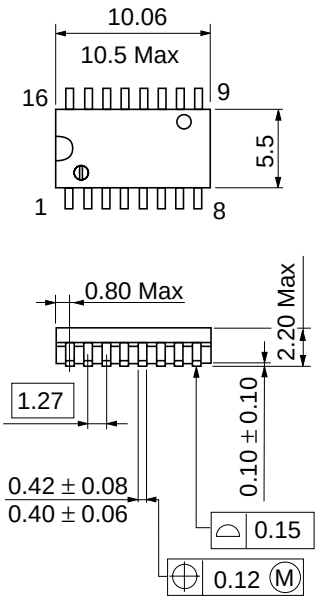
Waveform – 1

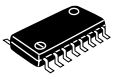


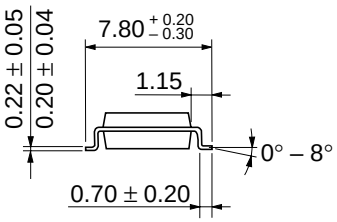
Waveform – 2



Package Dimensions



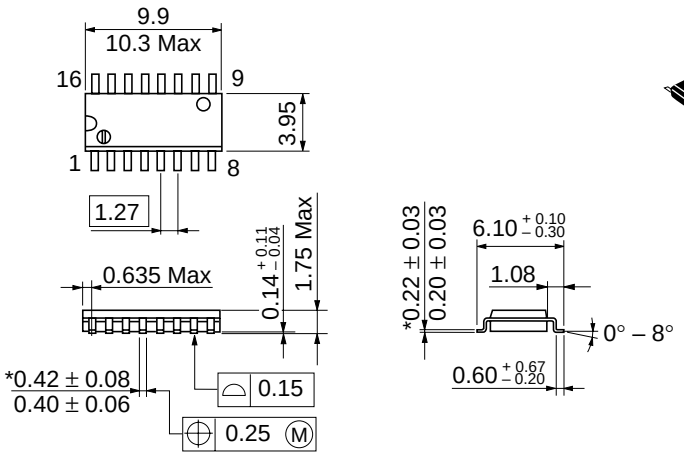




Dimension including the plating thickness
Base material dimension

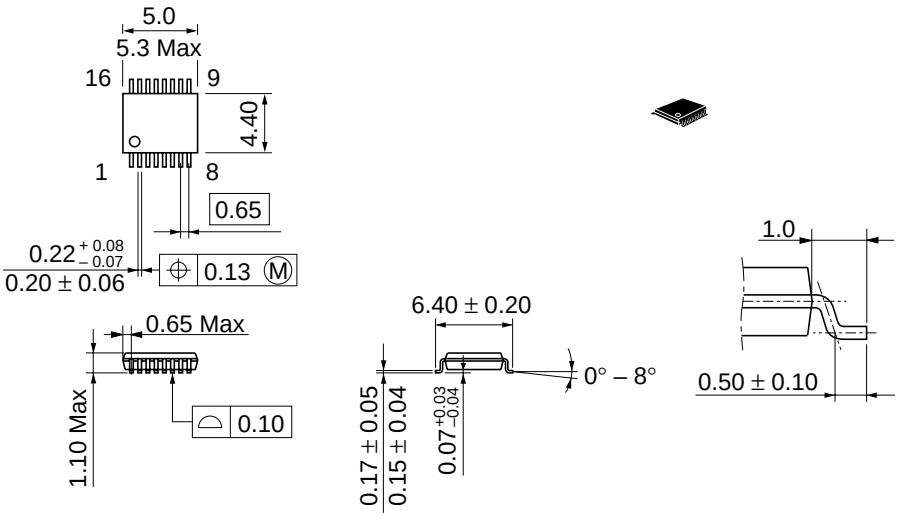
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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