16-bit Address Comparator

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Description

The HD74HC677 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input infomation applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A_1 through A_7 must be low and that inputs A_8 through A_{16} must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The HD74HC677 features an enable input (G). When G is low, the device is enabled. When G is high, the device is disabled and the output is high regardless of the A and P inputs.

Features

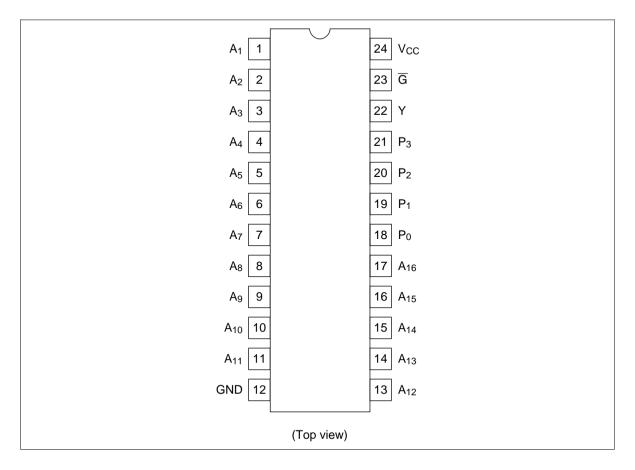
- High Speed Operation: t_{pd} (A to Y) = 17 ns typ ($C_L = 50 \text{ pF}$)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (Ta = 25°C)



Function Table

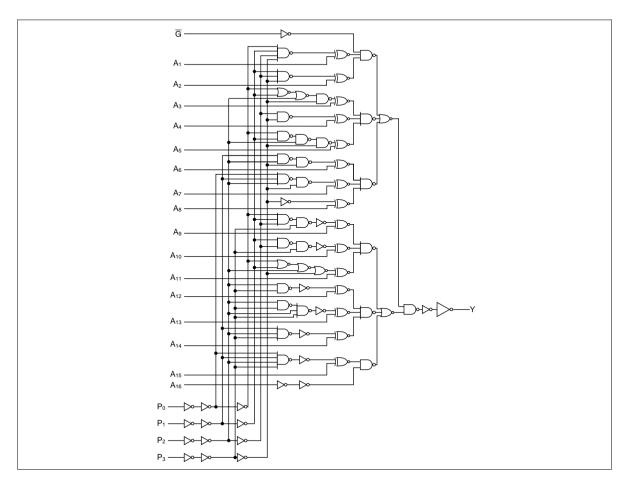
	Inp	uts																			
G	\mathbf{P}_{3}	\mathbf{P}_2	\mathbf{P}_1	\mathbf{P}_{0}	\mathbf{A}_1	\mathbf{A}_{2}	\mathbf{A}_{3}	\mathbf{A}_{4}	A_{5}	A_6	A ₇	\mathbf{A}_{8}	A_9	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄	\mathbf{A}_{15}	\mathbf{A}_{16}	Output Y
L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	L	L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	L	L	Н	L	L	L	Н	Н	Н	Н	н	Н	Н	Н	Н	н	Н	Н	н	Н	L
L	L	L	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	L	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	L	Н	L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	L	Н	Н	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	L	Н	Н	Н	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	L	Н	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	L
L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	L
L	Н	Н	L	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	L
L	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	Н	L
L	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	L
L	All other combinations											Н									
Н	Any combination										Н										

Pin Arrangement



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Logic Diagram



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DC Characteristics

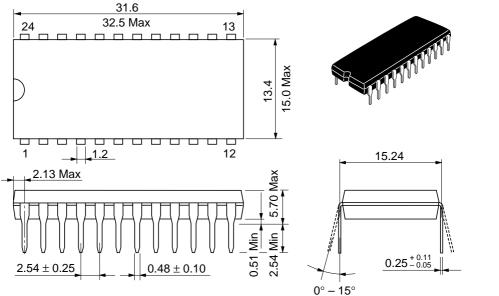
			Ta =	25°C	;	Ta = - +85°C	-40 to			
ltem	Symbol	V_{cc} (V)	Min	Тур	Мах	Min	Max	Unit	Test Condition	ns
Input voltage	V _{IH}	2.0	1.5			1.5	—	V		
		4.5	3.15	—	_	3.15	—	_		
		6.0	4.2		_	4.2	—	_		
	V _{IL}	2.0			0.5	—	0.5	V		
		4.5			1.35	—	1.35	-		
		6.0		_	1.8	_	1.8	-		
Output voltage	V _{OH}	2.0	1.9	2.0	_	1.9	_	V	$Vin = V_{IH} \text{ or } V_{IL}$	I _{OH} = -20 μA
		4.5	4.4	4.5		4.4	_	-		
		6.0	5.9	6.0		5.9	_	-		
		4.5	4.18	_	_	4.13	_	_		I _{он} = -4 mА
		6.0	5.68			5.63	_	-		I _{он} = -5.2 mА
	V _{OL}	2.0		0.0	0.1	—	0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$	I _{oL} = 20 μA
		4.5		0.0	0.1	_	0.1	_		
		6.0		0.0	0.1	—	0.1	-		
		4.5		_	0.26	_	0.33	-		$I_{OL} = 4 \text{ mA}$
		6.0		_	0.26	_	0.33	_		I _{oL} = 5.2 mA
Input current	lin	6.0	_	_	±0.1	_	±1.0	μA	$Vin = V_{cc} \text{ or } GN$	ND
Quiescent supply current	I _{cc}	6.0	—	—	4.0	_	40	μA	Vin = V _{cc} or G	ND, lout = $0 \mu A$

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AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

			Ta =	: 25°C	;	Ta = - +85°C	–40 to C		
Item	Symbol	V_{cc} (V)	Min	Тур	Мах	Min	Мах	Unit	Test Conditions
Propagation delay	t _{PLH}	2.0	—	—	310	_	390	ns	P to Y
time	t _{PHL}	4.5	—	23	62	_	78	_	
		6.0	_		52	_	66	_	
	t _{PLH}	2.0	_	_	180	_	225	ns	A to Y
	t _{PHL}	4.5	_	17	36	_	45	_	
		6.0	_	_	31	_	38	_	
	t _{PLH}	2.0	_	_	125	_	155	ns	G to Y
	t _{PHL}	4.5	_	13	25	_	31	_	
		6.0	_	_	21	_	26	-	
Output rise/fall	t _{TLH}	2.0	_	_	75	_	95	ns	
time	t _{THL}	4.5	_	5	15	_	19	_	
		6.0	_	—	13	_	16	-	
Input capacitance	Cin	_	_	5	10	_	10	pF	

Unit: mm



Hi	itachi Code	DP-24
JE	EDEC	Conforms
EI	AJ	Conforms
W	eight (reference value)	3.1 g

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