HD14024B

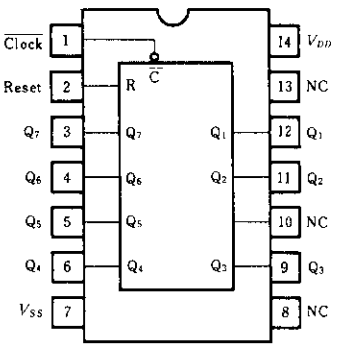
Seven Stage Ripple Counter

The HD14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of V_{DD}), however the Clock input has increased noise immunity due to Hysteresis, with no maximum Clock input rise or fall time. The Output of each counter stage is buffered.

■ FEATURES

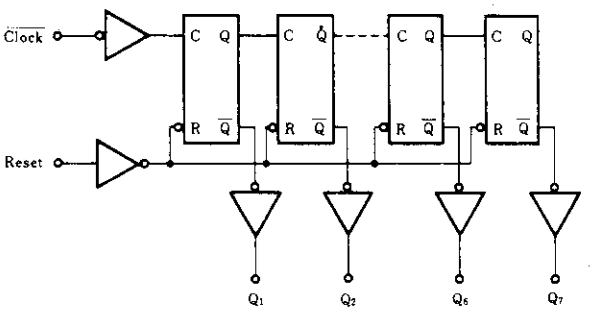
- Quiescent Current = 5nA/pkg typ. @5V
- 8-MHz Operation @10V typ.
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B and MC14024B

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM

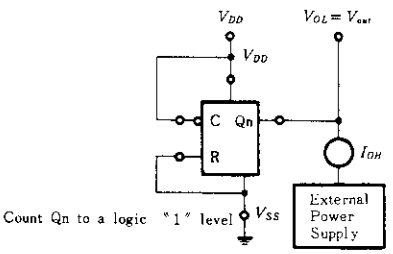


■ TRUTH TABLE

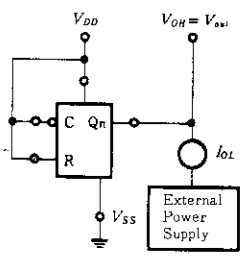
Clock	Reset	Outputs State
L	L	No Change
L	H	All Outputs are low
H	L	No Change
H	H	All Outputs are low
⌐	L	No Change
⌐	H	All Outputs are low
⌐	L	Advance to next state
⌐	H	All Outputs are low

■ DC CHARACTERISTIC TEST CIRCUIT

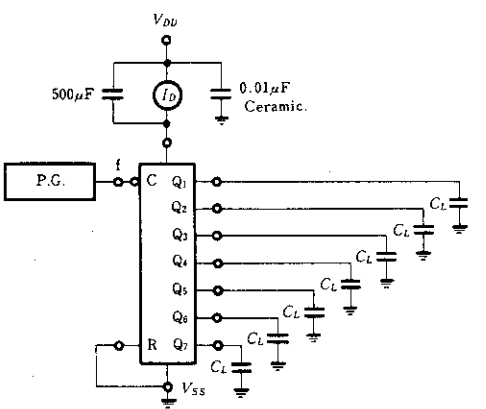
● I_{OH}



● I_{OL}



■ POWER DISSIPATION TEST CIRCUIT



■ ELECTRICAL CHARACTERISTICS

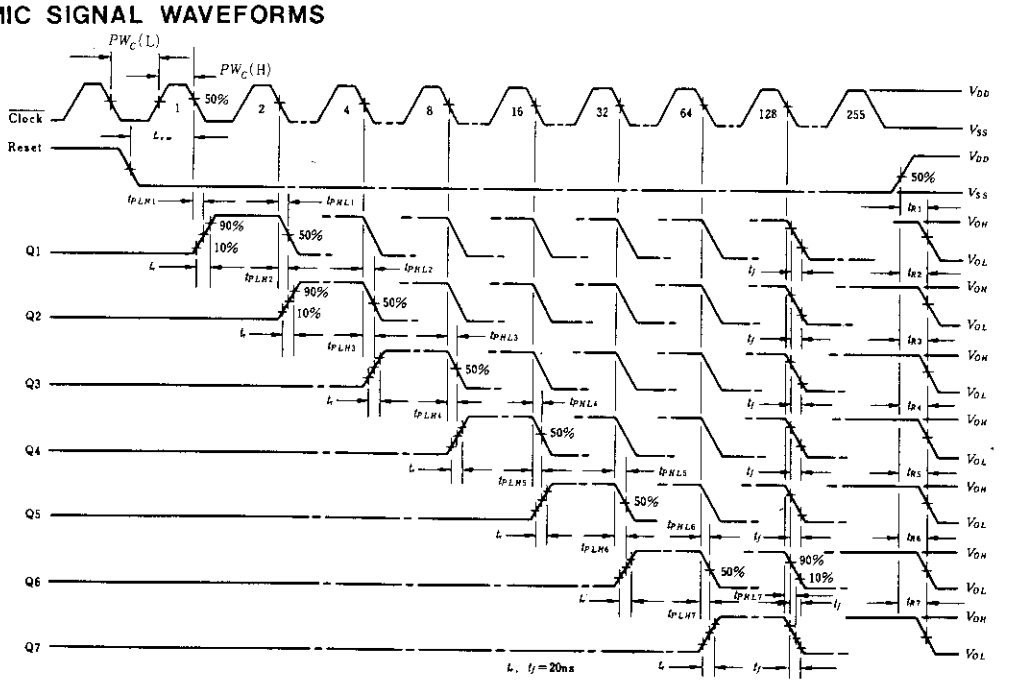
Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40°C min	−40°C max	25°C min	25°C typ	25°C max	85°C min	85°C max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5$V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	$V_{OH}=4.6$V	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	$V_{OH}=9.5$V	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	$V_{OH}=13.5$V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4$V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5$V	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5$V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}		$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic+I_{DD}, Per Gate $C_L=50$pF, $f=1$ kHz	—	—	—	0.31	—	—	—	μA
		10		—	—	—	0.60	—	—	—	
		15		—	—	—	0.89	—	—	—	

* To calculate total supply current at frequency other than 1kHz.
@ $V_{DD}=5.0$V $I_T=(0.31\mu A/kHz)f+I_{DD}$, @ $V_{DD}=10$V $I_T=(0.60\mu A/kHz)f+I_{DD}$, @ $V_{DD}=15$V $I_T=(0.89\mu A/kHz)f+I_{DD}$

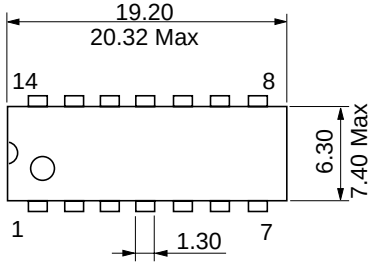
■ SWITCHING CHARACTERISTICS (C_L=50pF, Ta=25°C)

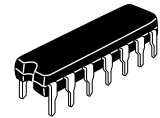
Characteristic		Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	100	250	ns
			10	—	50	150	
			15	—	37	100	
Propagation Delay Time	Clock to Q_1	t_{PLH}, t_{PHL}	5.0	—	380	600	ns
			10	—	150	230	
			15	—	110	175	
	Clock to Q_7		5.0	—	1,000	3,000	
			10	—	400	750	
			15	—	300	565	
	Reset to Q_n		5.0	—	500	800	
			10	—	250	400	
			15	—	180	300	
Clock Pulse Width		PW_C	5.0	500	200	—	ns
			10	165	60	—	
			15	125	40	—	
Reset Pulse Width		PW_R	5.0	600	375	—	ns
			10	350	200	—	
			15	260	150	—	
Reset Removal Time		t_{rem}	5.0	625	250	—	ns
			10	190	75	—	
			15	145	50	—	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	No Limit			
			10				
			15				
Clock Frequency		f_{max}	5.0	—	2.5	1.0	MHz
			10	—	8.0	3.0	
			15	—	12	4.0	

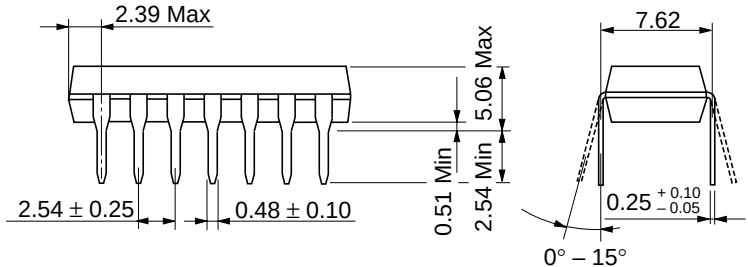
■ DYNAMIC SIGNAL WAVEFORMS



Unit: mm







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Weight (reference value)	0.97 g

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