*Multi*GEN™ GF9102A
Decimating/Interpolating Digital Filter

DATA SHEET

FEATURES

- **improved performance over TMC2242 in applications not requiring 1:1 low pass filtering**
- **low power (60mA typical at *f* = 20MHz)**
- **40 MHz maximum clock rate**
- **single device exceeds CCIR 601 lowpass filter requirements**
- **true unity gain (0.0 dB) at DC**
- **reduced output ringing with constant input in interpolation mode**
- **built-in TRS code protection**
- **12 bit inputs and 16 bit outputs in 2's complement signed or unsigned formats**
- **user-selectable 8 to 16 bit output rounding**
- **can also be operated as a 9 or 21 tap chroma bandpass filter under user control**
- **single +5 V power supply**
- **three state outputs**

APPLICATIONS

- CCIR 601-compliant oversampling video A/D and D/A conversion
- 2:1 interpolation and decimation
- 4:2:2 to 4:4:4 format conversion
- Chroma bandpass filtering

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GF9102ACPM	44 Pin PLCC	0° to 70° C
GF9102ACTM	44 Pin PLCC Tape	0° to 70° C

DEVICE DESCRIPTION

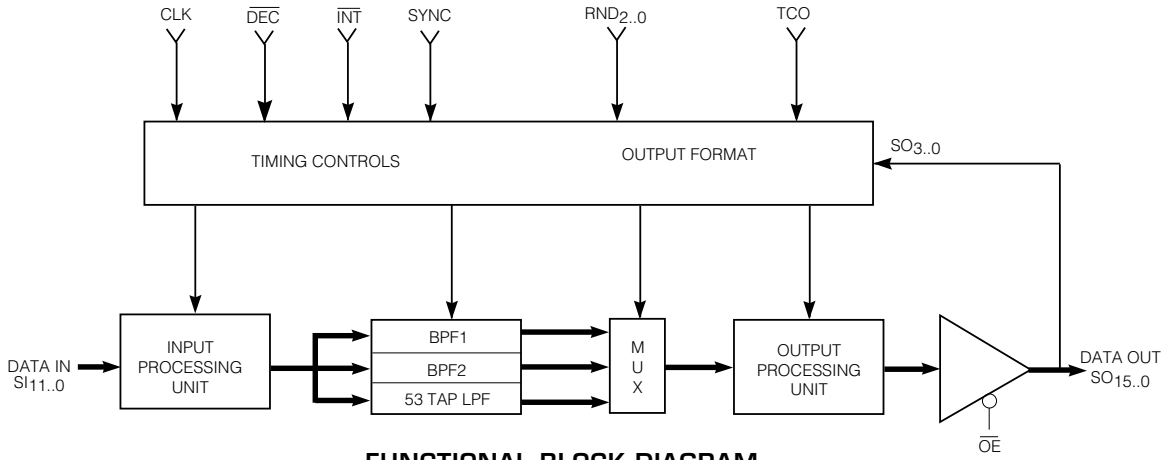
The GF9102A is a linear phase FIR digital filter that is usable in a variety of video signal processing applications. The device contains three separate fixed coefficient filters and can be operated in three basic modes: 53 tap low pass filter, 9 tap chroma bandpass filter or 21 tap chroma bandpass filter.

In the 53 tap low pass filter mode, the GF9102A can replace the TMC2242 in all applications, except those requiring 1:1 low pass filtering, for improved performance and full CCIR 601 compatibility. Specific improvements include true unity gain at DC, 12.4 dB attenuation at fs/4 with a single device, reduced output ringing with constant input in interpolate mode, support for signed and unsigned data formats, rounding to 10 and 8 bit CCIR 601 data formats, masking of serial digital TRS codes in the data stream, and elimination of the non-saturated-type overflow condition. The device can be operated in both TMC2242 compatible modes and in GF9102A enhanced modes.

When used as a decimating post-filter with a double speed oversampling analog-digital converter, the device greatly reduces the cost and complexity of the associated analog anti-aliasing pre-filter. In a similar fashion, when used as an interpolating pre-filter with a double speed oversampling digital-analog converter, the GF9102A simplifies the analog reconstruction post-filter. The GF9102A also exceeds the requirements for conversion between 4:2:2 and 4:4:4 signal formats.

For chroma filtering applications, the GF9102A can be operated as a 9 or 21 tap bandpass filter by selecting the appropriate operating mode.

The GF9102A is packaged in a 44 pin PLCC and is pin compatible with the TMC2242. The device operates with a single +5 V supply.



FUNCTIONAL BLOCK DIAGRAM

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PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	DESCRIPTION
CLK	42	I	System Clock. TTL input. All timing specifications are referenced to the rising edge of clock.
SYNC	43	I	Data Synchronization. TTL input with internal pull-up. This input is used to synchronize the incoming data with the GF9102A by holding SYNC high on clock N and low on clock N+1 when the first data word is presented to the input $SI_{11..0}$. SYNC may be held low until resynchronization is desired, or it may be clocked at half the clock rate.
$SI_{11..0}$	40, 37, 36, 35, 34, 33, 32, 31, 30, 27, 26, 25	I	Input Data Port. TTL inputs with internal pull-downs. Data is presented to this registered 12-bit data input port. This port can be programmed as two's complement signed or unsigned binary format. See the following section on input data format. Data is latched internally on every clock in decimate mode, and on every other clock in interpolate mode. SI_{11} is the MSB.
TCO	2	I	Two's Complement Output Format Control. TTL input with internal pull-down. When TCO is high, output data is presented in two's complement format. When TCO is low, the output is inverted offset binary, obtained by inverting bits SO_{14} through SO_0, leaving SO_{15} unchanged.
$\overline{INT}$	44	I	Interpolate. Active low TTL input with internal pull-up. When the interpolate control is low, data is input at full clock speed and the chip inserts zeros between samples, padding the input to match the output rate. The GF9102A then interpolates between these alternate input data points to achieve full output data rate.
$\overline{DEC}$	1	I	Decimate. Active low TTL input with internal pull-down. When the decimate control is low, the output register is driven at half system clock speed, decimating the output data stream. When $\overline{DEC}$ and $\overline{INT}$ are low, the GF9102A will be programmed as a 21 tap or 9 tap bandpass filter depending on the state of the SYNC input. See Operation Mode Control below for more detail.
$RND_{2..0}$	22, 23, 24	I	Output Rounding Control. TTL inputs with internal pull-down. These pins set the position of the effective least significant bit of the output port by adding a rounding bit to the next lower internal bit and zeroing all outputs below the rounding bit. Additional rounding functions are added with the SO_1 control input. See Table 6.
$SO_{15..0}$	4, 5, 6, 7, 8, 9, 10, 11, 14, 15, 16, 17, 18, 19, 20, 21	O	Output Data Port. TTL outputs ($SO_{3..0}$ are bi-directional pins with an internal pull-down). The filtered result is available at this registered 16-bit output port, half LSB rounded as determined by the rounding control word $RND_{2..0}$. SO_{15} is the MSB. The $SO_{3..0}$ control inputs enable additional formatting and rounding features as described below.
$SO_{3..0}$	18, 19, 20, 21	I/O	Output Data Port. TTL bi-directional pins with internal pull-down. The SO_0 control input enables the unsigned input and output format. The SO_1 control input enables 8-bit rounding or CCIR 601 8-bit and 10-bit modes of operation. $SO_{3..2}$ are reserved for future functions.
$\overline{OE}$	3	I	Output Enable. Active low TTL input with internal pull-up. When this asynchronous input is high, the output data port is in the high impedance state.
VDD	13, 29, 38		+5 V ± 5% power supply.
GND	12, 28, 39, 41		Ground

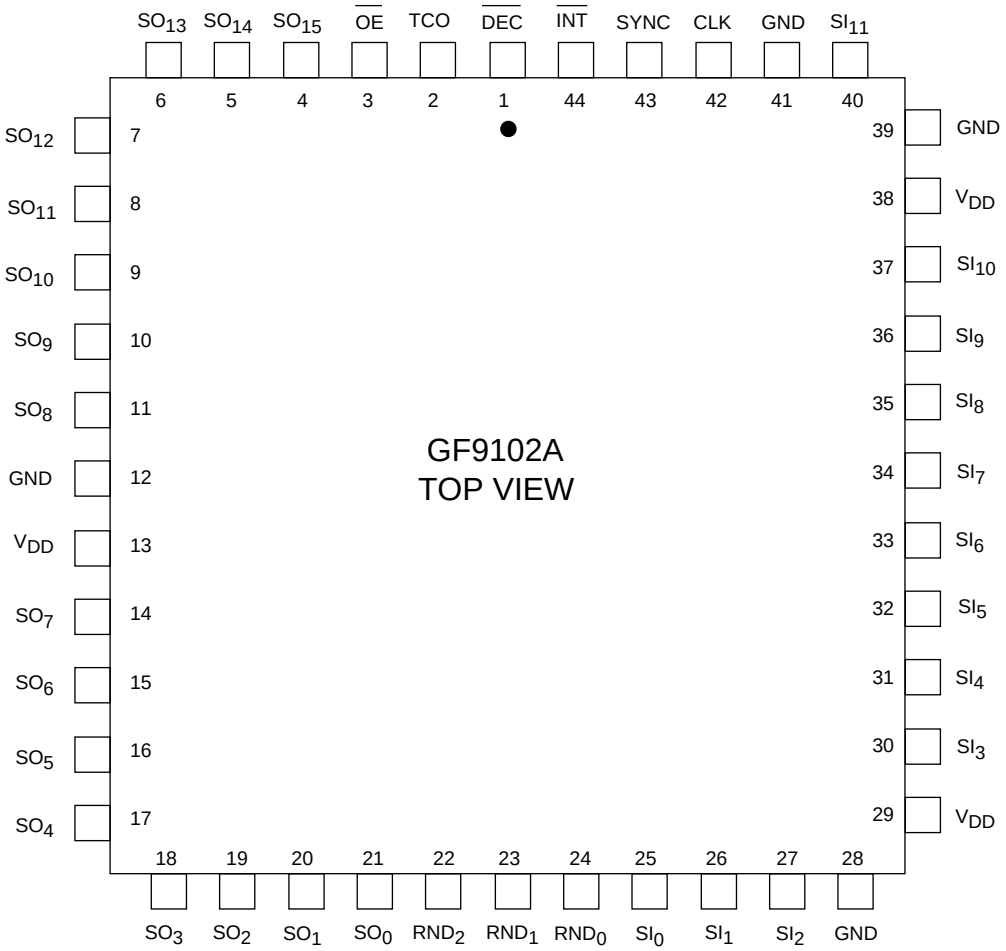

Fig. 1 GF9102A Pin Connections

LOWPASS FILTER CHARACTERISTICS at SAMPLING FREQUENCY OF 27MHz

PARAMETER	VALUE
Filter Order	53
Pass Band Ripple	< ± 0.02 dB
Pass Band Edge	5.75 MHz
DC Gain	0.00 dB
6.75 MHz ($fs/4$) Attenuation	12.4 dB
Minimum Stop Band Attenuation	>58 dB
Stop Band Edge	7.4 MHz

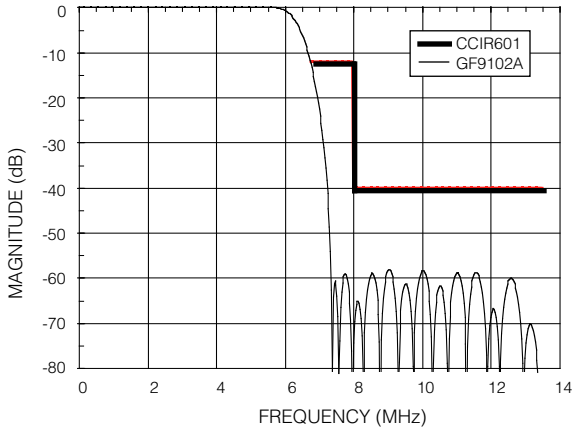

Fig. 2 Frequency Response of the Decimation/Interpolation Filter (Sampling at 27 MHz)

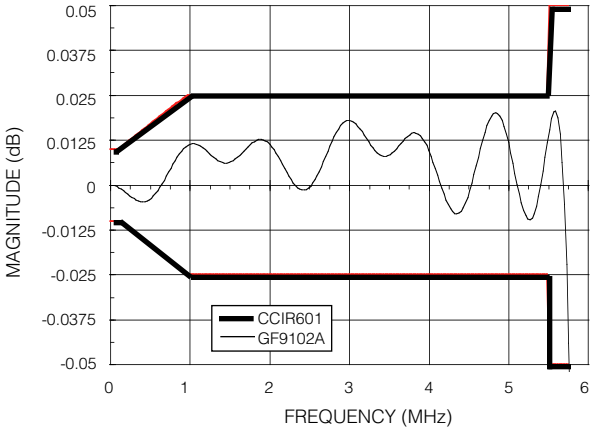

Fig. 3 Frequency Response of the Decimation/Interpolation Filter Passband (Sampling at 27 MHz)

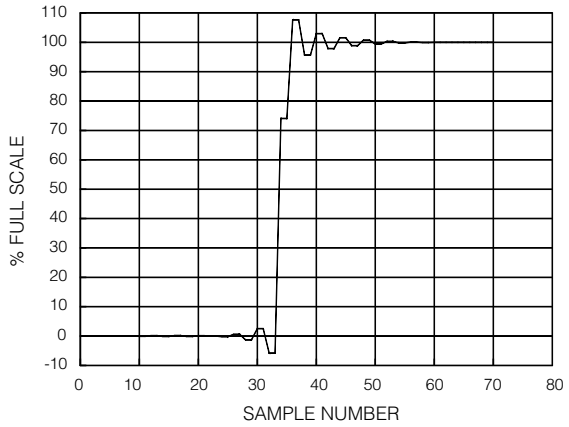

Fig. 4 Step Response of Decimation Filter

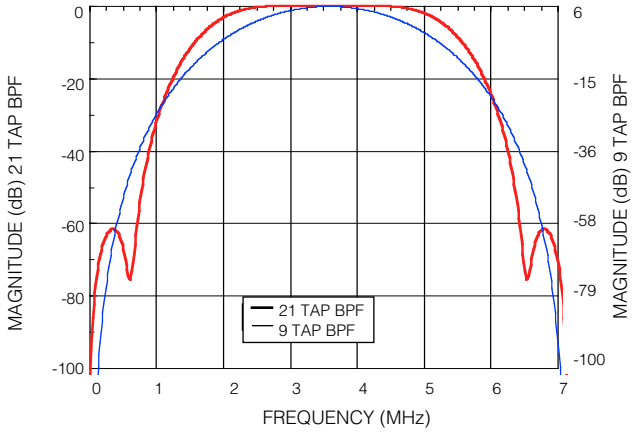

Fig. 5 Frequency Response of the Bandpass Filter (Sampling at 14.31818 MHz)

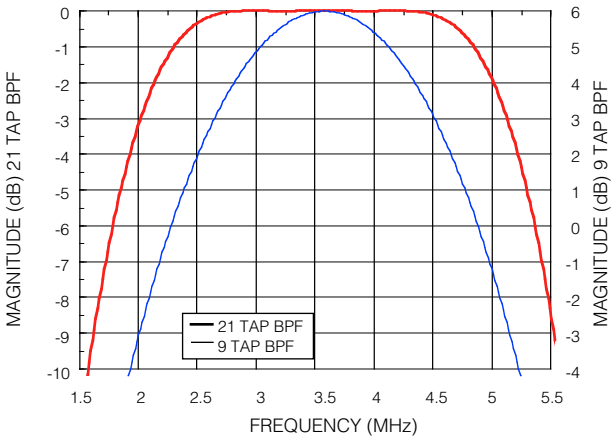

Fig. 6 Frequency Response of the Bandpass Filter Transition Band (Sampling at 14.31818 MHz)

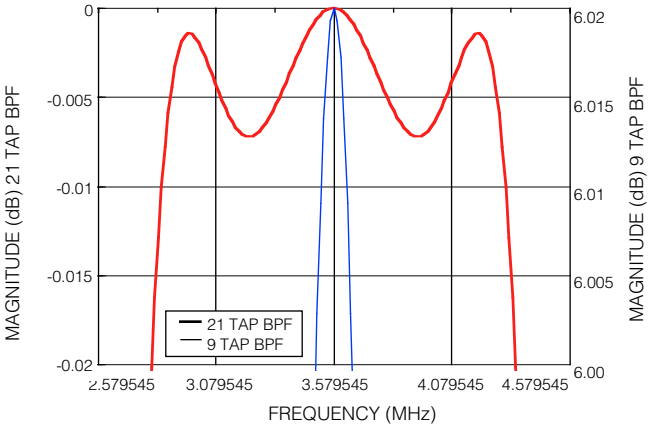

Fig. 7 Frequency Response of the Bandpass Filter Passband (Sampling at 14.31818 MHz)

Table 1: Input Data Format and Bit Weighting

Two's complement signed binary, data range: $-1 \le SI < 1$

SI_{11}	SI_{10}	SI_9	SI_8	SI_7	SI_6	SI_5	SI_4	SI_3	SI_2	SI_1	SI_0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}

Unsigned binary, data range: $0 \le SI < 256$

SI_{11}	SI_{10}	SI_9	SI_8	SI_7	SI_6	SI_5	SI_4	SI_3	SI_2	SI_1	SI_0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}

Table 2: Output Data Format and Bit Weighting

Two's complement signed binary, data range: $-1 \le SO < 1$

SO_{15}	SO_{14}	SO_{13}	SO_{12}	SO_{11}	SO_{10}	SO_9	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1	SO_0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Unsigned binary, data range: $0 \le SO < 256$

SO_{15}	SO_{14}	SO_{13}	SO_{12}	SO_{11}	SO_{10}	SO_9	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1	SO_0
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

Table 3: Operation Mode Control

$\overline{DEC}$	$\overline{INT}$	Sync	Mode	Description	Device Latency	Notes
0	0	0	Bandpass1	21 Tap Bandpass	18 Clock Cycles	2
0	0	1	Bandpass2	9 Tap Bandpass Gain=2	18 Clock Cycles	2
0	1	Sync	Decimating	Gain=1	33 Clock Cycles	1
1	0	Sync	Interpolating	Gain=0.5	33 Clock Cycles	1
1	0	Sync	Interpolating	Gain=1 for unsigned input[3]	33 Clock Cycles	2
1	1	Sync	Pass through	Top 12 bit pass through	33 Clock Cycles	2

Notes: 1. This operating mode is compatible with TMC2242.
2. This is an enhanced operating mode of the GF9102A.
3. This mode is invoked using the SO_0 pin. See I/O Format control below.

Table 4: **I/**O Format Control

$RND_{2..0}$	SO_0[3]	TCO	Input[5]	Output[5]	Notes
RND = 000	Output	0	Signed	I_Unsigned	1
		1	Signed	Signed	
RND ≠ 000	0	0	Signed	I_Unsigned	1
		1	Signed	Signed	
RND ≠ 000	1	0	Unsigned[4]	Unsigned	2
		1	Unsigned	Signed	Limit output up to 15 bits

Notes:
1. This operating mode is compatible with TMC2242.
2. This is an enhanced operating mode of the GF9102A.
3. SO_0, the LSB of the output is a bi-directional pad with a large pull-down resistor. This pin does not have to be connected. When this pin is not connected the GF9102A defaults to a mode compatible with the TMC2242.
4. Application notes for the TMC2242 suggest grounding the MSB of the input if the input data is unsigned as in most A/D converters. This method limits the input to 11 bits and leads to potential output non-saturated type overflow since the MSB of the output is ignored.
5. Signed: two's complement binary data.
   I_unsigned: invert all bits in signed data except for the MSB; also called inverted offset binary.
   Unsigned: invert MSB of signed data; also called offset binary.

Table 5: Output Rounding Control

$RND_{2..0}$	SO_1[3]	No. of Output Bits	Description	Notes
000	Output	16	Rounding to 16 bit	1
001	Output	15	Rounding to 15 bit	1
010	0	14	Rounding to 14 bit	1
011	0	13	Rounding to 13 bit	1
100	0	12	Rounding to 12 bit	1
101	0	11	Rounding to 11 bit	1
110	0	10	Rounding to 10 bit	1
111	0	9	Rounding to 9 bit	1
100	1	8	Rounding to 8 bit	2
110	1	10	CCIR 601 10 bit data format[4]	2
101	1	8	CCIR 601 8 bit data format[5]	2

Notes: 1. This operating mode is compatible with TMC2242.

2. This is an enhanced operating mode of the GF9102A.

3. SO_1, the second LSB of the output is a bi-directional pad with a large pull-down resistor. This pin does not have to be connected. When this pin is not connected the GF9102A defaults to a mode compatible with the TMC2242.

4. CCIR 601 10 bit data format range from Hex 004 to 3FB.

. 5. CCIR 601 8 bit data format range from Hex 01 to FE.

Table 6: Extra Control Input Pins using the Four Least Significant Bi-directional Output Pads $SO_{3..0}$

Conditions to allow Control Inputs	Output Pad[1]	Function	Notes
RND ≠ 000	$SO_0 = 1$	Unsigned input	2
RND = 100	$SO_1 = 1$	8 bit output rounding	2
RND = 110	$SO_1 = 1$	CCIR 601 10 bit data format	2
RND = 101	$SO_1 = 1$	CCIR 601 8 bit data format	2
RND = 1XX	SO_2	Reserved	
RND = 1XX	SO_3	Reserved	

Notes: 1. $SO_{3..0}$ pins are bi-directional with a large pull-down resistor. These pins do not have to be connected. When these pins are not connected the GF9102A defaults to a mode compatible with the TMC2242.

2. This is an enhanced operating mode of the GF9102A.

Table 7: Input Step Response

INPUT	OUTPUT				
	DECIMATION		INTERPOLATION		
	$\overline{INT}$ = 1, $\overline{DEC}$ = 0	SYNC	$\overline{INT}$ = 0, $\overline{DEC}$ = 1	SYNC	
XXX	XXX	1	XXX	1	
400	XX	0	XX	0	
400	XX	0	XX	0	
•	•	•	•	•	
55 cycles •	•	•	•	•	
•	•	•	•	•	
400	4000	0	2000	0	
400	4000	0	2000	0	
000	4000	0	2000	0	
•	•	•	•	•	
•	•	•	•	•	
•	•	•	•	•	
000	44E2	0	244A	0	Maximum Ringing
000	44E2	0	1F6A	0	
000	2F6A	0	1000	0	
000	2F6A	0	0096	0	
000	FC4C	0	FBB6	0	Minimum Ringing
000	FC4C	0	FF68	0	
•	•	•	•	•	
•	•	•	•	•	
•	•	•	•	•	
000	0000	0	0000	0	Steady State

NOTE: TCO = 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.3 to +7.0V
Input Voltage Range	0.5 to (VDD + 0.5)V
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec)	260°C

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

ELECTRICAL CHARACTERISTICS

Conditions: V_{DD} = 5 V, T_A = 0° to 70°C, R_L = 150 Ω to GND and 144 Ω AC coupled unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.75	5	5.25	volts
Supply Current Quiescent	I_{DDQ}	V_{DD} = Max, V_{IN} = 0V	-	5	10	mA
Supply Current Unloaded	I_{DDU}	V_{DD} = Max, $\overline{OE}$ = V_{DD} , f = 20 MHz	-	60[1]	95	mA
Input Voltage, Logic Low	V_{IL}		-	-	0.8	volts
Input Voltage, Logic High	V_{IH}		2.0	-	-	volts
Switching Threshold	V_T	TTL	-	1.5	-	volts
Input Current: (TTL Inputs)	I_{IN}	V_{IN} = $V_{DD\ OR}$ V_{SS}	-10	±1	10	µA
Inputs with Pulldown Resistors		V_{IN} = V_{DD}	35	115	222	µA
Inputs with Pullup Resistors		V_{IN} = V_{SS}	-35	-115	-214	µA
Ouput Voltage, Logic Low	V_{OL}	V_{DD} = Min, I_{OL} = 6mA	-	0.2	0.4	volts
Ouput Voltage, Logic High	V_{OH}	V_{DD} = Min, I_{OH} = -6mA	2.4	4.5	-	volts
Hi-Z Output Leakage Current	I_{OZ}	V_{DD} = Max, $\overline{OE}$ = 1	-10	±1	10	µA
Short Circuit Output Current	I_{OS}	V_{DD} = Max, output high one pin to ground, one second duration max	-	-	210	mA
Input Capacitance	C_{IN}	T_A = 25°C, f = 1MHz	-	-	10	pF
Output Capacitance	C_{OUT}	T_A = 25°C, f = 1MHz	-	-	10	pF
Ambient Temperature, Still Air	T_A		0	-	70	°C

NOTE 1: Supply current may fluctuate with changes in data pattern.

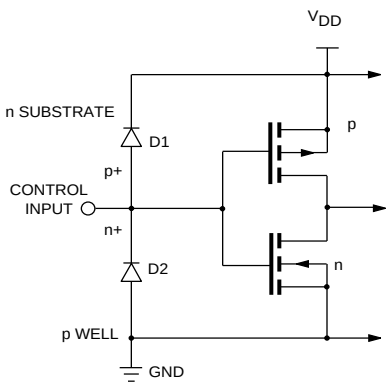

Fig. 8a Equivalent Input Circuit

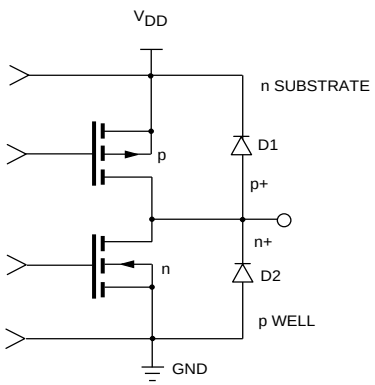

Fig. 8b Equivalent Output Circuit

SWITCHING CHARACTERISTICS, T_A from 0°C to 70°C unless otherwise specified.

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_D	Output delay	V_{DD}=Min, C_L=25 pF	-	-	15	ns
t_{OH}	Output hold	V_{DD}=Max, C_L=25 pF	3	-	-	ns
t_{EN}	Output enable	V_{DD}=Min, C_L=25 pF	-	-	15	ns
t_{DIS}	Output disable	V_{DD}=Min, C_L=25 pF	-	-	15	ns
t_{CY}	Cycle time		25	-	-	ns
t_{PWL}	Clock pulse width low		10	-	-	ns
t_{PWH}	Clock pulse width high		10	-	-	ns
t_S	Input setup time		6	-	-	ns
t_H	Input hold time		0	-	-	ns

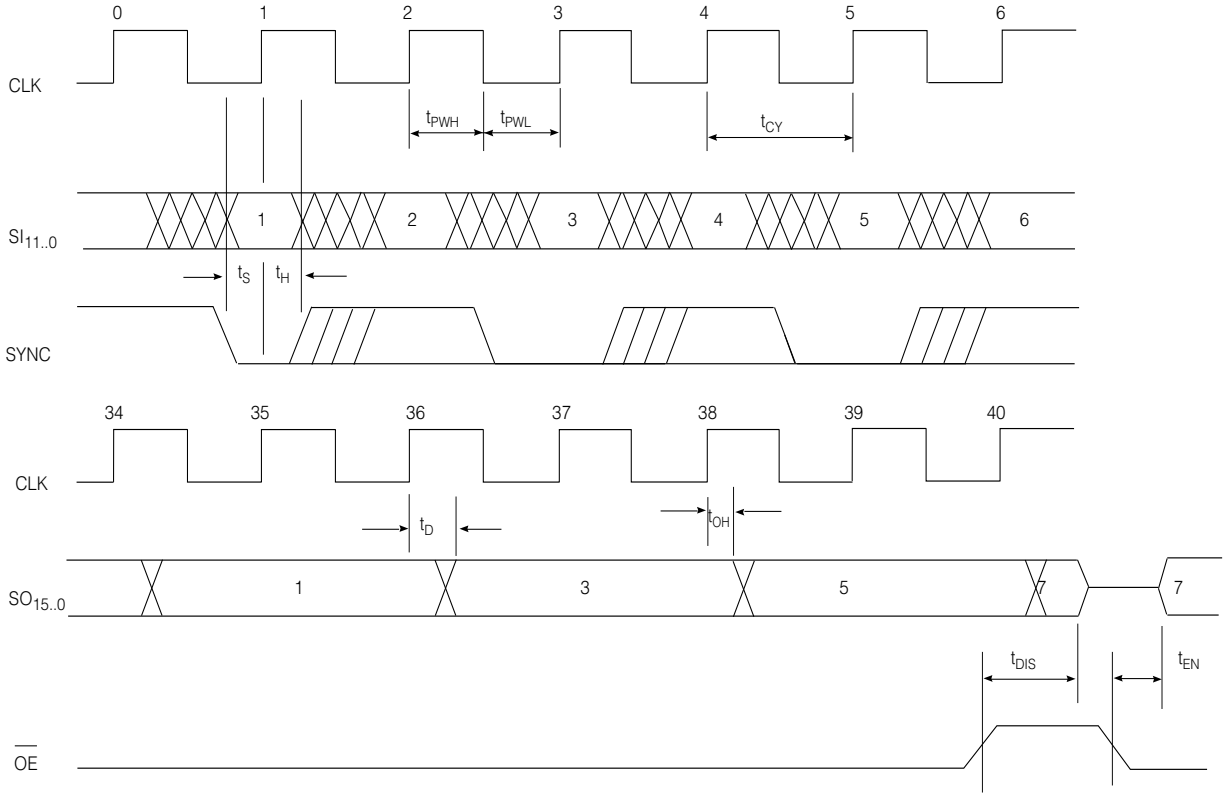

Fig. 9 Timing Diagram - Decimation $\overline{INT}$ = 1, $\overline{DEC}$ = 0, SYNC = SYNC

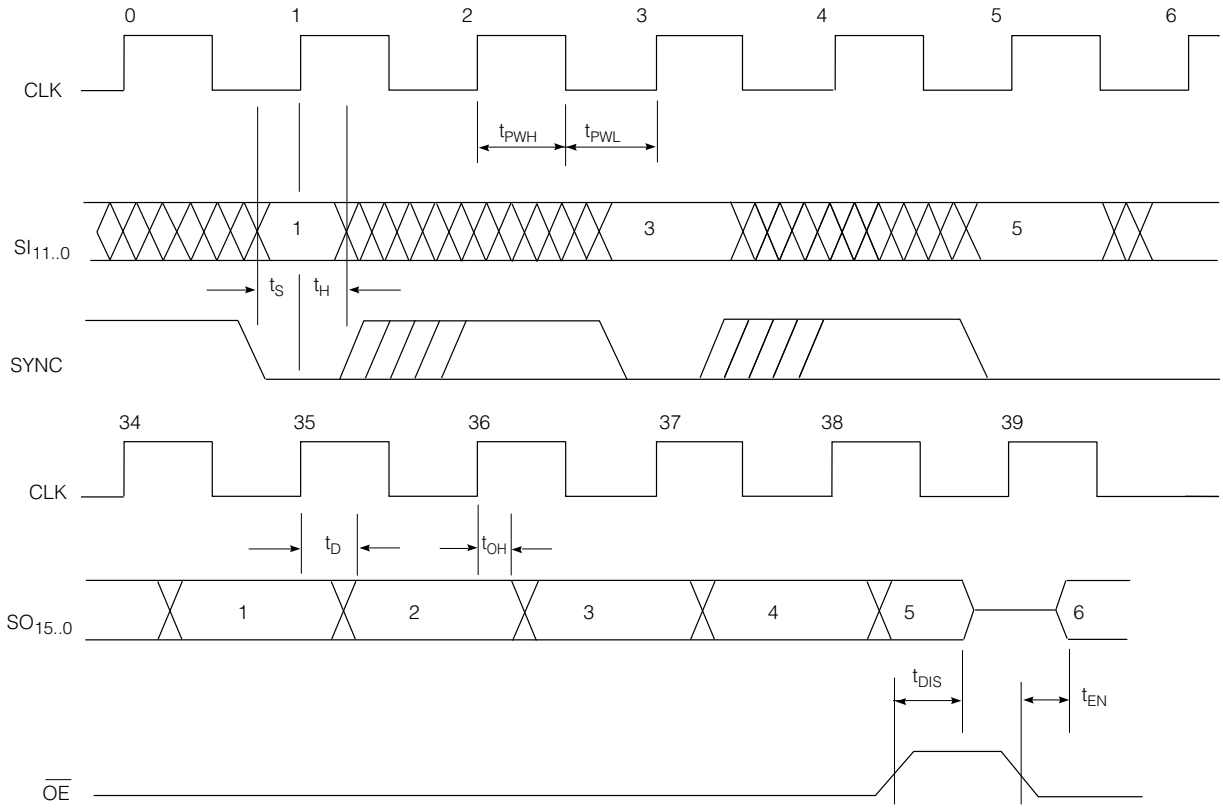

Fig. 10 Timing Diagram - Interpolation $\overline{INT}$ = 0, $\overline{DEC}$ = 1, SYNC = SYNC

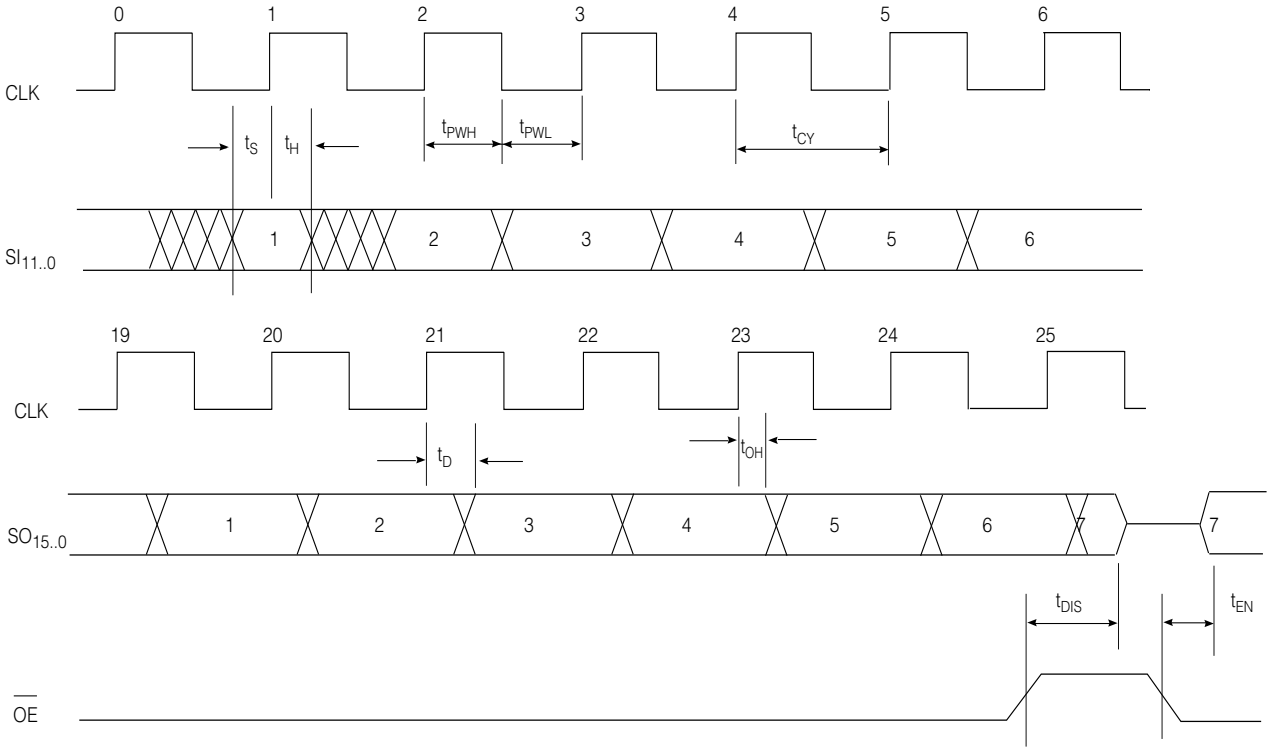

Fig. 11 Timing Diagram - Decimation $\overline{INT}$ = 0, $\overline{DEC}$ = 0, SYNC = 0 or SYNC = 1

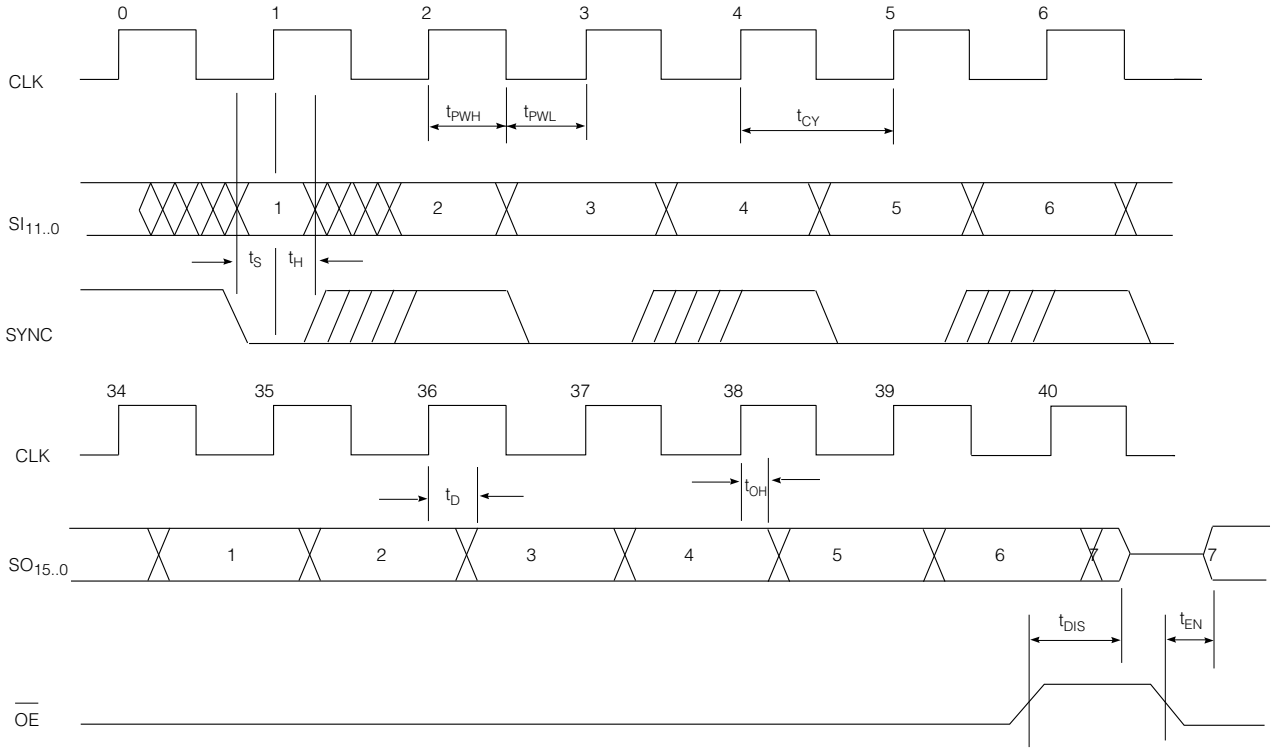

Fig. 12 Timing Diagram - Decimation $\overline{INT}$ = 1, $\overline{DEC}$ = 1, SYNC = SYNC

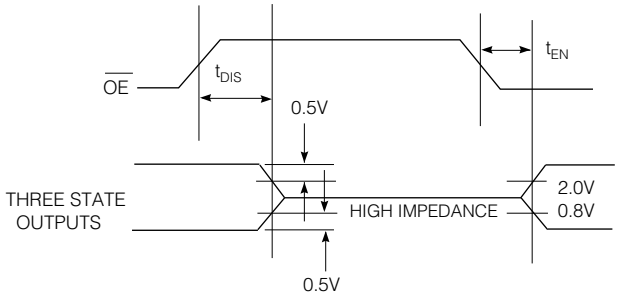

Fig. 13 Threshold Levels for Three State Measurement