FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16312-1E

32-bit Proprietary Microcontrollers

CMOS

FR30 Family MB91151A Series

MB91151A

■ DESCRIPTION

The MB91151A is a single-chip microcontroller using a 32-bit RISC-CPU (FR30 family) as its core.

■ FEATURES

CPU

- 32-bit RISC (FR30) , load/store architecture, 5-stage pipeline
- General-purpose registers : 32 bits × 16
- 16-bit fixed-length instructions (basic instructions) , 1 instruction/ 1 cycle
- Memory-to-memory transfer, bit processing, barrel shift processing : Optimized for embedded applications
- Function entrance/exit instructions, and multiple load/store instructions of register contents, instruction systems supporting high level languages
- Register interlock functions, efficient assembly language description
- Branch instructions with delay slots : Reduced overhead time in branching executions
- Internal multiplier/supported at instruction level
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupt (PC and PS saving) : 6 cycles, 16 priority levels

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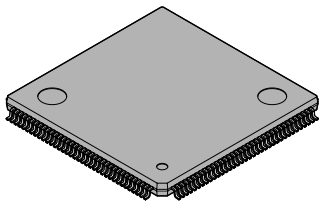
■ PACKAGE

144-pin plastic LQFP



(FPT-144P-M08)

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Bus Interface

- 16-bit address output, 8/16-bit data input and output
- Basic bus cycle : 2-clock cycle
- Support for interface for various types of memory
- Unused data/address pins can be configured as input/output ports
- Support for little endian mode

Internal RAM

Instruction RAM : 2 Kbytes
Data RAM : 32 Kbytes

DMAC

DMAC in descriptor format for placing transfer parameters on to the main memory.
Capable of transferring a maximum of eight internal and external factors combined.
Three channels for external factors

Bit Search Module

Searches in one cycle for the position of the bit that changes from the MSB in one word to the initial 1/0.

Timers

- 16-bit OCU × 8 channels, ICU × 4 channels, Free-run timer × 1 channel
- 8/16-bit up/down timer/counter (8-bit × 2 channels or 16-bit × 1 channel)
- 16-bit PPG timer × 6 channels. The output pulse cycle and duty can be varied as desired.
- 16-bit reload timer × 4 channels

D/A Converter

- 8-bit × 3 channels

A/D Converter (Sequential Comparison Type)

- 10-bit × 8 channels
- Sequential conversion method (conversion time : 5.0 μs@33 MHz)
- Single conversion or scan conversion can be selected, and one-shot or continuous or stop conversion mode can be set respectively.
- Conversion starting function by hardware/software.

Serial I/O

- UART × 4 channels. Any of them is capable of serial transfer in sync with clock attached with the LSB/MSB switching function.
- Serial data output and serial clock output are selectable by push-pull/open drain software.
- A 16-bit timer (U-timer) is contained as a dedicated baud rate generator allowing any baud rate to be generated.

Clock Switching Function

- Gear function : Operating clock ratios to the basic clock can be set independently for the CPU and peripherals from four types, 1 : 1, 1 : 2, 1 : 4 or 1 : 8.

Interrupt Controller

External interrupt input (16 channels in total)

- Allows the rising edge/falling edge/H level/L level to be set.

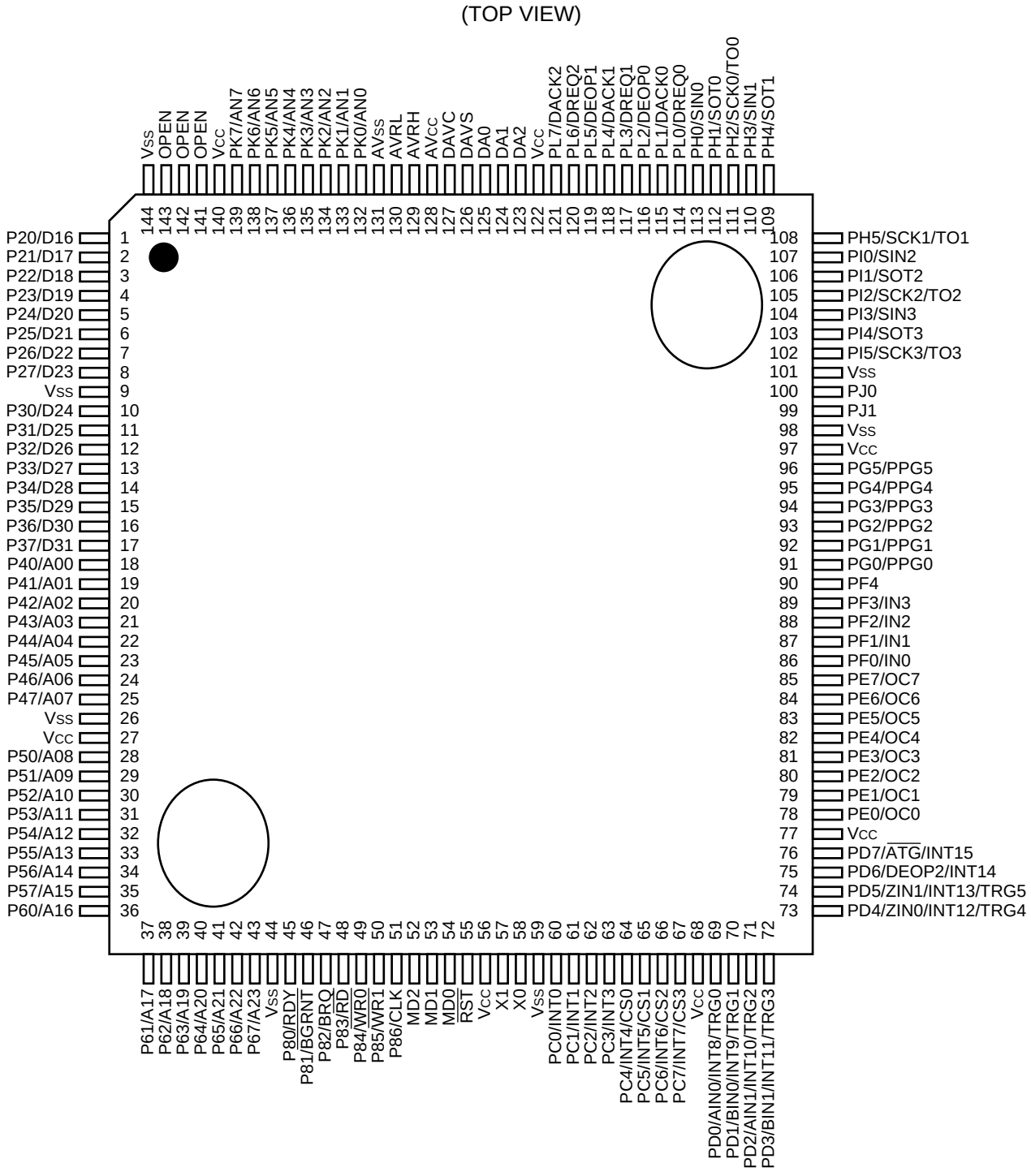
Internal interrupt factors

- Interrupt by resources and delay interrupt

Others

- Reset cause : Power on reset/watchdog timer/software reset/external reset
- Low power consumption mode : Sleep/stop
- Package : 144-pin LQFP
- CMOS technology (0.35 μm)
- Power supply voltage : 3.15 V to 3.6 V

■ PIN ASSIGNMENT



(FPT-144P-M08)

■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
1 2 3 4 5 6 7 8	D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27	C	Bit 16 to bit 23 of external data bus These pins are activated only in 16-bit external bus mode. These pins are available as ports in single-chip and 8-bit external bus modes.
10 11 12 13 14 15 16 17	D24/P30 D25/P31 D26/P32 D27/P33 D28P34 D29/P35 D30/P36 D31/P37	C	Bit 24 to bit 31 of external data bus These pins are available as ports in single-chip mode.
18 19 20 21 22 23 24 25 28 29 30 31 32 33 34 35	A00/P40 A01/P41 A02/P42 A03/P43 A04/P44 A05/P45 A06/P46 A07/P47 A08/P50 A09/P51 A10/P52 A11/P53 A12/P54 A13/P55 A14/P56 A15/P57	F	Bit 0 to bit 15 of external address bus These pins are activated in external bus mode. These pins are available as ports in single-chip mode.
36 37 38 39 40 41 42 43	A16/P60 A17/P61 A18/P62 A19/P63 A20/P64 A21/P65 A22/P66 A23/P67	O	Bit 16 to bit 23 of external address bus These pins are available as ports when the address bus is not in use.
45	RDY/P80	C	External RDY input This function is activated when external RDY input is allowed. Input “0” when the bus cycle being executed does not end. This pin is available as a port when external RDY input is not in use.

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Pin No.	Pin name	Circuit type	Function
46	$\overline{\text{BGRNT}}$/P81	F	External bus release acceptance output This function is activated when external bus release acceptance output is allowed. Output “L” upon releasing of the external bus. This pin is available as a port when external bus release acceptance output is not allowed.
47	BRQ/P82	C	External bus release request input This function is activated when external bus release request input is allowed. Input “1” when the release of the external bus is desired. This pin is available as a port when external bus release request input is not in use.
48	$\overline{\text{RD}}$/P83	F	External bus read strobe output This function is activated when external bus read strobe output is allowed. This pin is available as a port when external bus read strobe output is not allowed.
49	$\overline{\text{WR0}}$/P84	F	External bus write strobe output This function is activated in external bus mode. This pin is available as a port in single chip mode.
50	$\overline{\text{WR1}}$/P85	F	External bus write strobe output This function is activated in external bus mode when the bus width is 16 bits. This pin is available as a port in single chip mode or when the external bus width is 8 bits.
51	CLK/P86	F	System clock output The pin outputs the same clock as the external bus operating frequency. The pin is available as a port when it is not used to output the clock.
52 53 54	MD2 MD1 MD0	G	Mode pins To use these pins, connect them directly to either V_{CC} or V_{SS}. Use these pins to set the basic MCU operating mode.
55	$\overline{\text{RST}}$	B	External reset input
57 58	X1 X0	A	High-speed clock oscillation pins
60 61 62 63	INT0/PC0 INT1/PC1 INT2/PC2 INT3/PC3	H	External interrupt request input 0-3 Since this input is used more or less continuously when the corresponding external interrupt is allowed, output by the port needs to be stopped except when it is performed deliberately. Since this port is allowed to input also in standby mode, it can be used to reset the standby state. These pins are available as ports when external interrupt request input is not in use.

(Continued)

Pin No.	Pin name	Circuit type	Function
64 65 66 67	INT4/PC4/CS0 INT5/PC5/CS1 INT6/PC6/CS2 INT7/PC7/CS3	H	These pins also serve as the chip select output and external interrupt request input 4 to 7. When the chip select output is not allowed, these pins are available as external interrupt requests or ports. Since this input is used more or less continuously when the corresponding external interrupt is allowed, output by the port needs to be stopped except when it is performed deliberately. Since this port is also allowed to input in standby mode, the port can be used to reset the standby state. These pins are available as ports when external interrupt request input and chip select output are not in use.
69 70 71 72 73 74	PD0/AIN0/INT8/TRG0 PD1/BIN0/INT9/TRG1 PD2/AIN1/INT10/TRG2 PD3/BIN1/INT11/TRG3 PD4/ZIN0/INT12/TRG4 PD5/ZIN1/INT13/TRG5	H	External interrupt request input 8 to 13 Since this input is used more or less continuously when the corresponding external interrupt is allowed, output by the port needs to be stopped except when it is performed deliberately. [AIN, BIN] Up/down timer input. [TRG] PPG external trigger input. Since this input is used more or less continuously while input is allowed, output by the port needs to be stopped except when it is performed deliberately. These pins are available as ports when the external interrupt request input, up timer counter input, and PPG external trigger input are not in use.
75	PD6/DEOP2/INT14	H	External interrupt request input 14 Since this input is used more or less continuously when the corresponding external interrupt is allowed, output by the port needs to be stopped except when it is performed deliberately. [DEOP2] DMA external transfer end output. This function is activated when DMAC external transfer end output is allowed. This pin is available as a port when it is not in use as the external interrupt request input or DMA external transfer end output.
76	PD7/$\overline{\text{ATG}}$/INT15	H	External interrupt request input 15 Since this input is used more or less continuously when the corresponding external interrupt is allowed, output by the port needs to be stopped except when it is performed deliberately. [$\overline{\text{ATG}}$] A/D converter external trigger input. Since this input is used more or less continuously when selected as an A/D activation factor, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when it is not in use as the external interrupt request input or A/D converter external trigger input.

(Continued)

Pin No.	Pin name	Circuit type	Function
78 79 80 81 82 83 84 85	PE0/OC0 PE1/OC1 PE2/OC2 PE3/OC3 PE4/OC4 PE5/OC5 PE6/OC6 PE7/OC7	F	Output compare output These pins are available as ports when output compare output is not allowed.
86 87 88 89	PF0/IN0 PF1/IN1 PF2/IN2 PF3/IN3	F	Input capture input This function is activated when the input capture operation is input. These pins are available as ports when input capture input is not in use.
90	PF4	F	General I/O port
91 92 93 94 95 96	PG0/PPG0 PG1/PPG1 PG2/PPG2 PG3/PPG3 PG4/PPG4 PG5/PPG5	F	PPG timer output This function is activated when PPG timer output is allowed. These pins are available as ports when PPG timer output is not allowed.
99 100	PJ1 PJ0	Q	General I/O port
102	PI5/SCK3/TO3	P	UART3 clock I/O, Reload timer 3 output When UART3 clock output is not allowed, reload timer 3 can be output by allowing it. This pin is available as a port when neither UART3 clock output nor reload timer output is allowed.
103	PI4/SOT3	P	UART3 data output This function is activated when UART3 data output is allowed. This pin is available as a port when UART3 clock output is not allowed.
104	PI3/SIN3	P	UART3 data input Since this input is used more or less continuously while UART3 is engaged in input operations, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when UART3 output data input is not in use.

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Pin No.	Pin name	Circuit type	Function
105	PI2/SCK2/TO2	P	UART2 clock I/O, Reload timer 2 output When UART2 clock output is not allowed, reload timer 2 can be output by allowing it. This pin is available as a port when neither UART2 clock output nor reload timer output is allowed.
106	PI1/SOT2	P	UART2 data output This function is activated when UART2 data output is allowed. This pin is available as a port when UART2 clock output is not allowed.
107	PI0/SIN2	P	UART2 data input Since this input is used more or less continuously while UART2 is engaged in input operations, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when UART2 data input is not in use.
108	PH5/SCK1/TO1	P	UART1 clock I/O, Reload timer 1 output When UART1 clock output is not allowed, reload timer 1 can be output by allowing it. This pin is available as a port when neither UART1 clock output nor reload timer output is allowed.
109	PH4/SOT1	P	UART1 data output This function is activated when UART1 data output is allowed. This pin is available as a port when UART1 clock output is not allowed.
110	PH3/SIN1	P	UART1 data input Since this input is used more or less continuously while UART1 is engaged in input operations, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when UART1 data input is not in use.
111	PH2/SCK0/TO0	P	UART0 clock I/O, Reload timer 0 output When UART0 clock output is not allowed, reload timer 0 can be output by allowing it. This pin is available as a port when neither UART0 clock output nor reload timer output is allowed.
112	PH1/SOT0	P	UART0 data output This function is activated when UART0 data output is allowed. This pin is available as a port when UART0 clock output is not allowed.
113	PH0/SIN0	P	UART0 data input Since this input is used more or less continuously while UART0 is engaged in input operations, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when UART0 data input is not in use.
114	DREQ0/PL0	F	DMA external transfer request input Since this input is used more or less continuously when selected as a DMAC transfer factor, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when DMA external transfer request input is not in use.

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Pin No.	Pin name	Circuit type	Function
115	DACK0/PL1	F	DMA external transfer request acceptance output This function is activated when the DMAC external transfer request acceptance is allowed to be output. This pin is available as a port when the DMAC transfer request acceptance is not allowed to be output.
116	DEOP0/PL2	F	DMA external transfer end output This function is activated when the end of DMAC external transfer is allowed to be output.
117	DREQ1/PL3	F	DMA external transfer request input Since this input is used more or less continuously when selected as a DMAC transfer factor, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when DMA external transfer request input is not in use.
118	DACK1/PL4	F	DMA external transfer request acceptance output This function is activated when the DMAC external transfer request acceptance is allowed to be output. This pin is available as a port when DMAC transfer request acceptance output is not allowed.
119	DEOP1/PL5	F	DMA external transfer end output This function is activated when the end of DMAC external transfer is allowed to be output.
120	DREQ2/PL6	F	DMA external transfer request input Since this input is used more or less continuously when selected as a DMAC transfer factor, output by the port needs to be stopped except when it is performed deliberately. This pin is available as a port when DMA external transfer request input is not in use.
121	DACK2/PL7	F	DMA external transfer request acceptance output This function is activated when the DMAC external transfer request acceptance is allowed to be output. This pin is available as a port when DMAC transfer request acceptance output is not allowed.
123 124 125	DA2 DA1 DA0	—	D/A converter output This function is activated when D/A converter output is allowed.
126	DAVS	—	Power supply pin for the D/A converter
127	DAVC	—	Power supply pin for the D/A converter
128	AV_{CC}	—	Vcc power supply for the A/D converter
129	AVRH	—	A/D converter reference voltage (high potential side) Be sure to turn on/off this pin with potential higher than AVRH applied to V_{CC}.
130	AVRL	—	A/D converter reference voltage (low potential side)
131	AV_{SS}	—	V_{SS} power supply for the A/D converter

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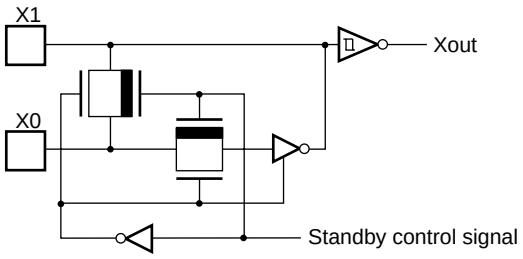
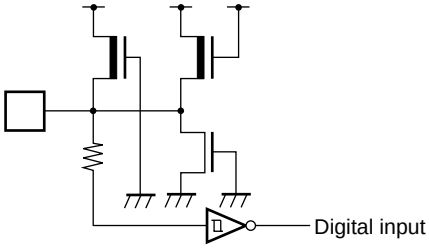
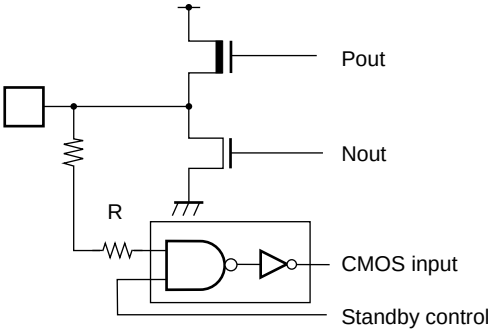
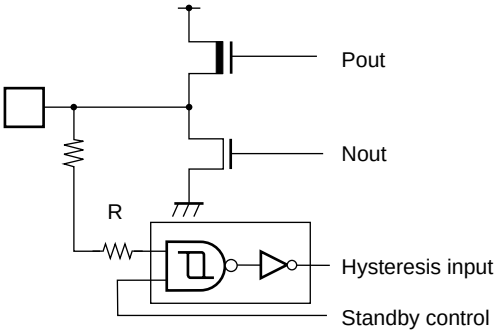
Pin No.	Pin name	Circuit type	Function
132 133 134 135 136 137 138 139	AN0/PK0 AN1/PK1 AN2/PK2 AN3/PK3 AN4/PK4 AN5/PK5 AN6/PK6 AN7/PK7	N	A/D converter analog input These pins are activated when the AIC register is designated for analog input. These pins are available as ports when A/D converter analog input is not in use.
27, 56, 68, 77, 97, 122, 140	V_{CC}	—	Power supply pin (V_{CC}) for digital circuit Always power supply pin (V_{CC}) must be connected to the power supply.
9, 26, 44, 59, 98, 101, 144	V_{SS}	—	Earth level (V_{SS}) for digital circuit Always power supply pin (V_{SS}) must be connected to the power supply.

Note : On the majority of pins listed above, the I/O port and the resource I/O are multiplexed, such as XXXX/Pxx. When the port and the resource output compete against each other on these pins, priority is given to the resource.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• High-speed oscillation circuit Oscillation feedback resistor = approx. 1 MΩ
B		• CMOS hysteresis input pin CMOS hysteresis input (standby control not attached) Pull-up resistor
C		• CMOS level I/O pin CMOS level output CMOS level input (attached with standby control) I_{OL} = 4 mA
F		• CMOS hysteresis I/O pin CMOS level output CMOS hysteresis input (attached with standby control) I_{OL} = 4 mA

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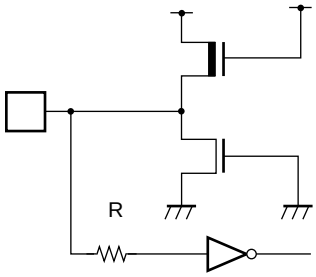
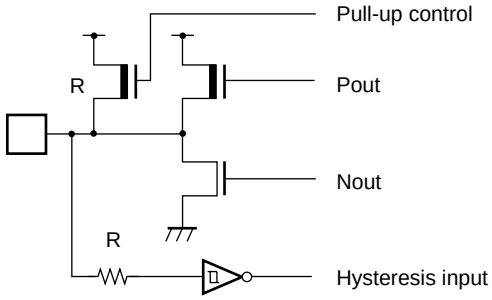
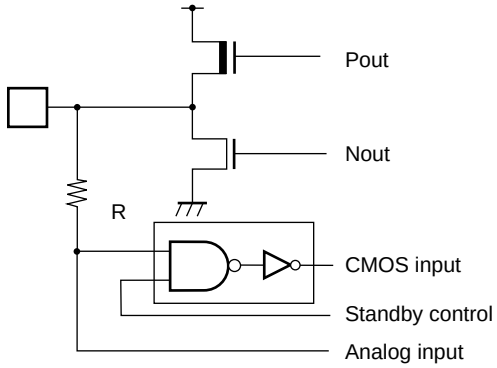
Type	Circuit	Remarks
G		• CMOS level input pin CMOS level input (standby control not attached)
H		• CMOS hysteresis I/O pin with pull-up control CMOS level output CMOS level input (standby control not attached) Pull-up resistance = approx. 50 kΩ (Typ) I_{OL} = 4 mA
N		• Analog/CMOS level I/O pin. CMOS level output CMOS level input (attached with standby control) Analog input (Analog input is enabled when AIC's corresponding bit is set to "1.") I_{OL} = 4 mA

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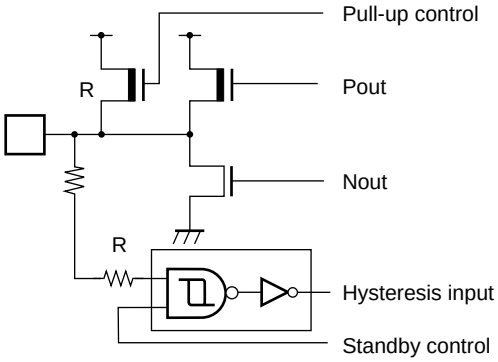
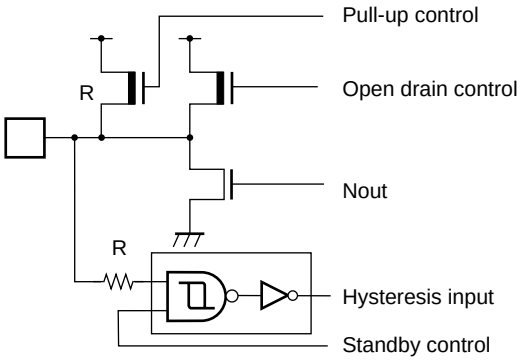
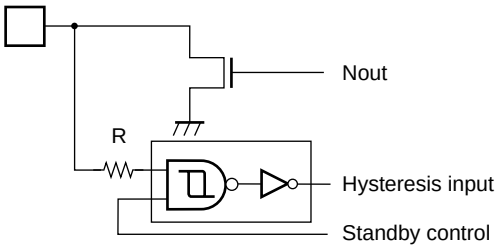
Type	Circuit	Remarks
O		• CMOS hysteresis I/O pin with pull-up control CMOS level output CMOS hysteresis input (attached with standby control) Pull-up resistance = approx. 50 kΩ (Typ) I_{OL} = 4 mA
P		• CMOS hysteresis I/O pin with pull-up control. CMOS level output (attached with open drain control) CMOS hysteresis input (attached with standby control) Pull-up resistance = approx. 50 kΩ (Typ) I_{OL} = 4 mA
Q		• Open drain I/O pin • 5 V tolerance of voltage • CMOS hysteresis input (attached with standby control) I_{OL} = 15 mA

■ HANDLING DEVICES

1. Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

2. Treatment of Pins

- **Treatment of unused pins**
  Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.
- **Treatment of open pins**
  Be sure to use open pins in open state.
- **Treatment of output pins**
  Shortcircuiting an output pin with the power supply or with another output pin or connecting a large-capacity load may causes a flow of large current. If this conditions continues for a lengthy period of time, the device deteriorates. Take great care not to exceed the absolute maximum ratings.
- **Mode pins** (**MD0**-**MD2**)
  These pins should be used directly connected to either V_{CC} or V_{SS}. In order to prevent noise from causing accidental entry into test mode, keep the pattern length as short as possible between each mode pin and V_{CC} or V_{SS} on the board and connect them with low impedance.
- **Power supply pins**
  When there are several V_{CC} and V_{SS} pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all V_{CC} and V_{SS} pins to the power supply or GND.

It is preferred to connect V_{CC} and V_{SS} of MB91151A to power supply with minimal impedance possible.

It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} at a position as close as possible to MB91151A.

- **Crystal oscillator circuit**
  Noises around X0 and X1 pins may cause malfunctions of MB91151A. In designing the PC board, layout X0 and X1 and crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.

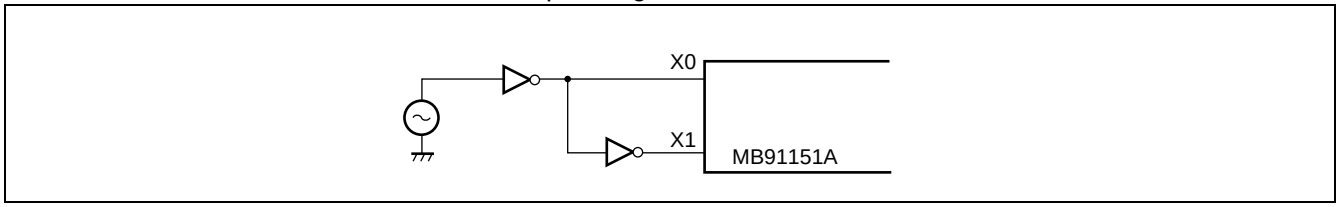
It is strongly recommended to design PC board so that X0, X1 pins are surrounded by grounding area for stable operation

3. Precautions

- **External Reset Input**
  It takes at least 5 machine cycle to input “L” level to the $\overline{RST}$ pin and to ensure inner reset operation properly.
- **External Clocks**
  When using an external clock, normally, a clock of which the phase is opposite to that of X0 must be supplied to the X0 and X1 pins simultaneously. However, when using the clock along with STOP (oscillation stopped) mode, the X1 pin stops when “H” is input in STOP mode. To prevent one output from competing against another, an external resistor of about 1 kΩ should be provided.

The following figure shows an example usage of an external clock.

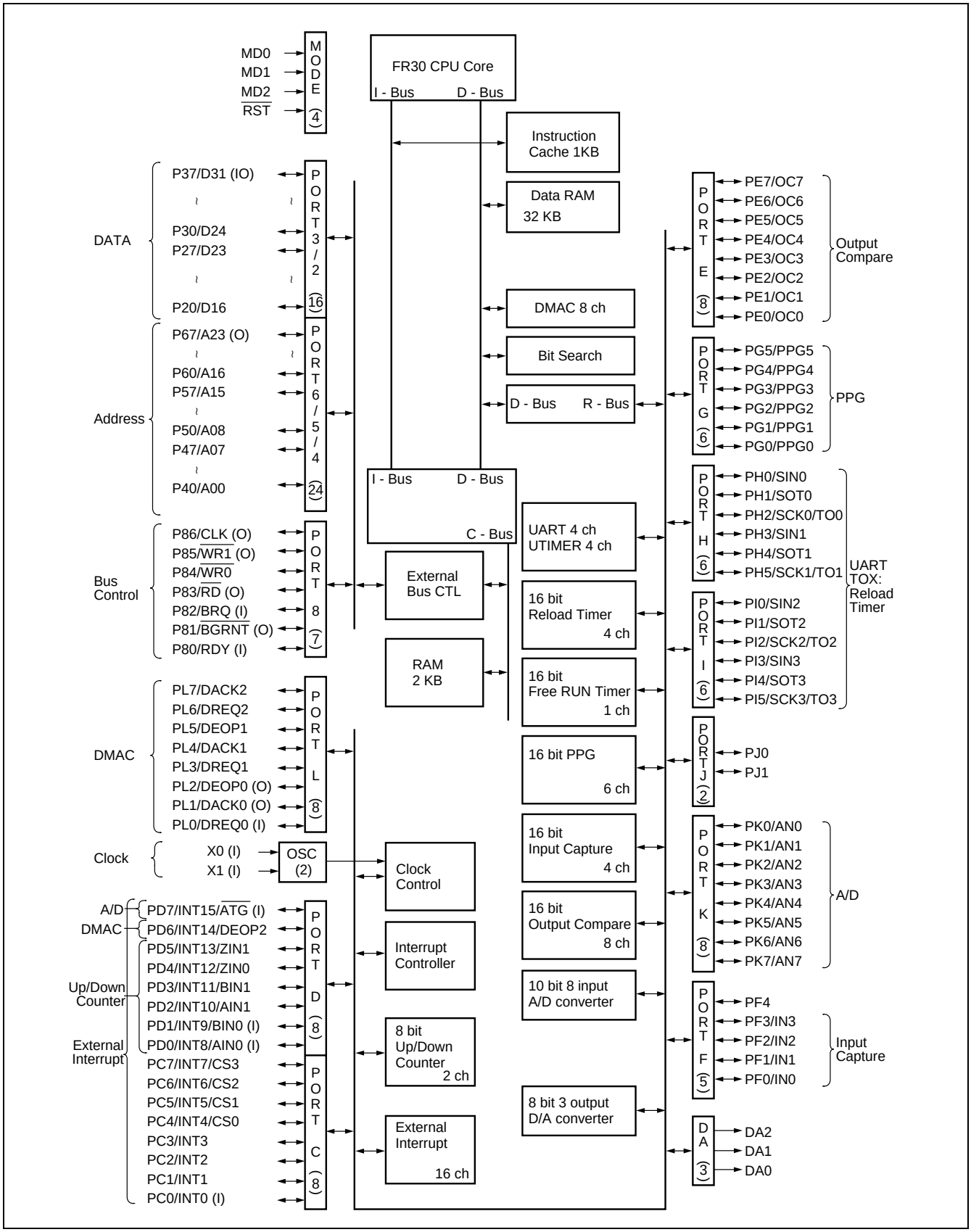
An example usage of an external clock



4. Caution During Powering Up

- **When powering up**
  When turning on the power supply, never fail to start from setting the $\overline{RST}$ pin to “L” level. And after the power supply voltage goes to V_{CC} level, at least after ensuring the time for 5 machine cycles, then set to “H” level.
- **Source oscillation input**
  At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.
- **Power on resetting**
  When powering up or when turning the power back on after the supply voltage drops below the operation assurance range, be sure to reset the power.
- **Power on sequence**
  Turn on the power in the order of V_{CC}, AV_{CC} and AVRH. The power should be disconnected in inverse order.
- **Even when an AD converter is not in use**, **connect AV_{CC} to the V_{CC} level and AV_{SS} to the V_{SS} level.**
- **Even when a DA converter is not in use**, **connect DAVC to the V_{CC} level and DAVS to the V_{SS} level.**

■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

The FR family has a logical address space of 4 Gbytes (2^{32} bytes) and the CPU linearly accesses the memory space.

- **Direct addressing area**

  The following area in the address space is used for I/O.

  This area is called direct addressing area and an operand address can be specified directly in an instruction.

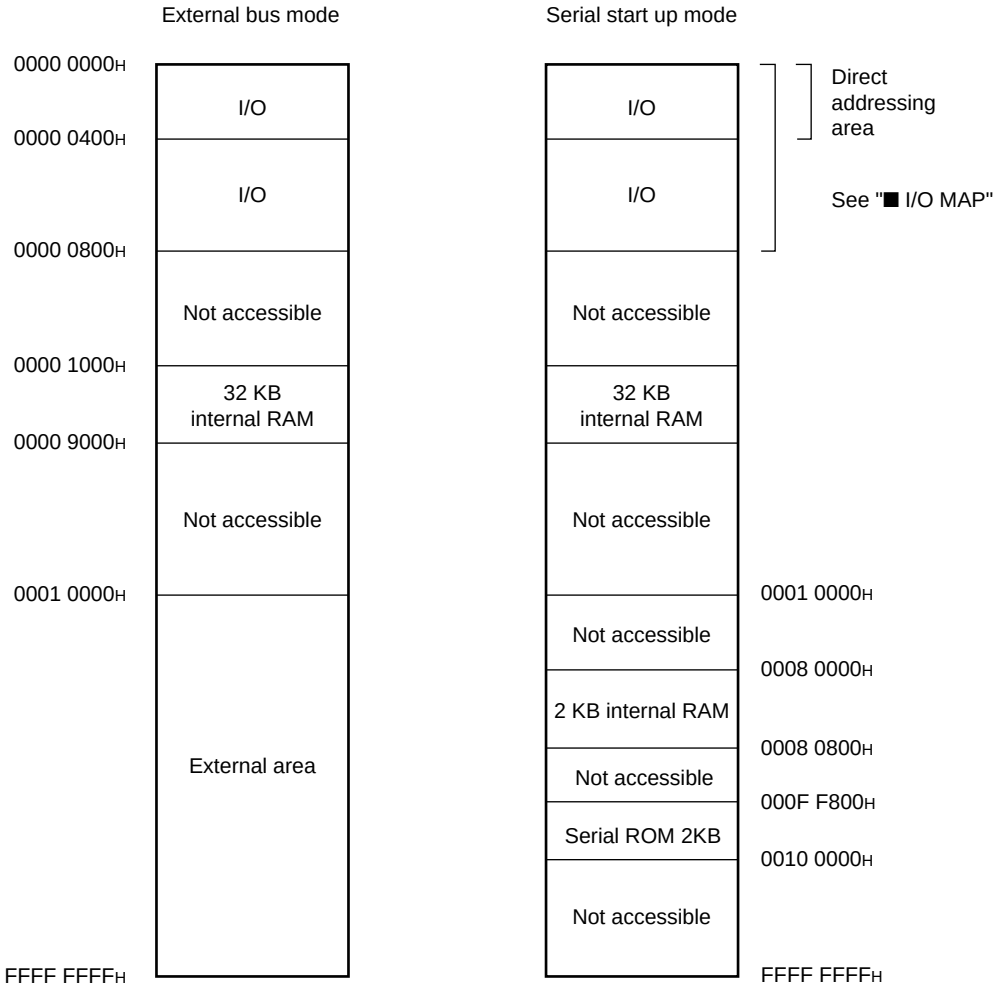
  The direct addressing area varies with the data size to be accessed as follows :

  → byte data access : 000_H-$0FF_H$

  → half word data access : 000_H-$1FF_H$

  → word data access : 000_H-$3FF_H$

2. Memory Map

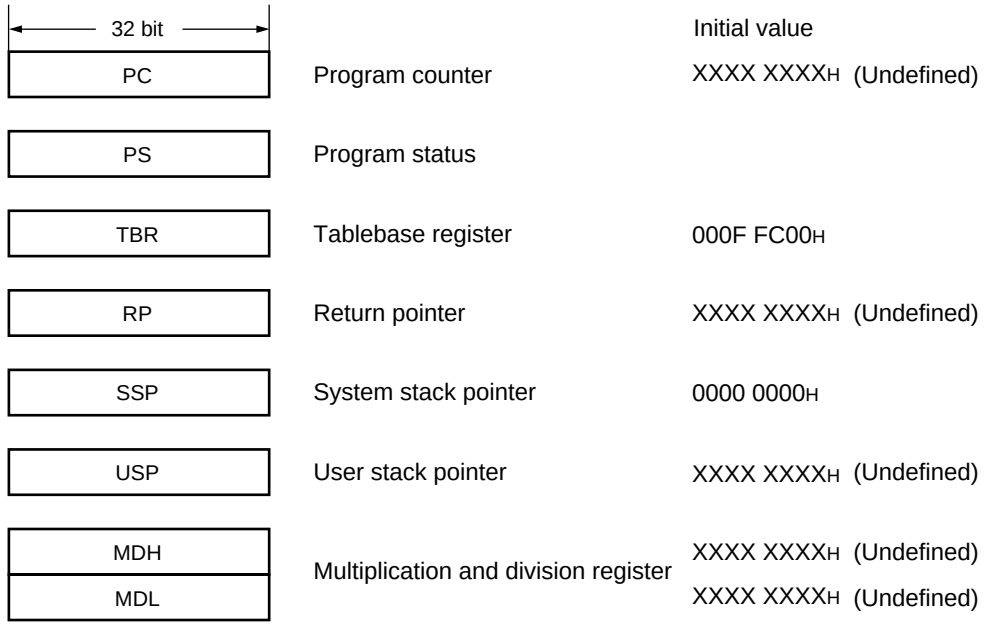


3. Registers

The family of FR microcontrollers has two types of registers : the registers residing in the CPU which are dedicated to applications and the general-purpose registers residing in the memory.

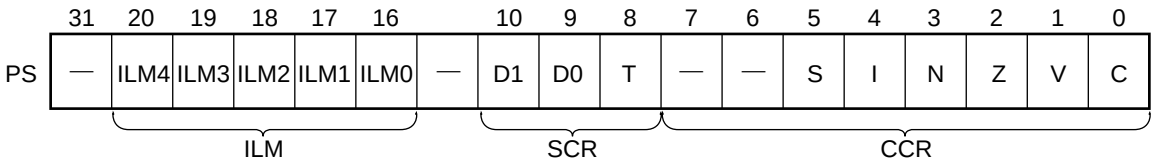
- **Dedicated registers** :

  Program counter (PC) : A 32-bit register to indicate the location where an instructions is stored.
  Program status (PS) : A 32-bit register to store a register pointer or a condition code.
  Tablebase register (TBR) : Holds the vector table lead address used when EIT (exceptions/interrupt/ trap) is processed.
  Return pointer (RP) : Holds the address to return from a subroutine.
  System stack pointer (SSP) : Points to the system stack space.
  User stack pointer (USP) : Points to the user stack space.
  Multiplication and division result register (MDH/MDL) : A 32-bit multiplication and division register.



- **Program status (PS)**

The PS register holds program status and is further divided into three registers which are a Condition Code Register (CCR) , a System condition Code Register (SCR) , and an Interrupt Level Mask register (ILM) .



- **Condition Code Register** (**CCR**)
  - S flag : Designates the stack pointer for use as R15.
  - I flag : Controls enabling and disabling of user interrupt requests.
  - N flag : Indicates the sign when arithmetic operation results are considered to be an integer represented by 2's complement.
  - Z flag : Indicates if arithmetic results were "0."
  - V flag : Considers the operand used for an arithmetic operation to be an integer represented by 2's complement and indicates if the operation resulted in an overflow.
  - C flag : Indicates whether or not an arithmetic operation resulted in a carry or a borrow from the most significant bit.

- **System condition Code Register** (**SCR**)
  - T flag : Designates whether or not to enable step trace trap.

- **Interrupt Level Mask register** (**ILM**)
  - ILM4 to ILM0 : Holds an interrupt level mask value to be used for level masking.
    An interrupt request is accepted only if the corresponding interrupt level among interrupt requests input to the CPU is higher than the value indicated by the ILM register.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-Low
0	0	0	0	0	0	Higher
		⋮			⋮	
0	1	0	0	0	15	
		⋮			⋮	
1	1	1	1	1	31	Lower

■ Instruction Cache

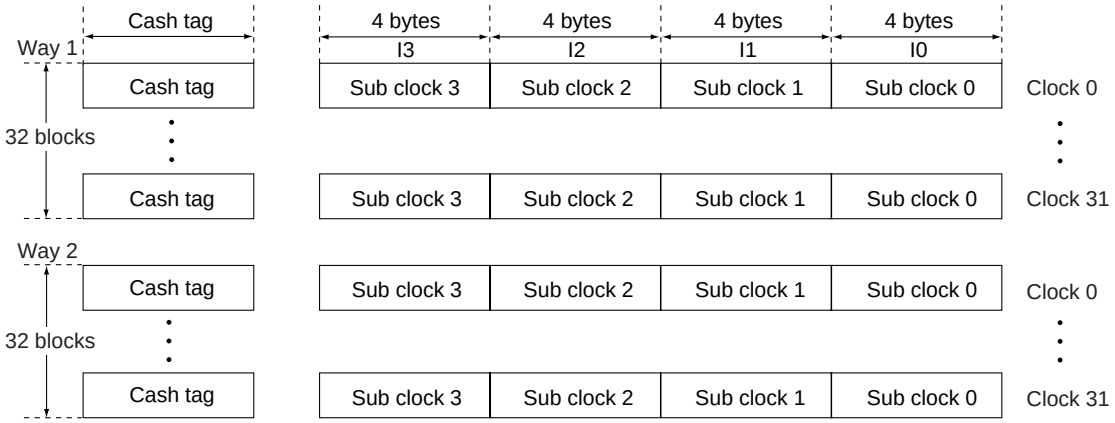
- **Description**

The instruction cache is a temporary storage memory. In the event that the instruction codes are accessed from a low speed external memory, it holds the accessed codes internally, and is used to increase the access speed for all subsequent accesses.

Direct read or write access can not be done by instruction cache or instruction cache tag using software.

- **Instruction cache configuration**
  - Basic instruction length of FR series **:** 2 bytes
  - Block layout **:** 2-way set associative type
  - Block
    1 way is configured of 32 blocks.
    1 block is 16 bytes (= 4 sub blocks)
    1 sub block is 4 bytes (= 1 bus access unit)

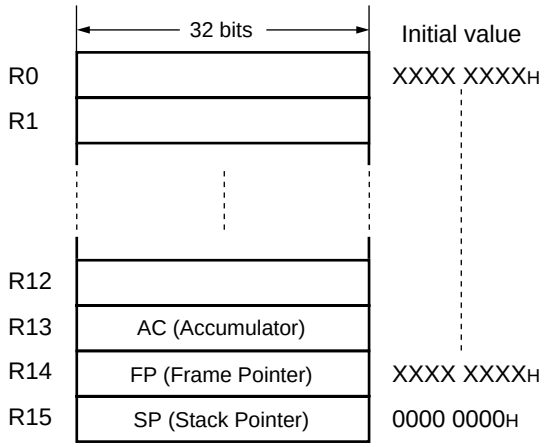
- **Instruction Cache Configuration**



■ GENERAL-PURPOSE REGISTERS

General-purpose registers are CPU registers R0 through R15 and used as accumulators during various operations and as memory access pointers (fields indicating addresses) .

- **Register Bank Configuration**



Of the 16 general-purpose registers, the following registers are assumed for specific applications. For this reason, some instructions are enhanced.

R13 : Virtual accumulator (AC)
R14 : Frame pointer (FP)
R15 : Stack pointer (SP)

Initial values to which R0 through R14 are reset are not defined. The initial value of R15 is 0000 0000H (the SSP value) .

■ MODE SETTING

1. Mode Pins

As shown below, three pins, MD2, MD1, and MD0 are used to indicate an operation.

Mode pins and set modes

Mode pin			Mode name	Reset vector access area	External data bus width	Bus modes
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	External vector mode 2	External	32 bits	Not available on this product type
0	1	1	External vector mode	Internal	(Mode register)	Single-chip mode*
1	—	—	—	—	—	Not available

* : Not available on this product type

2. Mode Data

The data which the CPU writes to “0000 07FF$_H$” after reset is called mode data.
It is the mode register (MODR) that exists at “0000 07FF$_H$.” Once a mode is set in this register, operations will take place in that mode. The mode register can be written only once after reset.
The mode specified in the register is enabled immediately after it is written.

MODR
Address : 0000 07FF$_H$

M1	M0	*	*	*	*	*	*

Initial value Access
XXXXXXXX W

Bus mode setting bits

W : Write only, X : Undefined

[bits 7 and 6] : M1, M0

These are bus mode setting bits. Specify the bus mode to be set to after writing to the mode register.

M1	M0	Function	Remarks
0	0	Single-chip mode	Setting not allowed
0	1	Internal RAM-external bus mode	
1	0	External bus mode	
1	1	—	Setting not allowed

Note : Of the above options, only “01” or “10“ should be set for this model.

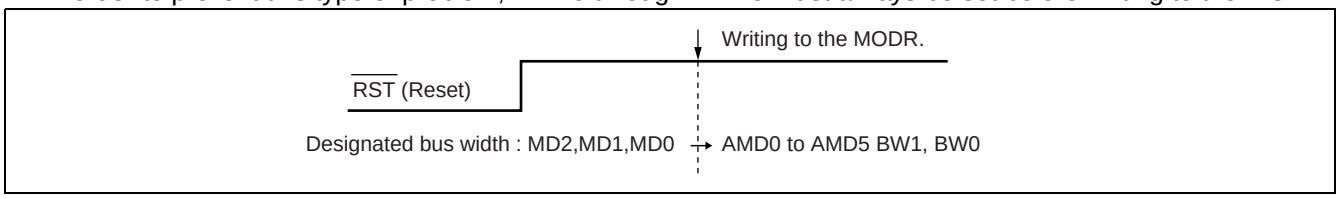
[bits 5 to 0] : *

These bits are reserved for the system.
“0” should be written to these bits at all times.

[Precautions When Writing to the MODR]

Before writing to the MODR, be sure to set AMD0 through AMD5 and determine the bus width in each CS (Chip Select) area.
The MODR does not have bus width setting bits.
The bus width value set with mode pins MD2 through MD0 is enabled before writing to the MODR and the bus width value set with BW1 and BW0 of AMD0 through AMD5 is enabled after writing to the MODR.
For example, the external reset vector is normally executed with area 0 (the area where CS0 is active) and the bus width at that time is determined by pins MD2 through MD0. Suppose that the bus width is set to 32 or 16 bits in MD2 though MD0 but no value is specified in AMD0. If the MODR is written in this state, area 0 then switches to 8-bit bus mode and operates the bus since the initial bus width in AMD0 is set to 8 bits. This causes a malfunction.

In order to prevent this type of problem, AMD0 through AMD5 must always be set before writing to the MODR.



■ I/O MAP

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR3 (R/W) XXXXXXXX	PDR2 (R/W) XXXXXXXX	—		Port Data Register
000004H	—	PDR6 (R/W) XXXXXXXX	PDR5 (R/W) XXXXXXXX	PDR4 (R/W) XXXXXXXX	
000008H	—			PDR8 (R/W) - XXXXXXX	
00000CH	—				
000010H	PDRF (R/W) - - - XXXXX	PDRE (R/W) XXXXXXXX	PDRD (R/W) XXXXXXXX	PDRC (R/W) XXXXXXXX	
000014H	PDRJ (R/W) - - - - - - 11	PDRI (R/W) - - XXXXXX	PDRH (R/W) - - XXXXXX	PDRG (R/W) - - XXXXXX	
000018H	—		PDRL (R/W) XXXXXXXX	PDRK (R/W) XXXXXXXX	
00001CH	SSR0 (R, R/W) 00001000	SIDR0/SODR0 (R, W) XXXXXXXX	SCR0 (R/W, W) 00000100	SMR0 (R/W) 00000 - 00	UART0
000020H	SSR1 (R, R/W) 00001000	SIDR1/SODR1 (R, W) XXXXXXXX	SCR1 (R/W, W) 00000100	SMR1 (R/W) 00000 - 00	UART1
000024H	SSR2 (R, R/W) 00001000	SIDR2/SODR2 (R, W) XXXXXXXX	SCR2 (R/W, W) 00000100	SMR2 (R/W) 00000 - 00	UART2
000028H	SSR3 (R, R/W) 00001000	SIDR3/SODR3 (R, W) XXXXXXXX	SCR3 (R/W, W) 00000100	SMR3 (R/W) 00000 - 00	UART3
00002CH	TMRLR0 (W) XXXXXXXX XXXXXXXX		TMR0 (R) XXXXXXXX XXXXXXXX		Reload Timer 0
000030H	—		TMCSR0 (R/W) - - - - 0000 00000000		
000034H	TMRLR1 (W) XXXXXXXX XXXXXXXX		TMR1 (R) XXXXXXXX XXXXXXXX		Reload Timer 1
000038H	—		TMCSR1 (R/W) - - - - 0000 00000000		
00003CH	TMRLR2 (W) XXXXXXXX XXXXXXXX		TMR2 (R) XXXXXXXX XXXXXXXX		Reload Timer 2
000040H	—		TMCSR2 (R/W) - - - - 0000 00000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000044H	TMRLR3 (W) XXXXXXXX XXXXXXXX		TMR3 (R) XXXXXXXX XXXXXXXX		Reload Timer 3
000048H	—		TMCSR3 (R/W) - - - - 0000 00000000		
00004CH	CDCR1 (R/W) 0 - - - 0000	—	CDCR0 (R/W) 0 - - - 0000	—	Communications prescaler 1
000050H	CDCR3 (R/W) 0 - - - 0000	—	CDCR2 (R/W) 0 - - - 0000	—	
000054H to 000058H	—				Reserved
00005CH	RCR1 (W) 00000000	RCR0 (W) 00000000	UDCR1 (R) 00000000	UDCR0 (R) 00000000	8/16 bit U/D Counter
000060H	CCRH0 (R/W) 00000000	CCRL0 (R/W, W) - 000X000	—	CSR0 (R/W, R) 00000000	
000064H	CCRH1 (R/W) - 0000000	CCRL1 (R/W, W) - 000X000	—	CSR1 (R/W, R) 00000000	
000068H	IPCP1 (R) XXXXXXXX XXXXXXXX		IPCP0 (R) XXXXXXXX XXXXXXXX		16 bit ICU
00006CH	IPCP3 (R) XXXXXXXX XXXXXXXX		IPCP2 (R) XXXXXXXX XXXXXXXX		
000070H	—	ICS23 (R/W) 00000000	—	ICS01 (R/W) 00000000	
000074H	OCCP1 (R/W) XXXXXXXX XXXXXXXX		OCCP0 (R/W) XXXXXXXX XXXXXXXX		16 bit OCU
000078H	OCCP3 (R/W) XXXXXXXX XXXXXXXX		OCCP2 (R/W) XXXXXXXX XXXXXXXX		
00007CH	OCCP5 (R/W) XXXXXXXX XXXXXXXX		OCCP4 (R/W) XXXXXXXX XXXXXXXX		
000080H	OCCP7 (R/W) XXXXXXXX XXXXXXXX		OCCP6 (R/W) XXXXXXXX XXXXXXXX		
000084H	OCS2, 3 (R/W) XXX00000 0000XX00		OCS0, 1 (R/W) XXX00000 0000XX00		
000088H	OCS6, 7 (R/W) XXX00000 0000XX00		OCS4, 5 (R/W) XXX00000 0000XX00		
00008CH	TCDT (R/W) 00000000 00000000		TCCS (R/W) 0 - - - - - - - 00000000		16 bit Freerun Timer
000090H	STPR0 (R/W) 0000 - - - -	STPR1 (R/W) 00000 - 00	STPR2 (R/W) 000000 - -	—	Stop Register 0, 1, 2
000094H	GCN1 (R/W) 00110010 00010000		—	GCN2 (R/W) 00000000	PPG ctl

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000098H	PTMR0 (R) 11111111 11111111		PCSR0 (W) XXXXXXXX XXXXXXXX		PPG0
00009CH	PDUT0 (W) XXXXXXXX XXXXXXXX		PCNH0 (R/W) 0000000 -	PCNL0 (R/W) 00000000	
0000A0H	PTMR1 (R) 11111111 11111111		PCSR1 (W) XXXXXXXX XXXXXXXX		PPG1
0000A4H	PDUT1 (W) XXXXXXXX XXXXXXXX		PCNH1 (R/W) 0000000 -	PCNL1 (R/W) 00000000	
0000A8H	PTMR2 (R) 11111111 11111111		PCSR2 (W) XXXXXXXX XXXXXXXX		PPG2
0000ACH	PDUT2 (W) XXXXXXXX XXXXXXXX		PCNH2 (R/W) 0000000 -	PCNL2 (R/W) 00000000	
0000B0H	PTMR3 (R) 11111111 11111111		PCSR3 (W) XXXXXXXX XXXXXXXX		PPG3
0000B4H	PDUT3 (W) XXXXXXXX XXXXXXXX		PCNH3 (R/W) 0000000 -	PCNL3 (R/W) 00000000	
0000B8H	PTMR4 (R) 11111111 11111111		PCSR4 (W) XXXXXXXX XXXXXXXX		PPG4
0000BCH	PDUT4 (W) XXXXXXXX XXXXXXXX		PCNH4 (R/W) 0000000 -	PCNL4 (R/W) 00000000	
0000C0H	PTMR5 (R) 11111111 11111111		PCSR5 (W) XXXXXXXX XXXXXXXX		PPG5
0000C4H	PDUT5 (W) XXXXXXXX XXXXXXXX		PCNH5 (R/W) 0000000 -	PCNL5 (R/W) 00000000	
0000C8H	EIRR0 (R/W) 00000000	ENIR0 (R/W) 00000000	EIRR1 (R/W) 00000000	ENIR1 (R/W) 00000000	Ext int
0000CCH	ELVR0 (R/W) 00000000 00000000		ELVR1 (R/W) 00000000 00000000		
0000D0H to 0000D8H	—				Reserved
0000DCH	—	DACR2 (R/W) - - - - - - - 0	DACR1 (R/W) - - - - - - - 0	DACR0 (R/W) - - - - - - - 0	D/A Converter
0000E0H	—	DADR2 (R/W) XXXXXXXX	DADR1 (R/W) XXXXXXXX	DADR0 (R/W) XXXXXXXX	
0000E4H	ADCR (R, W) 00101- XX XXXXXXXX		ADCS1 (R/W, W) 00000000	ADCS0 (R/W) 00000000	A/D Converter (Sequential type)
0000E8H	—			AICK (R/W) 00000000	Analog Input Control
0000ECH to 0000F0H	—				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000F4H	PCRI (R/W) - - 000000	PCRH (R/W) - - 000000	PCRD (R/W) 00000000	PCRC (R/W) 00000000	Pull Up Control
0000F8H	OCRI (R/W) - - 000000	OCRH (R/W) - - 000000	—		Open drain Control
0000FCH	DDRF (R/W) - - - 00000	DDRE (R/W) 00000000	DDRD (R/W) 00000000	DDRC (R/W) 00000000	Data Direction Register
000100H	—	DDRI (R/W) - 0000000	DDRH (R/W) - - 000000	DDRG (R/W) - - 000000	
000104H	—		DDRL (R/W) 00000000	DDRK (R/W) 00000000	
000108H to 0001FCH	—				Reserved
000200H	DPDP (R/W) - 0000000				DMAC
000204H	DACSR (R/W) 00000000 00000000 00000000 00000000				
000208H	DATCR (R/W) XXXXXXXX XXXX0000 XXXX0000 XXXX0000				
00020CH to 0003E0H	—				Reserved
0003E4H	ICHCR (R/W) - 000000				Instruction cache
0003E8H to 0003ECH	—				Reserved
0003F0H	BSD0 (W) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003E4H	BSD1 (R/W) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC (W) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR (R) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000400H	ICR00 (R/W) - - - - 1111	ICR01 (R/W) - - - - 1111	ICR02 (R/W) - - - - 1111	ICR03 (R/W) - - - - 1111	Interrupt Control unit
000404H	ICR04 (R/W) - - - - 1111	ICR05 (R/W) - - - - 1111	ICR06 (R/W) - - - - 1111	ICR07 (R/W) - - - - 1111	
000408H	ICR08 (R/W) - - - - 1111	ICR09 (R/W) - - - - 1111	ICR10 (R/W) - - - - 1111	ICR11 (R/W) - - - - 1111	
00040CH	ICR12 (R/W) - - - - 1111	ICR13 (R/W) - - - - 1111	ICR14 (R/W) - - - - 1111	ICR15 (R/W) - - - - 1111	
000410H	ICR16 (R/W) - - - - 1111	ICR17 (R/W) - - - - 1111	ICR18 (R/W) - - - - 1111	ICR19 (R/W) - - - - 1111	
000414H	ICR20 (R/W) - - - - 1111	ICR21 (R/W) - - - - 1111	ICR22 (R/W) - - - - 1111	ICR23 (R/W) - - - - 1111	
000418H	ICR24 (R/W) - - - - 1111	ICR25 (R/W) - - - - 1111	ICR26 (R/W) - - - - 1111	ICR27 (R/W) - - - - 1111	
00041CH	ICR28 (R/W) - - - - 1111	ICR29 (R/W) - - - - 1111	ICR30 (R/W) - - - - 1111	ICR31 (R/W) - - - - 1111	
000420H	ICR32 (R/W) - - - - 1111	ICR33 (R/W) - - - - 1111	ICR34 (R/W) - - - - 1111	ICR35 (R/W) - - - - 1111	
000424H	ICR36 (R/W) - - - - 1111	ICR37 (R/W) - - - - 1111	ICR38 (R/W) - - - - 1111	ICR39 (R/W) - - - - 1111	
000428H	ICR40 (R/W) - - - - 1111	ICR41 (R/W) - - - - 1111	ICR42 (R/W) - - - - 1111	ICR43 (R/W) - - - - 1111	
00042CH	ICR44 (R/W) - - - - 1111	ICR45 (R/W) - - - - 1111	ICR46 (R/W) - - - - 1111	ICR47 (R/W) - - - - 1111	
000430H	DICR (R/W) - - - - - - - 0	HRCL (R/W) - - - - 1111	—		Delay int
000434H to 00047CH	—				Reserved
000480H	RSRR/WTCR (R, W) 1-XXX-00	STCR (R/W, W) 000111- -	PDRR (R/W) - - - - 0000	CTBR (W) XXXXXXXX	Clock Control unit
000484H	GCR (R/W, R) 110011-1	WPR (W) XXXXXXXX	—		
000488H	PTCR (R/W) 00XX0XXX	—			PLL Control
00048CH to 0005FCH	—				Reserved

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000600H	DDR3 (W) 00000000	DDR2 (W) 00000000	—	—	Data Direction Register
000604H	—	DDR6 (W) 00000000	DDR5 (W) 00000000	DDR4 (W) 00000000	
000608H	—			DDR8 (W) - 0000000	
00060CH	ASR1 (W) 00000000 00000001		AMR1 (W) 00000000 00000000		T-unit
000610H	ASR2 (W) 00000000 00000010		AMR2 (W) 00000000 00000000		
000614H	ASR3 (W) 00000000 00000011		AMR3 (W) 00000000 00000000		
000618H	ASR4 (W) 00000000 00000100		AMR4 (W) 00000000 00000000		
00061CH	ASR5 (W) 00000000 00000101		AMR5 (W) 00000000 00000000		
000620H	AMD0 (R/W) - - - 00111	AMD1 (R/W) 0 - - 00000	AMD32 (R/W) 00000000	AMD4 (R/W) 0 - - 00000	
000624H	AMD5 (R/W) 0 - - 00000	—			
000628H	EPCR0 (W) - - - - 1100 -1111111		EPCR1 (W) - - - - - - - - 11111111		
00062CH	—				Reserved
000630H	—	PCR6 (R/W) 00000000	—		Pull Up Control
000634H to 0007F8H	—				Reserved
0007FCH	—		LER (W) - - - - - 000	MODR (W) XXXXXXXX	Little Endian Register Mode Register

Note : Do not execute RMW instructions on registers having a write-only bit.

RMW instructions (RMW : Read Modify Write)

AND	Rj, @Ri	OR	Rj, @Ri	EOR	Rj, @Ri
ANDH	Rj, @Ri	ORH	Rj, @Ri	EORH	Rj, @Ri
ANDB	Rj, @Ri	ORB	Rj, @Ri	EORB	Rj, @Ri
BANDL	#u4, @Ri	BORL	#u4, @Ri	BEORL	#u4, @Ri
BANDH	#u4, @Ri	BORH	#u4, @Ri	BEORH	#u4, @Ri

Data is undefined in “Reserved” or (—) areas.

( ) :	Access	W :	Write only
R/W :	Read/Write enabled	— :	Not in use
R :	Read only	X :	Undefined

■ INTERRUPT FACTORS AND ASSIGNMENT OF INTERRUPT VECTORS AND RESISTERS

Factor	Interrupt No.		Interrupt level	Offset	Default TBR address
	Decimal	Hex.			
Reset	0	00	—	$3FC_H$	$000FFFFC_H$
Reserved for the system	1	01	—	$3F8_H$	$000FFFF8_H$
Reserved for the system	2	02	—	$3F4_H$	$000FFFF4_H$
Reserved for the system	3	03	—	$3F0_H$	$000FFFF0_H$
Reserved for the system	4	04	—	$3EC_H$	$000FFFEC_H$
Reserved for the system	5	05	—	$3E8_H$	$000FFFE8_H$
Reserved for the system	6	06	—	$3E4_H$	$000FFFE4_H$
Reserved for the system	7	07	—	$3E0_H$	$000FFFE0_H$
Reserved for the system	8	08	—	$3DC_H$	$000FFFDC_H$
Reserved for the system	9	09	—	$3D8_H$	$000FFFD8_H$
Reserved for the system	10	0A	—	$3D4_H$	$000FFFD4_H$
Reserved for the system	11	0B	—	$3D0_H$	$000FFFD0_H$
Reserved for the system	12	0C	—	$3CC_H$	$000FFFCC_H$
Reserved for the system	13	0D	—	$3C8_H$	$000FFFC8_H$
Undefined instruction exception	14	0E	—	$3C4_H$	$000FFFC4_H$
Reserved for the system	15	0F	—	$3C0_H$	$000FFFC0_H$
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$
External interrupt 4	20	14	ICR04	$3AC_H$	$000FFFAC_H$
External interrupt 5	21	15	ICR05	$3A8_H$	$000FFFA8_H$
External interrupt 6	22	16	ICR06	$3A4_H$	$000FFFA4_H$
External interrupt 7	23	17	ICR07	$3A0_H$	$000FFFA0_H$
External interrupts 8 to 15	24	18	ICR08	$39C_H$	$000FFF9C_H$
Reserved for the system	25	19	—	398_H	$000FFF98_H$
UART0 (receiving complete)	26	1A	ICR10	394_H	$000FFF94_H$
UART1 (receiving complete)	27	1B	ICR11	390_H	$000FFF90_H$
UART2 (receiving complete)	28	1C	ICR12	$38C_H$	$000FFF8C_H$
UART3 (receiving complete)	29	1D	ICR13	388_H	$000FFF88_H$
Reserved for the system	30	1E	—	384_H	$000FFF84_H$
UART0 (sending complete)	31	1F	ICR15	380_H	$000FFF80_H$
UART1 (sending complete)	32	20	ICR16	$37C_H$	$000FFF7C_H$
UART2 (sending complete)	33	21	ICR17	378_H	$000FFF78_H$

(Continued)

Factor	Interrupt No.		Interrupt level	Offset	Default TBR address
	Decimal	Hex.			
UART3 (sending complete)	34	22	ICR18	374H	000FFF74H
System reservation	35	23	—	370H	000FFF70H
DMAC (End, Error)	36	24	ICR20	36CH	000FFF6CH
Reload timer 0	37	25	ICR21	368H	000FFF68H
Reload timer 1	38	26	ICR22	364H	000FFF64H
Reload timer 2	39	27	ICR23	360H	000FFF60H
Reload timer 3	40	28	ICR24	35CH	000FFF5CH
A/D (sequential type)	42	2A	ICR26	354H	000FFF54H
PPG0	43	2B	ICR27	350H	000FFF50H
PPG1	44	2C	ICR28	34CH	000FFF4CH
PPG2	45	2D	ICR29	348H	000FFF48H
PPG3	46	2E	ICR30	344H	000FFF44H
PPG4	47	2F	ICR31	340H	000FFF40H
PPG5	48	30	ICR32	33CH	000FFF3CH
U/Dcounter 0 (compare/underflow, overflow, up-down inversion)	49	31	ICR33	338H	000FFF38H
U/Dcounter 1 (compare/underflow, overflow, up-down inversion	50	32	ICR34	334H	000FFF34H
ICU0 (Read)	51	33	ICR35	330H	000FFF30H
ICU1 (Read)	52	34	ICR36	32CH	000FFF2CH
ICU2 (Read)	53	35	ICR37	328H	000FFF28H
ICU3 (Read)	54	36	ICR38	324H	000FFF24H
OCU0 (Match)	55	37	ICR39	320H	000FFF20H
OCU1 (Match)	56	38	ICR40	31CH	000FFF1CH
OCU2 (Match)	57	39	ICR41	318H	000FFF18H
OCU3 (Match)	58	3A	ICR42	314H	000FFF14H
OCU4/5 (Match)	59	3B	ICR43	310H	000FFF10H
OCU6/7 (Match)	60	3C	ICR44	30CH	000FFF0CH
Reserved for the system	61	3D	—	308H	000FFF08H
16-bit free-run timer	62	3E	ICR46	304H	000FFF04H
Delay interrupt factor bit	63	3F	ICR47	300H	000FFF00H

(Continued)

(Continued)

Factor	Interrupt No.		Interrupt level	Offset	Default TBR address
	Decimal	Hex.			
Reserved for the system (used by REALOS*)	64	40	—	$2FC_H$	$000FFEFC_H$
Reserved for the system (used by REALOS*)	65	41	—	$2F8_H$	$000FFEF8_H$
Reserved for the system	66	42	—	$2F4_H$	$000FFEF4_H$
Reserved for the system	67	43	—	$2F0_H$	$000FFEF0_H$
Reserved for the system	68	44	—	$2EC_H$	$000FFEEC_H$
Reserved for the system	69	45	—	$2E8_H$	$000FFEE8_H$
Reserved for the system	70	46	—	$2E4_H$	$000FFEE4_H$
Reserved for the system	71	47	—	$2E0_H$	$000FFEE0_H$
Reserved for the system	72	48	—	$2DC_H$	$000FFEDC_H$
Reserved for the system	73	49	—	$2D8_H$	$000FFED8_H$
Reserved for the system	74	4A	—	$2D4_H$	$000FFED4_H$
Reserved for the system	75	4B	—	$2D0_H$	$000FFED0_H$
Reserved for the system	76	4C	—	$2CC_H$	$000FFECC_H$
Reserved for the system	77	4D	—	$2C8_H$	$000FFEC8_H$
Reserved for the system	78	4E	—	$2C4_H$	$000FFEC4_H$
Reserved for the system	79	4F	—	$2C0_H$	$000FFEC0_H$
Used with the INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$

* : REALOS/FR uses 0X40 and 0X41 interrupts for system codes.

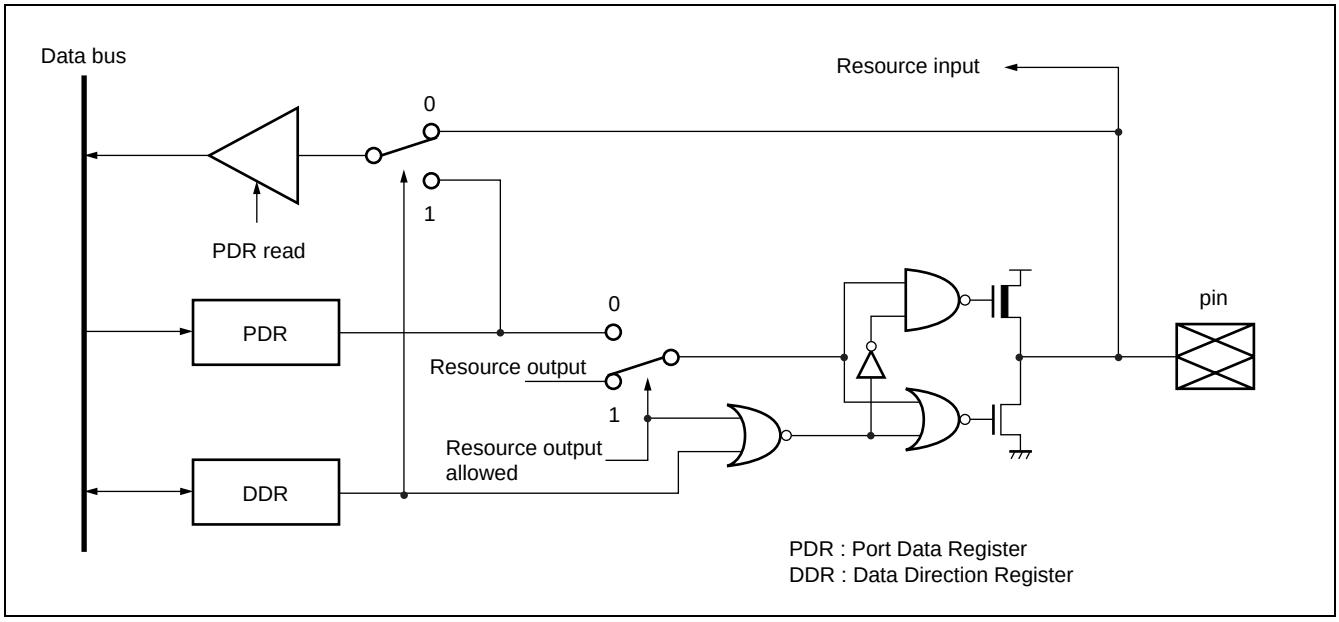
■ PERIPHERAL RESOURCES

1. I/O Port

(1) Port Block Diagram

This LSI is available as an I/O port when the resource associated with each pin is set not to use a pin for input/output.
The pin level is read from the port (PDR) when it is set for input. When the port is set for output, the value in the data register is read. The same also applies to reload by read modify write.
When switching from input to output, output data is set in the data register beforehand. However, if a read modify write instruction (such as bit set) is used at that time, keep in mind that it is the input data from the pin that is read, not the latch value of the data register.

- **Basic I/O Port**

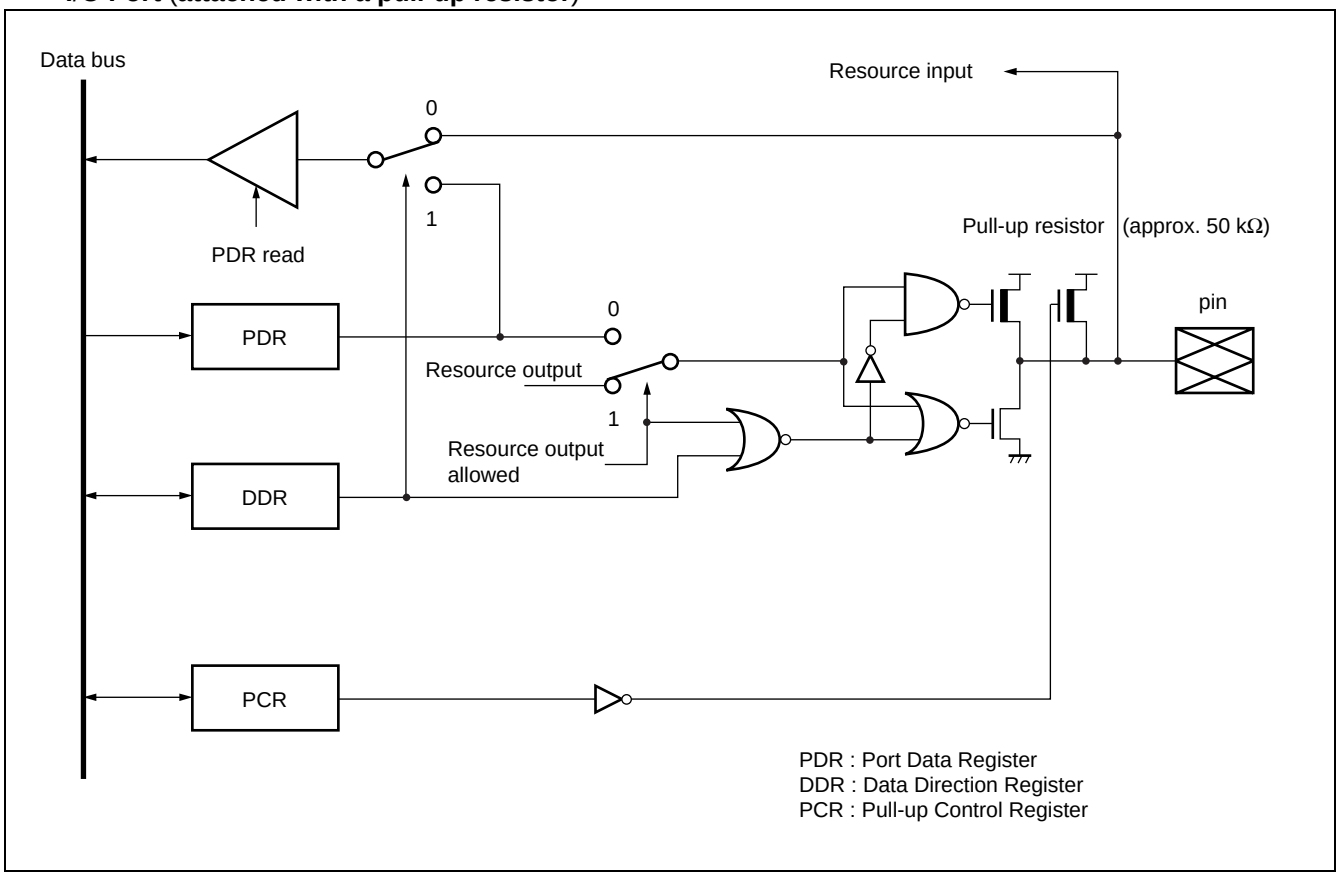


The I/O port consists of the PDR (Port Data Register) and the DDR (Data Direction Register) .

In input mode (DDR = “0”)	→	PDR read :	Reads the level of the corresponding external pin.
		PDR write :	Writes the set value to the PDR.
In output mode (DDR = “1”)	→	PDR read :	Reads the PDR value.
		PDR write :	Outputs the PDR value to the corresponding external pin.

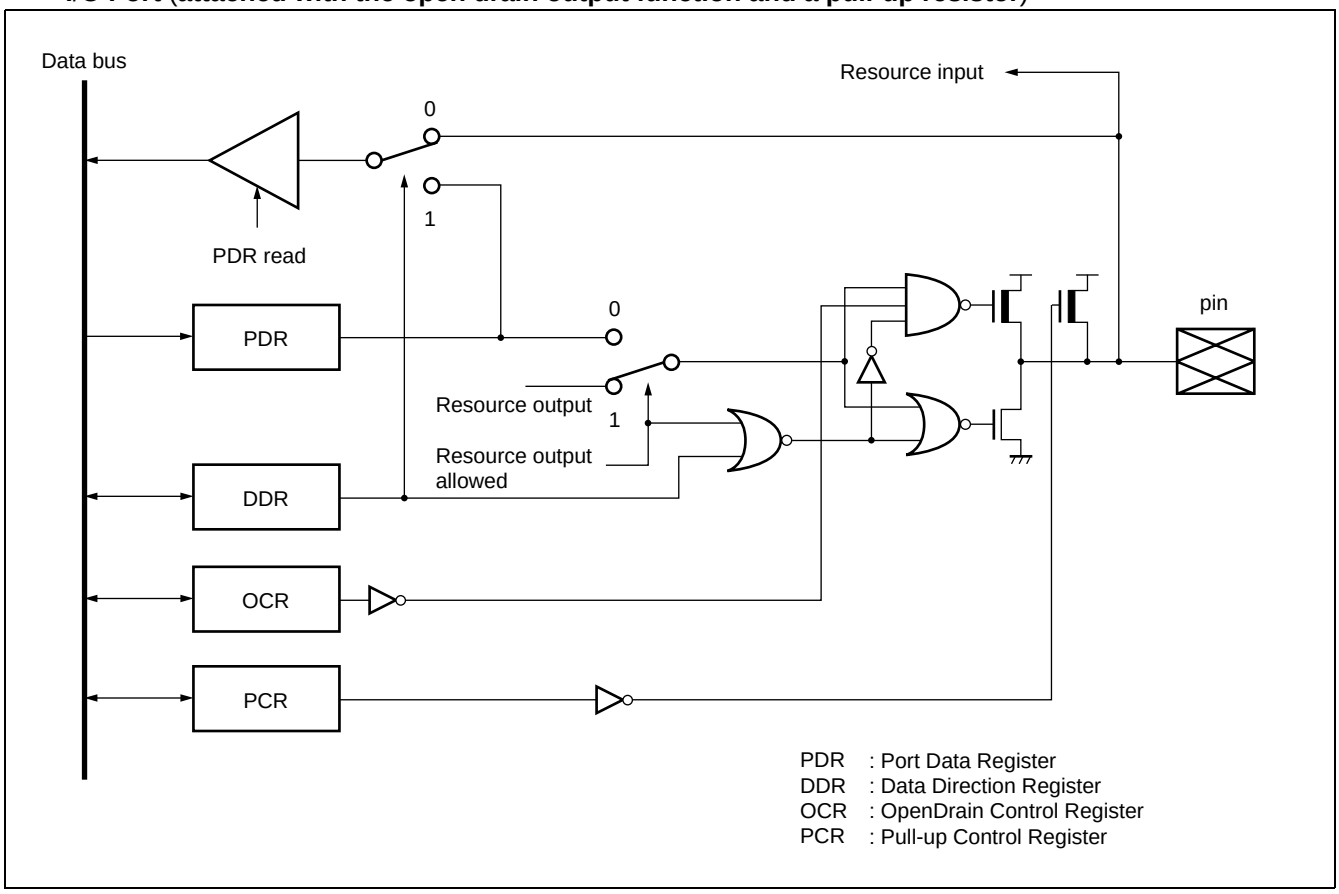
Notes : AIC controls switching between the resource and port of the analog pin (A/D) .
AICK (Analog Input Control register on port-K)
The register controls whether port K should be used for analog input or as a general-purpose port.
0 : General-purpose port
1 : Analog input (A/D)

• **I/O Port** (**attached with a pull-up resistor**)



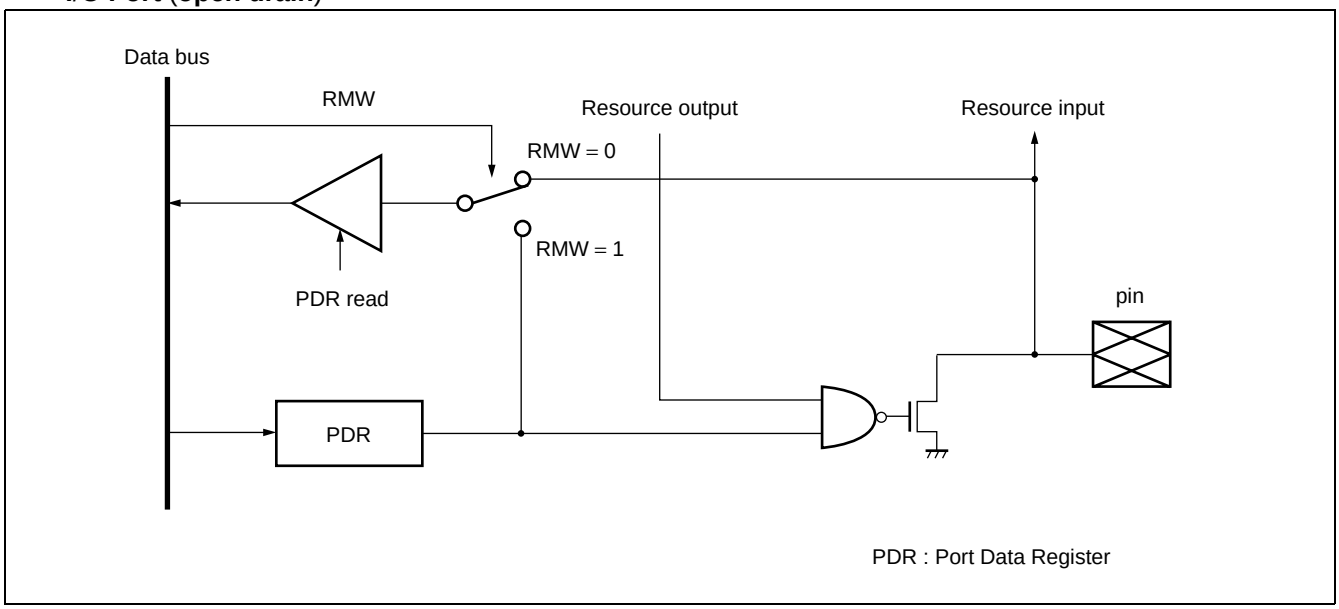
Notes : • Pull-up resistor control register (PCR) R/W
Controls turning the pull-up resistor on/off.
0 : Pull-up resistor disabled
1 : Pull-up resistor enabled
• In stop mode priority is also given to the setting of the pull-up resistor control register.
• This function is not available when a relevant pin is in use as an external bus pin. Do not write “1” to this register.

• **I/O Port** (**attached with the open drain output function and a pull-up resistor**)



Notes : • Pull-up resistor setup register (PCR) R/W
Controls turning the pull-up resistor on/off.
0 : Pull-up resistor disabled
1 : Pull-up resistor enabled
• Open drain control register (OCR) R/W
Controls open drain in output mode.
0 : Standard output port during output mode
1 : Open-drain output port during output mode
This register has no significance in input mode (output High-Z) . Input/output mode is determined by the direction register (DDR) .
• Priority is also given to the setting of the pull-up resistor control register in stop mode.
• When a relevant pin is used as an external bus pin, neither function is available. Do not write “1” to either register.

- **I/O Port** (**open drain**)



Notes : • When using as an input port or for resource input, set the PDR and resource output to “1.”
• During read by RMW, it is the PDR value that is read, not the pin value.

(2) Register Descriptions

- **Port Data Register (PDR)**

	7	6	5	4	3	2	1	0	Initial value	Access
PDR2 Address : 000001H	P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXXB	R/W
PDR3 Address : 000000H	P37	P36	P35	P34	P33	P32	P31	P30	XXXXXXXXB	R/W
PDR4 Address : 000007H	P47	P46	P45	P44	P43	P42	P41	P40	XXXXXXXXB	R/W
PDR5 Address : 000006H	P57	P56	P55	P54	P53	P52	P51	P50	XXXXXXXXB	R/W
PDR6 Address : 000005H	P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXXB	R/W
PDR8 Address : 00000BH	—	P86	P85	P84	P83	P82	P81	P80	- XXXXXXXB	R/W
PDRC Address : 000013H	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	XXXXXXXXB	R/W
PDRD Address : 000012H	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	XXXXXXXXB	R/W
PDRE Address : 000011H	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	XXXXXXXXB	R/W
PDRF Address : 000010H	—	—	—	PF4	PF3	PF2	PF1	PF0	- - - XXXXXB	R/W
PDRG Address : 000017H	—	—	PG5	PG4	PG3	PG2	PG1	PG0	- - XXXXXXB	R/W
PDRH Address : 000016H	—	—	PH5	PH4	PH3	PH2	PH1	PH0	- - XXXXXXB	R/W
PDRI Address : 000015H	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - XXXXXXB	R/W
PDRJ Address : 000014H	—	—	—	—	—	—	PJ1	PJ0	- - - - - - 11B	R/W
PDRK Address : 00001BH	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	XXXXXXXXB	R/W
PDRL Address : 00001AH	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	XXXXXXXXB	R/W

PDR2 to PDRL are the I/O data registers of the I/O port.
Input/output is controlled with corresponding DDR2 to DDRL.
R/W : Read/Write enabled, X : Undefined, — : Not in use

- **Data Direction Register (DDR)**

	7	6	5	4	3	2	1	0	Initial value	Access
DDR2 Address : 000601H	P27	P26	P25	P24	P23	P22	P21	P20	00000000B	W
DDR3 Address : 000600H	P37	P36	P35	P34	P33	P32	P31	P30	00000000B	W
DDR4 Address : 000607H	P47	P46	P45	P44	P43	P42	P41	P40	00000000B	W
DDR5 Address : 000606H	P57	P56	P55	P54	P53	P52	P51	P50	00000000B	W
DDR6 Address : 000605H	P67	P66	P65	P64	P63	P62	P61	P60	00000000B	W
DDR8 Address : 00060BH	—	P86	P85	P84	P83	P82	P81	P80	- 0000000B	W
DDRC Address : 0000FFH	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	00000000B	R/W
DDRD Address : 0000FEH	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00000000B	R/W
DDRE Address : 0000FDH	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	00000000B	R/W
DDRF Address : 0000FCH	—	—	—	PF4	PF3	PF2	PF1	PF0	- - - 00000B	R/W
DDRG Address : 000103H	—	—	PG5	PG4	PG3	PG2	PG1	PG0	- - 000000B	R/W
DDRH Address : 000102H	—	—	PH5	PH4	PH3	PH2	PH1	PH0	- - 000000B	R/W
DDRI Address : 000101H	—	TEST	PI5	PI4	PI3	PI2	PI1	PI0	- 0000000B	R/W
DDRK Address : 000107H	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W
DDRL Address : 000106H	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000B	R/W

DDR2 to DDRL control the I/O direction of the I/O port by bit.
DDR = 0 : Port input
DDR = 1 : Port output

Note : DDRI's bit 6 is a test bit. Be sure to write "0" to the bit.
"0" is the value that is read.

R/W : Read/Write enabled, W : Write only, — : Not in use

• **Pull-up Control Register** (**PCR**)

PCR6

Address : 000631H	7	6	5	4	3	2	1	0	Initial value	Access
	P67	P66	P65	P64	P63	P62	P61	P60	00000000B	R/W

PCRC

Address : 0000F7H	7	6	5	4	3	2	1	0	Initial value	Access
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	00000000B	R/W

PCRD

Address : 0000F6H	7	6	5	4	3	2	1	0	Initial value	Access
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00000000B	R/W

PCRH

Address : 0000F5H	7	6	5	4	3	2	1	0	Initial value	Access
	—	—	PH5	PH4	PH3	PH2	PH1	PH0	- - 000000B	R/W

PCRI

Address : 0000F4H	7	6	5	4	3	2	1	0	Initial value	Access
	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - 000000B	R/W

PCR6 to PCRI control the pull-up resistor when the corresponding I/O port is in input mode.
PCR = 0 : Pull-up resistor not available in input mode
PCR = 1 : Pull-up resistor available in input mode
The register has no significance in output mode (a pull-up resistor not available) .

• **Open Drain Control Register** (**OCR**)

OCRH

Address : 0000F9H	7	6	5	4	3	2	1	0	Initial value	Access
	—	—	PH5	PH4	PH3	PH2	PH1	PH0	- - 000000B	R/W

OCRI

Address : 0000F8H	7	6	5	4	3	2	1	0	Initial value	Access
	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - 000000B	R/W

OCRH and OCRI control open drain when the corresponding I/O port is in output mode.
OCR = 0 : Standard output port during output mode
OCR = 1 : Open drain output port during output mode
The register has no significance in input mode (output High-Z) .

• **Analog Input Control Register** (**AICR**)

AICK

Address : 0000EBH	7	6	5	4	3	2	1	0	Initial value	Access
	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W

The AICK controls each pin of a corresponding I/O port as follows :
AIC = 0 : Port input mode
AIC = 1 : Analog input mode
The register is reset to “0.”

R/W : Read/Write enabled, — : Not in use

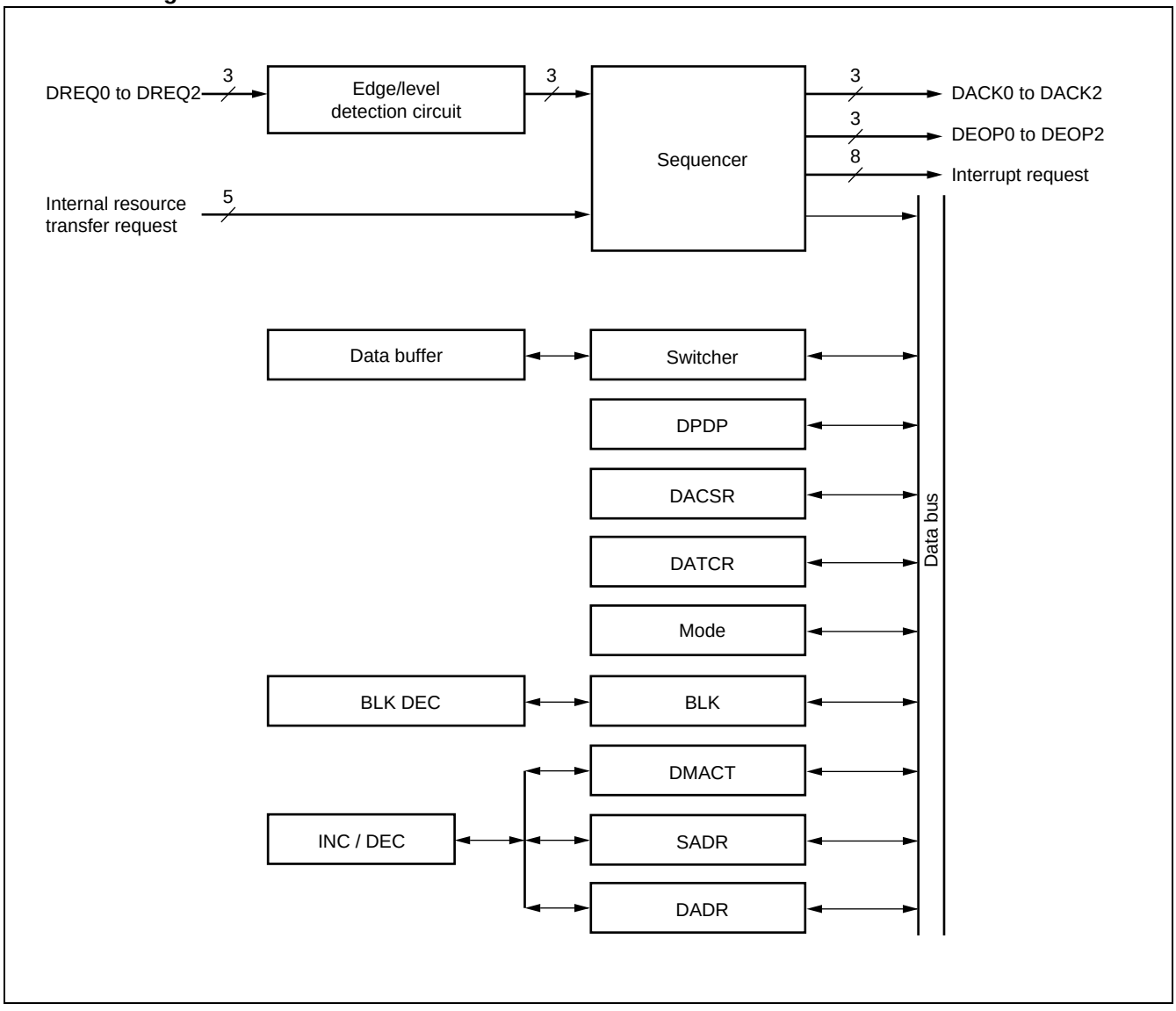
2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

- 8 channels
- Mode : single/block transfer, burst transfer and continuous transfer : 3 kinds of transfer
- Transfer all through the area
- Max 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

- **Block Diagram**

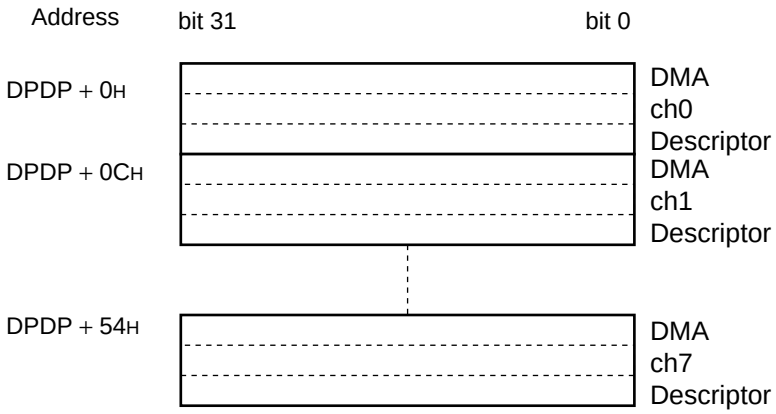


- **Registers** (**DMAC internal registers**)

Address	bit 31	bit 16	bit 0	Initial value	Access
00000200H	DPDP			XXXXXXXXB	R/W
00000201H				XXXXXXXXB	
00000202H				XXXXXXXXB	
00000203H				X0000000B	
00000204H	DACSR			00000000B	R/W
00000205H				00000000B	
00000206H				00000000B	
00000207H				00000000B	
00000208H	DATCR			XXXXXXXXB	R/W
00000209H				XXXX0000B	
0000020AH				XXXX0000B	
0000020BH				XXXX0000B	

R/W : Read/Write enabled
X : Undefined

- **Register** (**DMA descriptor**)

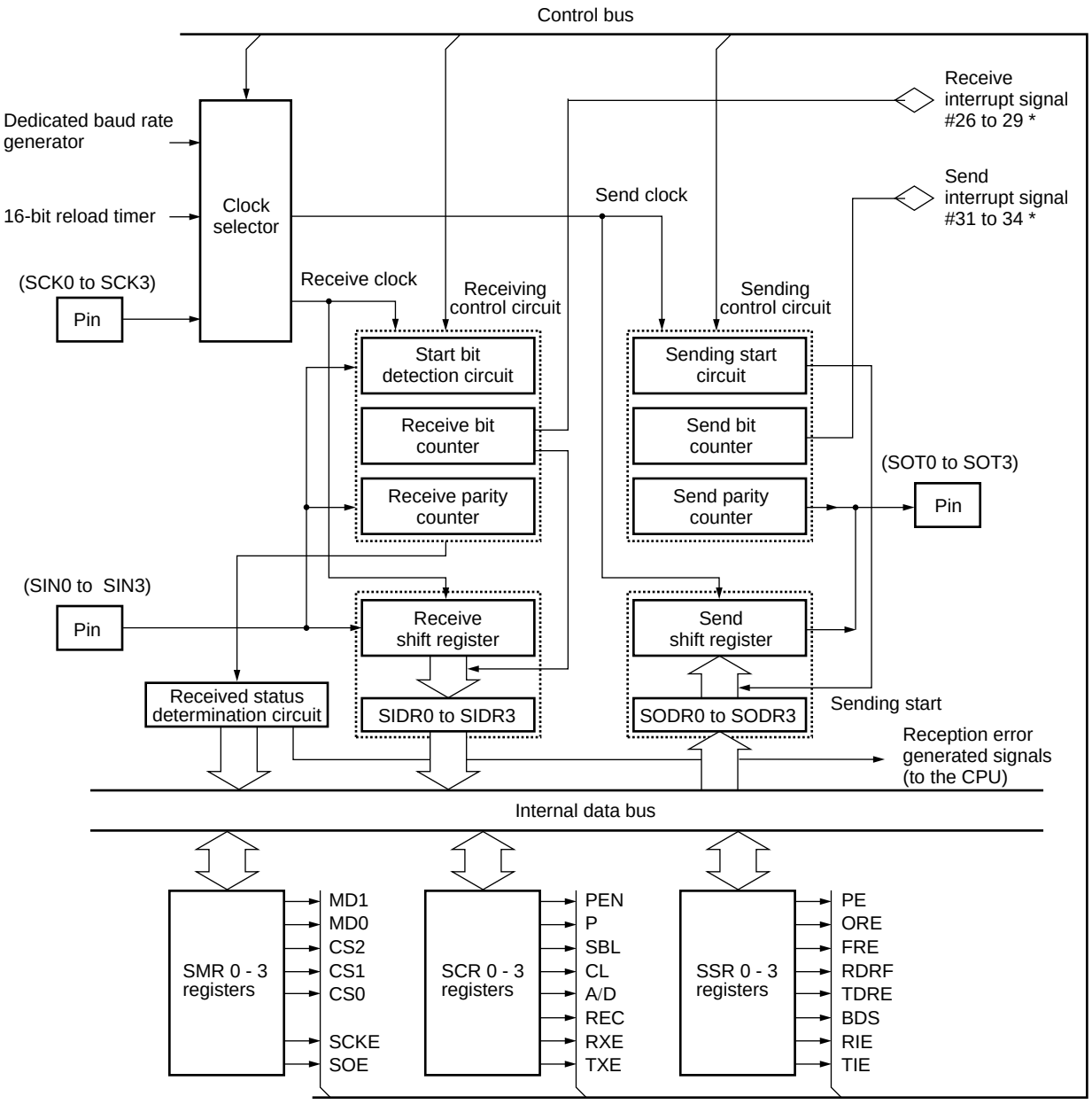


3. UART

The UART is a serial I/O port for asynchronous (start and stop synchronization) communication or CLK synchronous communication. This product type contains this UART for four channels. Its features are as follows :

- Full-duplex double buffer
- Capable of asynchronous (start and stop synchronization) and CLK synchronous communication.
- Support for multiprocessor mode
- Baud rate by a dedicated baud rate generator
- Baud rate by an internal timer
  The baud rate can be set with a 16-bit reload timer.
- Any baud rate can be set using an external clock.
- Error detection function (parity, framing, and overrun)
- NRZ-encoded transfer signals
- DMA transfer can be invoked by interrupt.

- **Block Diagram**



* : Interrupt numbers

- **Register List**

Address	bit 15	bit 8	bit 0	Initial value	Access
0000001EH	SCR0			00000100B	R/W, W
00000022H	SCR1			00000100B	R/W, W
00000026H	SCR2			00000100B	R/W, W
0000002AH	SCR3			00000100B	R/W, W
0000001FH	SMR0			00000-00B	R/W
00000023H	SMR1			00000-00B	R/W
00000027H	SMR2			00000-00B	R/W
0000002BH	SMR3			00000-00B	R/W
0000001CH	SSR0			00001000B	R, R/W
00000020H	SSR1			00001000B	R, R/W
00000024H	SSR2			00001000B	R, R/W
00000028H	SSR3			00001000B	R, R/W
0000001DH	SIDR0/SODR0			XXXXXXXXB	R, W
00000021H	SIDR1/SIDR1			XXXXXXXXB	R, W
00000025H	SIDR2/SIDR2			XXXXXXXXB	R, W
00000029H	SIDR3/SIDR3			XXXXXXXXB	R, W

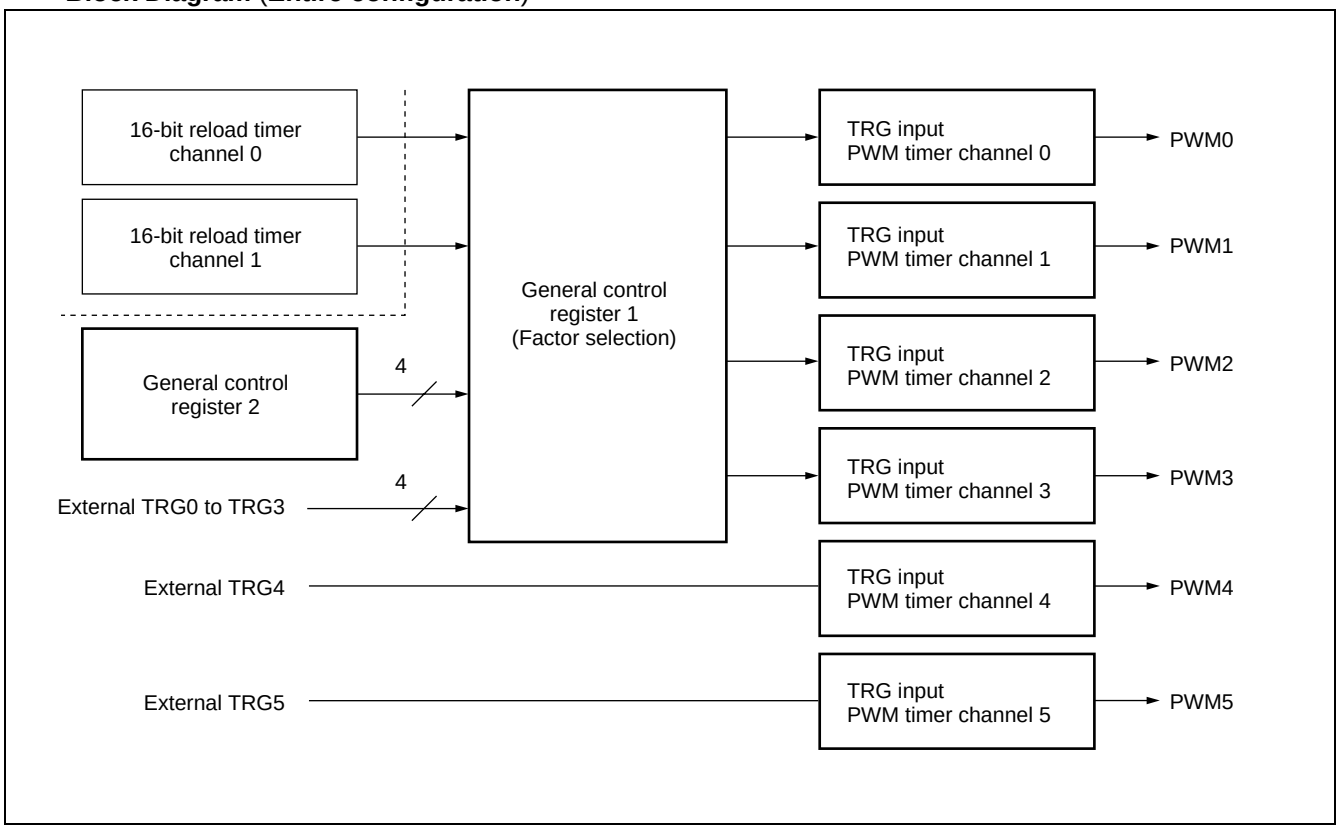
R/W : Read/Write enabled
R : Read only
W : Write only
— : Not in use
X : Undefined

4. PPG Timer

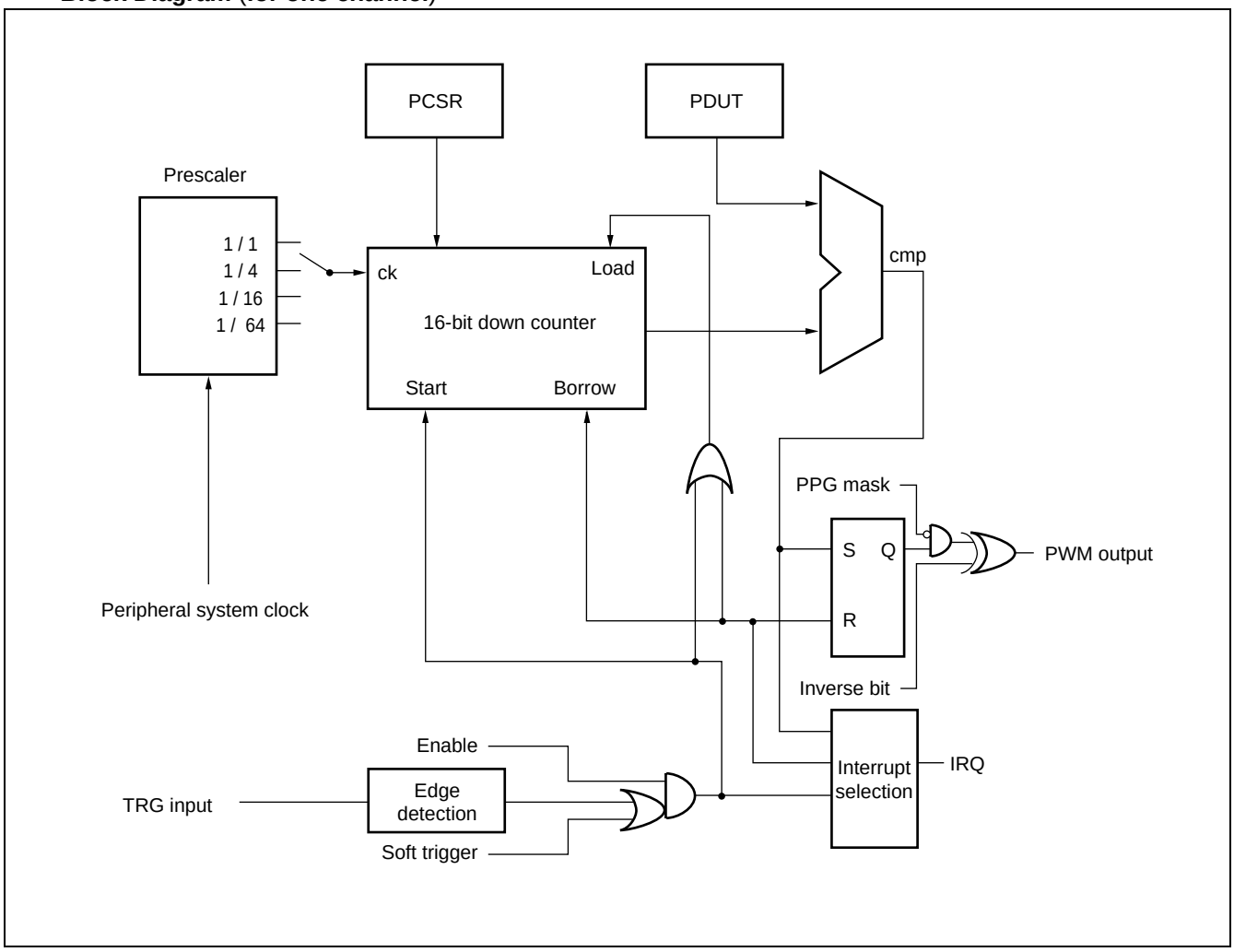
The PPG timer can output highly accurate PWM waveforms efficiently.
The MB91151A contains six PPG timer channels and its features are as follows :

- Each channel consists of a 16-bit down counter, a 16-bit data register attached with a frequency setting buffer, a 16-bit compare register attached with a duty setting buffer, and a pin controller.
- The count clock for the 16-bit down counter can be selected from the following four types :
  Internal clocks ϕ, ϕ/4, ϕ/16, and ϕ/64
- The counter value can be initialized by reset or counter borrow to "$FFFF_H$."
- PWM output (by channel)
- DMA transfer can be invoked by interrupt.

- **Block Diagram** (**Entire configuration**)



- **Block Diagram (for one channel)**



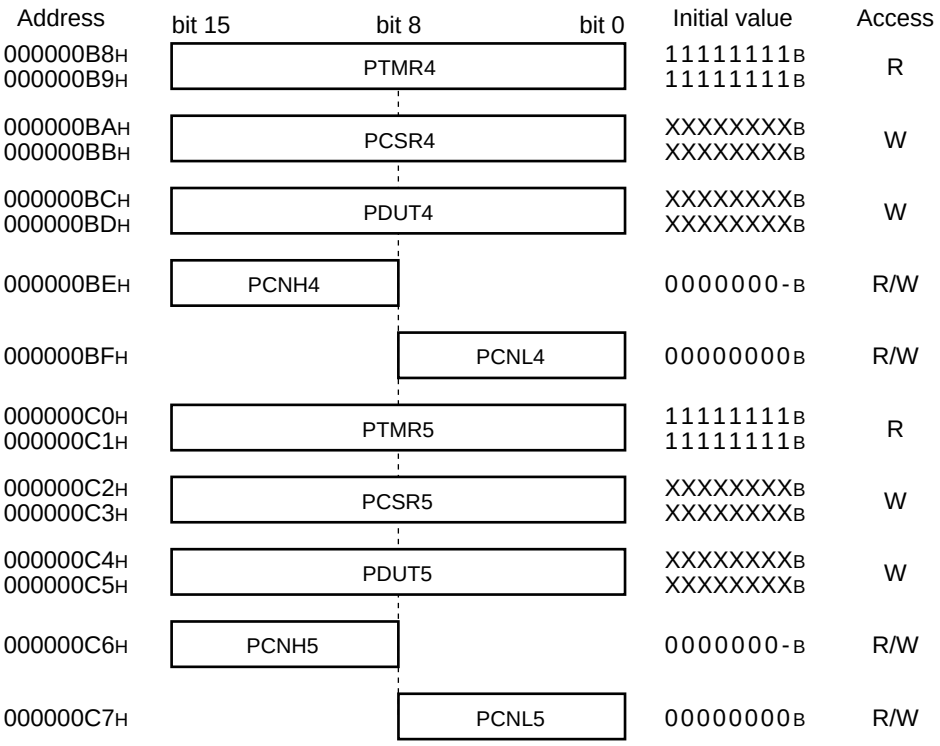
- **Register List**

Address	bit 15	bit 8	bit 0	Initial value	Accress
00000094H 00000095H	GCN1			00110010B 00010000B	R/W
00000097H		GCN2		00000000B	R/W
00000098H 00000099H	PTMR0			11111111B 11111111B	R
0000009AH 0000009BH	PCSR0			XXXXXXXXB XXXXXXXXB	W
0000009CH 0000009DH	PDUT0			XXXXXXXXB XXXXXXXXB	W
0000009EH	PCNH0			0000000-B	R/W
0000009FH		PCNL0		00000000B	R/W
000000A0H 000000A1H	PTMR1			11111111B 11111111B	R
000000A2H 000000A3H	PCSR1			XXXXXXXXB XXXXXXXXB	W
000000A4H 000000A5H	PDUT1			XXXXXXXXB XXXXXXXXB	W
000000A6H	PCNH1			0000000-B	R/W
000000A7H		PCNL1		00000000B	R/W
000000A8H 000000A9H	PTMR2			11111111B 11111111B	R
000000AAH 000000ABH	PCSR2			XXXXXXXXB XXXXXXXXB	W
000000ACH 000000ADH	PDUT2			XXXXXXXXB XXXXXXXXB	W
000000AEH	PCNH2			0000000-B	R/W
000000AFH		PCNL2		00000000B	R/W
000000B0H 000000B1H	PTMR3			11111111B 11111111B	R
000000B2H 000000B3H	PCSR3			XXXXXXXXB XXXXXXXXB	W
000000B4H 000000B5H	PDUT3			XXXXXXXXB XXXXXXXXB	W
000000B6H	PCNH3			0000000-B	R/W
000000B7H		PCNL3		00000000B	R/W

R/W : Read/Write enabled R : Read only W : Write only — : Not in use X : Undefined

(Continued)

(Continued)

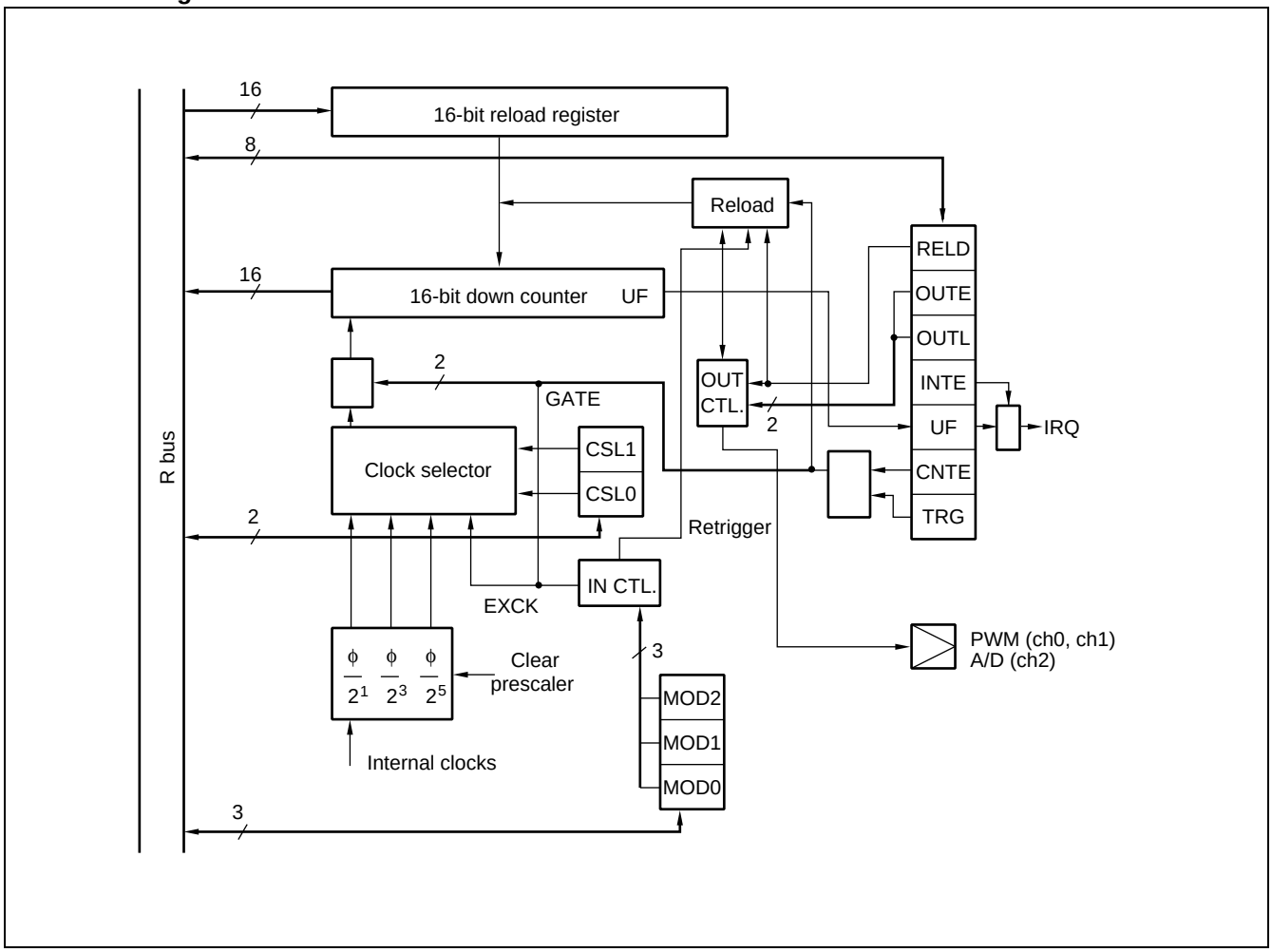


R/W : Read/Write enabled R : Read only
W : Write only — : Not in use
X : Undefined

5. 16-bit Reload Timer

The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload register, a prescaler for creating internal count clocks, and a control register.
The input clock can be selected from three internal clock types (2/8/32 machine clock divisions) .
DMA transfer can be invoked by interrupt.
This product type contains this 16-bit reload timer for four channels.

- **Block Diagram**



- **Register List**

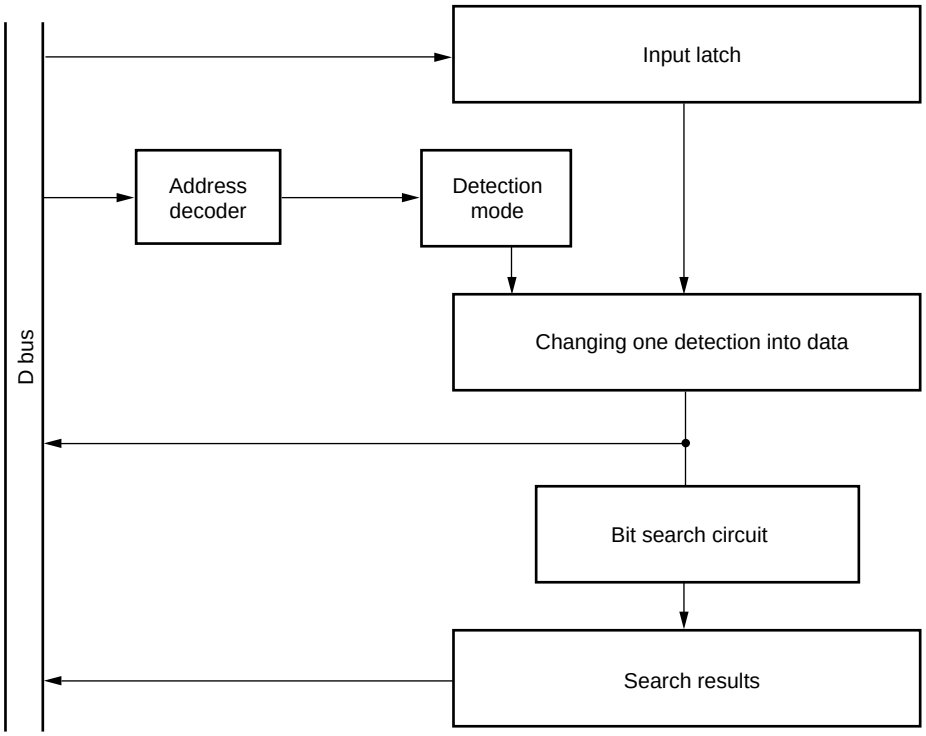
Address	bit 15 — bit 0	Initial value	Access
00000032H 00000033H	TMCSR0	----0000B 00000000B	R/W
0000003AH 0000003BH	TMCSR1	----0000B 00000000B	R/W
00000042H 00000043H	TMCSR2	----0000B 00000000B	R/W
0000004AH 0000004BH	TMCSR3	----0000B 00000000B	R/W
0000002EH 0000002FH	TMR0	XXXXXXXXB XXXXXXXXB	R
00000036H 00000037H	TMR1	XXXXXXXXB XXXXXXXXB	R
0000003EH 0000003FH	TMR2	XXXXXXXXB XXXXXXXXB	R
00000046H 00000047H	TMR3	XXXXXXXXB XXXXXXXXB	R
0000002CH 0000002DH	TMRLR0	XXXXXXXXB XXXXXXXXB	W
00000034H 00000035H	TMRLR1	XXXXXXXXB XXXXXXXXB	W
0000003CH 0000003DH	TMRLR2	XXXXXXXXB XXXXXXXXB	W
00000044H 00000045H	TMRLR3	XXXXXXXXB XXXXXXXXB	W

R/W : Read/Write enabled
R : Read only
W : Write only
— : Not in use
X : Undefined

6. Bit Search Module

The module searches data written to the input register for “0” or “1” or a “change” and returns the detected bit position.

- **Block Diagram**



- **Register List**

Address	bit 31	bit 16	bit 0	Initial value	Access
000003F0H	BSD0			XXXXXXXXB	W
000003F1H				XXXXXXXXB	
000003F2H				XXXXXXXXB	
000003F3H				XXXXXXXXB	
000003F4H	BSD1			XXXXXXXXB	R/W
000003F5H				XXXXXXXXB	
000003F6H				XXXXXXXXB	
000003F7H				XXXXXXXXB	
000003F8H	BSDC			XXXXXXXXB	W
000003F9H				XXXXXXXXB	
000003FAH				XXXXXXXXB	
000003FBH				XXXXXXXXB	
000003FCH	BSRR			XXXXXXXXB	R
000003FDH				XXXXXXXXB	
000003FEH				XXXXXXXXB	
000003FFH				XXXXXXXXB	

R/W : Read/Write enabled R : Read only
W : Write only X : Undefined

7. 8/10-bit A/D Converter (Sequential Conversion Type)

The A/D converter is a module that converts analog input voltage into a digital value. Its features are as follows :

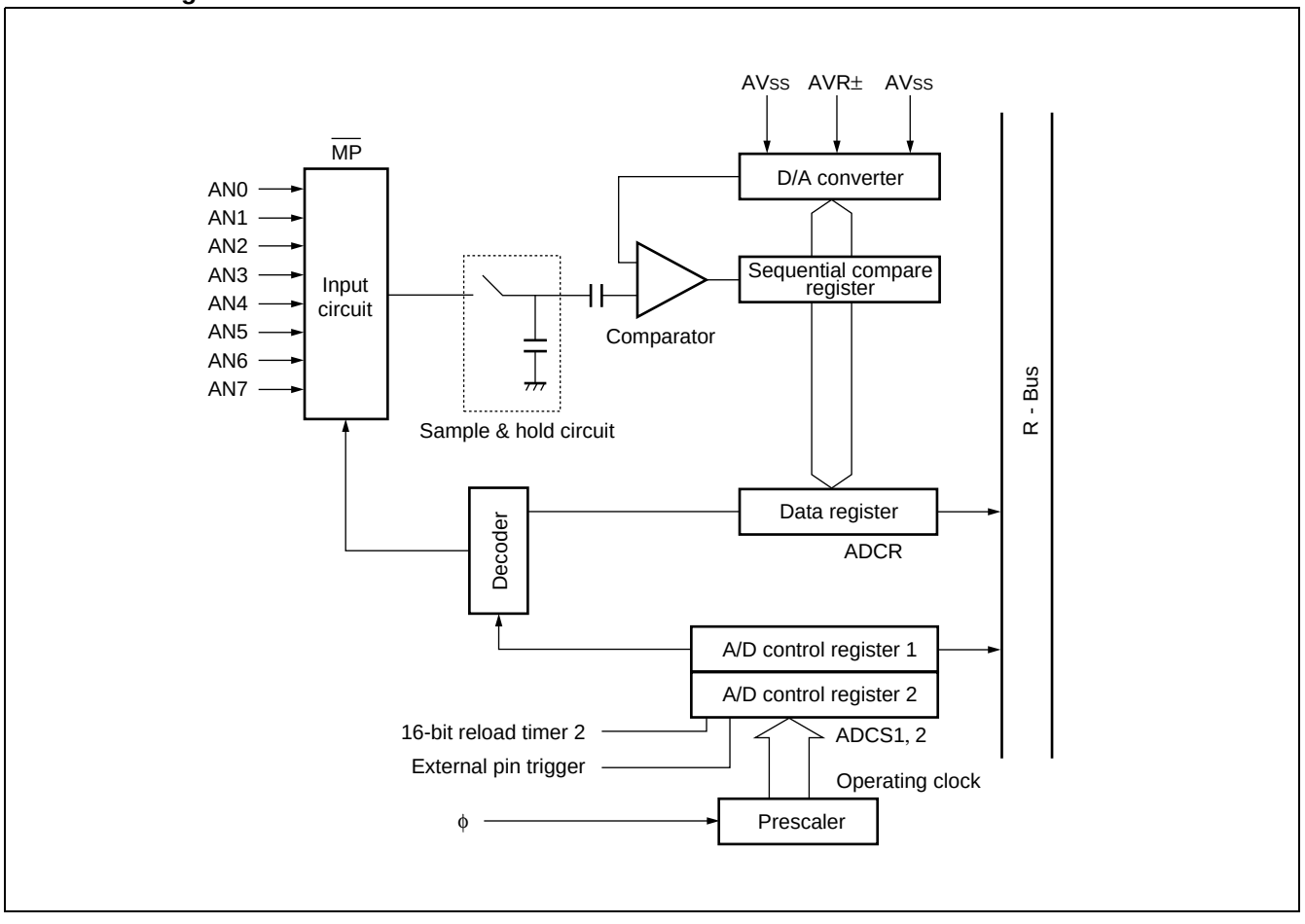
- A minimum conversion time of 5.0 µs/ch. (Including sampling time at a 33 MHz machine clock)
- Contains a sample and hold circuit.
- Resolution : 10 or 8 bits selectable.
- Selection of analog input from eight channels by program

  Single conversion mode : Selects and converts one channel.

  Continuous conversion mode : Converts a specified channel repeatedly.

  Stop and convert mode : Stops after converting one channel and stands by until invoked the next time. (Conversion invoking can be synchronized.)
- DMA transfer can be invoked by interrupt.
- Selection of an invoking factor from software, external pin trigger (falling edge) , and 16-bit reload timer (rising edge) .

- **Block Diagram**



- **Register List**

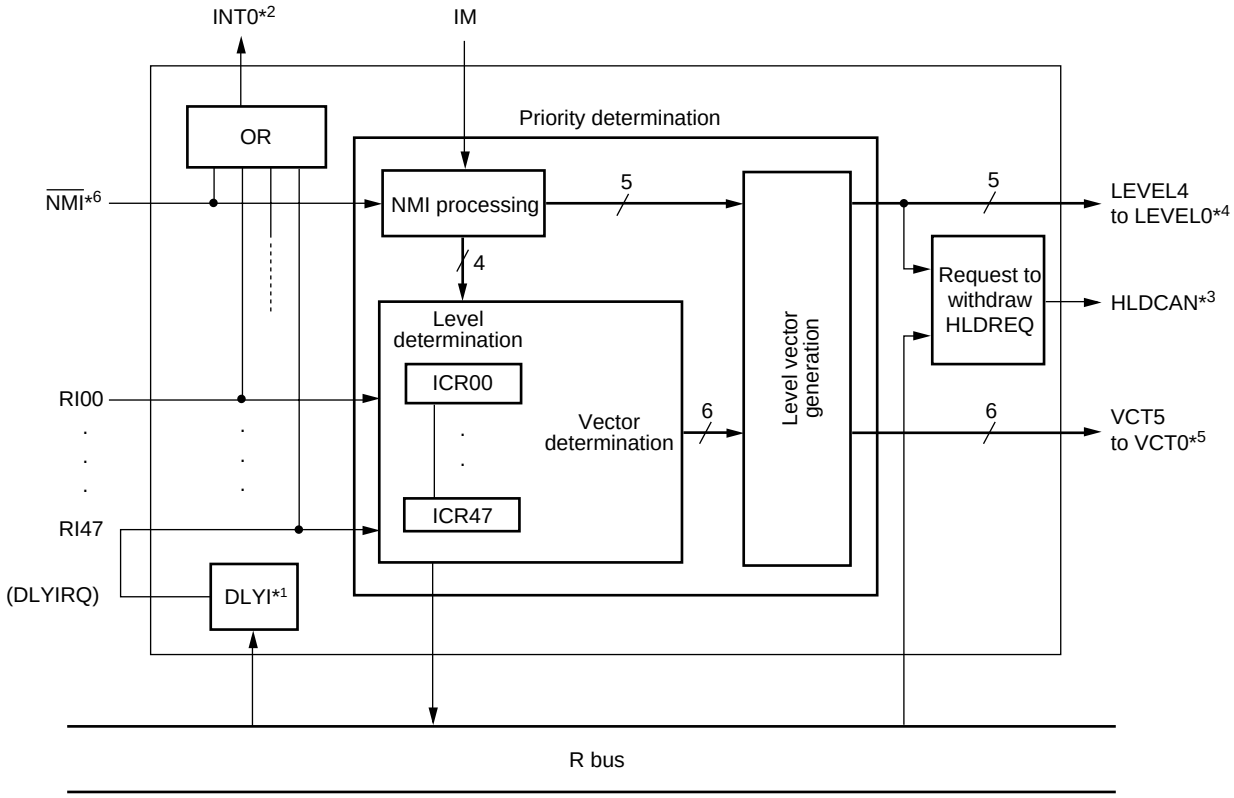
Address	bit 15		bit 0	Initial value	Access
000000E4H	ADCR			00101-XXB	W, R
000000E5H				XXXXXXXXB	R
000000E6H	ADCS1			00000000B	R/W, W
000000E7H		ADCS0		00000000B	R/W
000000EBH		AICK		00000000B	R/W

R/W : Read/Write enabled
R : Read only
W : Write only
— : Not in use
X : Undefined

8. Interrupt Controller

The interrupt controller accepts and arbitrates interrupts.

- **Block Diagram**



*1 : DLY1 represents the delay interrupt module (delay interrupt generator) . For detailed information, see “10. Delay Interrupt Module.”

*2 : INT0 is a wake-up signal for the clock controller in sleep or stop mode.

*3 : HLDCAN is a bus surrender request signal for bus masters except for the CPU.

*4 : LEVEL 4 to LEVEL 0 are interrupt level outputs.

*5 : VCT 5 to VCT 0 are interrupt vector outputs.

*6 : This product type does not have the NMI function.

• **Register List**

Address	bit 7 bit 0	Initial value	Access	Address	bit 7 bit 0	Initial value	Access
00000400H	ICR00	----1111B	R/W	00000414H	ICR20	----1111B	R/W
00000401H	ICR01	----1111B	R/W	00000415H	ICR21	----1111B	R/W
00000402H	ICR02	----1111B	R/W	00000416H	ICR22	----1111B	R/W
00000403H	ICR03	----1111B	R/W	00000417H	ICR23	----1111B	R/W
00000404H	ICR04	----1111B	R/W	00000418H	ICR24	----1111B	R/W
00000405H	ICR05	----1111B	R/W	00000419H	ICR25	----1111B	R/W
00000406H	ICR06	----1111B	R/W	0000041AH	ICR26	----1111B	R/W
00000407H	ICR07	----1111B	R/W	0000041BH	ICR27	----1111B	R/W
00000408H	ICR08	----1111B	R/W	0000041CH	ICR28	----1111B	R/W
00000409H	ICR09	----1111B	R/W	0000041DH	ICR29	----1111B	R/W
0000040AH	ICR10	----1111B	R/W	0000041EH	ICR30	----1111B	R/W
0000040BH	ICR11	----1111B	R/W	0000041FH	ICR31	----1111B	R/W
0000040CH	ICR12	----1111B	R/W	00000420H	ICR32	----1111B	R/W
0000040DH	ICR13	----1111B	R/W	00000421H	ICR33	----1111B	R/W
0000040EH	ICR14	----1111B	R/W	00000422H	ICR34	----1111B	R/W
0000040FH	ICR15	----1111B	R/W	00000423H	ICR35	----1111B	R/W
00000410H	ICR16	----1111B	R/W	00000424H	ICR36	----1111B	R/W
00000411H	ICR17	----1111B	R/W	00000425H	ICR37	----1111B	R/W
00000412H	ICR18	----1111B	R/W	00000426H	ICR38	----1111B	R/W
00000413H	ICR19	----1111B	R/W	00000427H	ICR39	----1111B	R/W

R/W : Read/Write enabled
— : Not in use

(Continued)

(Continued)

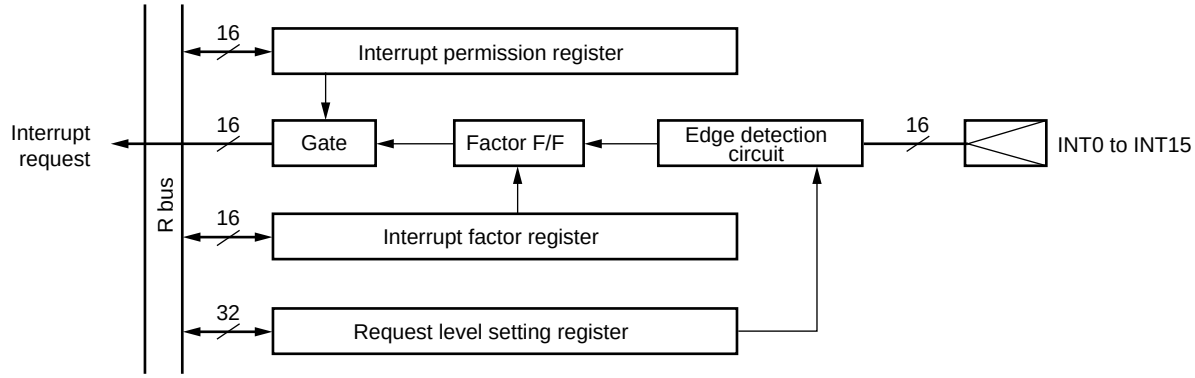
Address	bit 7 bit 0	Initial value	Access
00000428H	ICR40	----1111B	R/W
00000429H	ICR41	----1111B	R/W
0000042AH	ICR42	----1111B	R/W
0000042BH	ICR43	----1111B	R/W
0000042CH	ICR44	----1111B	R/W
0000042DH	ICR45	----1111B	R/W
0000042EH	ICR46	----1111B	R/W
0000042FH	ICR47	----1111B	R/W
00000431H	HRCL	----1111B	R/W
00000430H	DICR	-------0B	R/W

R/W : Read/Write enabled
— : Not in use

9. External Interrupt

The external interrupt controller controls external interrupt requests input to INT0 through INT15.
The level of requests to be detected can be selected from “H, ” “L, ” rising edge, and falling edge.

- **Block Diagram**



- **Register List**

Address	bit 15	bit 8	bit 0	Initial value	Access
000000C8H 000000C9H	EIRR0		ENIR0	00000000B 00000000B	R/W
000000CAH 000000CBH	EIRR1		ENIR1	00000000B 00000000B	R/W
000000CCH 000000CDH	ELVR0			00000000B 00000000B	R/W
000000CEH 000000CFH	ELVR1			00000000B 00000000B	R/W

R/W : Read/Write enabled

10. Delay Interrupt Module

The delay interrupt is a module that generates task switching interrupts. The use of this module allows the software to generate/cancel interrupt requests to the CPU.
For the block diagram of the delay interrupt module, see “8. Interrupt Controller.”

- **Register List**

Address	bit 7	bit 0	Initial value	Access
00000430H	DICR		- - - - - - - 0 B	R/W

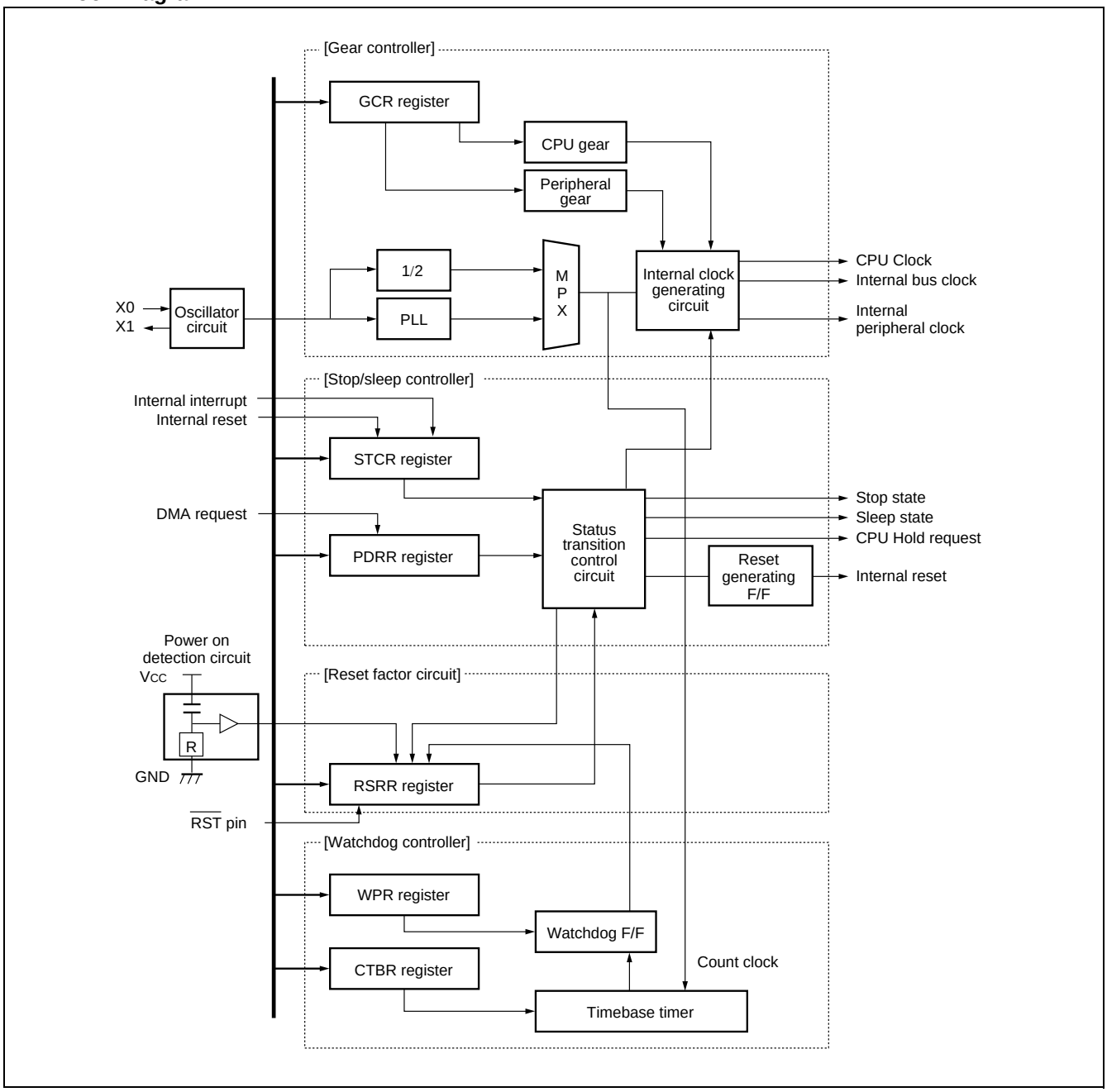
R/W : Read/Write enabled
— : Not in use

11. Clock Generator (Low power consumption mechanism)

The clock generator is responsible for the following functions :

- CPU clock generation (including the gear function)
- Peripheral clock generation (including the gear function)
- Reset generation and holding factors
- Standby function (including hardware standby)
- Contains PLL (multiplication circuit)

- **Block Diagram**



- **Register List**

Address	bit 15	bit 8	bit 0	Initial value	Access
00000480H	RSRR/WTCR			1-XXX-00B	R, W
00000481H		STCR		000111--B	R/W, W
00000482H	PDRR			----0000B	R/W
00000483H		CTBR		XXXXXXXXB	W
00000484H	GCR			110011-1B	R/W, R
00000485H		WPR		XXXXXXXXB	W

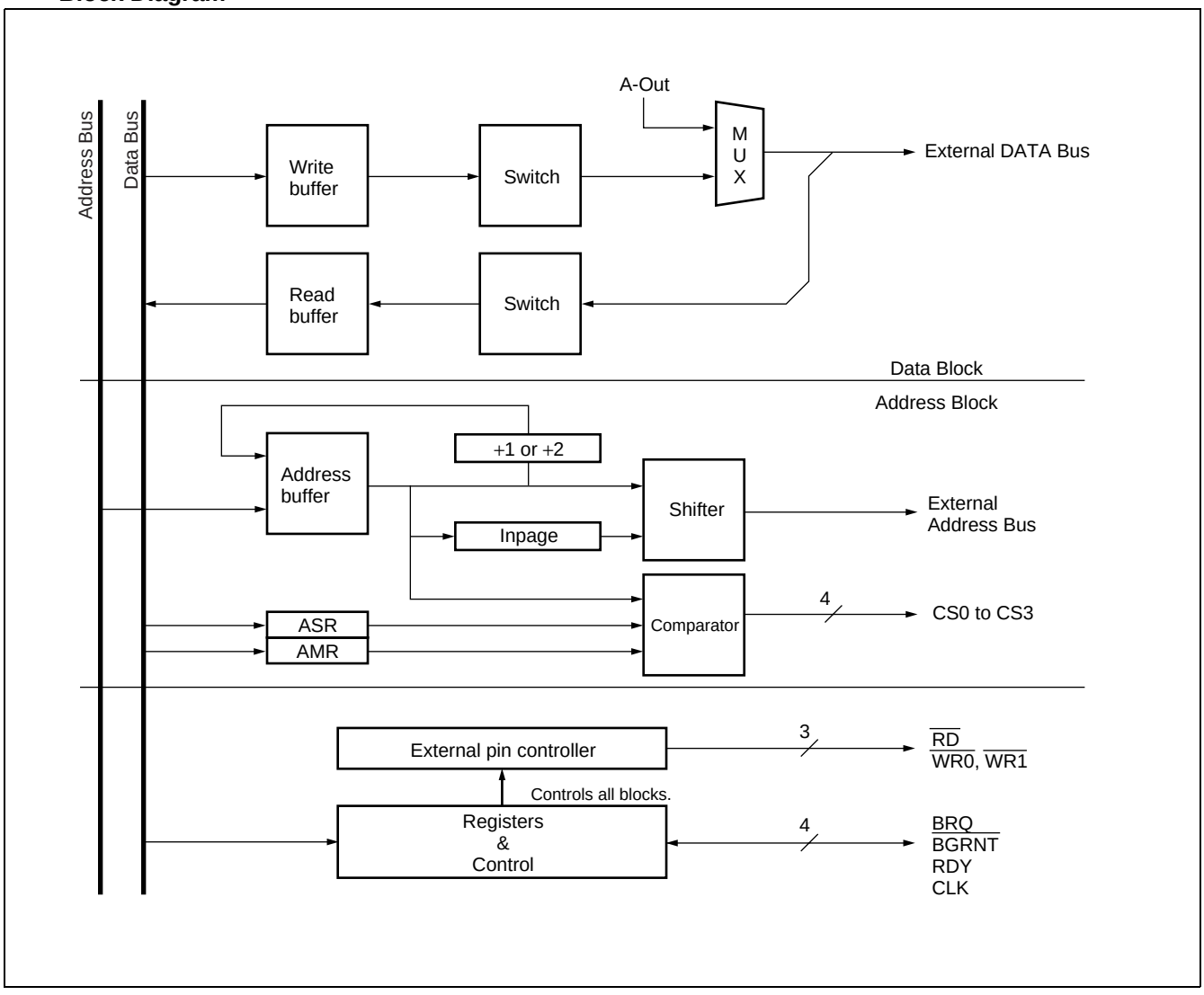
R/W : Read/Write enabled
R : Read only
W : Write only
— : Not in use
X : Undefined

12. External Bus Interface

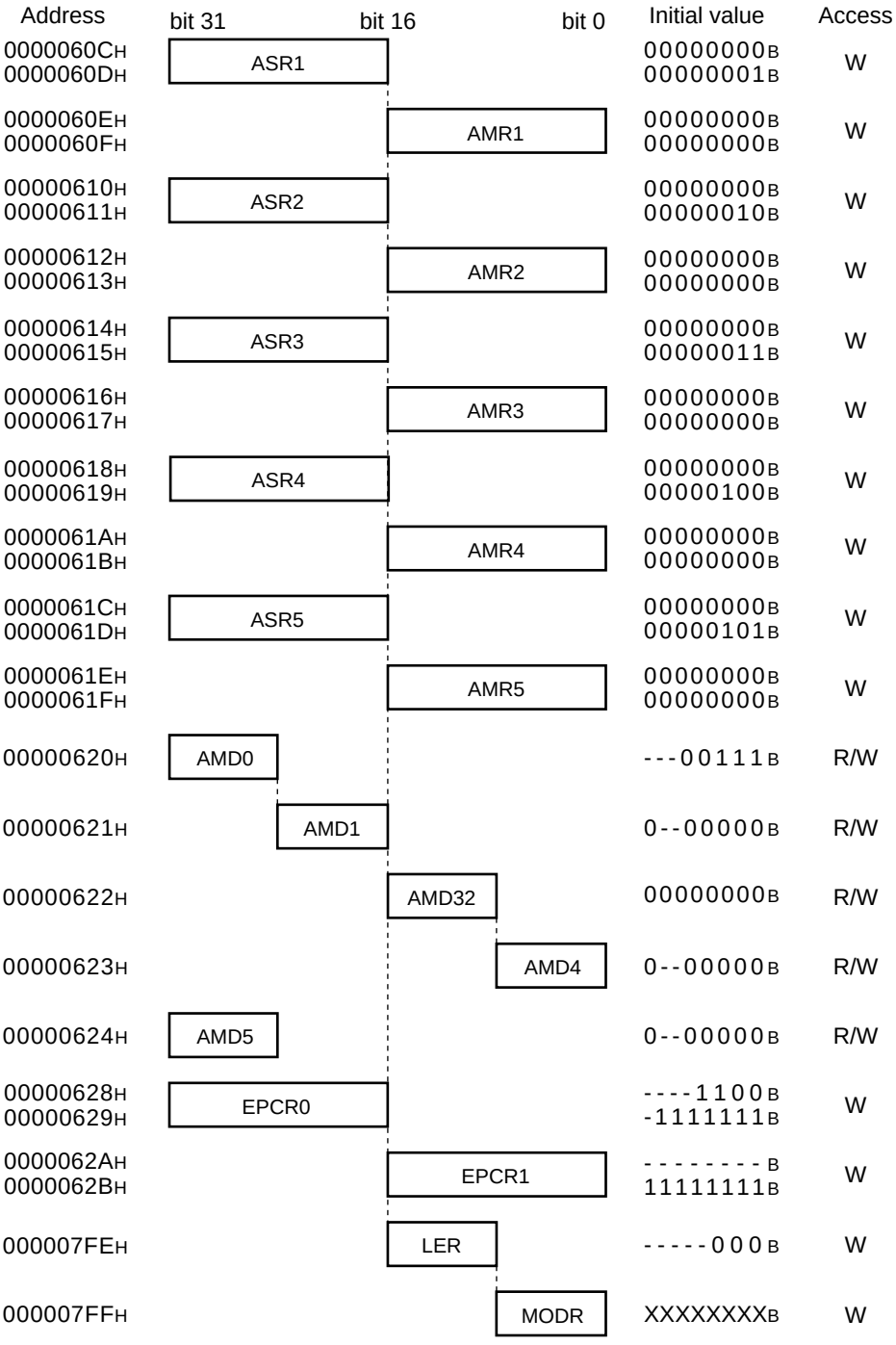
The external bus interface controls the interface between the external memory and the external I/O. Its features are as follows :

- 24-bit (16 MB) address output
- An 8/16-bit bus width can be set by chip select area.
- Inserts an automatic and programmable memory wait (for seven cycles at maximum) .
- Unused addresses/data pins are available as I/O ports.
- Support for little endian mode
- When use of a clock doubler, bus speed is half of CPU.
- The use is not allowed when the external bus exceeds 25 MHz.

- **Block Diagram**



- **Register List**



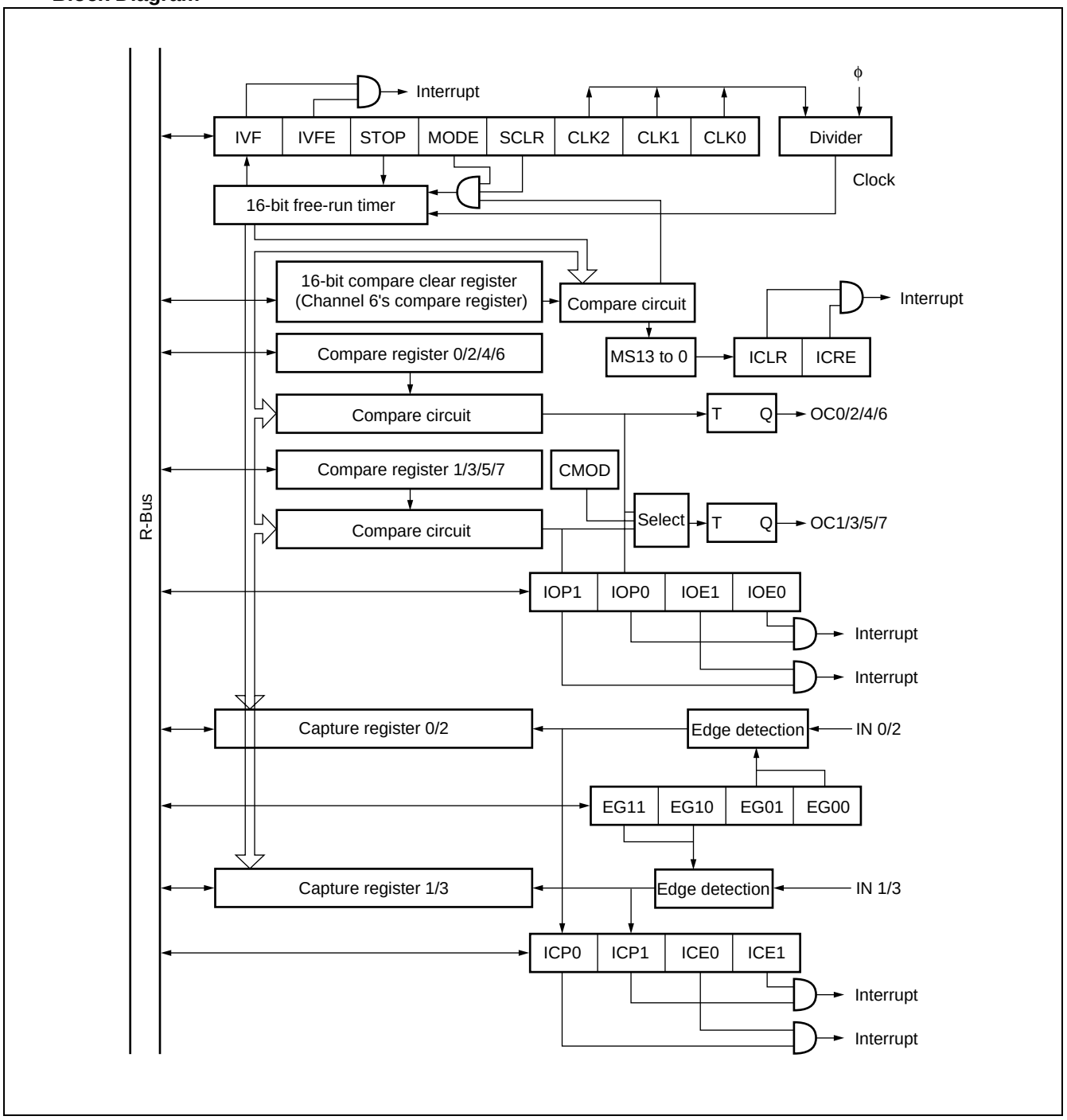
R/W : Read/Write enabled
W : Write only
— : Not in use
X : Undefined

13. Multifunction Timer

The multifunction timer unit consists of one 16-bit free-run timer, eight 16-bit output compare registers, four 16-bit input capture registers, and six 16-bit PPG timer channels. By using this function waveforms can be output based on the 16-bit free-run timer and the input pulse width and external clock cycle can also be measured.

- **Timer Components**
- 16-bit free-run timer (× 1)
  The 16-bit free-run timer consists of a 16-bit up counter, a control register, a 16-bit compare clear register, and a prescaler. The output value of this counter is used as the basic time (base timer) for output compare and input capture.
- Output compare (× 8)
  The output compare consists of eight 16-bit compare registers, a compare output latch, and a control register. When the 16-bit free-run timer value agrees to the compare register value, the output level can be inverted and an interrupt can also be generated.
- Input capture (× 4)
  The input capture consists of capture registers corresponding to four independent external input pins and a control register. By detecting any edge of signals input from external input pins, the 16-bit free-run timer value can be held in the capture register and an interrupt can be generated at the same time.
- 16-bit PPG timer (× 6)
  See “4. PPG Timer”.

- **Block Diagram**



- **Register List**

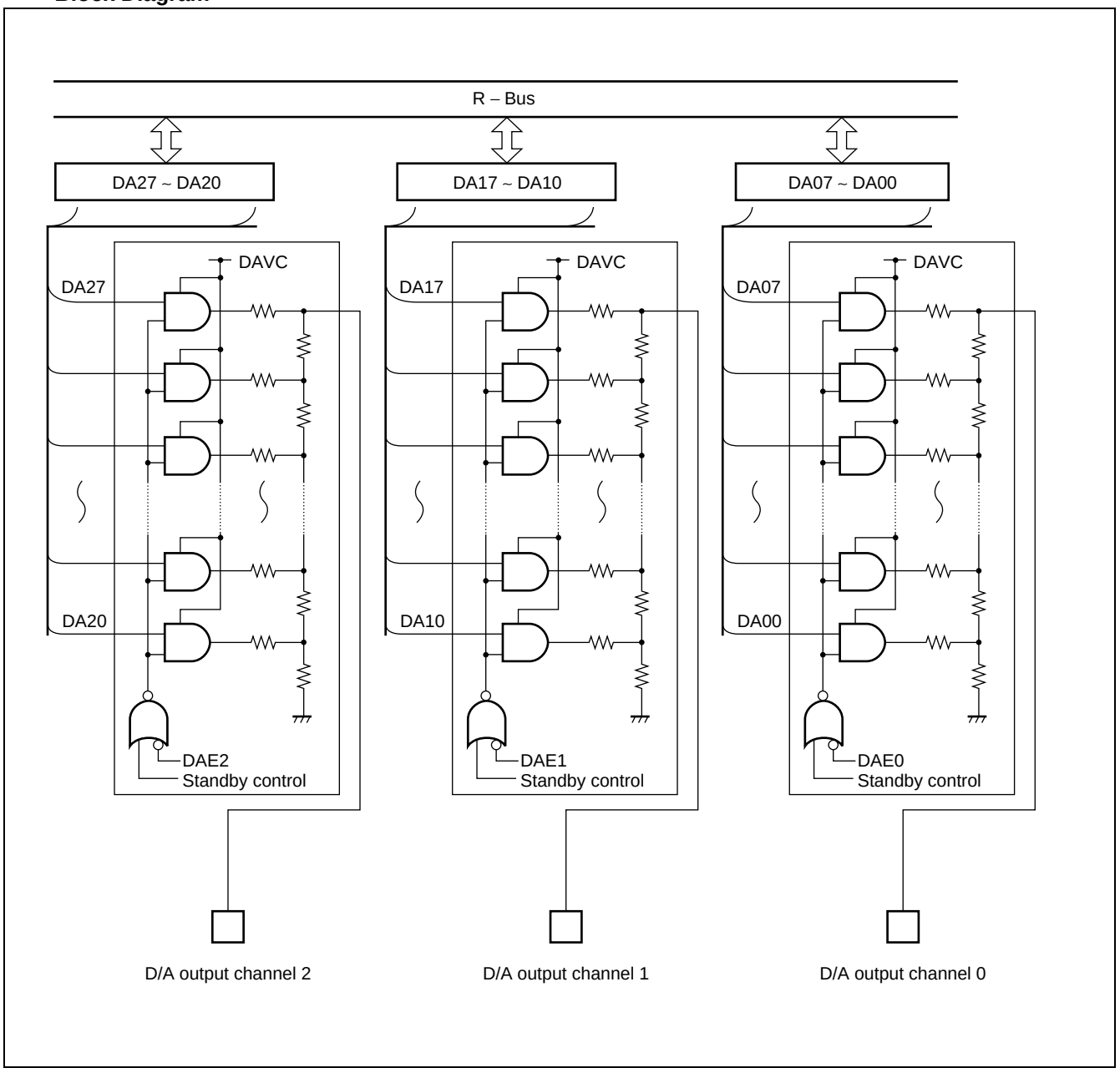
Address	bit15 ····· bit8	bit7 ····· bit0	Initial value	Access
000068H	IPCP1		XXXXXXXXB	R
000069H			XXXXXXXXB	R
00006AH	IPCP0		XXXXXXXXB	R
00006BH			XXXXXXXXB	R
00006CH	IPCP3		XXXXXXXXB	R
00006DH			XXXXXXXXB	R
00006EH	IPCP2		XXXXXXXXB	R
00006FH			XXXXXXXXB	R
000071H		ICS23	00000000B	R/W
000073H		ICS01	00000000B	R/W
000074H	OCCP1		XXXXXXXXB	R/W
000075H			XXXXXXXXB	R/W
000076H	OCCP0		XXXXXXXXB	R/W
000077H			XXXXXXXXB	R/W
000078H	OCCP3		XXXXXXXXB	R/W
000079H			XXXXXXXXB	R/W
00007AH	OCCP2		XXXXXXXXB	R/W
00007BH			XXXXXXXXB	R/W
00007CH	OCCP5		XXXXXXXXB	R/W
00007DH			XXXXXXXXB	R/W
00007EH	OCCP4		XXXXXXXXB	R/W
00007FH			XXXXXXXXB	R/W
000080H	OCCP7		XXXXXXXXB	R/W
000081H			XXXXXXXXB	R/W
000082H	OCCP6		XXXXXXXXB	R/W
000083H			XXXXXXXXB	R/W
000084H	OCS3,2		XXX00000B	R/W
000085H			0000XX00B	R/W
000086H	OCS1,0		XXX00000B	R/W
000087H			0000XX00B	R/W
000088H	OCS7,6		XXX00000B	R/W
000089H			0000XX00B	R/W
00008AH	OCS5,4		XXX00000B	R/W
00008BH			0000XX00B	R/W
00008CH	TCDT		00000000B	R/W
00008DH			00000000B	R/W
00008EH	TCCS		0 - - - - - - - B	R/W
00008FH			00000000B	R/W

R/W : Read/Write enabled R : Read only — : Not in use X : Undefined

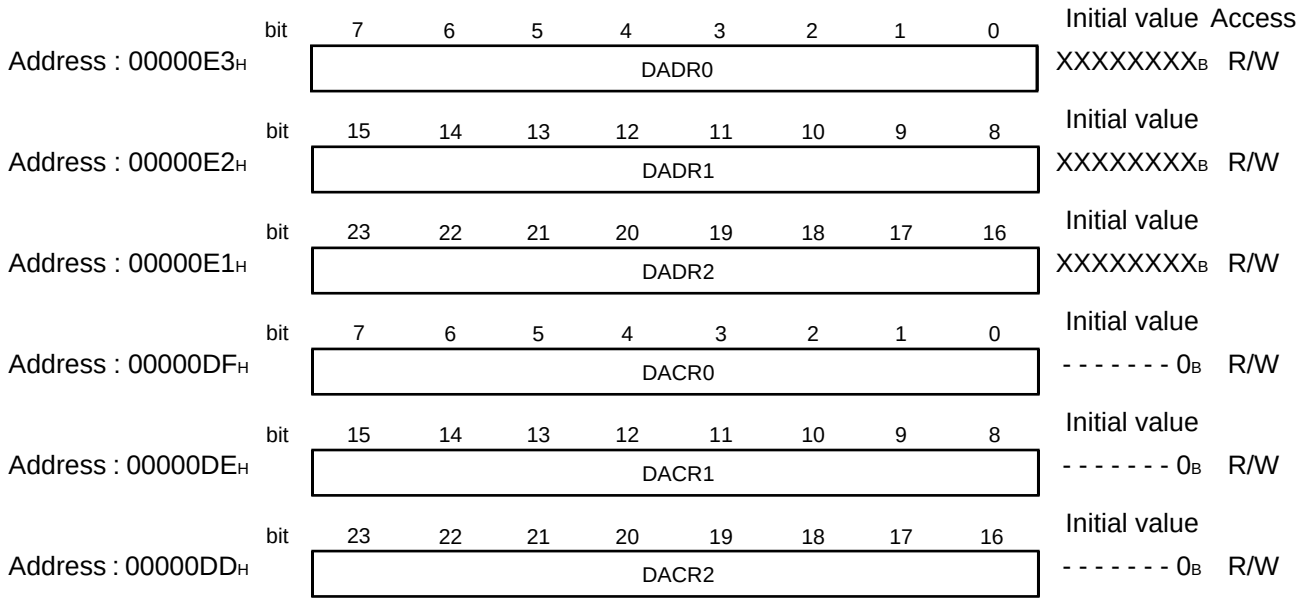
14. 8-bit D/A Converter

This block is of an 8-bit resolution, R-2R D/A converter. The block contains three D/A converter channels and each D/A control register can control output independently.
The D/A converter pin is a dedicated pin.

- **Block Diagram**



- **Register List**



R/W : Read/Write enabled, — : Not in use, X : Undefined

15. 8/16-bit Up/Down Counters/Timers

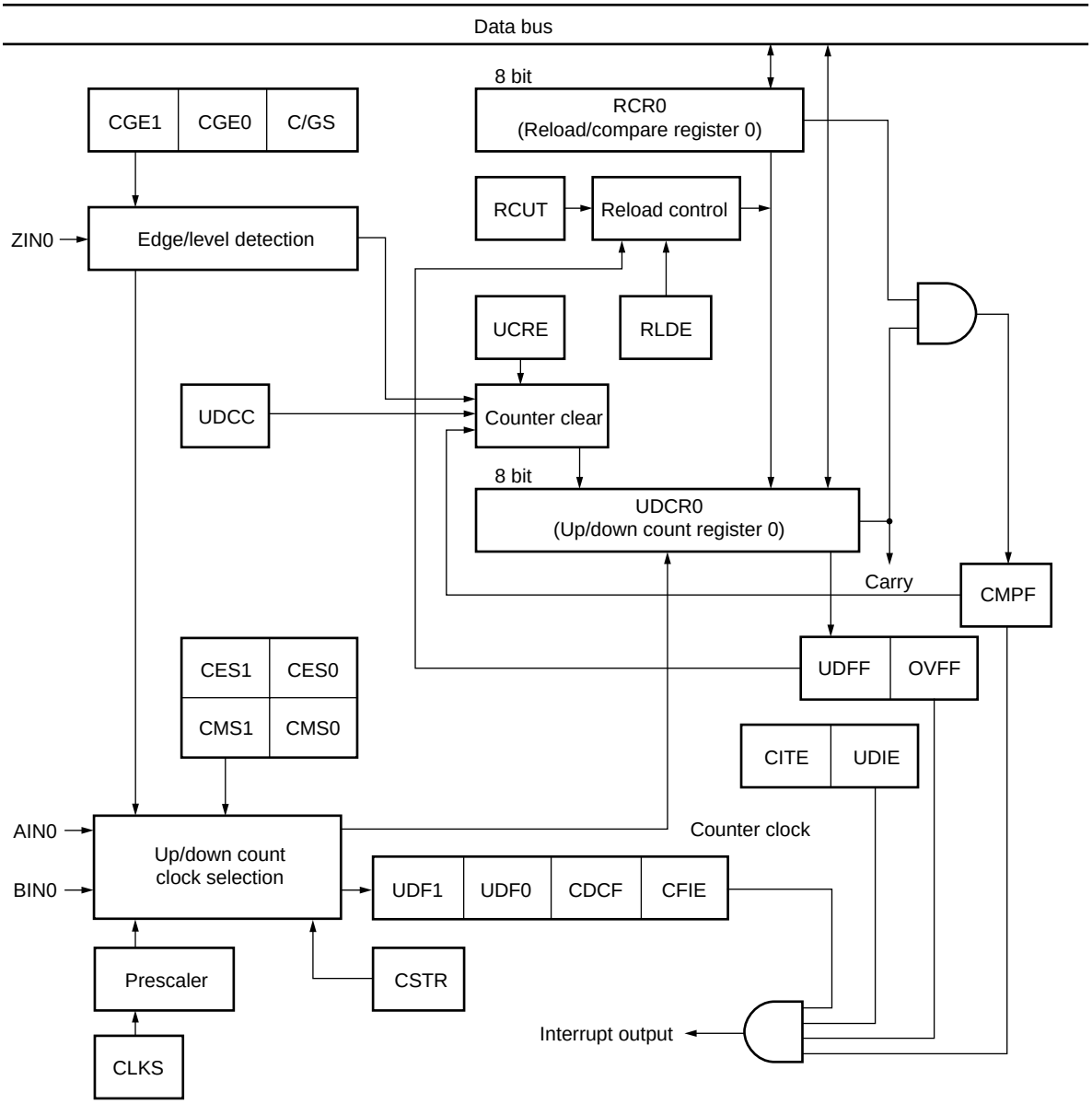
This is the up/down counter/timer block consisting of six event input pins, two 8-bit up/down counters, two 8-bit reload/compare registers, and their control circuits.

The features of this module are as follows :

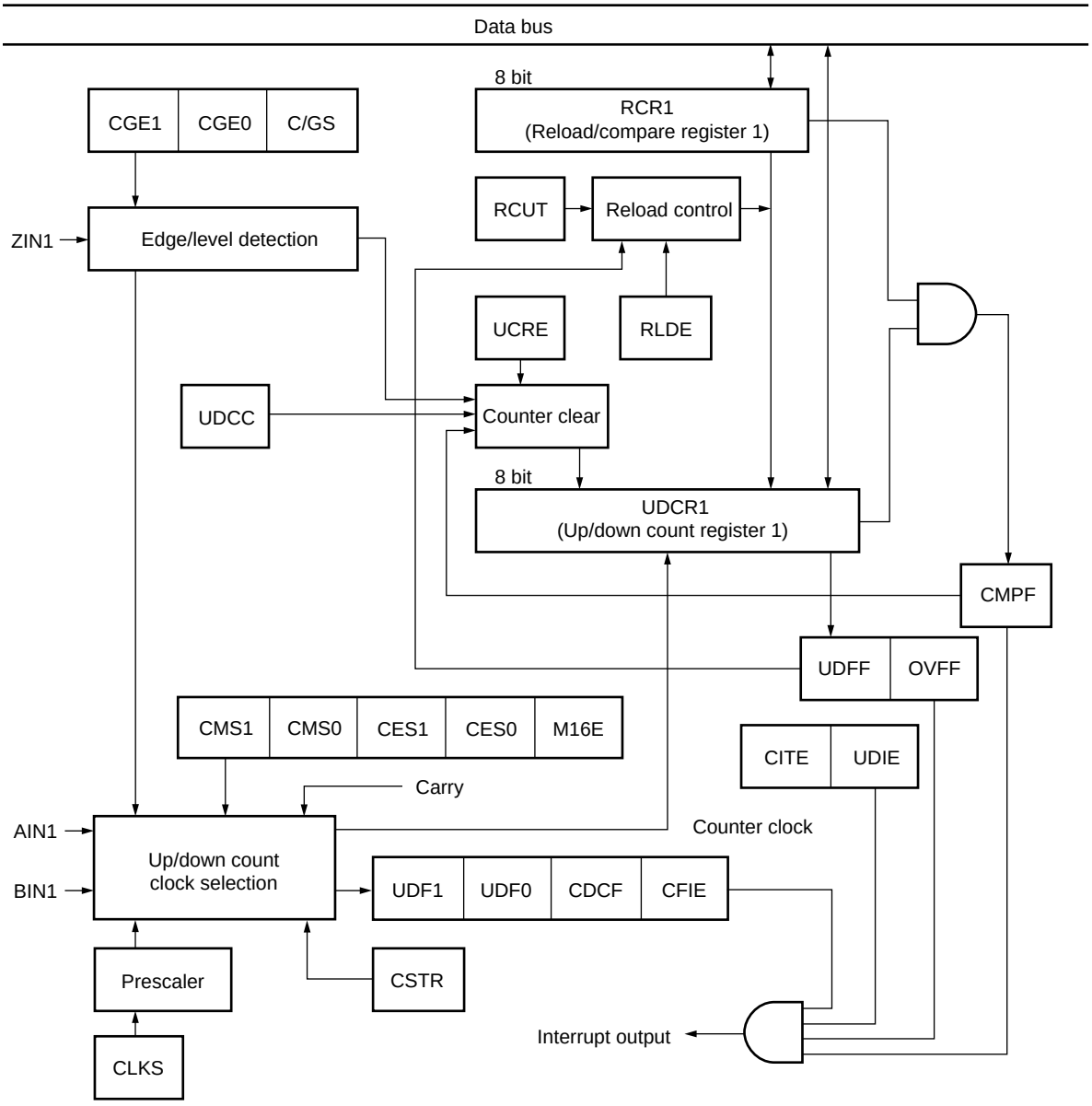
- Capable of counting in the (0) d- (255) d range by the 8-bit count register.
  (In 16-bit × 1 operating mode, the register can count in the (0) d- (65535) d range.)
- Four count modes to choose from by the count clock.
- In timer mode the count clock can be selected from two internal clock types.
- In up/down count mode an external pin input signal detection edge can be selected.
- The phase-difference count mode is suitable for encoder counting, such as of motors. Rotation angles, rotating speeds, and so on can be counted accurately and easily by inputting the output of phases A, B, and Z.
- Two types of function to choose from for the ZIN pin. (Enabled in all modes)
- Equipped with compare and reload functions which can be used individually or in combination. When combined, these functions can count up/down at any width.
- The immediately preceding count direction can be identified by the count direction flag.
- Capable of individually controlling interrupt generation when comparison results match, at occurrence of reload (underflow) or overflow, or when the count direction changes.

- **Block Diagram**

- 8/16-bit Up/Down Counter/Timer (channel 0)



- 8/16-bit Up/Down Counter/Timer (channel 1)



- **Register List**

	bit	7	6	5	4	3	2	1	0	Initial value	Access
Address : 00005F$_H$		UDCR0								00000000$_B$	R
	bit	15	14	13	12	11	10	9	8	Initial value	
Address : 00005E$_H$		UDCR1								00000000$_B$	R
	bit	7	6	5	4	3	2	1	0	Initial value	
Address : 00005D$_H$		RCR0								00000000$_B$	W
	bit	15	14	13	12	11	10	9	8	Initial value	
Address : 00005C$_H$		RCR1								00000000$_B$	W
	bit	7	6	5	4	3	2	1	0	Initial value	
Address : 000063$_H$		CSR0								00000000$_B$	R/W, R
	bit	7	6	5	4	3	2	1	0	Initial value	
Address : 000067$_H$		CSR1								00000000$_B$	R/W, R
	bit	7	6	5	4	3	2	1	0	Initial value	
Address : 000061$_H$		CCRL0								-000X000$_B$	R/W, W
	bit	7	6	5	4	3	2	1	0	Initial value	
Address : 000065$_H$		CCRL1								-000X000$_B$	R/W, W
	bit	15	14	13	12	11	10	9	8	Initial value	
Address : 000060$_H$		CCRH0								00000000$_B$	R/W
	bit	15	14	13	12	11	10	9	8	Initial value	
Address : 000064$_H$		CCRH1								-0000000$_B$	R/W

R/W : Read/Write enabled, R : Read only, W : Write only, — : Not in use, X : Undefined

16. Peripheral STOP Control

This function can be used to stop the clock of unused resources in order to conserve more power.

- **Register List**

Address	bit7 ..... bit0	Initial value	Access
000090H	STPR0	0000 - - - - B	R/W
000091H	STPR1	00000 - 00B	R/W
000092H	STPR2	000000 - - B	R/W

R/W : Read/Write enabled, — : Not in use

■ SERIAL START UP

The serial startup mode is the internal RAM (2 KB) serial write or RAM program startup mode using the internal dedicated ROM. While this mode executes communication through the UART channel 1 built in this model, it can also serve for data transfer to external flash memory. Either synchronous or asynchronous communication can be selected by setting the relevant pin. For asynchronous communication, a baud rate of 9600 bps can be used either at a machine clock frequency of 25 MHz (oscillation frequency of 12.5 MHz) orat a machine clock frequency of 33 MHz (oscillation frequency of 16.5 MHz) selectively.
(Note that serial startup using asynchronous communication cannot be performed at a machine clock frequency of 36 MHz at an oscillation frequency of 18 MHz.)

- Communication specifications

(1) Asynchronous communication at a machine clock frequency of 33 MHz

The device performs serial communication in the asynchronous (normal) mode of UART channel 1.
The baud rate is 9600 bps at a machine clock frequency of 33 MHz (based on a 16.5 MHz external crystal oscillator) .
Serial mode settings are : a data length of 8 bits, a stop bit length of 1 bit, no parity, and LSB-first transfer.

(2) Asynchronous communication at a machine clock frequency of 25 MHz

The device performs serial communication in the asynchronous (normal) mode of UART channel 1.
The baud rate is 9600 bps at a machine clock frequency of 25 MHz (based on a 12.5 MHz external crystal oscillator) .
Serial mode settings are : a data length of 8 bits, a stop bit length of 1 bit, no parity, and LSB-first transfer.

(3) Synchronous communication

The device performs serial communication in the synchronous (normal) mode of UART channel 1.
The baud rate can be set freely depending on the external clock input (the baud rate is determined directly by the external clock frequency) .
The maximum input frequency of the external clock is the peripheral operating clock frequency devided by 8.
(The peripheral operating clock setting is the fastest PLL frequency.)
Serial mode settings are : a data length of 8 bits, no parity, and LSB-first transfer.
In each fo these modes, the devices passes the following three items of download information data to the FR, byte by byte in sequence from the high-order byte :

1. Command data (00_H)

2. 4 bytes of the download destination RAM address (00080400_H to $000807FF_H$)

3. 4 bytes specifying the number of bytes download (up to $000003FF_H$)

Then the device gives resulting SUM check data (the lower eight bits extracted from these data items added together) , entering the RAM download routine.
The device then passes the data to be downloaded to RAM to the FR, byte by byte in sequence from the high-order byte, and the resulting SUM check data as well in the same way. Upon completion of transfer, a jump to RAM takes place and the downloaded program is executed.

Method of setting

	External pin name					
	MD2	**MD1**	**MD0**	**PG5**	**PG4**	**PG3**
Asynchronous communication • machine clock 33 MHz	1	1	0	1	0	0
Asynchronous communication • machine clock 25 MHz	1	1	0	1	0	1
Synchronous communication	1	1	0	1	1	0

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 3.6	V	
Analog supply voltage	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6	V	*1
Analog reference voltage	AVRH	V_{SS} – 0.3	V_{SS} + 3.6	V	*1
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Input voltage (open drain port J)	V_{I2}	V_{SS} – 0.3	V_{SS} + 5.5	V	
Analog pin input voltage	V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL}	—	10	mA	*2
“L” level average output current	I_{OLAV}	—	4	mA	*3
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	–10	mA	*2
“H” level average output current	I_{OHAV}	—	–4	mA	*3
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
“H” level total average output current	ΣI_{OHAV}	—	–20	mA	*4
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	0	+70	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : Take care not to exceed V_{CC} + 0.3 V when turning on the power, for example.
Take care also to prevent AV_{CC} from exceeding V_{CC} when turning on the power, for example.

*2 : The maximum output current stipulates the peak value of a single concerned pin.

*3 : The average output current stipulates the average current flowing through a single concerned pin over a period of 100 ms.

*4 : The total average output current stipulates the average current flowing through all concerned pins over a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.15	3.6	V	During normal operations.
		2.0	3.6		The RAM state is retained when stopped.
Analog supply voltage	AV_{CC}	V_{SS} + 3.15	V_{SS} + 3.6	V	
Analog reference voltage (High voltage side)	AVRH	AV_{CC}–0.3	AV_{CC}	V	
Analog reference voltage (Low voltage side)	AVRL	AV_{SS}	AV_{SS} + 0.3	V	
Operating temperature	T_A	0	+70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Input except for hysteresis input pin*	—	0.65 × V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	Hysteresis input pin*	—	0.8 × V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	Input except for hysteresis input pin*	—	V_{SS} – 0.3	—	0.25 × V_{CC}	V	
	V_{ILS}	Hysteresis input pin*	—	V_{SS} – 0.3	—	0.2 × V_{CC}	V	
"H" level output voltage	V_{OH}	Except for port J.	V_{CC} = 3.15 V, I_{OH} = 4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	Except for port J.	V_{CC} = 3.15 V, I_{OL} = 4.0 mA	—		0.4	V	
Input leakage current	I_{LI}	—	V_{CC} = 3.6 V, V_{SS} < V_I < V_{CC}	—	—	±5	µA	
"L" level output voltage	V_{OL2}	Port J	V_{CC} = 3.15 V, I_{OL} = 15 mA	—	—	0.4	V	Open drain
Output application voltage	V_D	Port J	—	V_{CC} – 0.3	—	V_{SS} + 5.0	V	Open drain
Pull-up resistance	R_{PULL}	$\overline{RST}$, pull-up pin	—	—	50	—	kΩ	
Power supply current	I_{CC}	V_{CC}	V_{CC} = 3.3 V	—	85	120	mA	
	I_{CCS}	V_{CC}	V_{CC} = 3.3 V	—	60	100	mA	During sleep mode
	I_{CCH}	V_{CC}	V_{CC} = 3.3 V, T_A = +25 °C	—	15	150	µA	In stop mpde
Input capacity	C_{IN}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, and AVRH	—	—	10	—	pF	

* : See "■ I/O CIRCUIT TYPE".

4. AC Characteristics

(1) Clock Timing Ratings

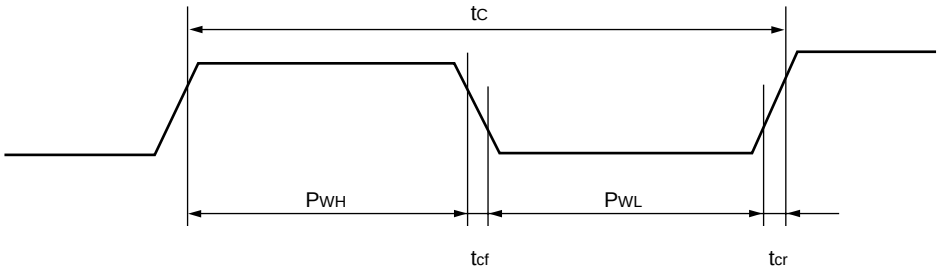
(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

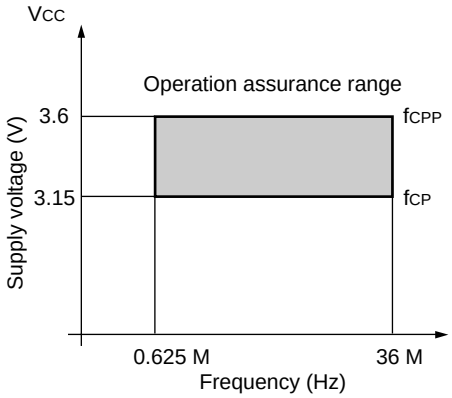
Parameter		Symbol	Pin name	Condition	Value		Unit	Remarks
					Min	Max		
Clock frequency (high speed and self oscillation)		f_C	X0, X1	—	10	18	MHz	Range in which self oscillation is allowed
Clock frequency (high speed and PLL in use)				—				Range in which self oscillation and the use of the PLL for external clock input are allowed
Clock frequency (High speed an 1/2 division input)				—	10	18	MHz	Range in which external clocks can be input
Clock cycle time		t_C	X0, X1	—	55.6	100	ns	
Input clock pulse width		P_{WH}	X0, X1	—	25	—	ns	
		P_{WL}			15	—	ns	
Input clock rising		t_{cr}	X0, X1	—	—	8	ns	(t_{cr}+t_{cf})
Input clock falling		t_{cf}						
Internal operating clock frequency	CPU system	f_{CP}	—	One wait is set with the wait controller.	0.625*3	36	MHz	
	Bus system	f_{CPB}			0.625*3	25*2		
	Peripheral system	f_{CPP}			0.625*3	33		Analog section excluded. *1
					1	33		Analog section *1
Internal operating clock cycle time	CPU system	t_{CP}	—		27.8	1600*3	ns	
	Bus system	t_{CPB}			40*2	1600*3		
	Peripheral system	t_{CPP}			30.3	1600*3		Analog section excluded. *1
					30.3	1000		Analog section *1

*1 : The target analog section is the A/D.

*2 : The maximum external bus operating frequency allowed is 25 MHz.

*3 : The value when a minimum clock frequency of 10 MHz is input to X0 and half a division of the oscillator circuit and the 1/8 gear are in use.

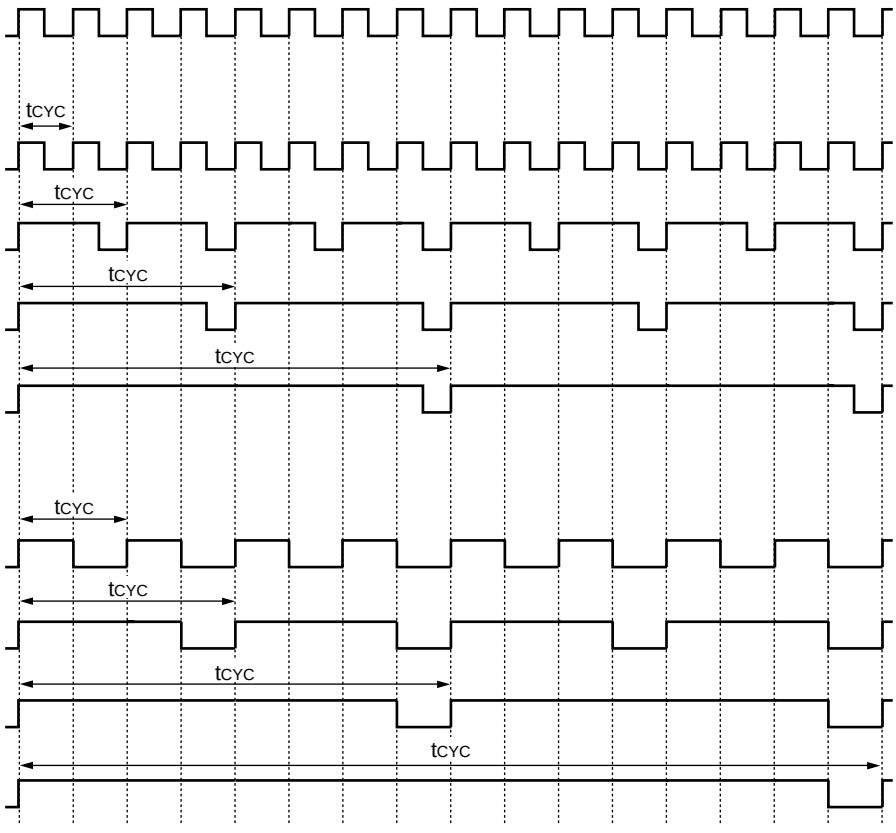




The relationship between the X0 input and the internal clock set with the CHC/CCK1/CCK0 bit of the GCR (Gear Control Register) is as shown next.

X0 input

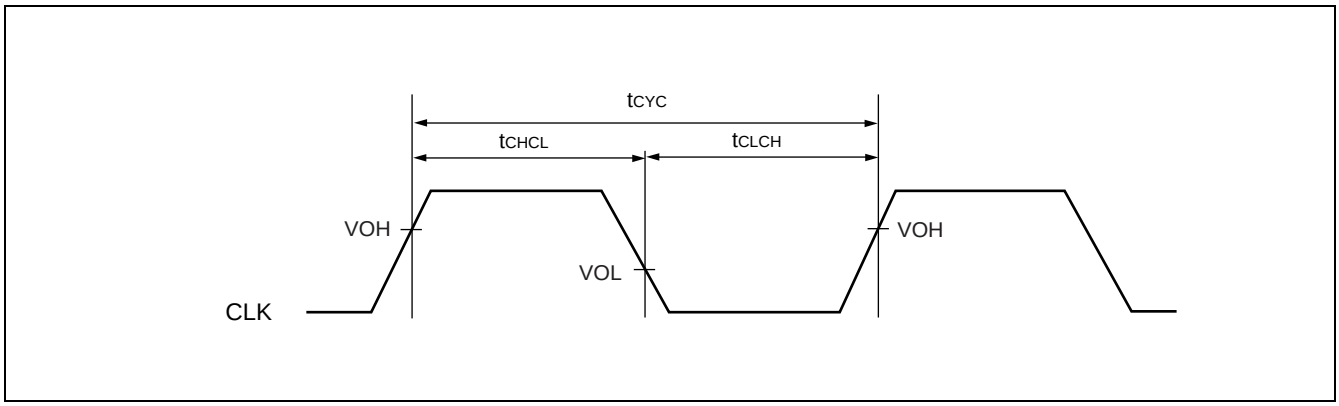
- Source oscillation × 1
  (GCR CHC bit : 0)
  - (a) Gear × 1 internal clock
    CCK1/0 : 00
  - (b) Gear × 1/2 internal clock
    CCK1/0 : 01
  - (c) Gear × 1/4 internal clock
    CCK1/0 : 10
  - (d) Gear × 1/8 internal clock
    CCK1/0 : 11
- Source oscillation × 1/2
  (GCR CHC bit : 1)
  - (a) Gear × 1 internal clock
    CCK1/0 : 00
  - (b) Gear × 1/2 internal clock
    CCK1/0 : 01
  - (c) Gear × 1/4 internal clock
    CCK1/0 : 10
  - (d) Gear × 1/8 internal clock
    CCK1/0 : 11



(2) Clock Output Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
				t_{CPB}	—		At using doubla
CLK↑→CLK↓	t_{CHCL}	CLK		t_{CYC}/2–10	t_{CYC}/2+10	ns	*2
CLK↓→CLK↑	t_{CLCH}	CLK		t_{CYC}/2–10	t_{CYC}/2+10	ns	*3



*1 : t_{CYC} is a frequency for one clock including a gear cycle.
The doubler is used when the CPU runs at 25 MHz or higher.

*2 : Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, or 1/8 is set, substitute 1/2, 1/4, or 1/8 for “n” in the following equations, respectively.
- Min : (1–n/2) × t_{CYC}–10
- Max : (1–n/2) × t_{CYC}+10

When the doubler is used, set the gear cycle to × 1.

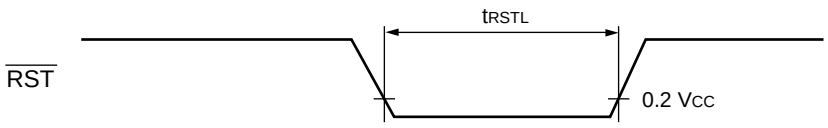
*3 : Rating at a gear cycle of × 1.
When a gear cycle of 1/2, 1/4, or 1/8 is set, substitute 1/2, 1/4, or 1/8 for “n” in the following equations, respectively.
- Min : n/2 × t_{CYC}–10
- Max : n/2 × t_{CYC}+10

When the doubler is used, set the gear cycle to × 1.

(3) Reset Input Ratings

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

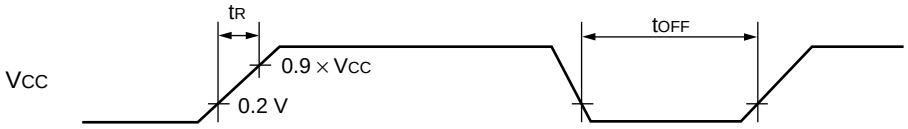
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	$t_{CP} \times 5$	—	ns	



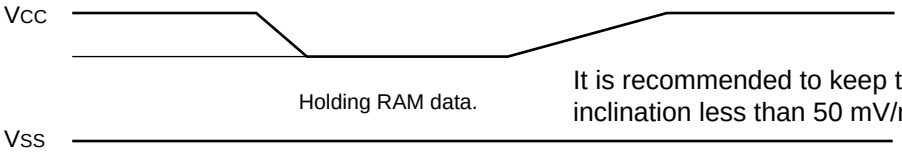
(4) Power On Reset

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

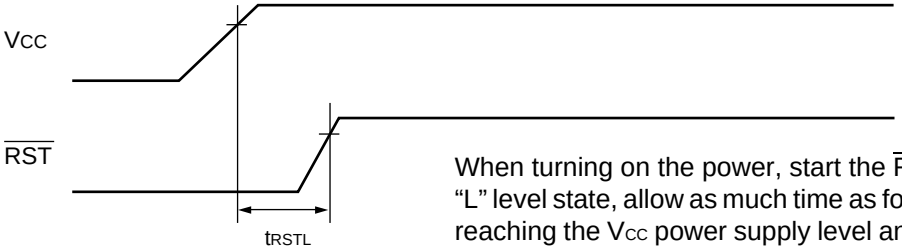
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	—	20	ms	V_{CC} < 0.2 V before turning up the power.
Power supply cutoff time	t_{OFF}			2	—	ms	



A rapid change in supply voltage might activate power on reset.
When the supply voltage needs to be varied while operating, it is recommended to minimize fluctuations to smoothly start up the voltage.



It is recommended to keep the rising inclination less than 50 mV/ms.



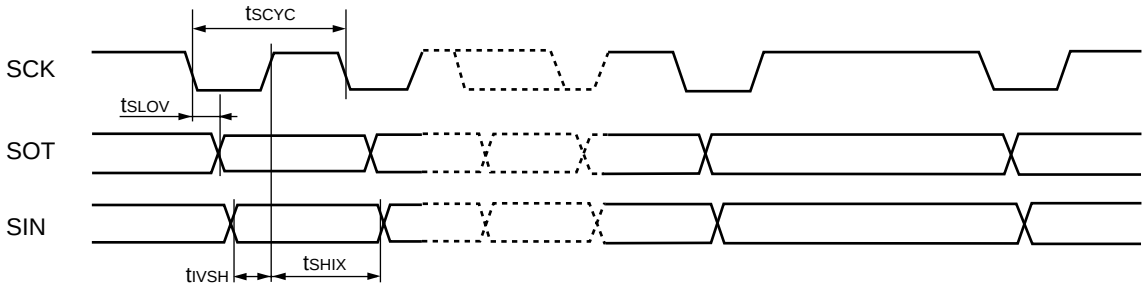
When turning on the power, start the $\overline{RST}$ pin in "L" level state, allow as much time as for t_{RSTL} after reaching the V_{CC} power supply level and then set the pin to the H level.

(5) Serial I/O (CH0 to CH4)

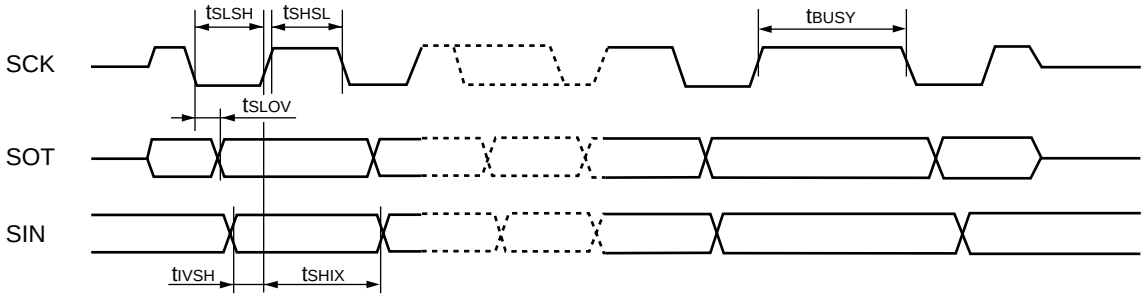
(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal clock	8 t_{CPP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—		−10	+50	ns	
Valid SIN → SCK ↑	t_{IVSH}	—		50	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	—		50	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External clock	4 t_{CPP} – 10	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CPP} – 10	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—		0	50	ns	
Valid SIN → SCK ↑	t_{IVSH}	—		50	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	—		50	—	ns	
Serial busy period	t_{BUSY}	—		—	6 t_{CPP}	ns	

Internal shift clock mode



External shift clock mode

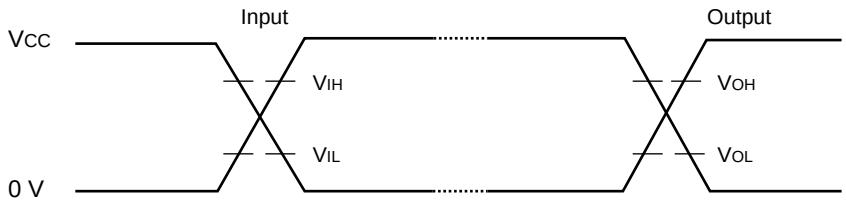


(6) External Bus Measurement Conditions

The following conditions apply to items that are not specifically stipulated.

- **AC characteristics measurement conditions**

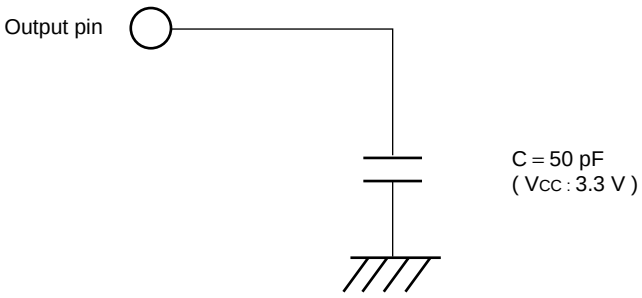
  V_{CC} : 3.3 V



V_{IH}	2.4 V	V_{OH}	1/2V_{CC}
V_{IL}	0.8 V	V_{OL}	1/2V_{CC}

(The input rise/fall time is less than 10 ns.)

- **Load condition**



(7) Normal Bus Access and Read/Write Operations

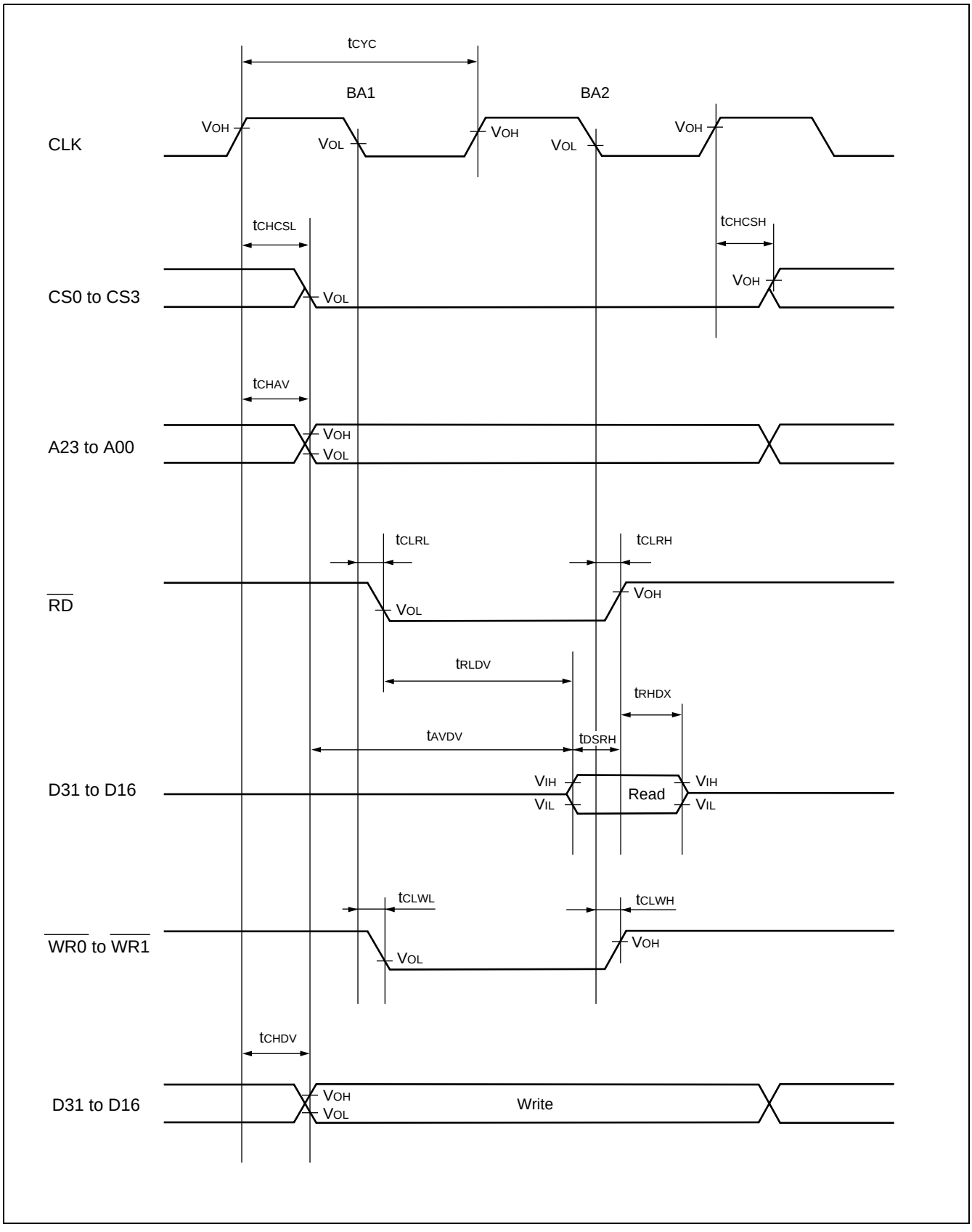
(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
CS0 to CS3 delay time	t_{CHCSL}	CLK CS0 to CS3	—	—	15	ns	
CS0 to CS3 delay time	t_{CHCSH}			—	15	ns	
Address delay time	t_{CHAV}	CLK A23 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK D31 to D16		—	15	ns	
$\overline{RD}$ delay time	t_{CLRL}	CLK $\overline{RD}$		—	10	ns	
$\overline{RD}$ delay time	t_{CLRH}			—	10	ns	
$\overline{WR0}$ to $\overline{WR1}$ delay time	t_{CLWL}	CLK $\overline{WR0}$ to $\overline{WR1}$		—	10	ns	
$\overline{WR0}$ to $\overline{WR1}$ delay time	t_{CLWH}			—	10	ns	
Valid address → valid data input time	t_{AVDV}	A23 to A00 D31 to D16		—	3 / 2 × t_{CYC} – 13	ns	*1, *2
$\overline{RD}$ ↓ → valid data input time	t_{RLDV}	$\overline{RD}$ D31 to D16		—	t_{CYC} – 25	ns	*1
Data setup → $\overline{RD}$ ↑ time	t_{DSRH}			25	—	ns	
$\overline{RD}$ ↑ → Rdata hold time	t_{RHDX}			0	—	ns	

*1 : If the bus is extended with either automatic wait insertion or RDY input, add the (t_{CYC} × the number of extended cycles) time to this value.

*2 : This is the value at the time of (gear cycle × 1) .
When the gear cycle is set to 1/2, 1/4 or 1/8, substitute “n” in the following formula with 1/2, 1/4 or 1/8 respectively.

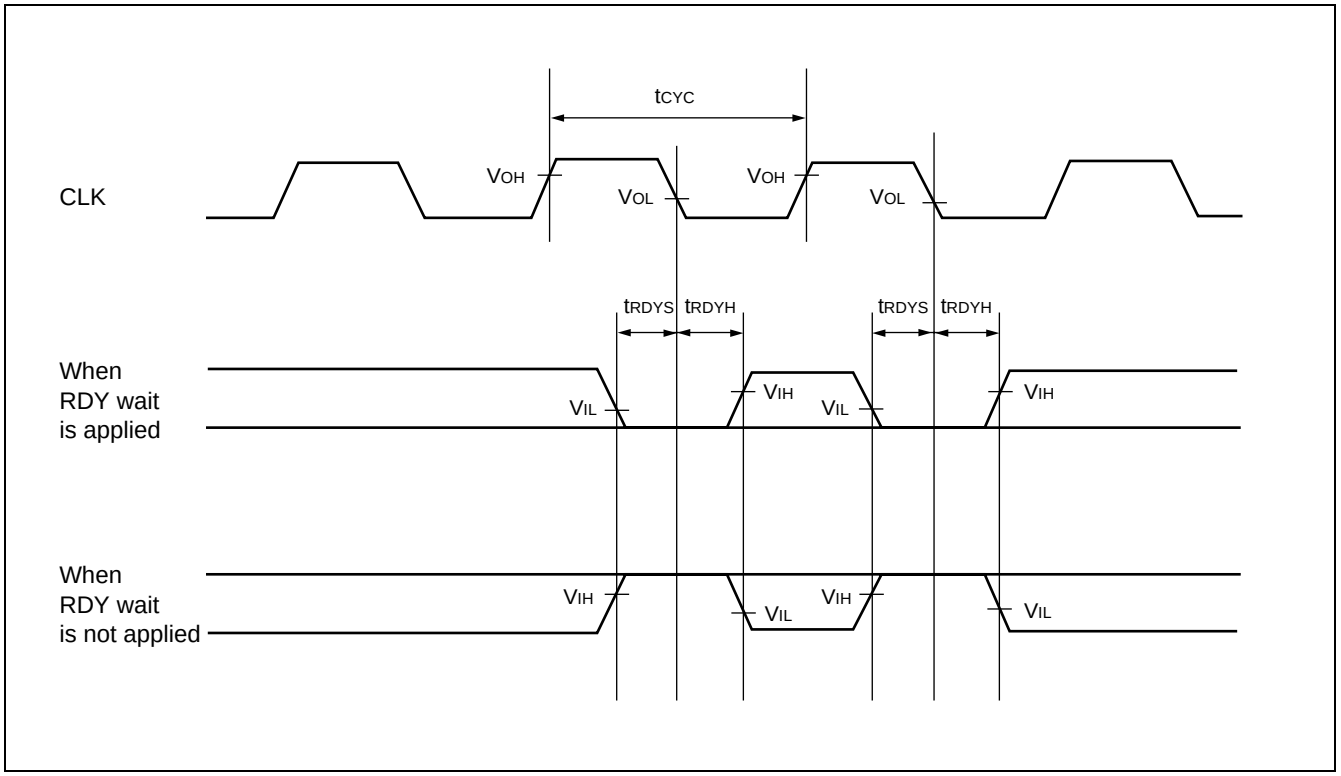
Formula : $(2 - n / 2) \times t_{CYC} - 13$


tCYC
BA1
BA2
CLK
VOH
VOL
tCHCSL
tCHCSH
CS0 to CS3
tCHAV
A23 to A00
tCLRL
tCLRH
RD
tRLDV
tRHDX
tAVDV
tDSRH
D31 to D16
VIH
VIL
Read
tCLWL
tCLWH
WR0 to WR1
tCHDV
D31 to D16
Write

(8) Ready Input Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY setup time → CLK ↓	t_{RDYS}	RDY CLK	—	20	—	ns	
CLK ↓ → RDY hold time	t_{RDYH}	RDY CLK		0	—	ns	

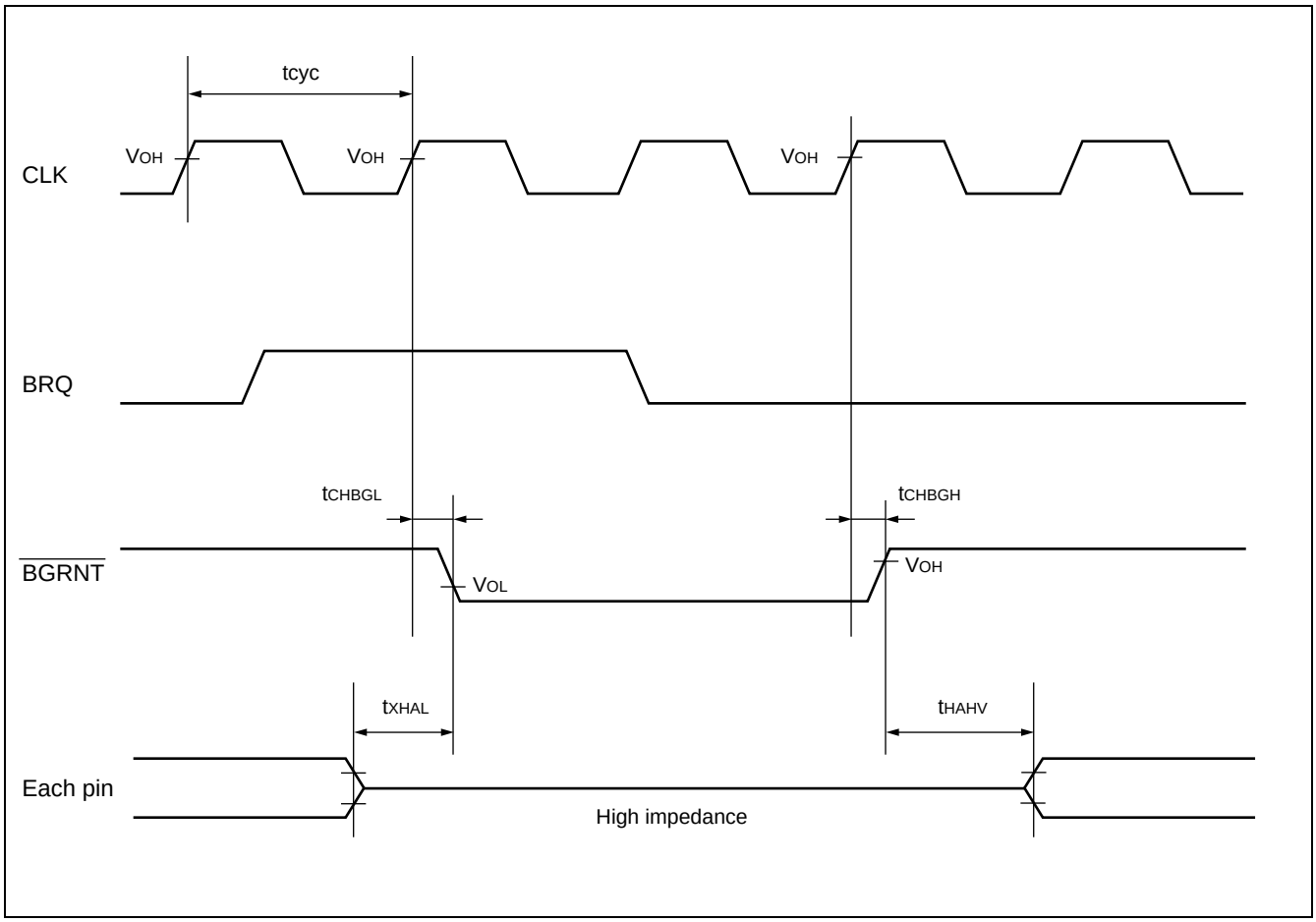


(9) Hold Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{BGRNT}$ delay time	t_{CHBGL}	CLK	—	—	10	ns	
$\overline{BGRNT}$ delay time	t_{CHBGH}	$\overline{BGRNT}$		—	10	ns	
Pin floating → $\overline{BGRNT}$ ↓ time	t_{XHAL}	$\overline{BGRNT}$		t_{CYC} – 10	t_{CYC} + 10	ns	
$\overline{BGRNT}$ ↑ → Pin valid time	t_{HAHV}			t_{CYC} – 10	t_{CYC} + 10	ns	

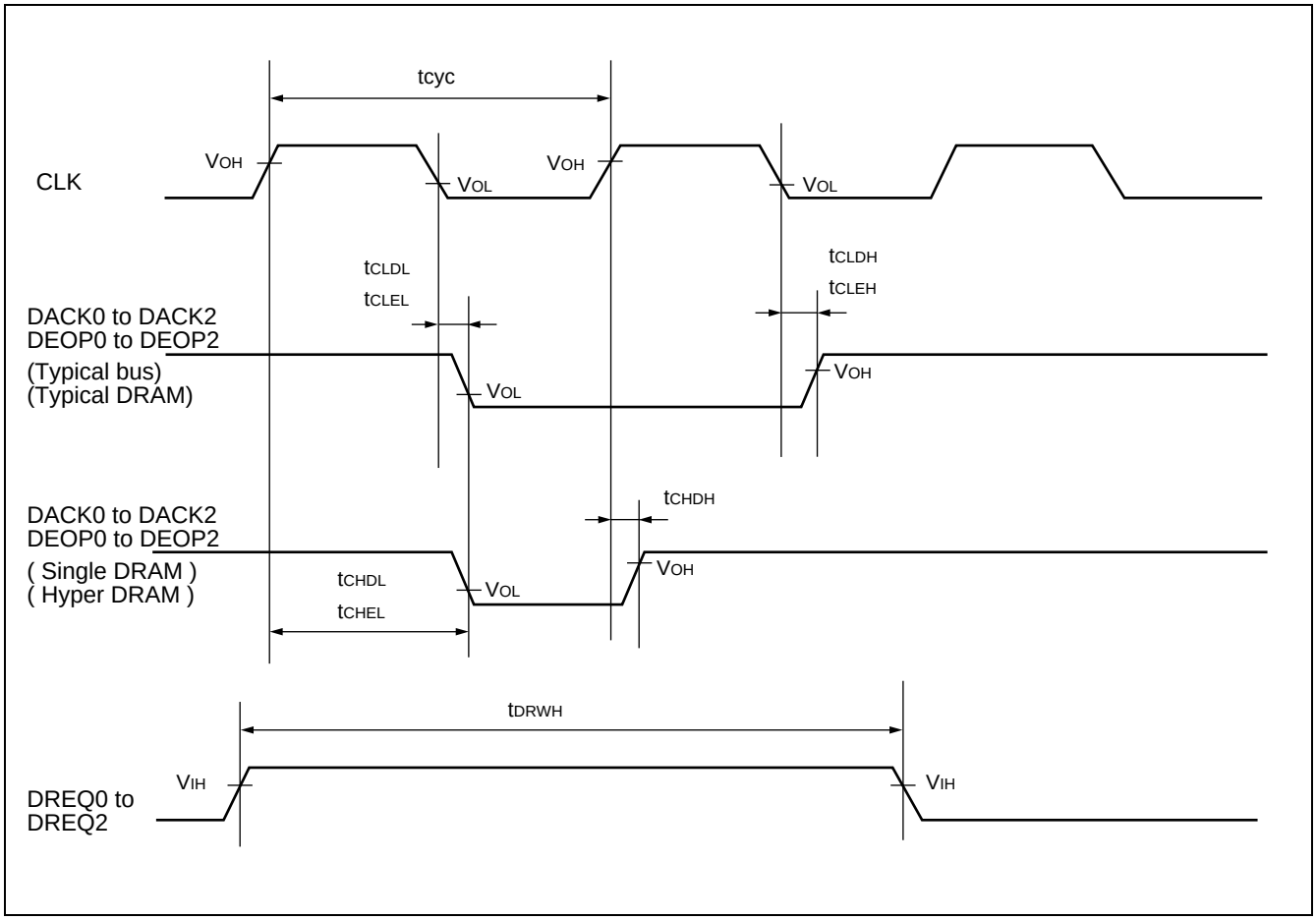
Note : More than one cycle exist after BRQ is fetched and before $\overline{BGRNT}$ changes.



(10) DMA Controller Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	2 t_{CYC}	—	ns	
DACK delay time (typical bus) (typical DRAM)	t_{CLDL}	CLK DACK0 to DACK2		—	6	ns	
	t_{CLDH}			—	6	ns	
DEOP delay time (typical bus) (typical DRAM)	t_{CLEL}	CLK DEOP0 to DEOP2		—	6	ns	
	t_{CLEH}			—	6	ns	
DACK delay time (Single Dram) (Hyper Dram)	t_{CHDL}	CLK DACK0 to DACK2		—	n / 2 × t_{CYC}	ns	
	t_{CHDH}			—	6	ns	
DEOP delay time (Single Dram) (Hyper Dram)	t_{CHEL}	CLK DEOP0 to DEOP2		—	n / 2 × t_{CYC}	ns	
	t_{CHEH}			—	6	ns	



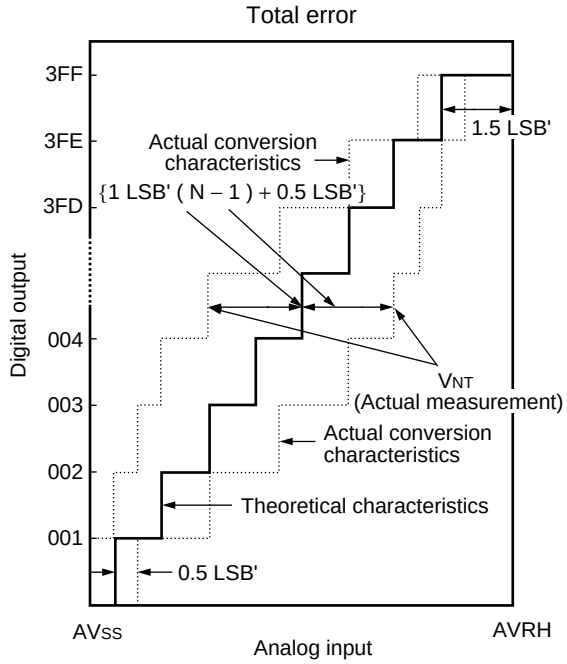
5. A/D Converter Electrical Characteristics

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter		Symbol	Pin name	Condition	Value			Unit	Remarks
					Min	Typ	Max		
Resolution		—	—	—	—	—	10	Bit	
Conversion time		—	—		5.1	—	—	µs	
Total error		—	—	AV_{CC} = 3.3 V, AVRH = 3.3 V	—	—	±4.0	LSB	
Linearity error		—	—		—	—	±3.5	LSB	
Differential linearity error		—	—		—	—	±2.0	LSB	
Zero transition error		V_{OT}	AN0 to AN7	AV_{CC} = 3.3 V, AV_{RH} = 3.3 V	AV_{SS} – 1.5	AV_{SS} + 0.5	AV_{SS} + 2.5	LSB	
Full-scale transition error		V_{FST}	AN0 to AN7		AV_{RH} – 5.5	AV_{RH} – 1.5	AV_{RH} + 0.5	LSB	
Analog input current		I_{AIN}	AN0 to AN7	—	—	0.1	10	µA	
Analog input voltage		V_{AIN}	AN0 to AN7		AV_{SS}	—	AV_{RH}	V	
Reference voltage		AV_{RH}	AVRH	—	—	—	AV_{CC}	V	
Supply current	Conversion in operation	I_A	AV_{CC}	AV_{CC} = 3.3 V	—	3.0	5.0	mA	
	Conversion stopped	I_{AH}			—	—	5.0	µA	
Reference voltage supply current	Conversion in operation	I_R	AVRH	AV_{CC} = 3.3 V, AVRH = 3.3 V	—	2.0	3.0	mA	
	Conversion stopped	I_{RH}			—	—	10	µA	
Interchannel variation		—	AN0 to AN7	—	—	—	4	LSB	

Notes :
- The smaller the |AVRH| is, the greater the error is in general.
- The external circuit output impedance of analog input should be used in compliance with the following requirements :
  External circuit output impedance ≤ 2 (kΩ)
  If the output impedance of the external circuit is too high, an analog voltage sampling duration shortage might occur. (Sampling duration = 1.4 µs : @33 MHz)

- **A/D Converter Glossary**
- Resolution : Analog changes that are identifiable by the A/D converter.
- Linearity error : The deviation of the straight line connecting the zero transition point (00 0000 0000 ⟷ 00 0000 0001) with the full-scale transition point (11 1111 1110 ⟷ 11 1111 1111) from actual conversion characteristics.
- Differential linearity error : The deviation of input voltage needed to change the output code by one LSB from the theoretical value.
- Total error : The difference between actual and theoretical conversion values including a zero transition/full-scale transition/linearity error.



$$1\ \text{LSB'}\ (\text{theoretical value}) = \frac{\text{AVRH} - \text{AV}_{SS}}{1024} \quad [\text{V}]$$

$$V_{OT}\text{'}\ (\text{theoretical value}) = \text{AV}_{SS} + 0.5\ \text{LSB'} \quad [\text{V}]$$

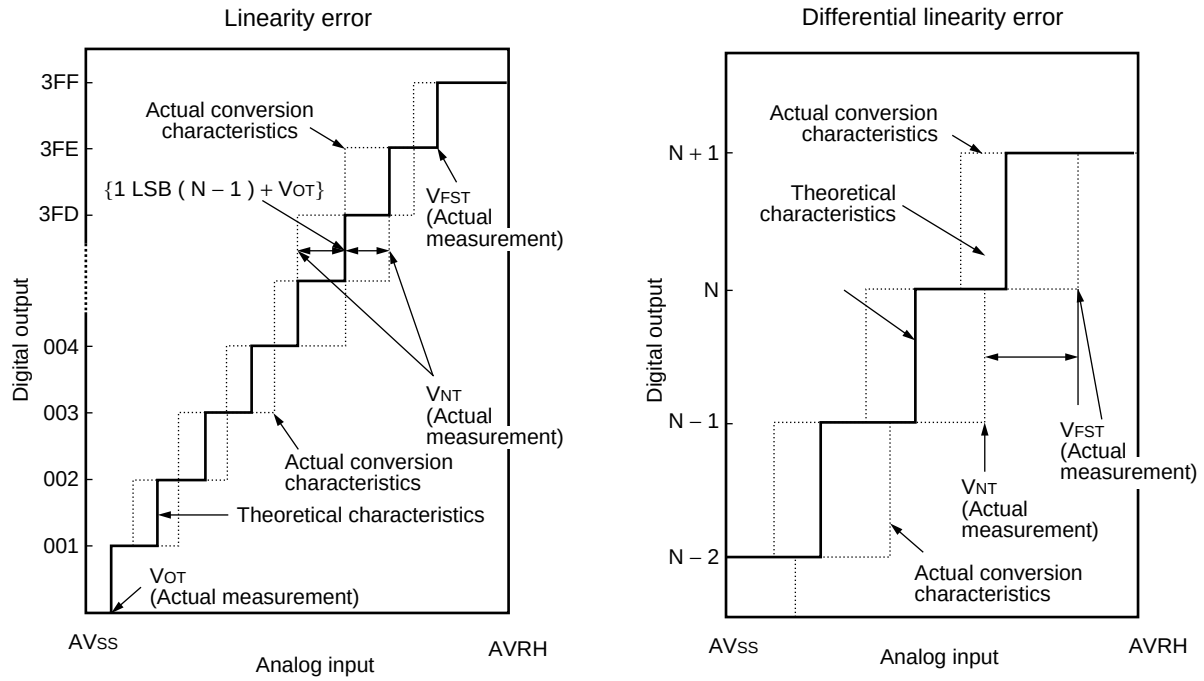
$$V_{FST}\text{'}\ (\text{theoretical value}) = \text{AVRH} - 1.5\ \text{LSB'} \quad [\text{V}]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (\text{N} - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

V_{NT} : Voltage at which digital output changes from (N + 1) to N.

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at which digital output changes from $(000)_H$ to $(001)_H$.

V_{FST} : Voltage at which digital output changes from $(3FE)_H$ to $(3FF)_H$.

6. D/A Converter Electrical Characteristics

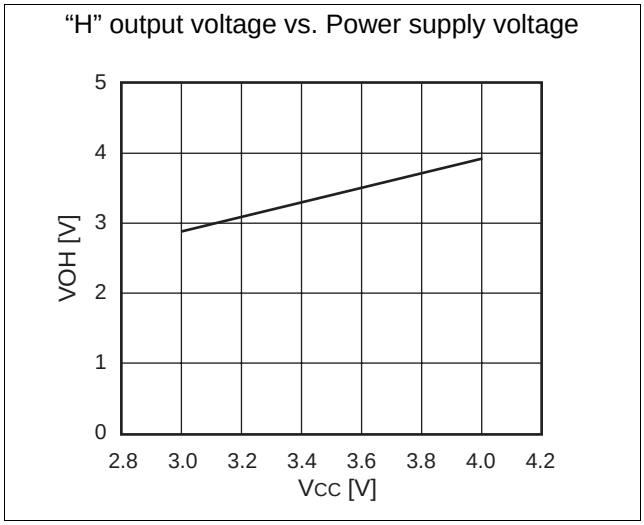
(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	—	8	Bit	
Differential linearity error	—	—	—	—	—	1	LSB	
Conversion time	—	—	—	—	—	20	µs	*
Analog output impedance	—	—	—	—	29	—	kΩ	

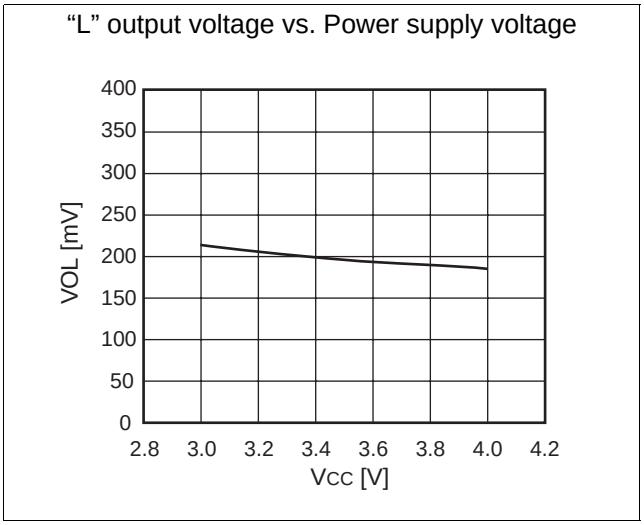
* : CL = 20 pF

■ EXAMPLE CHARACTERISTICS

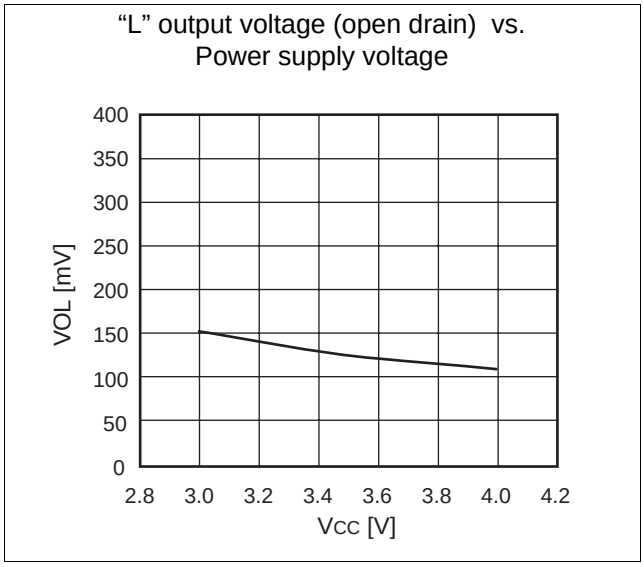
(1) “H” level output voltage



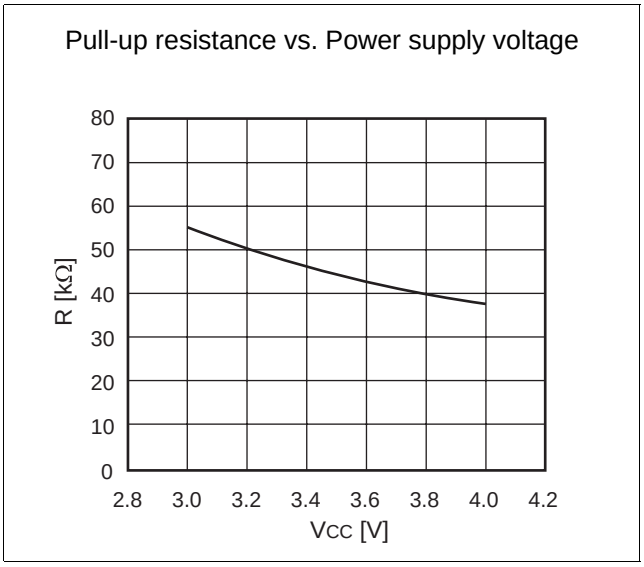
(2) “L” level output voltage



(3) “L” level output voltage (open drain)



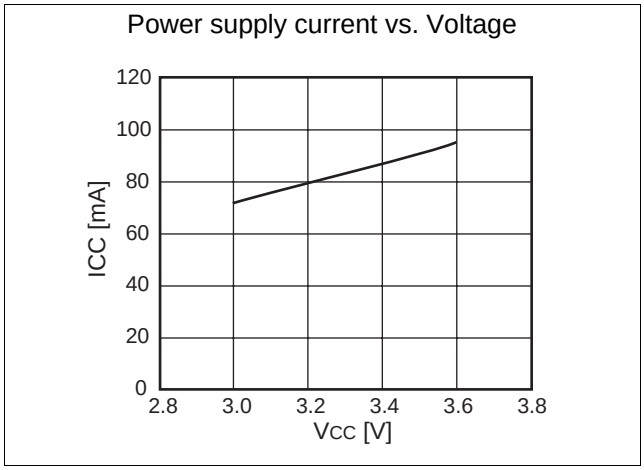
(4) Pull-up resistance



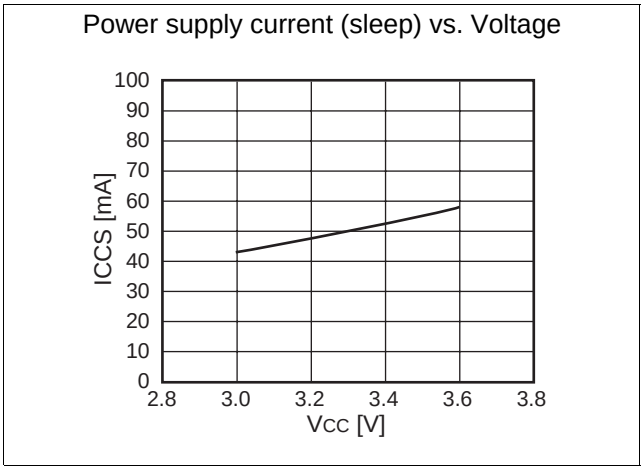
(Continued)

(Continued)

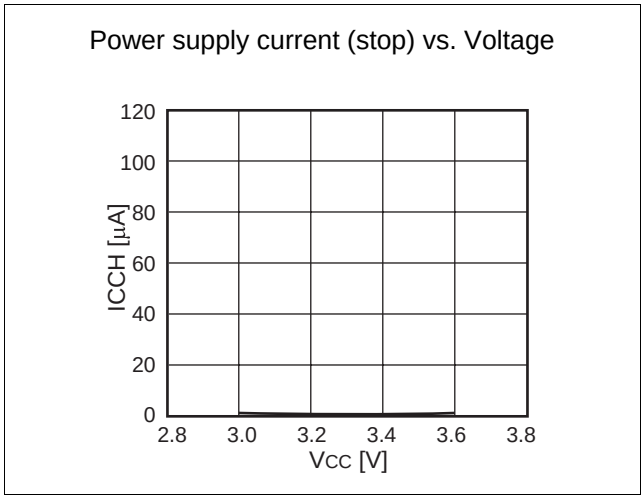
(5) Power supply current



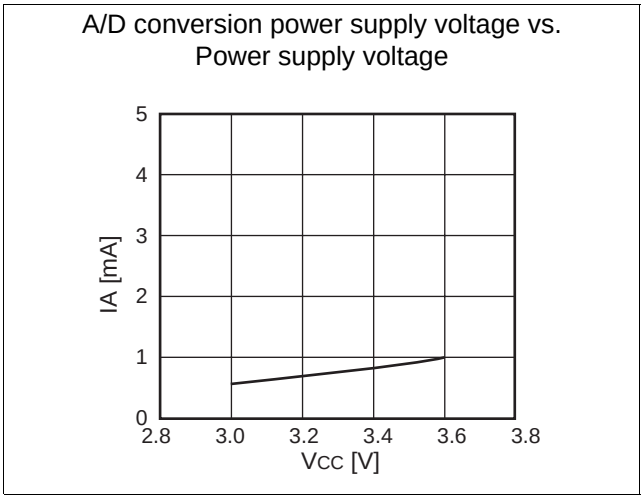
(6) Power supply current at sleeping



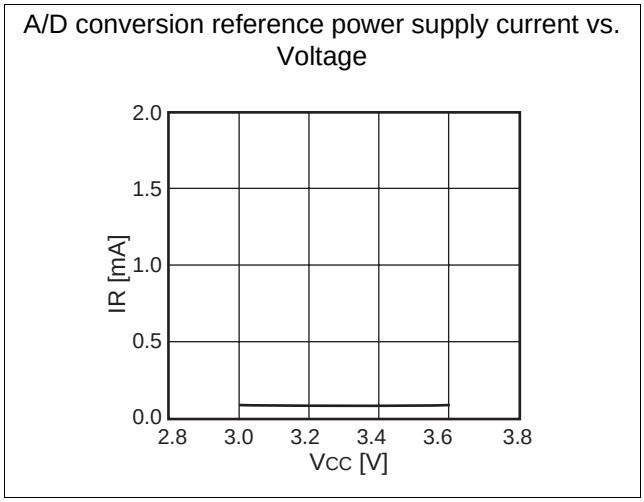
(7) Power supply current at stopping



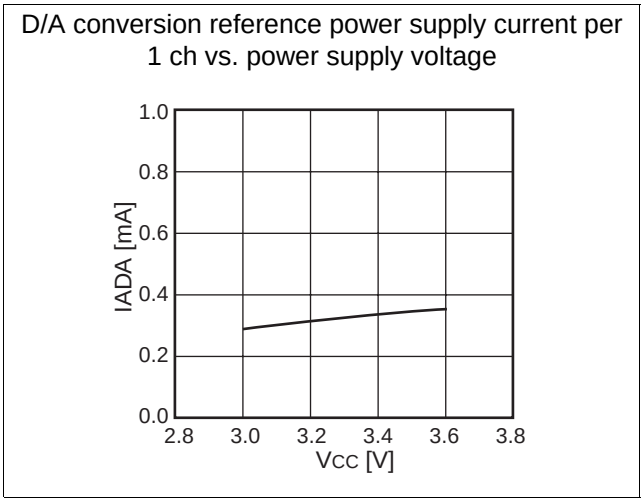
(8) A/D conversion power supply voltage (36 MHz)



(9) A/D conversion reference power supply current (36 MHz)



(10) D/A conversion reference power supply current per 1 ch



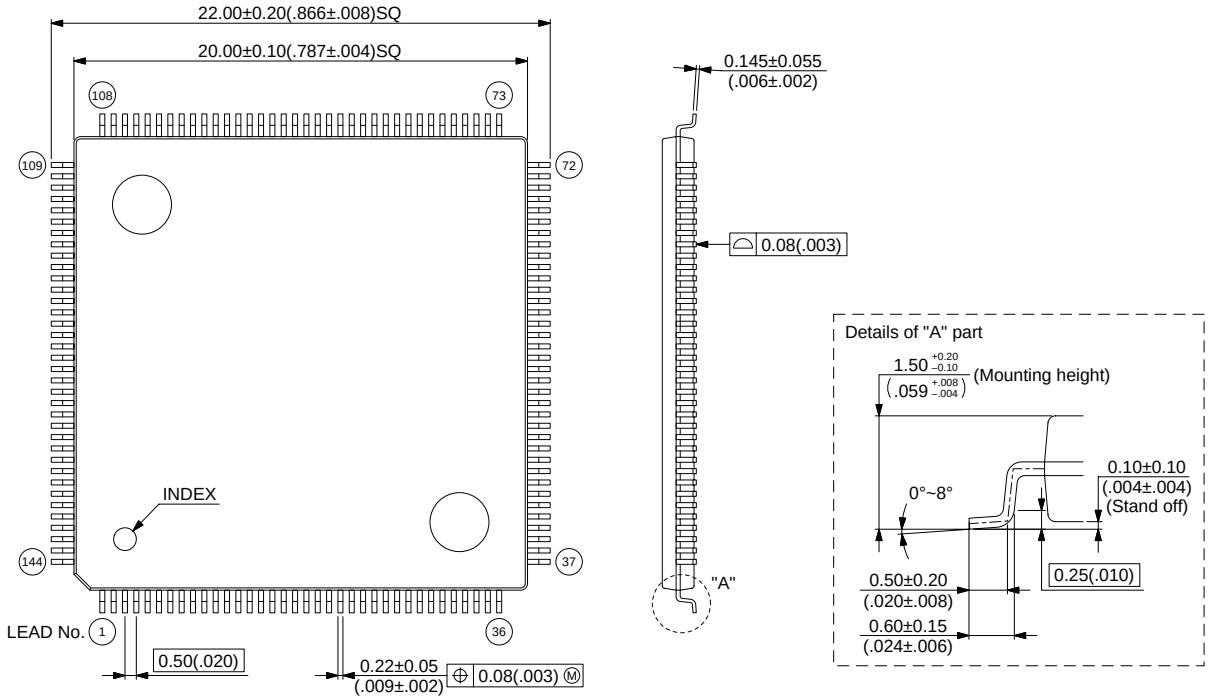
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91151APMT2-G	144-pin plastic LQFP (FPT-144P-M08)	

■ PACKAGE DIMENSION

144-pin plastic LQFP
(FPT-144P-M08)

*Pins width and pins thickness include plating thickness.



Dimensions in mm (inches)

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