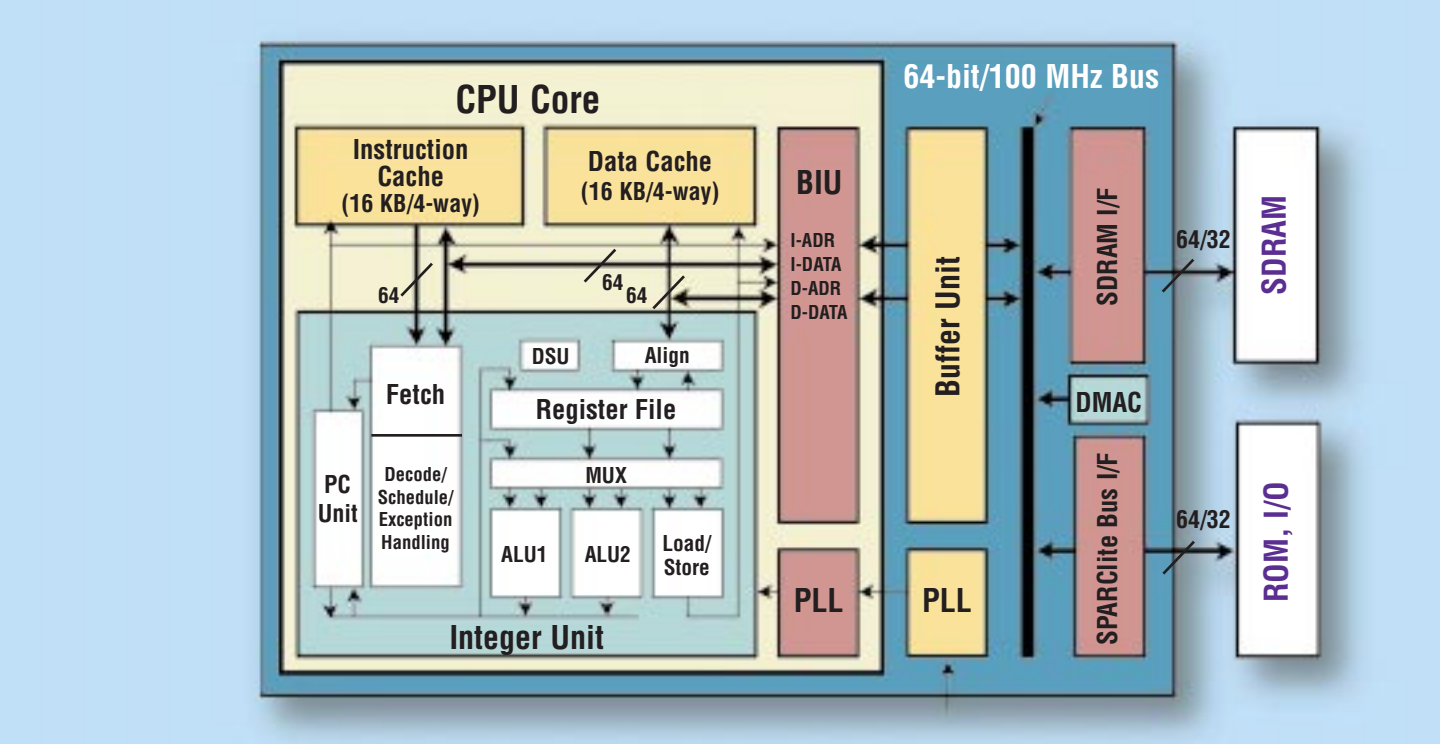
SPARClite Superscaler Embedded RISC Processor

MB86860



Features

- Internal Operating Frequency 200 MHz (max)
- 16 KB Instruction Cache (4-way)
- 16 KB Data Cache (4-way)
- PC-100 Compatible SDRAM Interface
- 8/16/32/64-bit Data Bus
- 2 DMA Channels
- Power-Down Mode

Description

The MB86860, based on the SPARC architecture from SPARC International, Inc., is a powerful embedded microprocessor that features a superscalar RISC CPU core and 64-bit SDRAM interface, along with 16 KB of each of I-cache and D-cache. With its 200-MHz superscalar CPU core capable of two simultaneous integer instructions, the device can perform integer arithmetic operations at a rate of approximately 420 MIPS, the highest level in its class.

Based on the SPARC architecture, the MB86860 series performs integer arithmetic operations compatible with conventional SPARC instructions running on Sun workstations. The MB86860 series has SPARClite buses compatible with the other SPARClite family devices so it can use existing hardware design resources such as peripheral chipsets, etc.

The MB86860 is targeted at network system applications, including hubs, routers, and systems that support ATM technology. The processor is also well suited for color printer applications. The MB86860 is available in a 352-pin BGA package.

SPARClite Superscalar Embedded RISC Processor

CPU Core	
Features	**Benefits**
Conforms to SPARC V8 architecture	Compatible with other SPARClite processors
Internal operating frequency maximum: 200 MHz	x1, x2, x3, x4, x5
2-issue super-scalar architecture	Higher performance
16 KB 4-way instruction cache	Faster local processing
16 KB 4-way data cache	Faster local processing
Power down mode	Saves power
Bi-endian support	Easy software development

SPARClite Bus Interface	
Features	**Benefits**
8/16/32/64-bit data bus	Backward hardware compatible with other SPARClite devices, design flexibility, cost savings
Burst-mode support	

Debug Support Functions	
Features	**Benefits**
Break function (instruction address/ external pins/software/single step)	Speeds up design debug
16-depth address trace buffer	Easier debug
Single step operation	Easier debug

Bus-Bridge DMA	
Features	**Benefits**
2 DMA channels	External bus-master support
Simultaneous operation: 1 channel	

Data Buffer Module	
Features	**Benefits**
4-column instruction Buffer	Minimal I/O latency
4-column x 2 read buffer	Minimal I/O latency
16-column write buffer	Minimal I/O latency

Other	
Features	**Benefits**
Core: 2.5V	Saves power
I/O Pins: 3.3V	Saves power
352-pin low-profile BGA package, no heat sink	Lower device cost

SDRAM Interface	
Features	**Benefits**
64/32 bit data bus widths	Design flexibility and cost savings
Maximum 100 MHz operation	PC-100 compatibility, faster memory access
Auto/self-refresh support	No glue logic
Parity function support	Flexible memory support

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