FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22005-1E

ASSP Communication Control

IEEE1394-SCSI Tailgate

MB86616

■ DESCRIPTION

The MB86616 is the LSI for protocol conversion to connect SCSI devices to the IEEE 1394 bus. This LSI integrates a 1394 controller compliant with the IEEE Standard for High Performance Serial Bus (IEEE Std. 1394-1995, or FireWire standard) and an SCSI protocol controller compliant with the SCSI-Fast20 standard on a single chip. It also incorporates the F²MC-16F as a processor for controlling the individual on-chip controllers, providing ease of control.

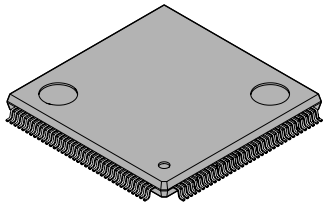
The IEEE 1394 controller unit has two ports for use in a cable environment and contains a differential transceiver and a comparator. It supports S400 data transfer rates. In addition, it supports the Chain command to continuously issue request packets for data transmission and reception, improving the efficiency of data transfer.

The SCSI protocol controller unit conforms to 8-bit Fast20 SCSI, enabling data transfer at a maximum of 20 Mbyte/s. For the SCSI bus terminal, the unit contains a totem pole type of single-end driver/receiver so that it can drive the SCSI bus directly.

While inheriting the AT architecture of the F²MC-16/16H family, the instruction set for the F²MC-16F CPU core incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions.

■ PACKAGE

144-pin Plastic LQFP



(FPT-144P-M08)

■ FEATURES

- **IEEE 1394 Controller Unit**
- Compliant with the IEEE Standard for High Performance Serial Bus (IEEE Std. 1394-1995
- Physical and link layer modules integrated on a single chip
- Two cable ports
- Data transfer rates supported : S100, S200, S400
- Data buffer dedicated to asynchronous transmission/reception
- 2-Kbyte (1/2/4 bank-switchable) , transmission/reception shared data buffer
- 128-byte buffer dedicated to asynchronous transmission and 128-byte buffer dedicated to asynchronous reception
- Automatic separation of the packet header and data upon reception and automatic packetization of information upon transmission
- 32-bit CRC generation and check functions
- Chain transfer function for data transfer sequence
- 4- and 4-conductor cables supported

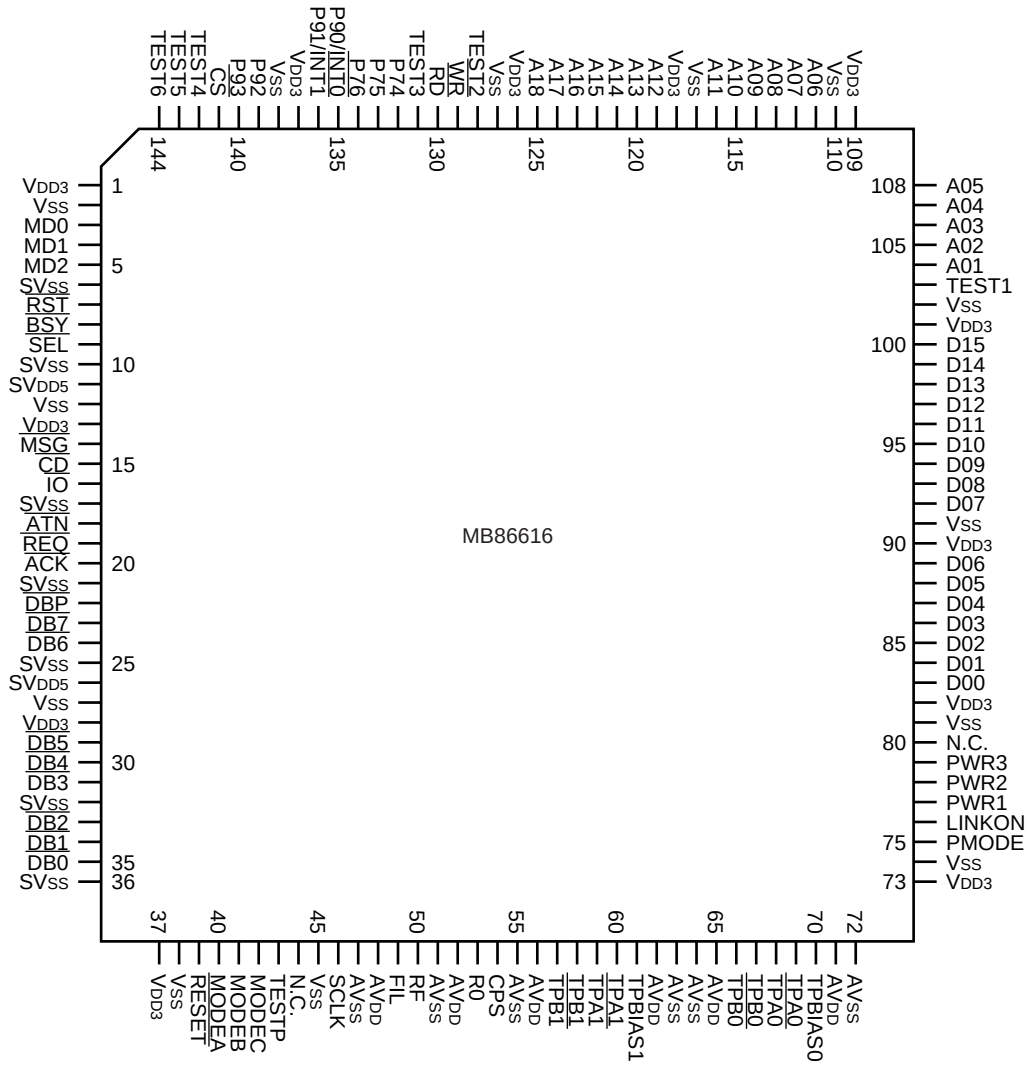
- **SCSI Protocol Controller Unit**
- Dedicated to initiator operation
- FAST-20 data transfer (8-bit)
  Synchronous transfer : 20 MBps Max. (Maximum offset value of 15)
  Asynchronous transfer : 5 MBps Max.
- Internal 16-byte FIFO data register
- Totem pole type of Fast20 single-end driver/receiver
- 28-bit transfer byte counter enabling simultaneous transfer of up to 256 Mbytes of data

- **F²MC-16F Unit**
- Minimum instruction execution time : 40.7 ns (at 24.576 MHz)
- Instruction set optimized for controller applications
- Instruction set supporting high-level languages (including C) and multi tasking

- **Miscellaneous**
- Supply voltage : 3.3 V and 5 V power supplies
- Package : LQFP-144 (FPT-144P-M08)

■ PIN ASSIGNMENT DRAWING

(TOP VIEW)



(FPT-144P-M08)

■ PIN ASSIGNMENT TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	—	V_{DD3}	37	—	V_{DD3}	73	—	V_{DD3}	109	—	V_{DD3}
2	—	V_{SS}	38	—	V_{SS}	74	—	V_{SS}	110	—	V_{SS}
3	ID	MD0	39	ID	$\overline{\text{RESET}}$	75	ID	PMODE	111	ID/O	A06
4	ID	MD1	40	ID	MODEA	76	O	LINKON	112	ID/O	A07
5	ID	MD2	41	ID	MODEB	77	ID	PWR1	113	ID/O	A08
6	—	SV_{SS}	42	ID	MODEC	78	ID	PWR2	114	ID/O	A09
7	SI/O	$\overline{\text{RST}}$	43	O	TESTP	79	ID	PWR3	115	ID/O	A10
8	SI/O	$\overline{\text{BSY}}$	44	—	N.C.	80	—	N.C.	116	ID/O	A11
9	SI/O	$\overline{\text{SEL}}$	45	—	V_{SS}	81	—	V_{SS}	117	—	V_{SS}
10	—	SV_{SS}	46	ID	SCLK	82	—	V_{DD3}	118	—	V_{DD3}
11	—	SV_{DD5}	47	—	AV_{SS}	83	ID/O	D00	119	ID/O	A12
12	—	V_{SS}	48	—	AV_{DD}	84	ID/O	D01	120	ID/O	A13
13	—	V_{DD3}	49	AO	FIL	85	ID/O	D02	121	ID/O	A14
14	SI/O	$\overline{\text{MSG}}$	50	AO	RF	86	ID/O	D03	122	ID/O	A15
15	SI/O	$\overline{\text{CD}}$	51	—	AV_{SS}	87	ID/O	D04	123	ID/O	A16
16	SI/O	$\overline{\text{IO}}$	52	—	AV_{DD}	88	ID/O	D05	124	ID/O	A17
17	—	SV_{SS}	53	AO	R0	89	ID/O	D06	125	ID/O	A18
18	SI/O	$\overline{\text{ATN}}$	54	I	CPS	90	—	V_{DD3}	126	—	V_{DD3}
19	SI/O	$\overline{\text{REQ}}$	55	—	AV_{SS}	91	—	V_{SS}	127	—	V_{SS}
20	SI/O	$\overline{\text{ACK}}$	56	—	AV_{DD}	92	ID/O	D07	128	O	TEST2
21	—	SV_{SS}	57	AI/O	$\overline{\text{TPB1}}$	93	ID/O	D08	129	IU/O	$\overline{\text{WR}}$
22	SI/O	$\overline{\text{DBP}}$	58	AI/O	TPB1	94	ID/O	D09	130	IU/O	$\overline{\text{RD}}$
23	SI/O	$\overline{\text{DB7}}$	59	AI/O	$\overline{\text{TPA1}}$	95	ID/O	D10	131	O	TEST3
24	SI/O	$\overline{\text{DB6}}$	60	AI/O	TPA1	96	ID/O	D11	132	ID/O	P74
25	—	SV_{SS}	61	AO	TPBIAS1	97	ID/O	D12	133	ID/O	P75
26	—	SV_{DD5}	62	—	AV_{DD}	98	ID/O	D13	134	ID/O	P76
27	—	V_{SS}	63	—	AV_{SS}	99	ID/O	D14	135	ID/O	P90/$\overline{\text{INT0}}$
28	—	V_{DD3}	64	—	AV_{SS}	100	ID/O	D15	136	ID/O	P91/$\overline{\text{INT1}}$
29	SI/O	$\overline{\text{DB5}}$	65	—	AV_{DD}	101	—	V_{DD3}	137	—	V_{DD3}
30	SI/O	$\overline{\text{DB4}}$	66	AI/O	$\overline{\text{TPB0}}$	102	—	V_{SS}	138	—	V_{SS}
31	SI/O	$\overline{\text{DB3}}$	67	AI/O	TPB0	103	O	TEST1	139	ID/O	P92
32	—	SV_{SS}	68	AI/O	$\overline{\text{TPA0}}$	104	ID/O	A01	140	ID/O	P93
33	SI/O	$\overline{\text{DB2}}$	69	AI/O	TPA0	105	ID/O	A02	141	IU/O	$\overline{\text{CS}}$
34	SI/O	$\overline{\text{DB1}}$	70	AO	TPBIAS0	106	ID/O	A03	142	O	TEST4
35	SI/O	$\overline{\text{DB0}}$	71	—	AV_{DD}	107	ID/O	A04	143	O	TEST5
36	—	SV_{SS}	72	—	AV_{SS}	108	ID/O	A05	144	O	TEST6

I/O types:

ID	: Digital input pin (with pull-down resistor)
O	: Digital output pin
ID/O	: Digital input/output pin (with pull-down resistor)
IU/O	: Digital input/output pin (with pull-up resistor)
SI/O	: SCSI input/output pin
AI	: Analog input pin
AO	: Analog output pin
AI/O	: Analog input/output pin

■ PIN DESCRIPTION

1. IEEE 1394 Interface

Signal name	I/O	Function
TPA0, TPA1	I/O	TPA positive-signal input/output pin at IEEE 1394 port
$\overline{\text{TPA0}}$, $\overline{\text{TPA1}}$	I/O	TPA negative-signal input/output pin at IEEE 1394 port
TPB0, TPB1	I/O	TPB positive-signal input/output pin at IEEE 1394 port
$\overline{\text{TPB0}}$, $\overline{\text{TPB1}}$	I/O	TPB negative-signal input/output pin at IEEE 1394 port
TPBIAS0, TPBIAS1	O	Common-voltage reference voltage output pin at IEEE 1394 port

2. SCSI Interface

Signal name	I/O	Function
$\overline{\text{REQ}}$, $\overline{\text{ACK}}$, $\overline{\text{ATN}}$, $\overline{\text{MSG}}$, $\overline{\text{CD}}$, $\overline{\text{IO}}$, $\overline{\text{RST}}$, $\overline{\text{BSY}}$, $\overline{\text{SEL}}$	I/O	SCSI control signal input/output pins
$\overline{\text{DB0}}$ to $\overline{\text{DB7}}$	I/O	Input/output pins for SCSI data bus
$\overline{\text{DBP}}$	I/O	Parity bit input/output pins for SCSI data bus

3. Internal CPU Pins (for Normal Operation Mode)

Note that the pin functions covered in this section are enabled only in the normal operation mode (with the MODEA pin = “L”) .

Signal name	I/O	Function
A01 to A18	O	Address output pins
D00 to D15	I/O	Data input pins
$\overline{\text{WR}}$	O	Write strobe signal output pin
$\overline{\text{RD}}$	O	Read strobe signal output pin
$\overline{\text{CS}}$	O	Pin to output the external flash ROM chip enable signal. This signal is output for accessing an address from F80000h to FFFFFFh in memory space.
P74 to P76 P90 to P93	I/O	General-purpose input/output port pins
MD0 to MD2	I	CPU block mode setting pins. Connect all of these pins to GND on this device.

4. CPU Interface (for External CPU Mode)

Note that the pin functions covered in this section are enabled only in the external CPU mode (with the MODEA pin = “H”) .

Signal name	I/O	Function
A01 to A09	I	External CPU address input pin
D00 to D15	I/O	External CPU data input/output pin
$\overline{CS}$	I	Pin to input the chip select signal to this device
$\overline{WR}$	I	Pin to input the write strobe signal to this device
$\overline{RD}$	I	Pin to input the read strobe signal to this device
$\overline{INT0}$	O	Interrupt request output pin for the IEEE 1394 block
$\overline{INT1}$	O	Interrupt request output pin for the SCSI block

5. Other Pins

Signal name	I/O	Function
$\overline{RESET}$	I	Reset signal input pin. Leave this pin at the “L” level while the IEEE 1394 block is operating with cable supplied power.
MODEA	I	Pin for setting the operation mode of this device. “L” input : Use the internal CPU. “H” input : Use an external CPU to control this device without using the internal CPU.
MODEB, MODEC	I	Connect these pins to GND.
SCLK	I	Reference clock input pin for the internal PLL (24.576 MHz)
RF	O	Connect this pin to GND via a 5.1 kΩ resistor.
FIL	O	External filter circuit connection pin for the internal PLL
R0	O	Connect this pin to GND via a 5.1 kΩ resistor.
CPS	I	Pin to input power supplied through the IEEE 1394 cable. The pin detects cable supplied power of 0 to 33 V (an external resistor is required to regulate/divide the voltage) . Connect this pin to GND if the device is not powered through the IEEE 1394 cable.
PMODE	I	Power input evaluation pin. “L” input : Operate the device with power supplied through the IEEE 1394 cable. (Only the IEEE 1394 block operates with the cable supplied power, with the other blocks left in the reset state.) “H” input : Operate the device with the system power supply.
PWR1 to PWR3	I	Pins to set the POWER_CLASS bit in the Self-ID packet which is transmitted during operation with power supplied through the IEEE 1394 cable. Note : The POWER_CLASS in the Self-ID packet transmitted during operation with the system power supply depends not on these pins but on the settings of the Pwr bits (Bits 2 to 0) in physical register #4.

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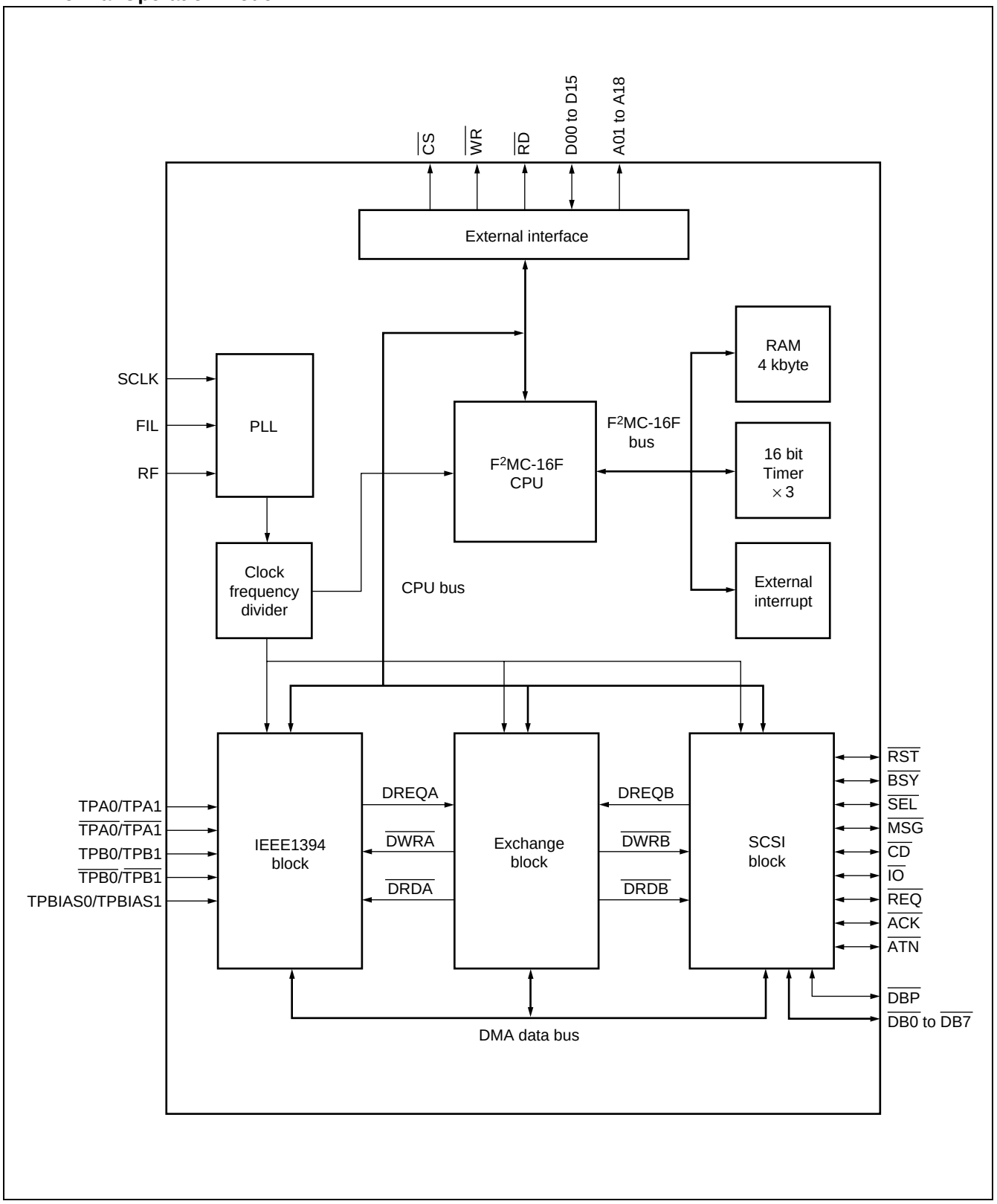
Signal name	I/O	Function
LINKON	O	Output pin for detection of Link-on packet reception. This pin outputs the “H” level signal upon reception of the Link-on packet during operation with power supplies through the IEEE 1394 cable. The output signal level changes to “L” the moment the PMODE signal becomes “H”. The output from this pin remains unchanged with PMODE = “H”. Leave this pin open when not in use.
TESTP, TEST1 to TEST6	O	Test pin. Leave it open.
N.C.	—	Leave this pin open.

6. Power/GND Pins

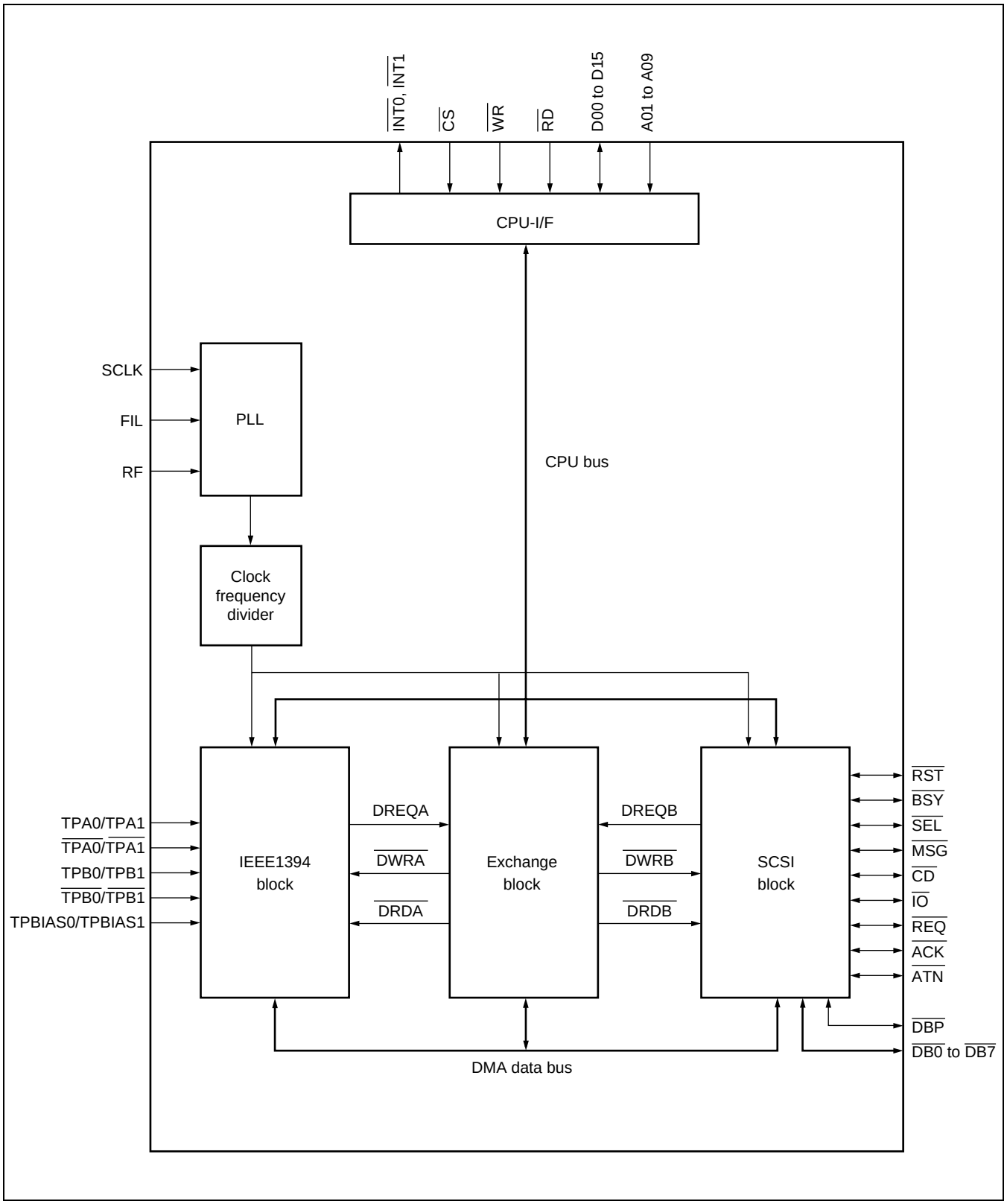
Signal name	I/O	Function
V_{DD3}	—	3.3 V digital power supply pin
V_{SS}	—	Digital ground pin
SV_{DD5}	—	5 V power supply pin for SCSI I/O
SV_{SS}	—	Ground pin for SCSI I/O
AV_{DD}	—	3.3 V analog power supply pin
AV_{SS}	—	Analog ground pin

■ BLOCK DIAGRAM

- **Normal Operation Mode**



- **External CPU Mode**



■ FUNCTIONS of BLOCKS

- **CPU Block**

This block controls the individual blocks. It incorporates the F²MC-16F as the core and RAM, 16-bit timers (3 channels) , and an external interrupt controller as peripheral circuits.

- **IEEE 1394 Block**

This block controls the IEEE 1394 interface.

- **SCSI Block**

This block controls the SCSI interface.

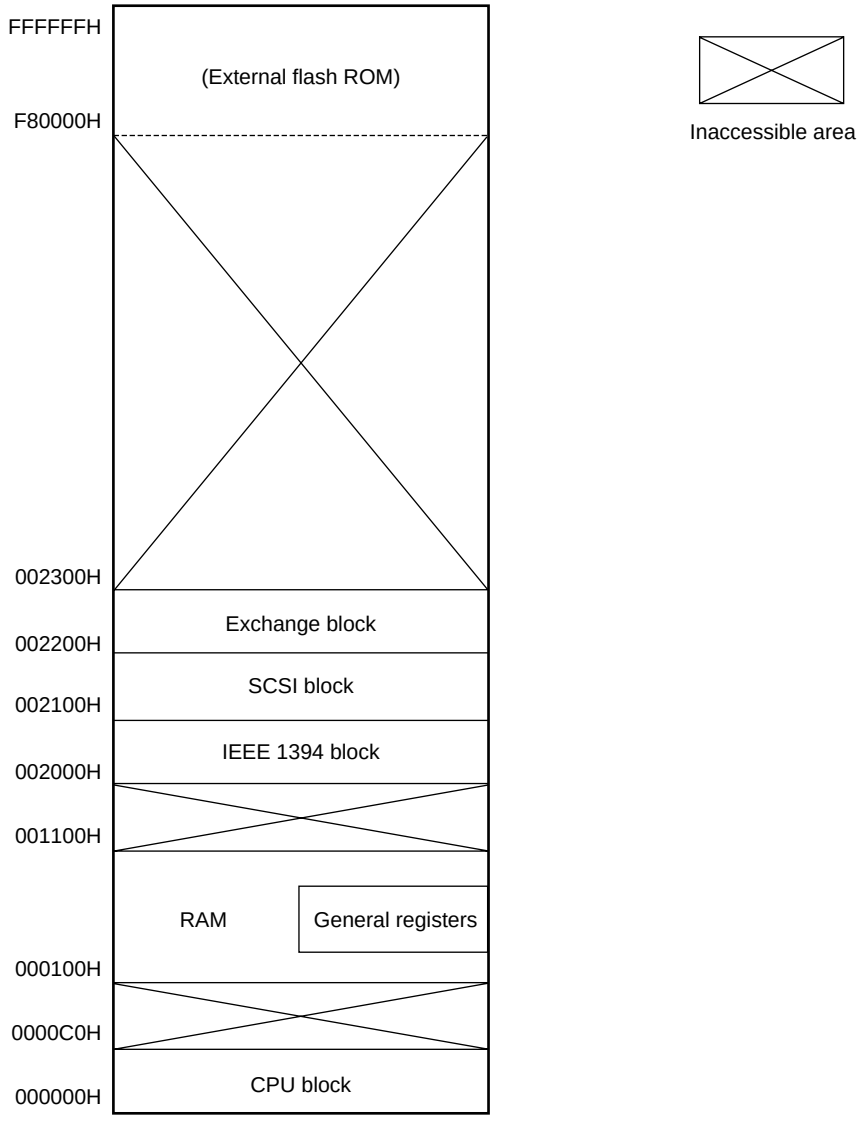
- **PLL Circuit**

This block generates clock signals for individual blocks from the reference clock signal generated by the clock module.

Reference oscillation frequency	: 24.576 MHz
Clock frequency for CPU block	: 24.576 MHz
Clock frequency for IEEE 1394 block	: 393.216 MHz (for bus) , 49.152 MHz (for internal operation)
Clock frequency for SCSI block	: 39.322 MHz
Clock frequency for Exchange block	: 39.322 MHz

■ INTERNAL REGISTERS

1. Memory Space



External ROM/external bus mode

2. CPU Block Internal Registers

Address (HEX)	WRITE operation		READ operation		Resource name
	Register name	Abbrevi-ation	Register name	Abbrevi-ation	
000000 to 000006	System reserved area	—	System reserved area	—	—
000007	Port-7 data register	PDR7	Port-7 data register	PDR7	Port 7
000008	System reserved area	—	System reserved area	—	—
000009	Port-9 data register	PDR9	Port-9 data register	PDR9	Port 9
00000A to 00000F	(reserved)	—	(reserved)	—	—
000010 to 000016	System reserved area	—	System reserved area	—	—
000017	Port-7 direction register	DDR7	Port-7 direction register	DDR7	Port 7
000018	System reserved area	—	System reserved area	—	—
000019	Port-9 direction register	DDR9	Port-9 direction register	DDR9	Port 9
000019 to 00002F	(reserved)	—	(reserved)	—	—
000030	Interrupt/DTP enable register	ENIR	Interrupt/DTP enable register	ENIR	DTP/external interrupt
000031	Interrupt/DTP source register	ENRR	Interrupt/DTP source register	ENRR	
000032	Request level set register	ELVR	Request level set register	ELVR	
000033 to 00003F	(reserved)	—	(reserved)	—	—
000040	Timer control status #0	TMCSR0	Timer control status #0	TMCSR0	16-bit timer #0
000041					
000042	(reserved)	—	16 bit timer #0	TMT0	
000043					
000044	16-bit timer reload #0	TMRLR0	(reserved)	—	
000045					
000046 to 000047	(reserved)	—	(reserved)	—	—
000048	Timer control status #1	TMCSR1	Timer control status #1	TMCSR1	16-bit timer #1
000049					
00004A	(reserved)	—	16 bit timer #1	TMT1	
00004B					
00004C	16 bit timer reload #1	TMRLR1	(reserved)	—	
00004D					
00004E to 00004F	(reserved)	—	(reserved)	—	—

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Address (HEX)	WRITE operation		READ operation		Resource name
	Register name	Abbrevi-ation	Register name	Abbrevi-ation	
000050	Timer control status #2	TMCSR2	Timer control status #2	TMCSR2	16-bit timer #2
000051					
000052	(reserved)	—	16 bit timer #2	TMT2	
000053					
000054	16 bit timer reload #2	TMRLR2	(reserved)	—	
000055					
000056 to 00008F	(reserved)	—	(reserved)	—	—
000090 to 00009E	System reserved area	—	System reserved area	—	—
00009F	Delayed interrupt source generate/reset register	DIRR	Delayed interrupt source generate/reset register	DIRR	Delayed interrupt
0000A0	Standby control register	STBYC	Standby control register	STBYC	Low power consumption
0000A1 to 0000A2	(reserved)	—	(reserved)	—	—
0000A3	Middle address control register	MACR	(reserved)	—	External pin
0000A4	High address control register	HACR	(reserved)	—	External pin
0000A5	External pin control register	EPCR	(reserved)	—	External pin
0000A6 to 0000A7	(reserved)	—	(reserved)	—	—
0000A8	Watchdog timer control register	TWC	Watchdog timer control register	TWC	Watchdog timer
0000A9	Time-base timer control register	TBTC	Time-base timer control register	TBTC	Time-base timer
0000AA to 0000AF	(reserved)	—	(reserved)	—	—
0000B0	Interrupt control register 0	ICR0	Interrupt control register 0	ICR0	Interrupt controller
0000B1	Interrupt control register 1	ICR1	Interrupt control register 1	ICR1	
0000B2	System reserved area	—	System reserved area	—	
0000B3	System reserved area	—	System reserved area	—	
0000B4	Interrupt control register 4	ICR4	Interrupt control register 4	ICR4	
0000B5	Interrupt control register 5	ICR5	Interrupt control register 5	ICR5	
0000B6	System reserved area	—	System reserved area	—	

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Address (HEX)	WRITE operation		READ operation		Resource name
	Register name	Abbrevi-ation	Register name	Abbrevi-ation	
0000B7	Interrupt control register 7	ICR7	Interrupt control register 7	ICR7	Interrupt controller
0000B8	Interrupt control register 8	ICR8	Interrupt control register 8	ICR8	
0000B9	Interrupt control register 9	ICR9	Interrupt control register 9	ICR9	
0000BA	Interrupt control register 10	ICR10	Interrupt control register 10	ICR10	
0000BB	System reserved area	—	System reserved area	—	
0000BC	System reserved area	—	System reserved area	—	
0000BD	System reserved area	—	System reserved area	—	
0000BE	System reserved area	—	System reserved area	—	
0000BF	Interrupt control register 15	ICR15	Interrupt control register 15	ICR15	

3. IEEE 1394 Block Internal Registers

Address (HEX)	WRITE operation		READ operation	
	Register name	Abbreviation	Register name	Abbreviation
002000	mode-control	MCTL	mode-control	MCTL
002002	(reserved)	—	flag & status	FLST
002004	instruction-fetch	INST	instruction-fetch	INST
002006	Interrupt-mask set register	INTM	Interrupt-code display register	INTC
002008	(reserved)	—	Reception acknowledge display register	RACK
00200A	A-buffer data port transmit register	SADP	A-buffer data port receive register	RADP
00200C	D-buffer data port transmit register	SDDP	D-buffer data port receive register	RDDP
00200E	(reserved)	—	(reserved)	—
002010	(reserved)	—	(reserved)	—
002012	Transmission ASYNC-des-ID set register	SADID	(reserved)	—
002014	Transmission ASYNC-PKT-param set register	SAPP	Reception ASYNC-PKT-param display register	RAPP
002016	Transmission ASYNC-data-length set register	SADL	Reception ASYNC-data-length display register	RADL
002018	Transmission ASYNC-ex-tcode set register	SAET	Reception ASYNC-ex-tcode display register	RAET
00201A	Transmission ASYNC-source-bus-ID set register	SASID	Reception ASYNC-source-ID display register	RASID
00201C	Transmission ASYNC-rcode set register	SARC	Reception ASYNC-rcode display register	RARC
00201E	Transmission ASYNC-des-offset set register (upper)	SADOU	Reception ASYNC-des-offset display register (upper)	RADOU
002020	Transmission ASYNC-des-offset set register (middle)	SADOM	Reception ASYNC-des-offset display register (middle)	RADOM
002022	Transmission ASYNC-des-offset set register (lower)	SADOL	Reception ASYNC-des-offset display register (lower)	RADOL
002024	Total chain data-length set register (upper)	CSDLU	Remaining chain data byte counter (upper)	CRBCU
002026	Total chain data length set register (lower)	CSDLL	Remaining chain data byte counter (lower)	CRBCL
002028	Chain transmission des-ID set register	CDID	Ping time monitor	PTMN
00202A	Chain transmission des-offset set register (upper)	CDOU	(reserved)	—
00202C	Chain transmission des-offset set register (middle)	CDOM	(reserved)	—

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Address (HEX)	WRITE operation		READ operation	
	Register name	Abbreviation	Register name	Abbreviation
00202E	Chain transmission des-offset set register (lower)	CDOL	(reserved)	—
002030	Chain transmission data-length set register	CSDL	Received packet transfer rate display register	PSPD
002032	Chain retry-limit set register	CRLM	Cycle-timer-monitor display register (upper)	CTMU
002034	(reserved)	—	Cycle-timer-monitor display register (lower)	CTML
002036	(reserved)	—	Revision display register	REVM
002038	PHY/LINK register address set register	PLRA	PHY/LINK register address set register	PLRA
00203A	PHY/LINK register access port (Write)	WPLAP	PHY/LINK register access port (Read)	RPLAP
00203C to 0000FE	(reserved)	—	(reserved)	—

4. SCSI Block Internal Registers

Address (HEX)	WRITE operation		READ operation	
	Register name	Abbreviation	Register name	Abbreviation
002100	Bus Device ID	BDID	Bus Device ID	BDID
002102	SCSI Control	SCTL	SCSI Control	SCTL
002104	SCSI Command	SCMD	SCSI Command	SCMD
002106	Transfer Mode	TMOD	Transfer Mode	TMOD
002108	Interrupt Sense	INTS	Interrupt Sense	INTS
00210A	SCSI Diagnostic Control	SDGC	Phase Sense	PSNS
00210C	(reserved)	—	SCSI Block Status	SSTS
00210E	(reserved)	—	SCSI Error Status	SERR
002110	Phase Control	PCTL	Phase Control	PCTL
002112	Extend Transfer Counter	TCE	Extend Transfer Counter	TCE
002114	Data Register (SCSI output)	DREG	Data Register (SCSI input)	DREG
002116	Temporary (SCSI output)	TEMP	Temporary (SCSI input)	TEMP
002118	Transfer Counter (High)	TCH	Transfer Counter (High)	TCH
00211A	Transfer Counter (Mid)	TCM	Transfer Counter (Mid)	TCM
00211C	Transfer Counter (Low)	TCL	Transfer Counter (Low)	TCL
00211E	REQ/ACK Timeout Set	RATO	Modified Byte Counter	MBC
002120 to 0000FE	(reserved)	—	(reserved)	—

5. Exchange Block Internal Registers

Address (HEX)	WRITE operation		READ operation	
	Register name	Abbreviation	Register name	Abbreviation
002200	Mode Control	EMOD	Mode Control	EMOD
002202	Signal Control	ESCTL	Signal Sense	ESSNS
002204	Data Port (Input)	EDPI	Data Port (Output)	EDPO
002206 to 0000FE	(reserved)	—	(reserved)	—

■ ABSOLUTE MAXIMUM RATINGS

(Vss = 0 V)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_{DD3}	V_{SS} – 0.5	4.0	V
	V_{DD5}*1	V_{SS} – 0.5	6.0	V
Input voltage	V_{I3}	V_{SS} – 0.5	V_{DD3} + 0.5	V
	V_{I5}*1	V_{SS} – 0.5	V_{DD5} + 0.5	V
Output voltage	V_{O3}	V_{SS} – 0.5	V_{DD3} + 0.5	V
	V_{O5}*1	V_{SS} – 0.5	V_{DD5} + 0.5	V
Ambient storage temperature	Tst	–55	+125	°C
Operating junction temperature	Tj	–40	+125	°C
Output current*2	I_O	I_{OL} = 4 mA	±14	mA
Overshoot	—	V_{DD3} + 1.0*3		V
Undershoot	—	V_{SS} – 1.0*3		V

*1 : For SCSI I/O

*2 : Maximum supply current which can flow in steady state. Exceeding it is allowed only within 1 second per LSI unit excluding the SCSI I/O.

*3 : Within 50 ns

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Vss = 0 V)

Parameter			Symbol	Values			Unit
				Min.	Typ.	Max.	
Power supply voltage	3.3 V power supply		V_{DD3}	3.0	3.3	3.6	V
	5 V power supply (for SCSI-I/O)		V_{DD5}	4.5	5.0	5.5	V
“H” level input voltage	CMOS Normal*1		V_{IHN}	$V_{DD3} \times 0.65$	—	$V_{DD3} + 0.3$	V
	CMOS Schmitt*2		V_{IHS}	$V_{DD3} \times 0.80$	—	$V_{DD3} + 0.3$	V
	SCSI		V_{IHSC}	2.0	—	$V_{DD5} + 0.3$	V
“L” level input voltage	CMOS Normal*1		V_{ILN}	V_{SS}	—	$V_{DD3} \times 0.25$	V
	CMOS Schmitt*2		V_{ILS}	V_{SS}	—	$V_{DD3} \times 0.20$	V
	SCSI		V_{ILSC}	V_{SS}	—	0.8	V
Differential input voltage (for data transfer)	IEEE1394		V_{IDD}	118	—	260	mV
Differential input voltage (for arbitration)	IEEE1394		V_{IDA}	168	—	265	mV
Common-mode input voltage	IEEE1394	S100	$V_{CM}100$	1.165	—	2.515	V
		S200	$V_{CM}200$	0.935	—	2.515	V
		S400	$V_{CM}400$	0.523	—	2.515	V
Receiving input jitter	IEEE1394		—	—	—	0.315	ns
Receiving input skew	IEEE1394		—	—	—	0.8	ns
Operating temperature			Ta	0	—	70	°C

*1 : D00 to D15

*2 : MD0 to MD2, $\overline{\text{RESET}}$, MODEA to MODEC, PMODE, PWR1 to PWR3, A01 to A18, $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, P74 to P76, P90 to P93, TEST2 to TEST6.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

The DC characteristics guarantee the worst-case values of static characteristics of the input/output buffers within the recommended operating condition ranges.

(1) Digital I/O Pins

(V_{DD3} = 3.3 ± 0.3 V, Vss = 0 V, Ta = 0 to 70 °C)

Parameter		Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
"H" level output voltage		V_{OH}	I_{OH} = –4 mA	V_{DD} – 0.5	—	V_{DD}	V
"L" level output voltage		V_{OL}	I_{OL} = 4 mA	V_{SS}	—	0.4	V
Output short-circuit current*1		I_{OS}	V_O = 0 V or V_{DD}	—	—	± 60	mA
Input leakage current*2	Normal Input	I_{LI}	V_I = 0 V to V_{DD}	–5	—	5	µA
	3state Input	I_{LZ}					
Input resistance	pull-up	Rpu	V_{IL} = 0 V	25	50	200	kΩ
	pull-down	Rpd	V_{IH} = V_{DD}				

*1 : Maximum current that flows when the output pin is connected to Vdd or Vss, for one second per LSI pin.

*2 : The input leakage current may exceed the above value when an input buffer with pull-up or pull-down resistor is used.

(2) SCSI I/O Pins

(V_{DD5} = 5.0 ± 0.5 V, Vss = 0 V, Ta = 0 to 70 °C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
"H" level output voltage	V_{OHSC}	I_{OH} = –7 mA	2	—	V_{DD}	V
"L" level output voltage	V_{OLSC}	I_{OL} = 48 mA	V_{SS}	—	0.5	V
Input hysteresis voltage width	V_{HYS}	—	0.2	—	—	V

(3) IEEE 1394 Driver and Comparator

- **Driver**

(V_{DD3} = 3.3 ± 0.3 V, Vss = 0 V, Ta = 0 to 70 °C)

Parameter		Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Differential output voltage		V_{OD}	R_L = 56 Ω	172	—	265	mV
Common-mode output current	S100	I_{CM}	Driver enable, signaling off	–0.81	—	0.44	mA
	S200	$I_{SP}200$	S200 speed signaling enable	–2.53	—	–4.84	mA
	S400	$I_{SP}400$	S400 speed signaling enable	–8.10	—	–12.40	mA
Off-state voltage		V_{OFF}	Driver disable	—	—	20	mV
Common-mode output voltage	S100	V_{OM}	Driver enable, signaling off	1.665	—	2.015	V
	S200	$V_{SP}200$	S200 speed signaling enable	1.438	—	2.015	V
	S400	$V_{SP}400$	S400 speed signaling enable	1.030	—	2.015	V

- **Comparator**

(V_{DD3} = 3.3 ± 0.3 V, Vss = 0 V, Ta = 0 to 70 °C)

Parameter		Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Common-mode input current		I_{IC}	Driver disable	–20	—	20	µA
Arbitration Comparator	H-level detection	V_{ACH}	—	168	—	—	mV
	Z-level detection	V_{ACZ}	—	–89	—	89	mV
	L-level detection	V_{ACL}	—	—	—	168	mV
Port-status Comparator	connection detection	V_{PCH}	—	1.0	—	—	V
	disconnection detection	V_{PCL}	—	—	—	0.6	V

(4) Supply Current

(V_{DD3} = 3.3 ± 0.3 V, V_{DD5} = 5.0 ± 0.5 V, Vss = 0 V, Ta = 0 to 70 °C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Supply current (3.3 V power supply)	I_{DD3}	—	—	—	300	mA
Supply current (5.0 V power supply)	I_{DD5}	—	—	—	100	mA

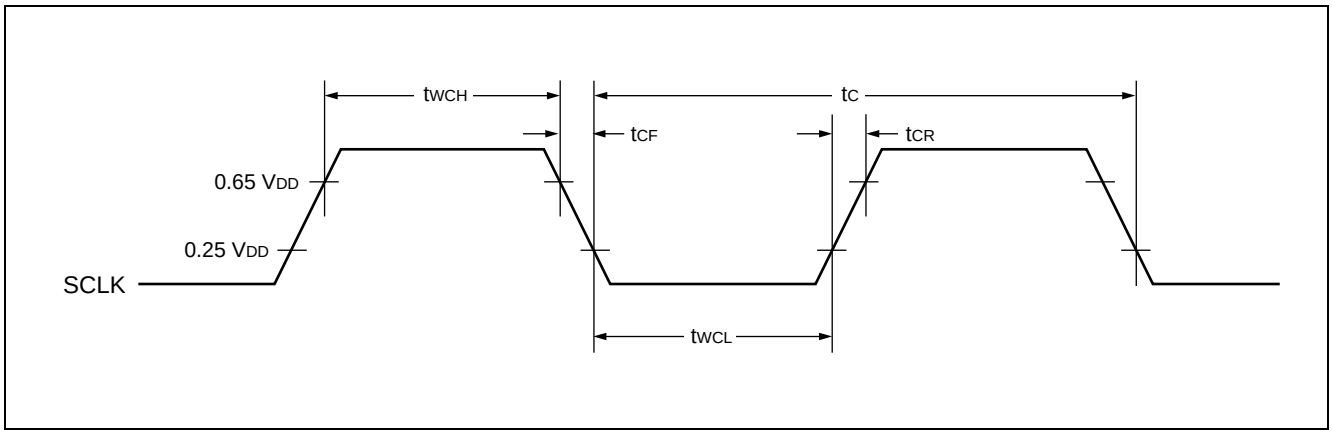
2. AC CHARACTERISTICS

(1) Clock Input

Parameter		Symbol	Pin name	Values			Unit
				Min.	Typ.	Max.	
Clock frequency		F_C	SCLK	—	24.576	—	MHz
Clock cycle time		t_C		—	$1/F_C$	—	ns
"H" and "L" level clock pulse widths		t_{WCH}, t_{WCL}		15	—	—	ns
Clock rise time, clock fall time		t_{CR}, t_{CF}		—	—	3	ns
Clock input to each block	CPU block	F_{CPU}	—	—	24.576	—	MHz
		t_{CPU}	—	—	1/Fcpu	—	ns
	IEEE 1394 block	F_{1394}	—	—	393.216	—	MHz
	SCSI block	F_{SCSI}	—	—	39.322	—	MHz
		t_{SCSI}	—	—	1/Fscsi	—	ns
	Exchange block	F_{EXC}	—	—	39.322	—	MHz
CPU block machine clock (Note 1)		t_{CYC}	—	tcpu	—	16 tcpu	ns
IEEE 1394 bus (Note 2)		F_{1394B}	—	98.304	196.608	393.216	MHz
SCSI bus (Synchronous transfer)		F_{SCSIB}	—	1.229	—	19.661	MHz

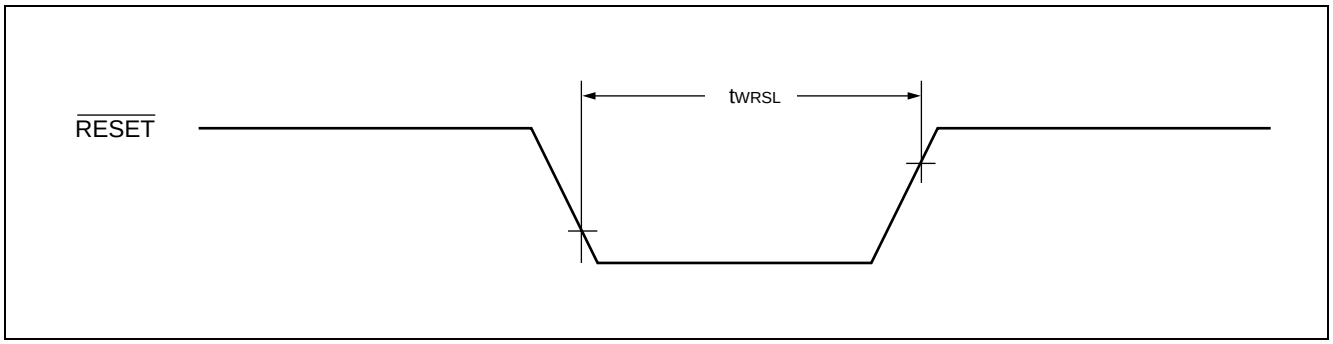
Note1 : The maximum value assumes the minimum speed (1/16) set by the clock gear feature.

Note2 : The values are transfer rates at S100/S200/S400.



(2) Reset Input

Parameter	Symbol	Pin name	Values			Unit
			Min.	Typ.	Max.	
“L” level reset pulse width	t_{WRSL}	$\overline{RESET}$	5 tcp	—	—	ns



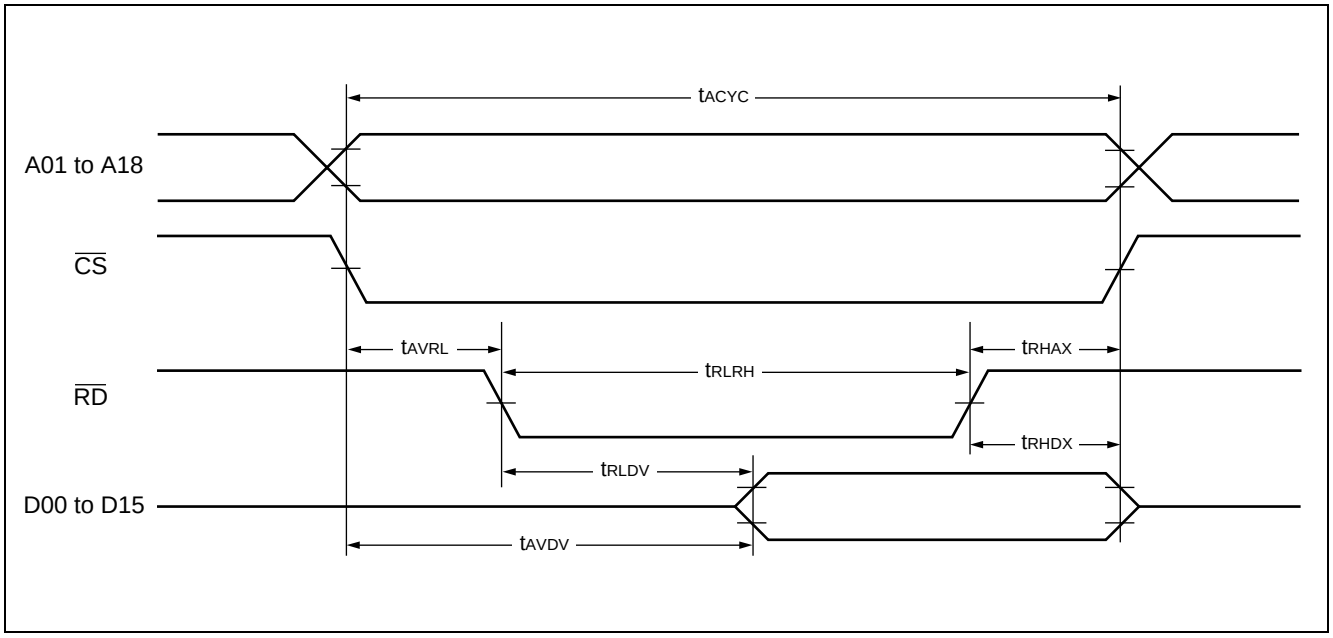
(3) External Bus Interface (Flash ROM Interface)

3-1 Bus Read

(Load pin capacitance = 30 pF)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Address cycle time	t_{ACYC}	A01 to A18, $\overline{CS}$	(2 + n*) tcyc – 10	—	ns
Valid address→$\overline{RD}$↓	t_{AVRL}	A01 to A18, $\overline{CS}$, $\overline{RD}$	tcyc / 2 – 13	—	ns
$\overline{RD}$ "L" level pulse width	t_{RLRH}	$\overline{RD}$	(1 + n*) tcyc – 25	—	ns
$\overline{RD}$↓ →Valid data	t_{RLDV}	$\overline{RD}$, D00 to D15	—	(1 + n*)tcyc – 30	ns
$\overline{RD}$↑→Data hold	t_{RHDX}	$\overline{RD}$, D00 to D15	0	—	ns
Valid address→Valid data	t_{AVDV}	A01 to A18, $\overline{CS}$, D00 to D15	—	(3 / 2 + n*)tcyc – 10	ns
$\overline{RD}$↑→Valid address	t_{RHAX}	$\overline{RD}$, A01 to A18, $\overline{CS}$	tcyc / 2 – 20	—	ns

*: n is the number of wait cycle.(no wait ; n = 0)
The number of wait cycle is set by external pin control registor.

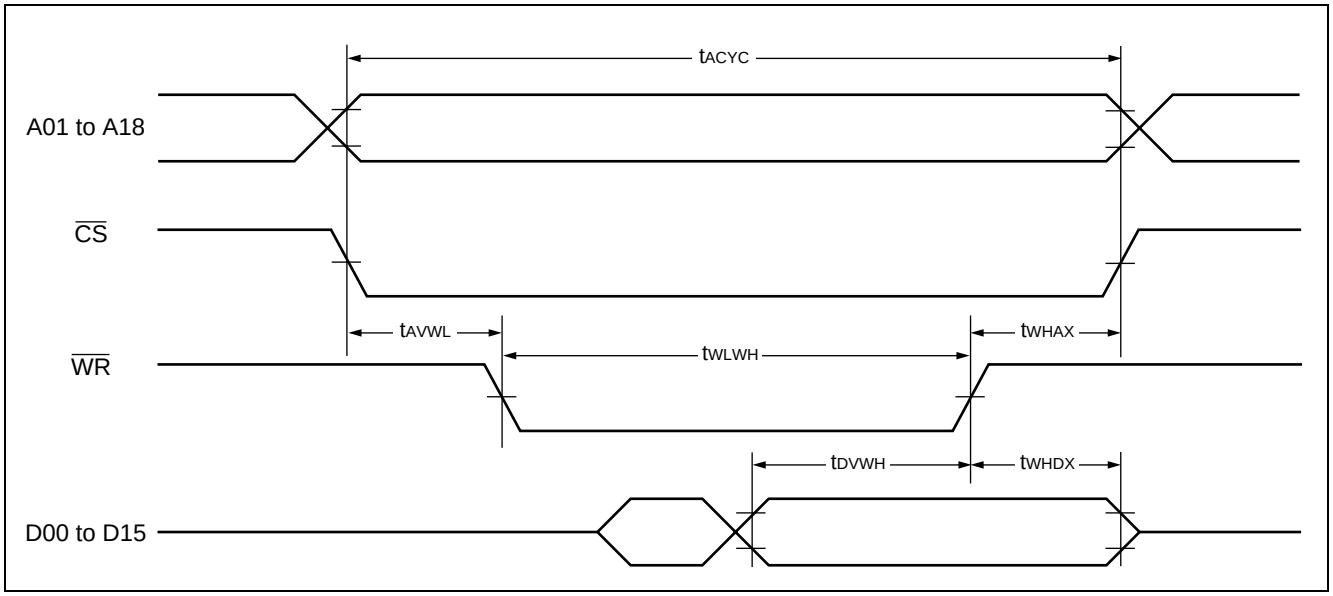


3-2 Bus Write

(Load pin capacitance = 30 pF)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Address cycle time	t_{ACYC}	A01 to A18, $\overline{CS}$	(2 + n*) tcyc – 10	—	ns
Valid address→$\overline{WR}$↓	t_{AVWL}	A01 to A18, $\overline{CS}$, $\overline{WR}$	tcyc / 2 – 13	—	ns
$\overline{WR}$ "L" level pulse width	t_{WLWH}	$\overline{WR}$	(1 + n*) tcyc – 20	—	ns
Written data→$\overline{WR}$↑	t_{DVWH}	$\overline{WR}$, D00 to D15	(1 + n*) tcyc – 25	—	ns
$\overline{WR}$↑→Data hold	t_{WHDX}	$\overline{WR}$, D00 to D15	tcyc / 2 – 15	—	ns
$\overline{WR}$↑→Valid address	t_{WHAX}	$\overline{WR}$, A01 to A18, $\overline{CS}$	tcyc / 2 – 15	—	ns

*: n is the number of wait cycle.(no wait ; n = 0)
The number of wait cycle is set by external pin control registor.



(4) IEEE 1394 Driver

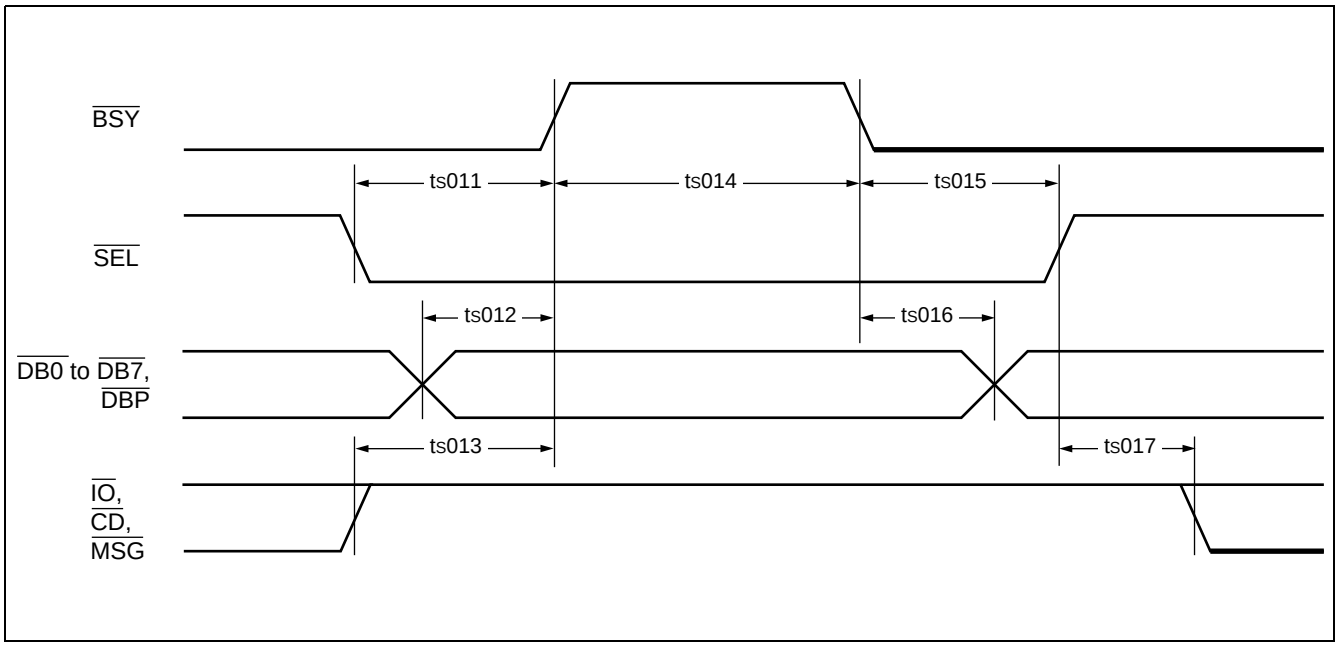
Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Transmission jitter	t_{JT}	TPA, $\overline{TPA}$, TPB, $\overline{TPB}$	—	±0.15	ns
Transmission skew	t_{DK}		—	±0.10	ns
Transmission rise time, fall time *	t_{DR}, t_{DF}		—	1.2	ns

* : Measurement conditions : C_L = 10 pF, R_L = 56 Ω

(5) SCSI Interface

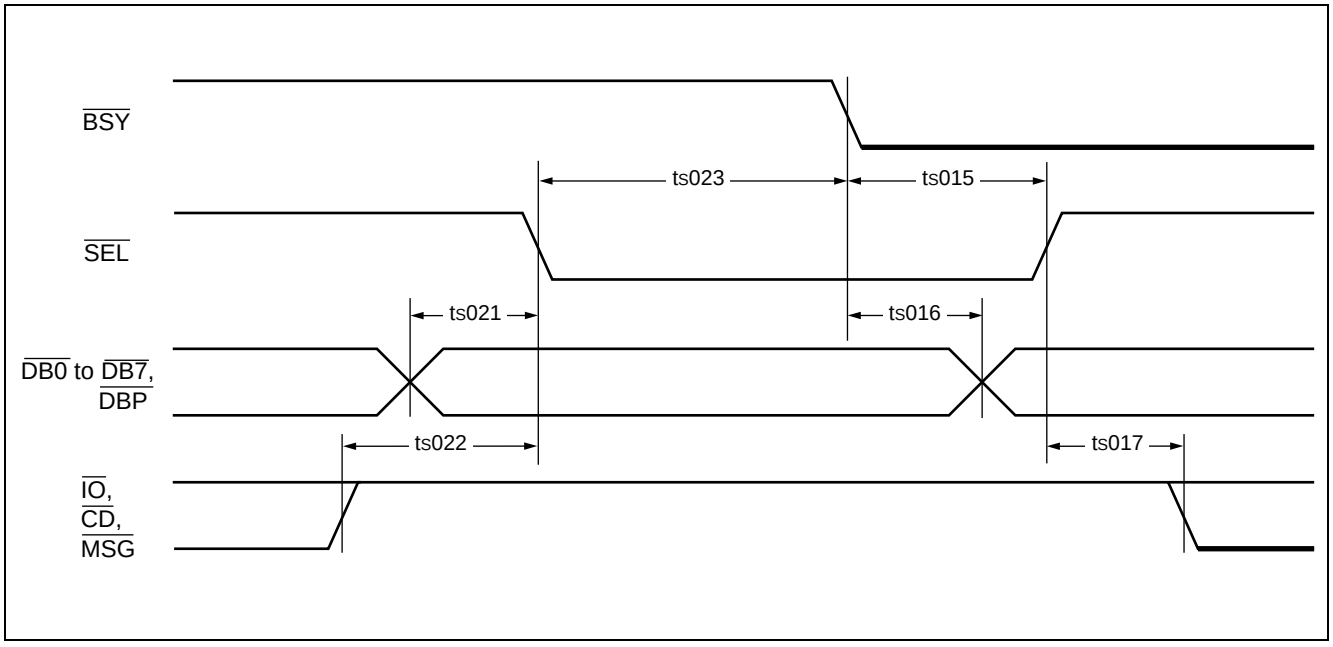
5-1 Target Selection Operation (with Arbitration)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{SEL}\downarrow\rightarrow\overline{BSY}\uparrow$	ts011	$\overline{SEL}$, $\overline{BSY}$	0	—	ns
ID assert$\rightarrow\overline{BSY}\uparrow$	ts012	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$	0	—	ns
$\overline{IO}\uparrow\rightarrow\overline{BSY}\uparrow$	ts013	$\overline{IO}$, $\overline{BSY}$	0	—	ns
$\overline{BSY}\uparrow\rightarrow\overline{BSY}\downarrow$	ts014	$\overline{BSY}$	18 tscsi	19 tscsi + 20	ns
$\overline{BSY}\downarrow\rightarrow\overline{SEL}\uparrow$	ts015	$\overline{BSY}$, $\overline{SEL}$	0	—	ns
$\overline{BSY}\downarrow\rightarrow$ID hold	ts016	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$	10	—	ns
$\overline{SEL}\uparrow\rightarrow$Phase signal output	ts017	$\overline{SEL}$, $\overline{IO}$ $\overline{CD}$, $\overline{MSG}$	9 tscsi	10 tscsi + 20	ns



5-2 Target Selection Operation (without Arbitration)

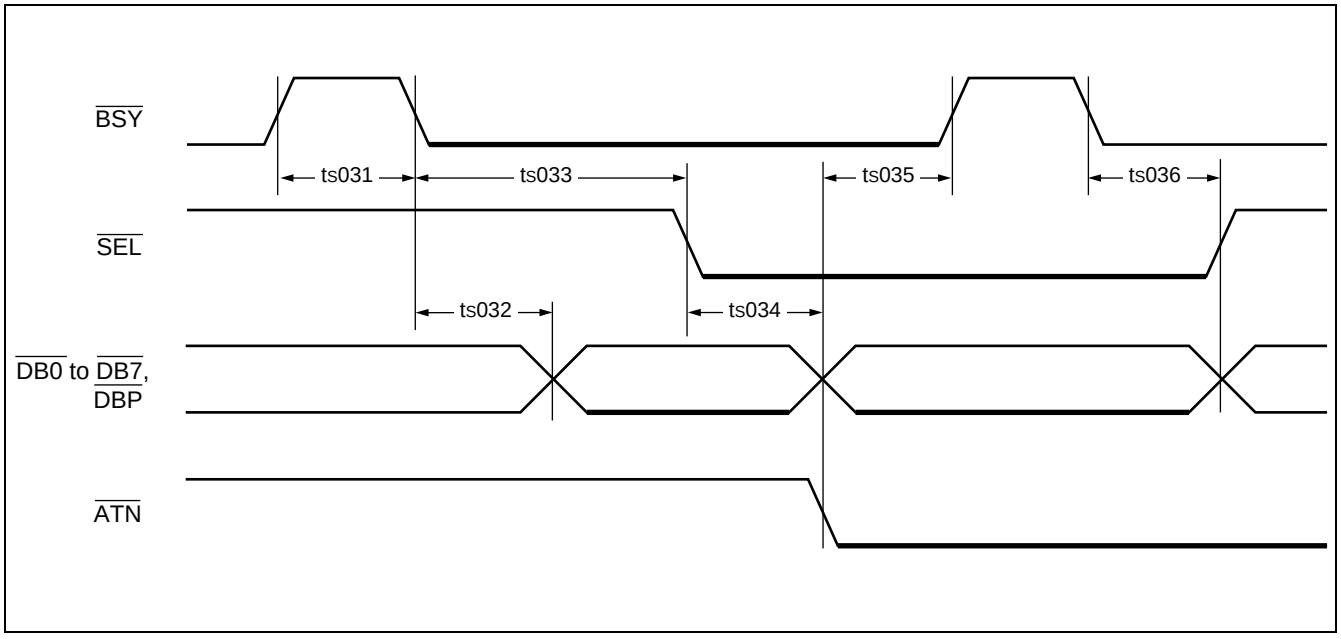
Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
ID assert→$\overline{SEL}$↓	ts021	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{SEL}$	0	—	ns
$\overline{IO}$↑→$\overline{SEL}$↓	ts022	$\overline{IO}$, $\overline{SEL}$	0	—	ns
$\overline{SEL}$↓→$\overline{BSY}$↓	ts023	$\overline{SEL}$, $\overline{BSY}$	18 tscsi	19 tscsi + 20	ns
$\overline{BSY}$↓→$\overline{SEL}$↑	ts015	$\overline{BSY}$, $\overline{SEL}$	0	—	ns
$\overline{BSY}$↓→ID hold	ts016	$\overline{BSY}$, $\overline{DBP}$ $\overline{DB0}$ to $\overline{DB7}$	10	—	ns
$\overline{SEL}$↑ →Phase signal output	ts017	$\overline{SEL}$, $\overline{IO}$, $\overline{CD}$, $\overline{MSG}$	9 tscsi	10 tscsi + 20	ns



5-3 Initiator Selection Operation (with Arbitration)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Bus free→$\overline{\text{BSY}}$↓	ts031	$\overline{\text{BSY}}$	(21 + n*) tscsi	(22 + n*) tscsi + 20	ns
$\overline{\text{BSY}}$↓→Self-ID output	ts032	$\overline{\text{BSY}}$, $\overline{\text{DBP}}$, $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$	0	15	ns
$\overline{\text{BSY}}$↓→$\overline{\text{SEL}}$↓	ts033	$\overline{\text{BSY}}$, $\overline{\text{SEL}}$	128 tscsi − 10	128 tscsi + 15	ns
$\overline{\text{SEL}}$↓→$\overline{\text{ATN}}$↓ & ID output	ts034	$\overline{\text{SEL}}$, $\overline{\text{ATN}}$, $\overline{\text{DBP}}$, $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$	52 tscsi − 10	52 tscsi + 15	ns
ID output→$\overline{\text{BSY}}$↑	ts035	$\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, $\overline{\text{BSY}}$	8 tscsi − 10	8 tscsi + 15	ns
$\overline{\text{BSY}}$↓→$\overline{\text{SEL}}$↑ & ID hold	ts036	$\overline{\text{BSY}}$, $\overline{\text{SEL}}$, $\overline{\text{DBP}}$, $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$	8 tscsi	9 tscsi + 20	ns

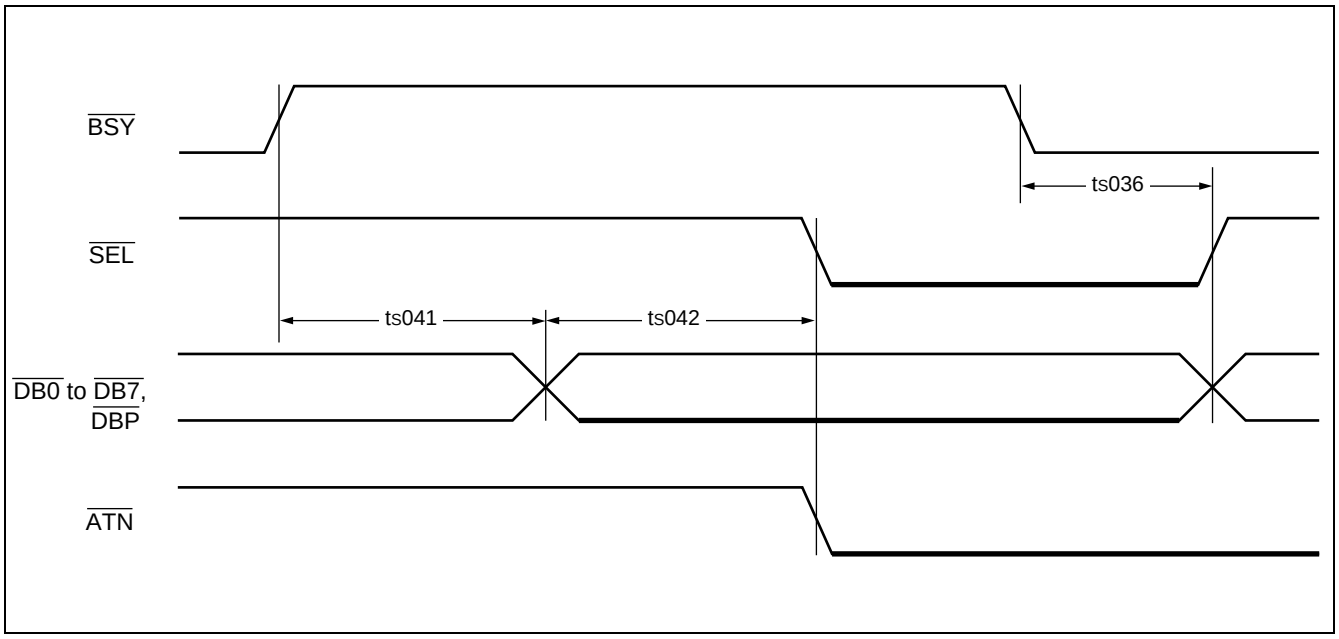
* : SCSI block TCL register value



5-4 Initiator Selection Operation (without Arbitration)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Bus free→ID output	ts041	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$	(21 + n*) tscsi	(22 + n*) tscsi + 10	ns
ID output→$\overline{SEL}$↓ & $\overline{ATN}$↓	ts042	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{SEL}$, $\overline{ATN}$	44 tscsi − 15	44 tscsi + 10	ns
$\overline{BSY}$↓→$\overline{SEL}$↑ & ID hold	ts036	$\overline{BSY}$, $\overline{SEL}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	8 tscsi	9 tscsi + 20	ns

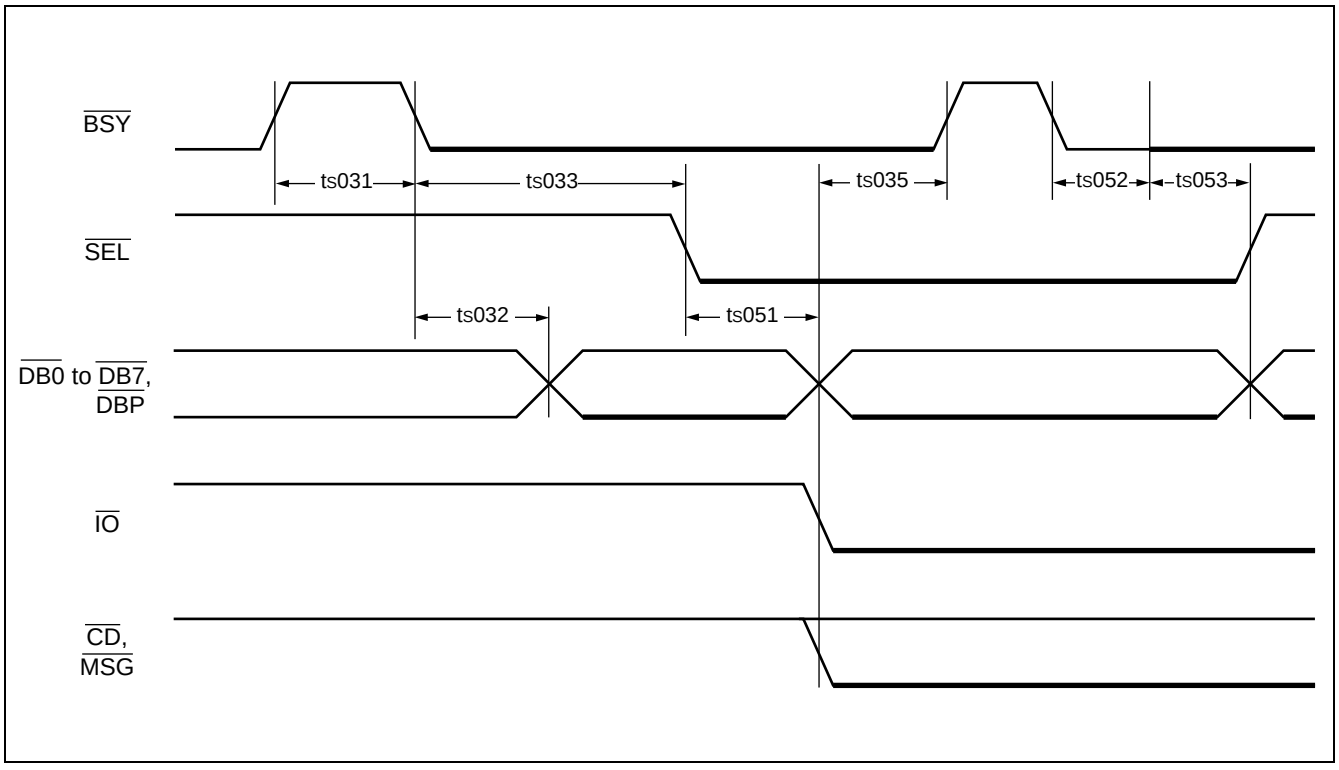
* : SCSI block TCL register value



5-5 Target Reselection Operation

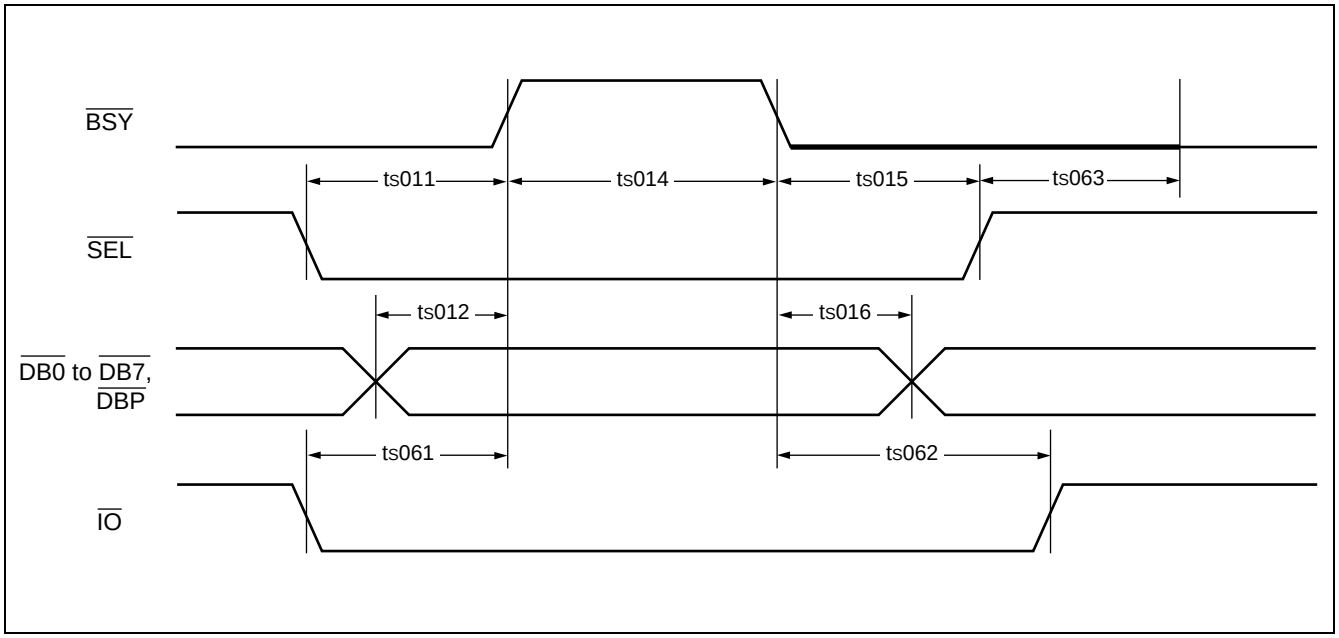
Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Bus free→$\overline{BSY}$↓	ts031	$\overline{BSY}$	(21 + n*) tscsi	(22 + n*) tscsi + 20	ns
$\overline{BSY}$↓ →Self-ID output	ts032	$\overline{BSY}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	0	15	ns
$\overline{BSY}$↓→$\overline{SEL}$↓	ts033	$\overline{BSY}$, $\overline{SEL}$	128 tscsi – 10	128 tscsi + 15	ns
$\overline{SEL}$↓→Phase signal & ID output	ts051	$\overline{SEL}$, $\overline{IO}$, $\overline{CD}$, $\overline{MSG}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	52 tscsi – 10	52 tscsi + 15	ns
ID output→$\overline{BSY}$↑	ts035	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$	8 tscsi – 10	8 tscsi + 15	ns
$\overline{BSY}$↓→$\overline{BSY}$↓output	ts052	$\overline{BSY}$	8 tscsi	9 tscsi + 20	ns
$\overline{BSY}$↓output→ $\overline{SEL}$↑ & ID hold	ts053	$\overline{BSY}$, $\overline{SEL}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	4 tscsi	9 tscsi + 20	ns

* : SCSI block TCL register value



5-6 Initiator Reselection Operation

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{SEL}\downarrow\rightarrow\overline{BSY}\uparrow$	ts011	$\overline{SEL}$, $\overline{BSY}$	0	—	ns
ID assert$\rightarrow\overline{BSY}\uparrow$	ts012	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$	0	—	ns
$\overline{IO}\downarrow\rightarrow\overline{BSY}\uparrow$	ts061	$\overline{IO}$, $\overline{BSY}$	0	—	ns
$\overline{BSY}\uparrow\rightarrow\overline{BSY}\downarrow$	ts014	$\overline{BSY}$	18 tscsi	19 tscsi + 20	ns
$\overline{BSY}\downarrow\rightarrow\overline{SEL}\uparrow$	ts015	$\overline{BSY}$, $\overline{SEL}$	0	—	ns
$\overline{BSY}\downarrow\rightarrow$ID hold	ts016	$\overline{BSY}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	10	—	ns
$\overline{BSY}\downarrow\rightarrow\overline{IO}$ hold	ts062	$\overline{BSY}$, $\overline{IO}$	10	—	ns
$\overline{SEL}\uparrow\rightarrow\overline{BSY}\downarrow$ (Output stop)	ts063	$\overline{SEL}$, $\overline{BSY}$	8 tscsi	9 tscsi + 20	ns



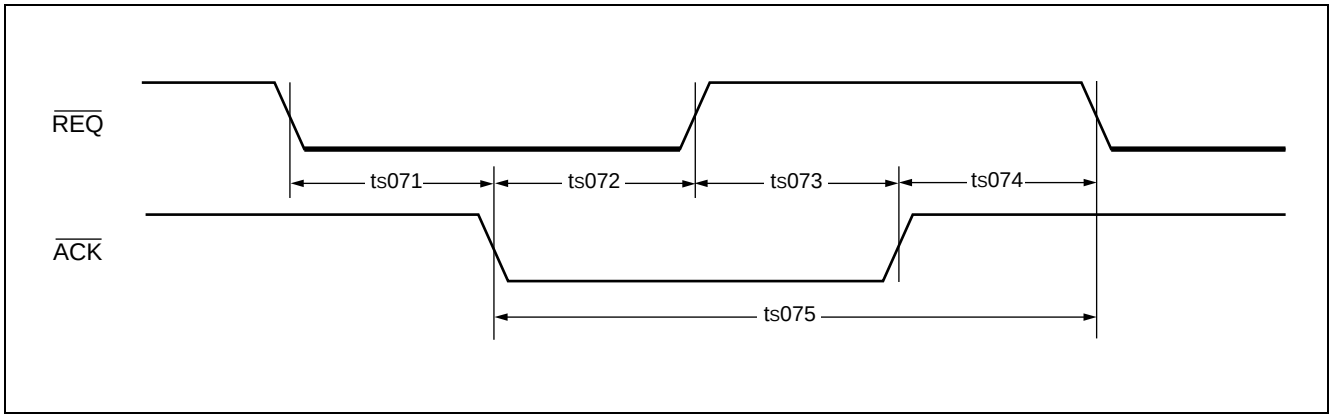
5-7 Target Asynchronous Transfer (REQ/ACK Timing)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{REQ}\downarrow\rightarrow\overline{ACK}\downarrow$	ts071	$\overline{REQ}$, $\overline{ACK}$	0	—	ns
$\overline{ACK}\downarrow\rightarrow\overline{REQ}\uparrow$	ts072	$\overline{ACK}$, $\overline{REQ}$	0	25	ns
$\overline{REQ}\uparrow\rightarrow\overline{ACK}\uparrow$	ts073	$\overline{REQ}$, $\overline{ACK}$	0	—	ns
$\overline{ACK}\uparrow\rightarrow\overline{REQ}\downarrow$ (Note 2)	ts074	$\overline{ACK}$, $\overline{REQ}$	0	25	ns
$\overline{ACK}\downarrow\rightarrow\overline{REQ}\downarrow$ (Notes 1, 2)	ts075	$\overline{ACK}$, $\overline{REQ}$	8 tscsi	9 tscsi + 5	ns

Note1 : The "$\overline{ACK}$ rise to $\overline{REQ}$ fall" time is regulated by (ts072 + ts073 + ts074) or ts075, whichever is longer.

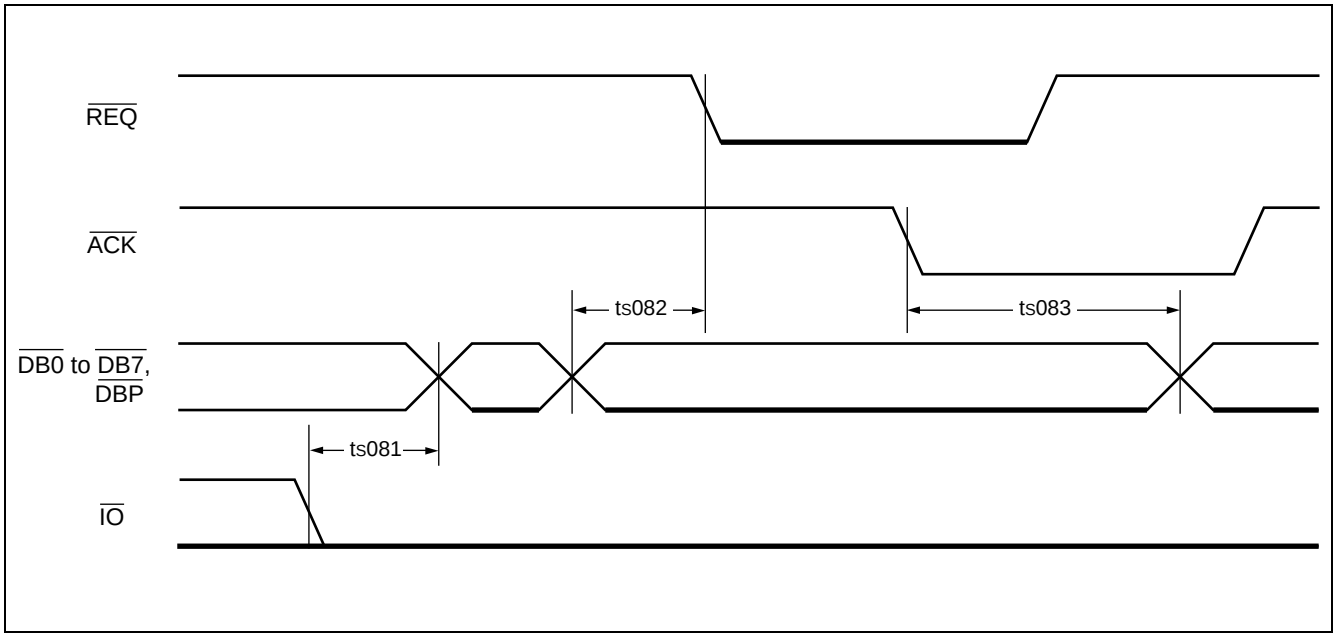
Note2 : In the following cases, the time regulation is not applied because data transfer is aborted.

- The data register is empty during data output to the SCSI bus.
- The data register is full during data input from the SCSI bus.



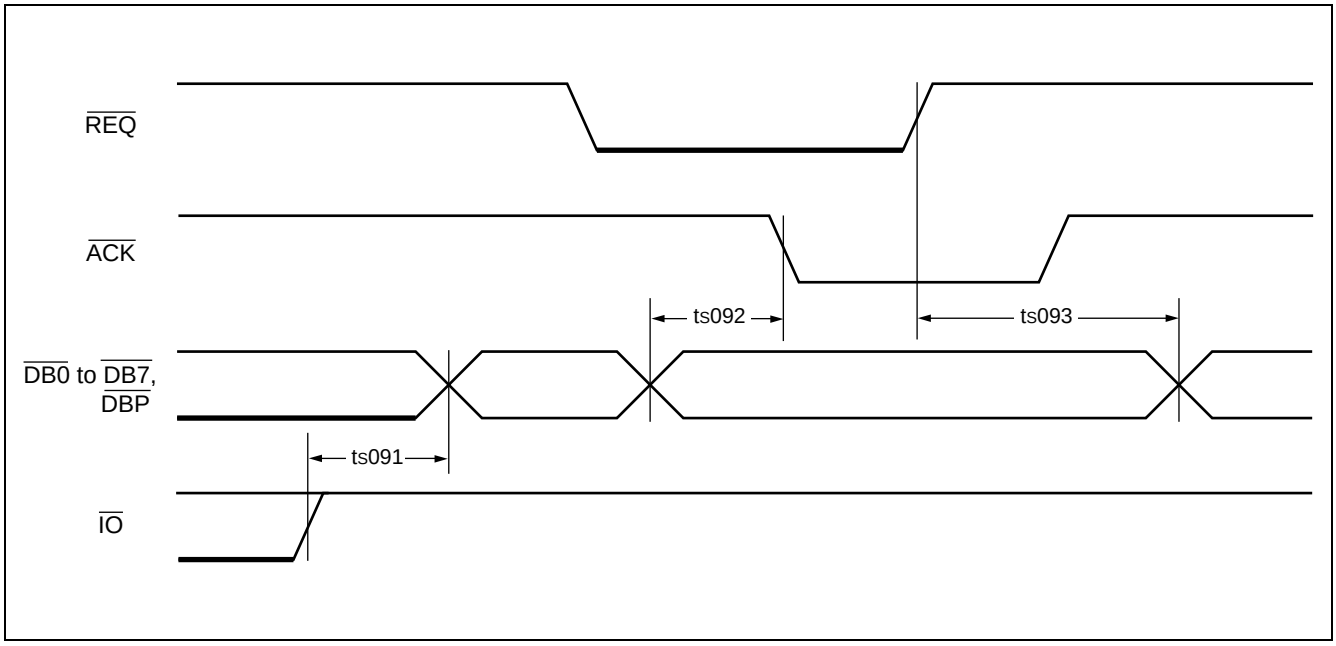
5-8 Target Asynchronous Transfer (Data Output)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}\downarrow \rightarrow$Data bus drive	ts081	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	33 tscsi	34 tscsi + 10	ns
Data output assert$\rightarrow\overline{REQ}\downarrow$	ts082	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{REQ}$	8 tscsi – 5	—	ns
$\overline{ACK}\downarrow \rightarrow$Data hold	ts083	$\overline{ACK}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	0	—	ns



5-9 Target Asynchronous Transfer (Data Input)

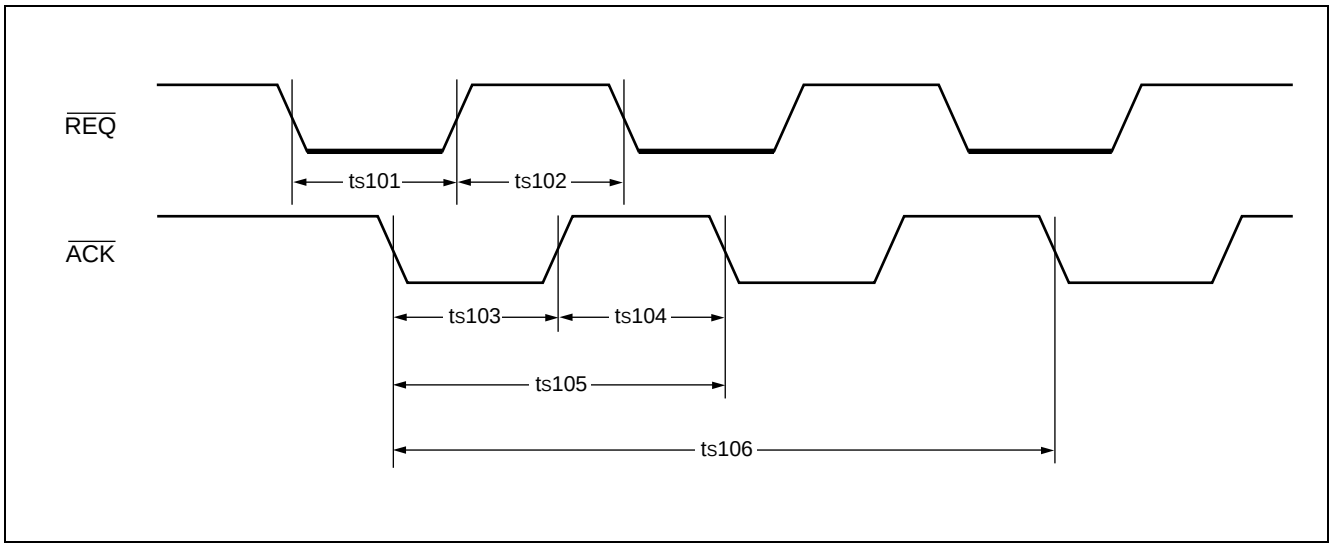
Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}\uparrow \rightarrow$Data bus driving stop	ts091	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	0	10	ns
Data setup$\rightarrow\overline{ACK}\downarrow$	ts092	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{ACK}$	10	—	ns
$\overline{REQ}\uparrow \rightarrow$Data hold	ts093	$\overline{REQ}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	5	—	ns



5-10 Target Synchronous Transfer (REQ/ACK Timing)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{\text{REQ}}$ assert time	ts101	$\overline{\text{REQ}}$	n*•tscsi	—	ns
$\overline{\text{REQ}}$ negate time	ts102	$\overline{\text{REQ}}$	n*•tscsi	—	ns
$\overline{\text{ACK}}$ assert time	ts103	$\overline{\text{ACK}}$	10	—	ns
$\overline{\text{ACK}}$ negate time	ts104	$\overline{\text{ACK}}$	10	—	ns
$\overline{\text{ACK}}$ cycle time (1)	ts105	$\overline{\text{ACK}}$	1 tscsi	—	ns
$\overline{\text{ACK}}$ cycle time (2)	ts106	$\overline{\text{ACK}}$	3 tscsi	—	ns

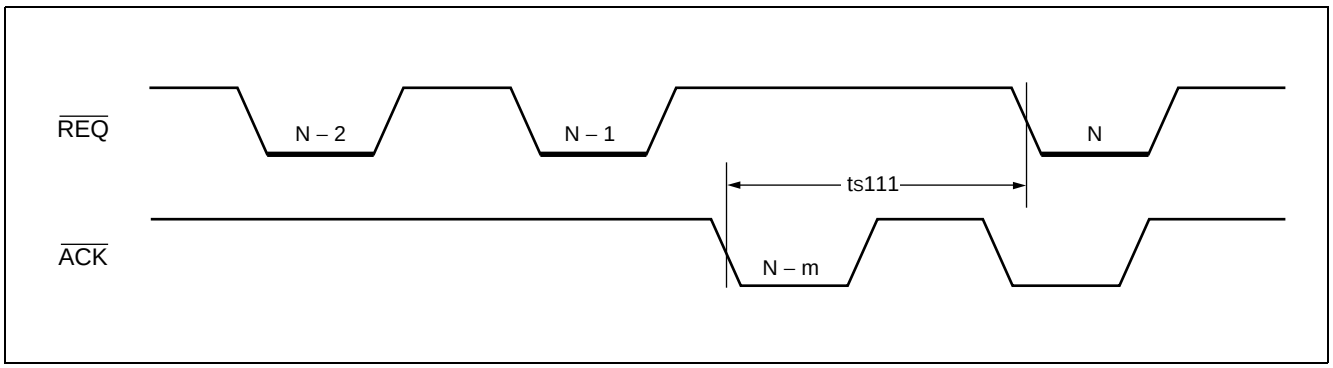
* : Value set in bits 3 to 0 in the SCSI block TMOD register



5-11 Target Synchronous Transfer (REQ Output Delay Time)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{REQ}$ output delay time (Note)	ts111	$\overline{ACK}$, $\overline{REQ}$	3 tscsi	4 tscsi + 10	ns

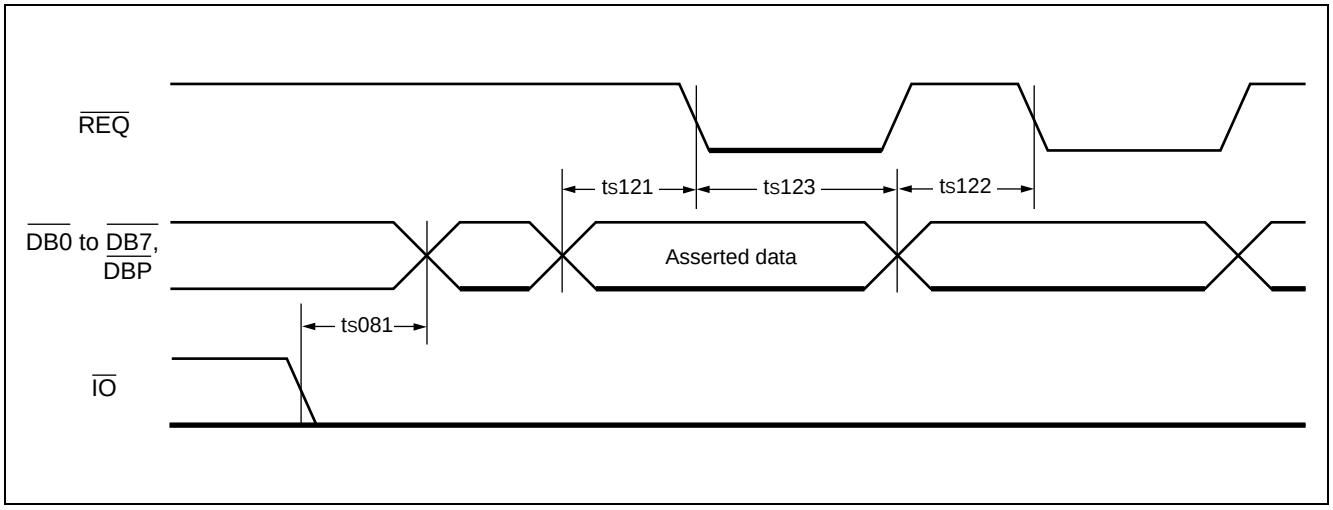
Note : The minimum time from the reception of ACK in the (N-m) -th byte to the output of REQ in the N-th byte with Maximum offset count = m.
The following timing chart assumes that REQ output is aborted because output of REQ in the N-1-th byte has made the number of offsets the maximum offset count = m.
The maximum offset count is set by bits 7 to 4 in the SCSI block transfer mode register.



5-12 Target Synchronous Transfer (Data Output)

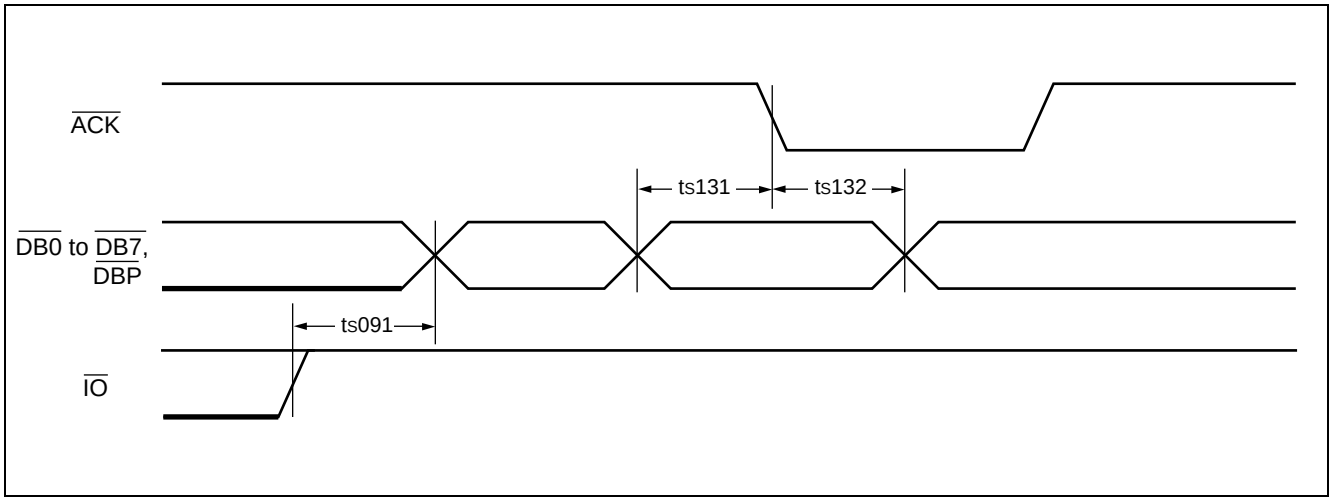
Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}$↓→Data bus drive	ts081	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	33 tscsi	34 tscsi + 10	ns
Data output assert→$\overline{REQ}$↓	ts121	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{REQ}$	8 tscsi – 5	—	ns
	ts122	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{REQ}$	n*•tscsi – 5	—	ns
$\overline{REQ}$↓→Data hold	ts123	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{REQ}$	n*•tscsi	—	ns

* : Value set in bits 3 to 0 in the SCSI block TMOD register



5-13 Target Synchronous Transfer (Data Input)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}\uparrow \rightarrow$Data bus driving stop	ts091	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	0	10	ns
Data setup$\rightarrow\overline{ACK}\downarrow$	ts131	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{ACK}$	5	—	ns
$\overline{ACK}\downarrow \rightarrow$Data hold	ts132	$\overline{ACK}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	5	—	ns



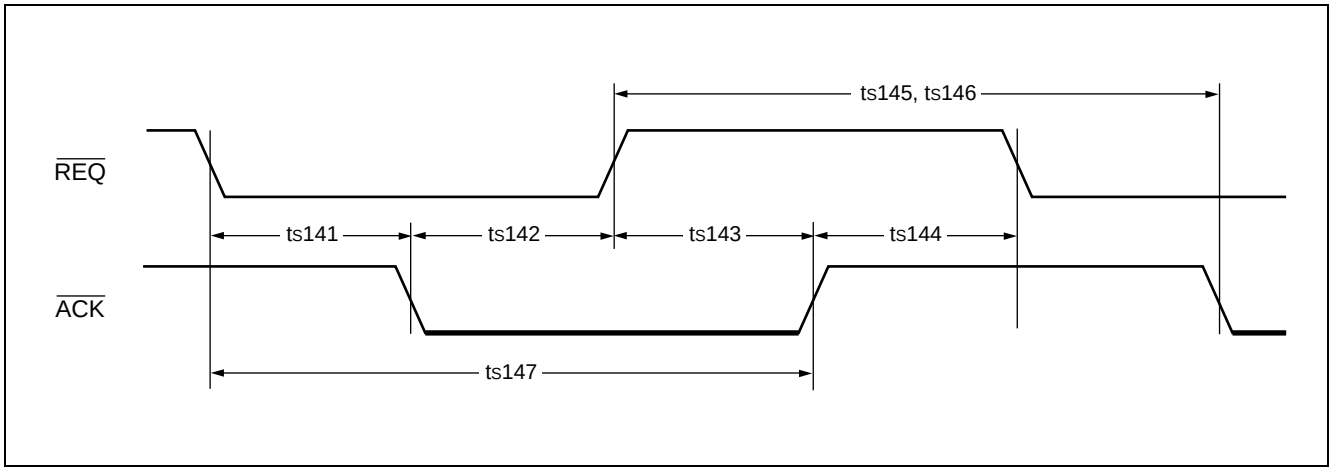
5-14 Initiator Asynchronous Transfer (REQ/ACK Timing)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{REQ}\downarrow\rightarrow\overline{ACK}\downarrow$ (Note 3)	ts141	$\overline{REQ}$, $\overline{ACK}$	0	25	ns
$\overline{ACK}\downarrow\rightarrow\overline{REQ}\uparrow$	ts142	$\overline{ACK}$, $\overline{REQ}$	0	—	ns
$\overline{REQ}\uparrow\rightarrow\overline{ACK}\uparrow$ (Note 3)	ts143	$\overline{REQ}$, $\overline{ACK}$	0	1 tscsi	ns
$\overline{ACK}\uparrow\rightarrow\overline{REQ}\downarrow$	ts144	$\overline{ACK}$, $\overline{REQ}$	0	—	ns
$\overline{REQ}\uparrow\rightarrow\overline{ACK}\downarrow$ (Notes 1, 3)	ts145	$\overline{REQ}$, $\overline{ACK}$	8 tscsi	9 tscsi + 5	ns
$\overline{REQ}\uparrow\rightarrow\overline{ACK}\downarrow$ (Notes 2, 3)	ts146	$\overline{REQ}$, $\overline{ACK}$	4 tscsi	5 tscsi + 5	ns
$\overline{REQ}\downarrow\rightarrow\overline{ACK}\uparrow$ (Notes 2, 3)	ts147	$\overline{REQ}$, $\overline{ACK}$	8 tscsi	9 tscsi + 5	ns

Note1 : Applies to data output to the SCSI bus.
The "$\overline{REQ}$ rise to $\overline{ACK}$ fall" time is regulated by (ts143 + ts144 + ts141) or ts145, whichever is longer.

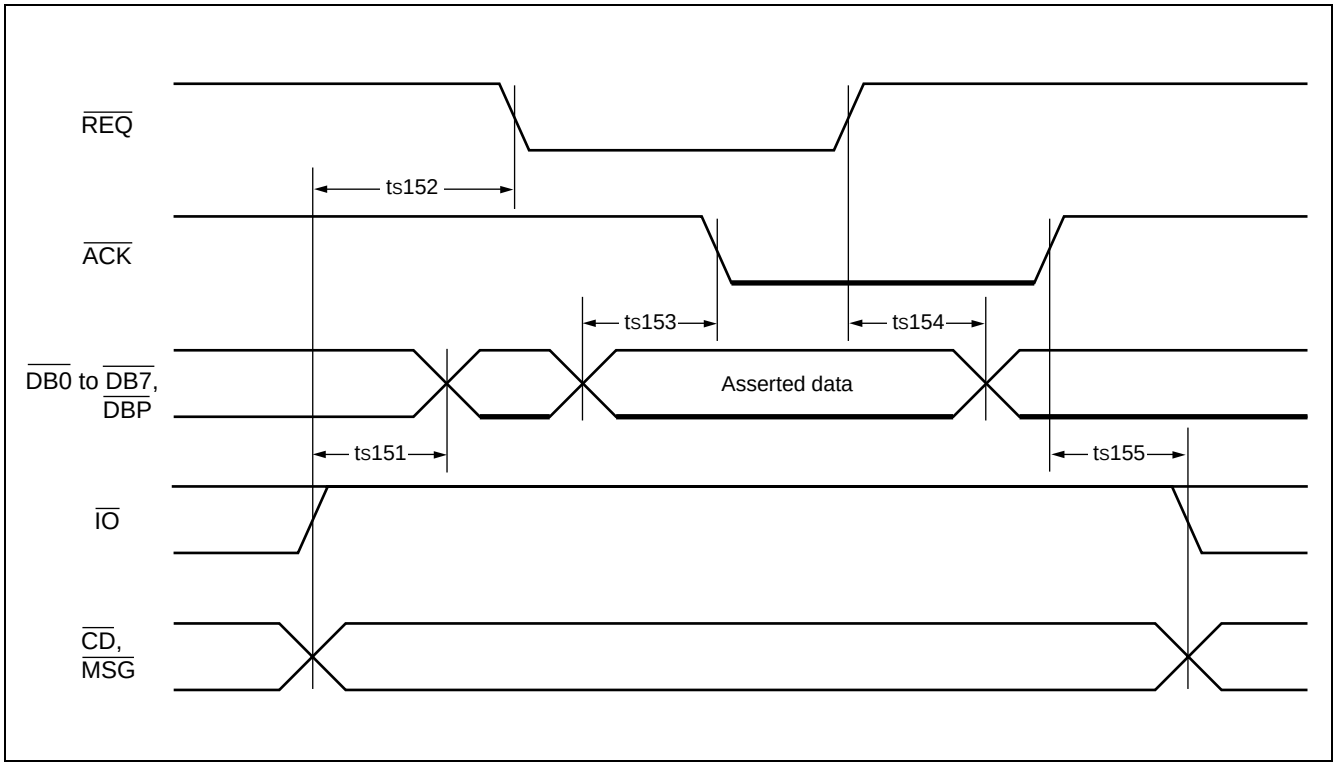
Note2 : Applies to data input from the SCSI bus.
The "$\overline{REQ}$ rise to $\overline{ACK}$ fall" time is regulated by (ts143 + ts144 + ts141) or ts146, whichever is longer.
The "$\overline{REQ}$ fall to $\overline{ACK}$ rise" time is regulated by (ts141 + ts142 + ts143) or ts147, whichever is longer.

Note3 : In the following cases, either time regulation is not applied because data transfer is aborted.
- The data register is empty during data output to the SCSI bus.
- The data register is full during data input from the SCSI bus.
- $\overline{ATN}$ is output upon detection of a parity error during data input from the SCSI bus.
- During transfer of the first or last byte



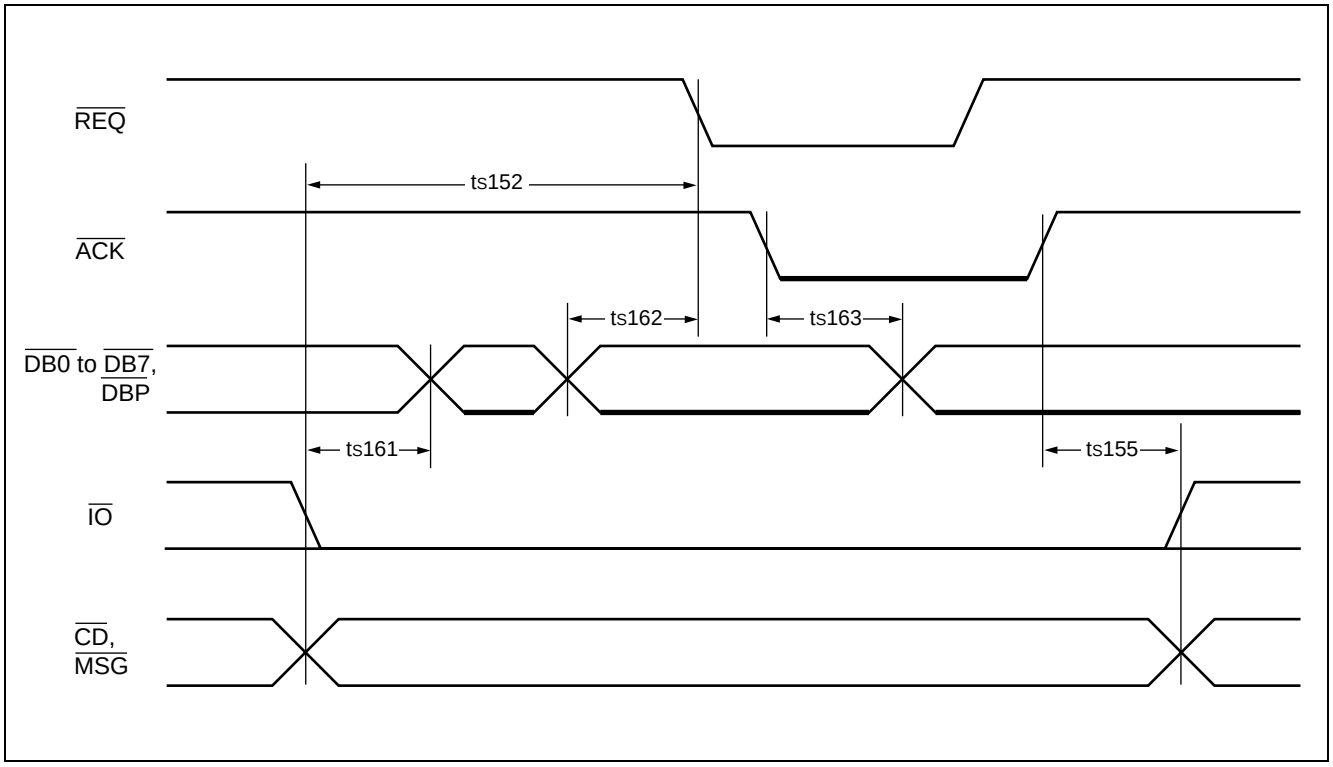
5-15 Initiator Asynchronous Transfer (Data Output)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}\uparrow \rightarrow$Data bus drive	ts151	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	0	10	ns
Phase signal assert$\rightarrow\overline{REQ}\downarrow$	ts152	$\overline{IO}$, $\overline{CD}$, $\overline{MSG}$, $\overline{REQ}$	30	—	ns
Data output assert$\rightarrow\overline{ACK}\downarrow$	ts153	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{ACK}$	8 tscsi – 5	—	ns
$\overline{REQ}\uparrow \rightarrow$Data hold	ts154	$\overline{REQ}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	0	—	ns
$\overline{ACK}\uparrow \rightarrow$Phase signal hold	ts155	$\overline{ACK}$, $\overline{IO}$, $\overline{CD}$, $\overline{MSG}$	10	—	ns



5-16 Initiator Asynchronous Transfer (Data Input)

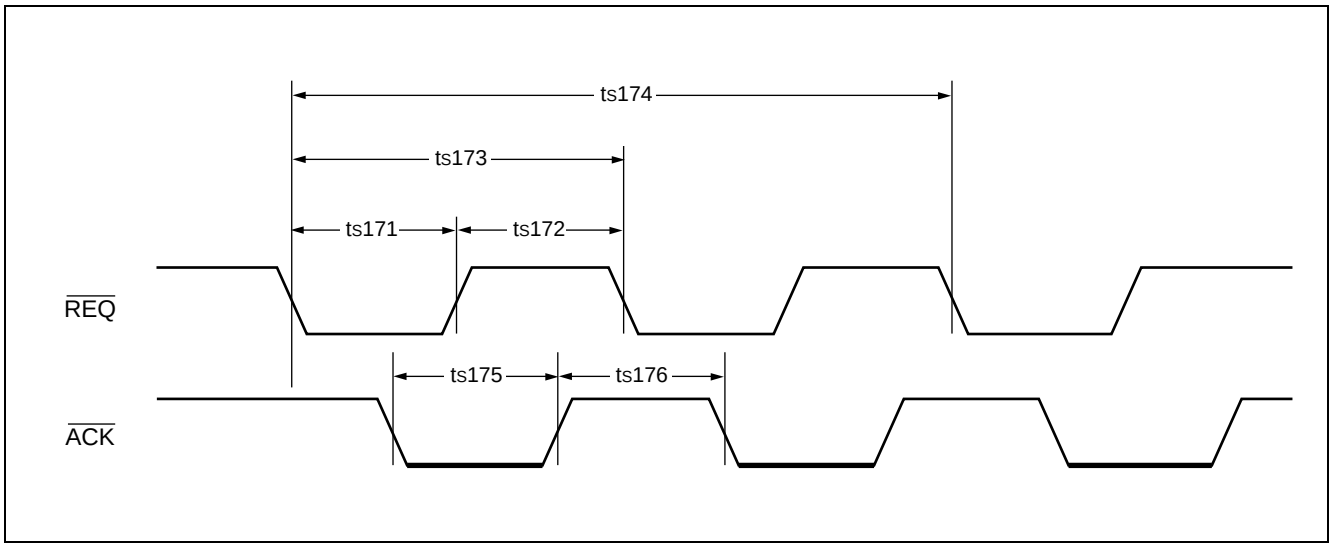
Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}\downarrow \rightarrow$Data bus drive stop	ts161	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	—	30	ns
Phase signal assert$\rightarrow\overline{REQ}\downarrow$	ts152	$\overline{IO}$, $\overline{CD}$, $\overline{MSG}$, $\overline{REQ}$	30	—	ns
Data setup$\rightarrow\overline{REQ}\downarrow$	ts162	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{REQ}$	10	—	ns
$\overline{ACK}\downarrow \rightarrow$Data hold	ts163	$\overline{ACK}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	5	—	ns
$\overline{ACK}\uparrow \rightarrow$Phase signal hold	ts155	$\overline{ACK}$, $\overline{IO}$, $\overline{CD}$, $\overline{MSG}$	10	—	ns



5-17 Initiator Synchronous Transfer (REQ/ACK Timing)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{\text{REQ}}$ assert time	ts171	$\overline{\text{REQ}}$	10	—	ns
$\overline{\text{REQ}}$ negate time	ts172	$\overline{\text{REQ}}$	10	—	ns
$\overline{\text{REQ}}$ cycle time (1)	ts173	$\overline{\text{REQ}}$	1 tscsi	—	ns
$\overline{\text{REQ}}$ cycle time (2)	ts174	$\overline{\text{REQ}}$	3 tscsi	—	ns
$\overline{\text{ACK}}$ assert time	ts175	$\overline{\text{ACK}}$	n*•tscsi	—	ns
$\overline{\text{ACK}}$ negate time	ts176	$\overline{\text{ACK}}$	n*•tscsi	—	ns

* : Value set in bits 3 to 0 in the SCSI block TMOD register



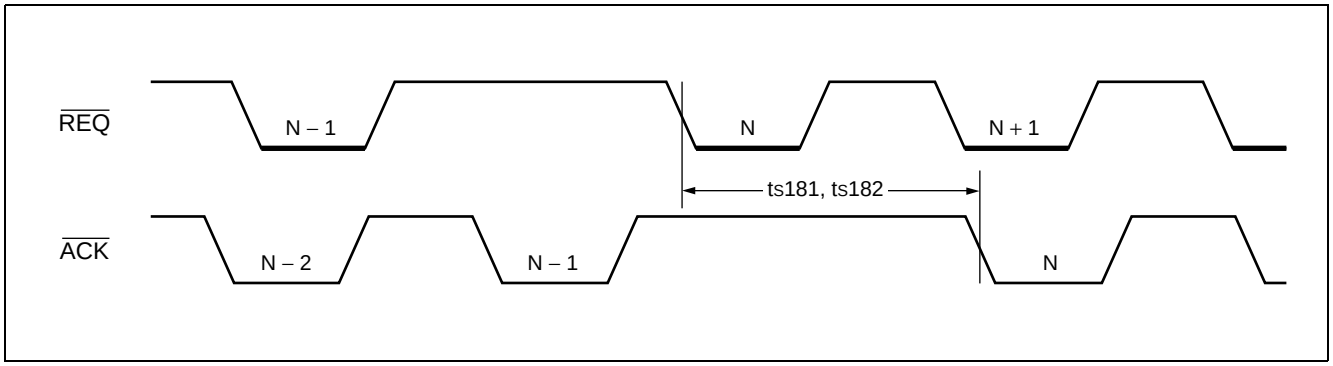
5-18 Initiator Synchronous Transfer (ACK Output Delay Time)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{ACK}$ output delay time (1) (Notes 1, 2)	ts181	$\overline{REQ}$, $\overline{ACK}$	9 tscsi	12 tscsi + 5	ns
$\overline{ACK}$ output delay time (2) (Notes 1, 3)	ts182	$\overline{REQ}$, $\overline{ACK}$	3 tscsi	4 tscsi + 5	ns

Note1 : The minimum time from the reception of REQ in the N-th byte to the output of ACK in the N-th byte.

Note2 : Applies to data input from the SCSI bus, with the maximum offset count set to 8 to 15.
The maximum offset count is set by bits 7 to 4 in the SCSI block transfer mode register.

Note3 : Applies in any case other than Note 2.

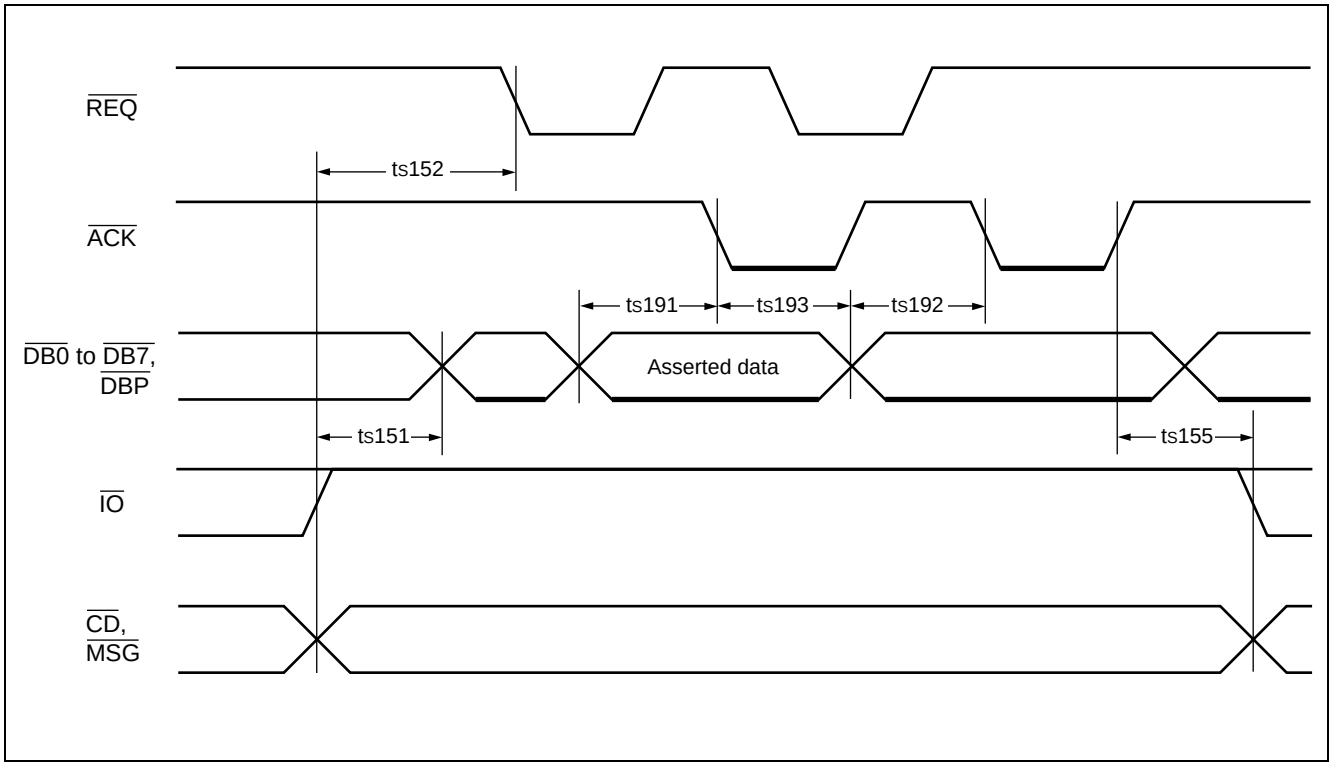


5-19 Initiator Synchronous Transfer (Data Output)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}$↑→Data bus drive	ts151	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	0	10	ns
Phase signal assert→$\overline{REQ}$↓	ts152	$\overline{IO}$, $\overline{CD}$, $\overline{MSG}$, $\overline{REQ}$	30	—	ns
Data output assert→$\overline{ACK}$↓ (Note)	ts191	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{ACK}$	8 tscsi – 5	—	ns
	ts192	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{ACK}$	n*•tscsi – 5	—	ns
$\overline{ACK}$↓→Data hold	ts193	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{ACK}$	n*•tscsi	—	ns
$\overline{ACK}$↑→Phase signal hold	ts155	$\overline{ACK}$, $\overline{IO}$, $\overline{CD}$, $\overline{MSG}$	10	—	ns

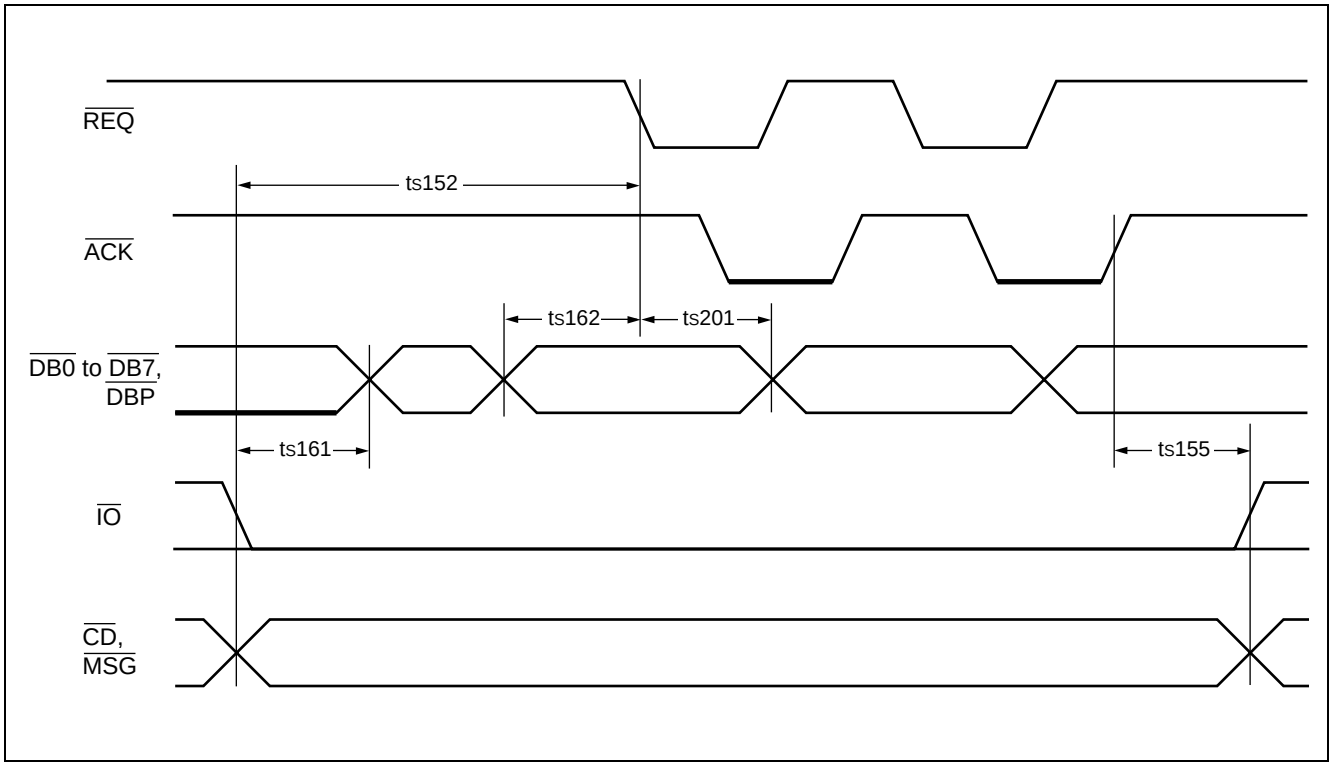
* : Value set in bits 3 to 0 in the SCSI block TMOD register

Note : The "data output assert to $\overline{ACK}$ fall" time is regulated by ts191 or ts192, whichever is shorter.



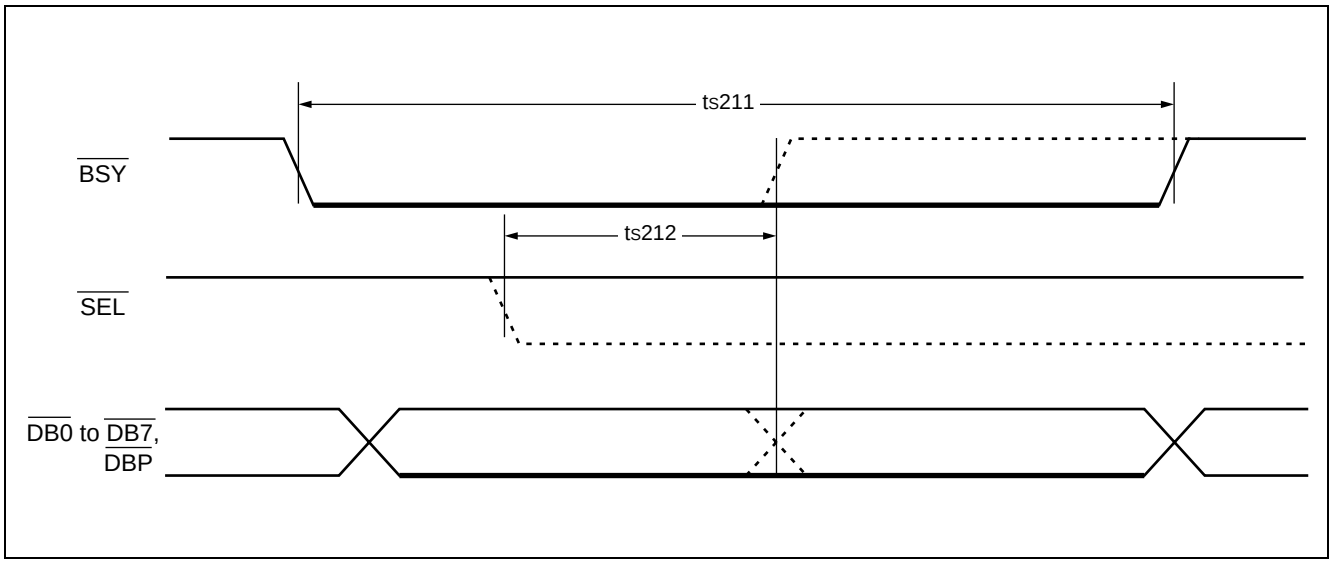
5-20 Initiator Synchronous Transfer (Data Input)

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{IO}\downarrow \rightarrow$Data bus drive stop	ts161	$\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	—	30	ns
Phase signal assert$\rightarrow\overline{REQ}\downarrow$	ts152	$\overline{IO}$, $\overline{CD}$, $\overline{MSG}$, $\overline{REQ}$	30	—	ns
Data setup$\rightarrow\overline{REQ}\downarrow$	ts162	$\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{REQ}$	5	—	ns
$\overline{REQ}\downarrow \rightarrow$Data hold	ts201	$\overline{REQ}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	5	—	ns
$\overline{ACK}\uparrow \rightarrow$Phase signal hold	ts155	$\overline{ACK}$, $\overline{IO}$, $\overline{CD}$, $\overline{MSG}$	10	—	ns



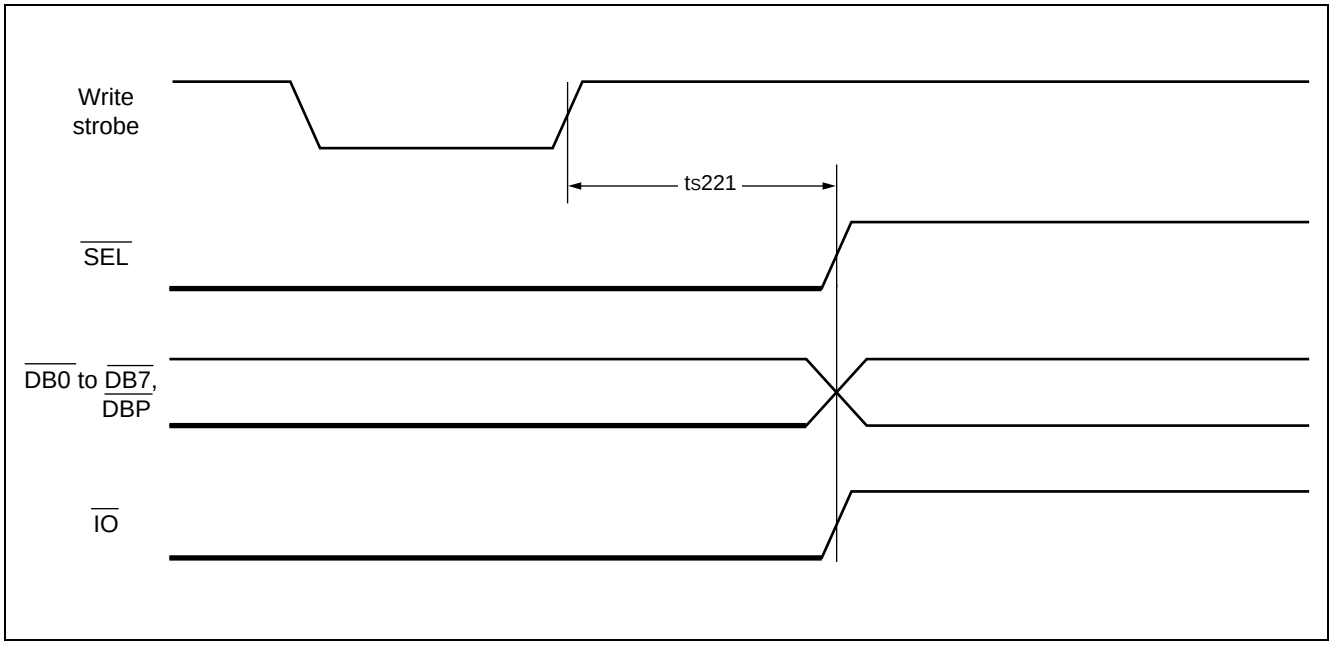
5-21 Arbitration Failure

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Arbitration start→ $\overline{BSY}$↑ & Self-ID output stop	ts211	$\overline{BSY}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	128 tscsi − 10	128 tscsi + 15	ns
Other device's $\overline{SEL}$↓→ $\overline{BSY}$↑ & Self-ID output stop	ts212	$\overline{SEL}$, $\overline{BSY}$, $\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$	8 tscsi	9 tscsi + 20	ns



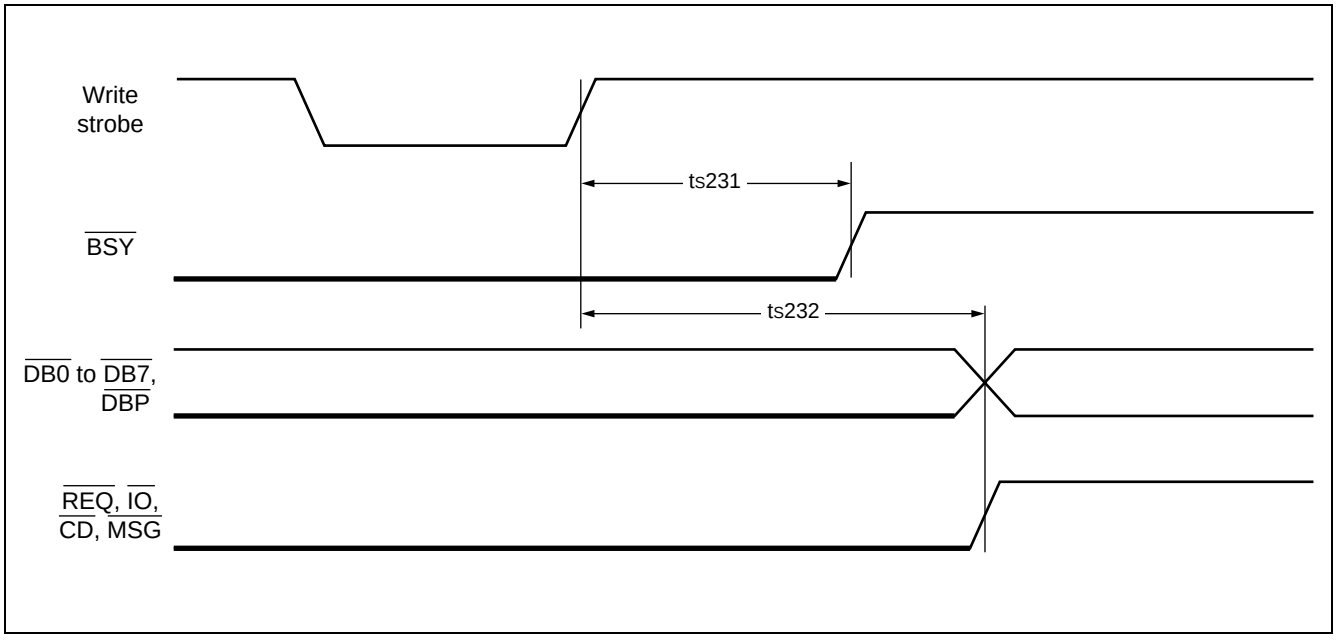
5-22 Selection/Reselection Time-out

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
TIME OUT interrupt reset→ SCSI bus clear	ts222	$\overline{SEL}$, $\overline{IO}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	3 tscsi − 10	3 tscsi + 15	ns



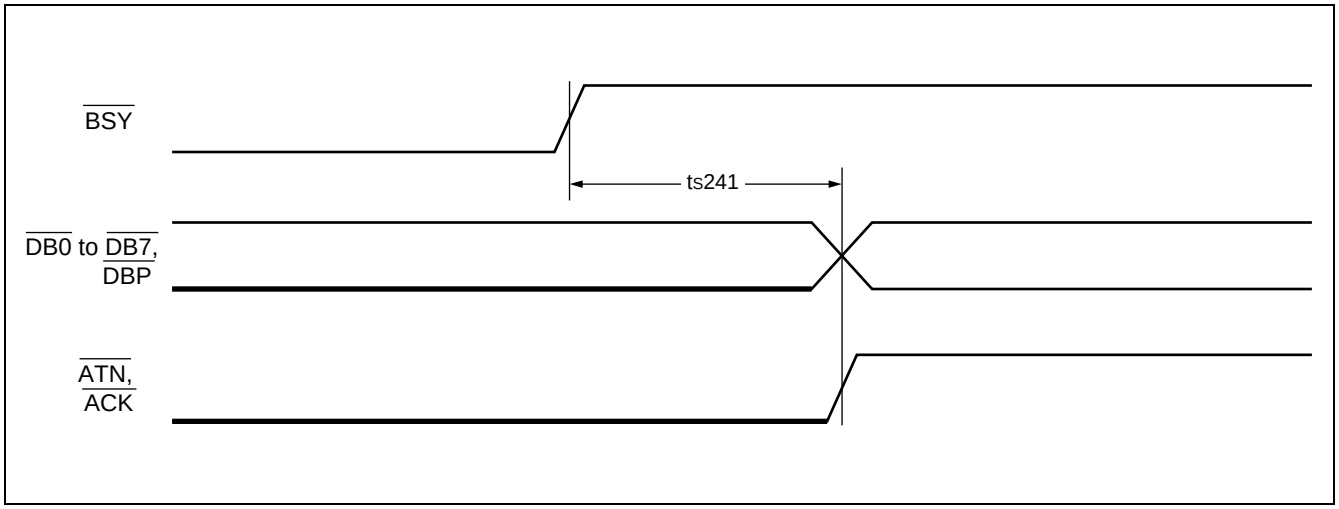
5-23 Target Disconnect Operation

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
REL command issue →$\overline{BSY}$↑	ts231	$\overline{BSY}$	3 tscsi – 10	3 tscsi + 15	ns
REL command issue→SCSI bus clear	ts232	$\overline{REQ}$, $\overline{IO}$, $\overline{CD}$, $\overline{MSG}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	3 tscsi – 10	3 tscsi + 15	ns



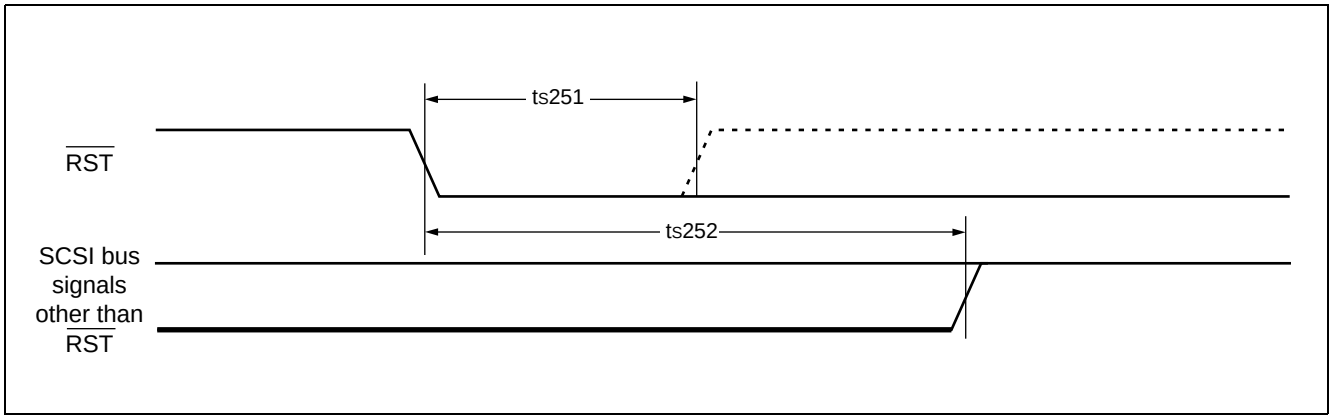
5-24 Initiator Disconnect Operation

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{BSY}\uparrow \rightarrow$SCSI bus clear	ts241	$\overline{BSY}$, $\overline{ACK}$, $\overline{ATN}$, $\overline{DBP}$, $\overline{DB0}$ to $\overline{DB7}$	—	21 tscsi + 20	ns



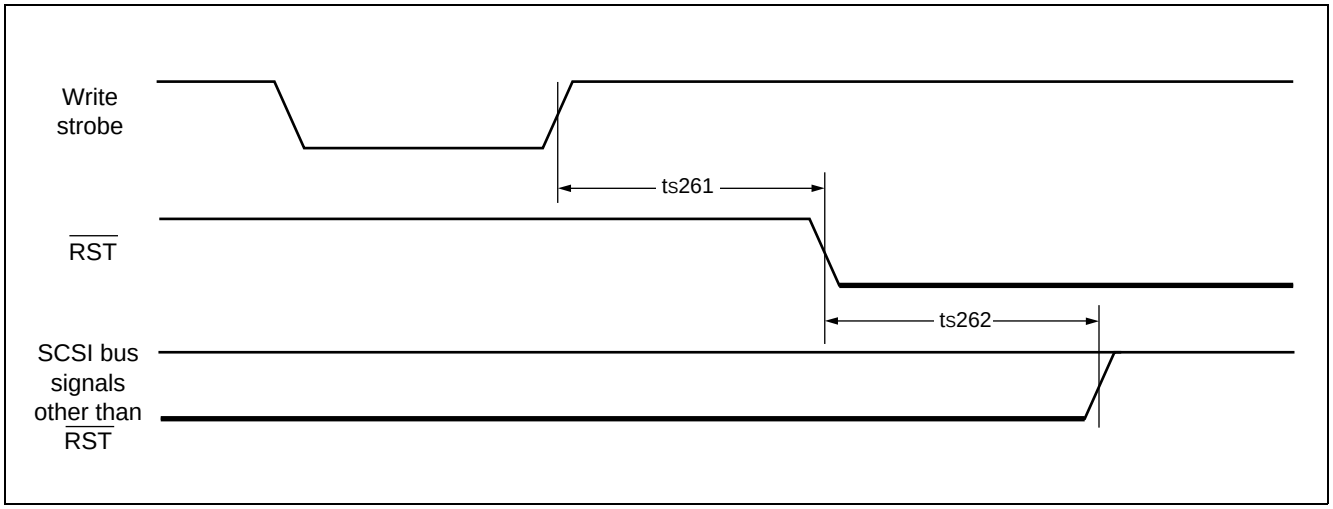
5-25 Reset Condition Detection

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Reset condition detection time	ts251	$\overline{RST}$	12 tscsi	—	ns
$\overline{RST}\downarrow\rightarrow$SCSI bus clear	ts252	All SCSI bus pins	—	12 tscsi + 20	ns



5-26 Reset Condition Generation

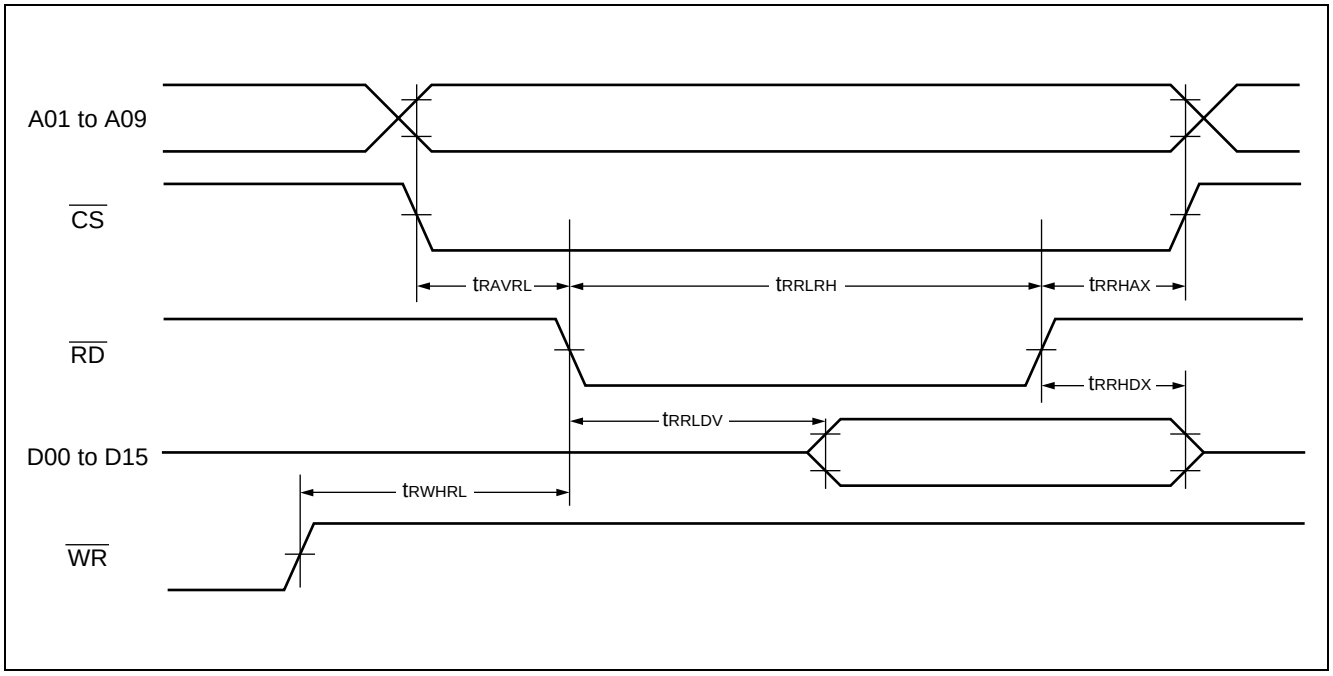
Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Write “1” to RST OUT bit→ $\overline{RST}$↓	ts261	$\overline{RST}$	—	10	ns
$\overline{RST}$↓→SCSI bus clear	ts262	All SCSI bus pins	—	10	ns
Write “0” to RST OUT bit→ $\overline{RST}$↑	ts263	$\overline{RST}$	—	10	ns



(6) IEEE 1394/SCSI/Exchange Block Register Access

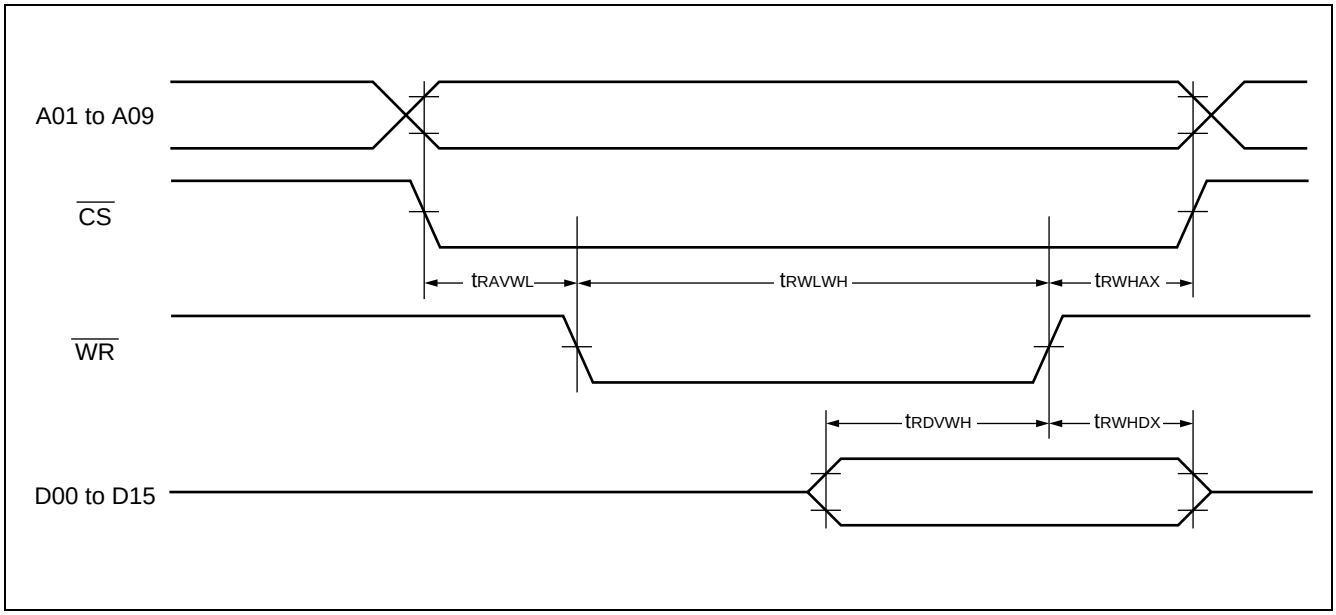
6-1 Read Operation

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Address setup	t_{RAVRL}	A01 to A09, $\overline{CS}$, $\overline{RD}$	10	—	ns
Address hold	t_{RRHAX}	A01 to A09 $\overline{CS}$, $\overline{RD}$	5	—	ns
$\overline{RD}$ “L” level pulse width	t_{RRLRH}	$\overline{RD}$	40	—	ns
$\overline{RD}\downarrow\rightarrow$Valid data	t_{RRLDV}	$\overline{RD}$, D00 to D15	—	25	ns
$\overline{RD}\uparrow\rightarrow$Data hold	t_{RRHDX}	$\overline{RD}$, D00 to D15	5	—	ns
$\overline{WR}\uparrow\rightarrow\overline{RD}\downarrow$	t_{RWHRL}	$\overline{WR}$, $\overline{RD}$	45	—	ns



6-2 Write Operation

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
Address setup	t_{RAVWL}	A01 to A09, $\overline{CS}$, $\overline{WR}$	10	—	ns
Address hold	t_{RWHAX}	A01 to A09 $\overline{CS}$, $\overline{WR}$	5	—	ns
$\overline{WR}$ "L" level pulse width	t_{RWLWH}	$\overline{WR}$	40	—	ns
Data setup	t_{RDVWH}	$\overline{WR}$, D00 to D15	30	—	ns
Data hold	t_{RWHDX}	$\overline{WR}$, D00 to D15	5	—	ns



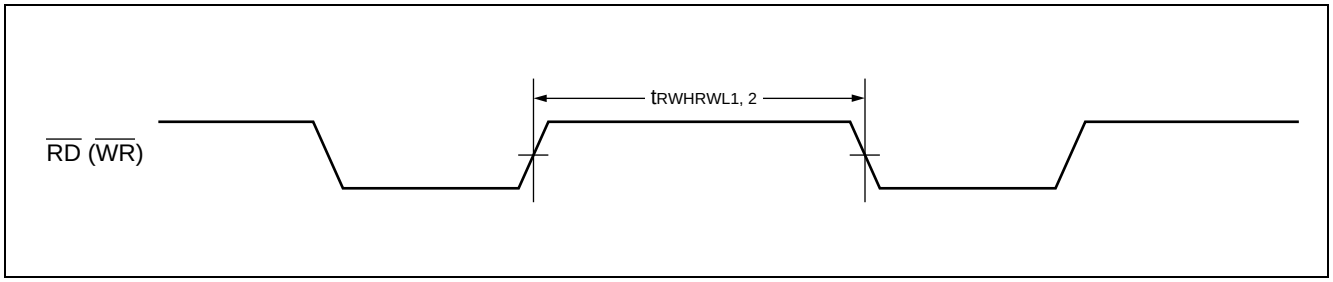
6-3 Register Access Recovery Time

- **Continuous Read/Write Operation**

Shown below is the timing of continuously reading or writing the register at the same address.

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{RD}$ ($\overline{WR}$) ↑→$\overline{RD}$ ($\overline{WR}$) ↓	$t_{RWHRWL1}$	$\overline{RD}$/$\overline{WR}$	25	—	ns
$\overline{RD}$ ($\overline{WR}$) ↑→$\overline{RD}$ ($\overline{WR}$) ↓ (Note)	$t_{RWHRWL2}$	$\overline{WR}$/$\overline{RD}$	45	—	ns

Note : Applies to access to an internal register of the IEEE 1394 block in forced sleep mode.

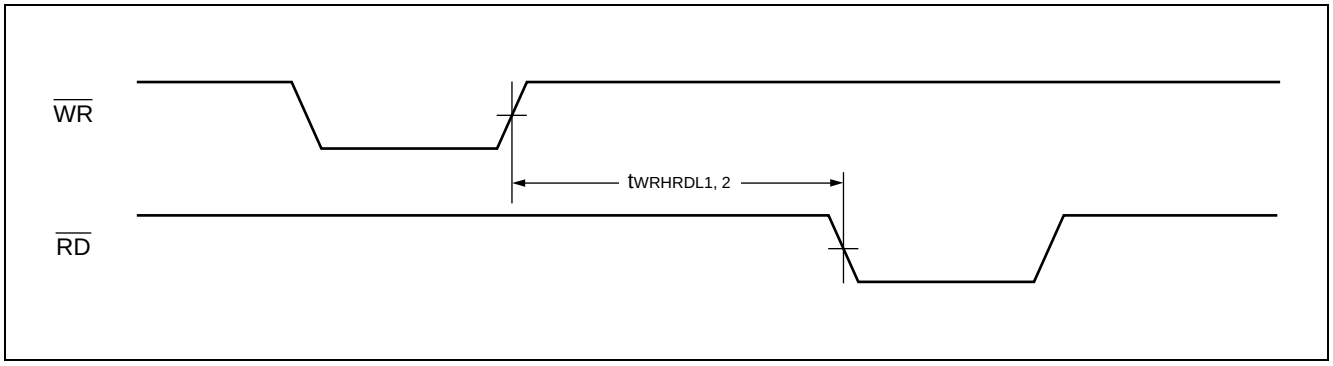


- **Write Operation→Read Operation**

Shown below is the timing of reading after writing the register at the same address.

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{WR}$↑→$\overline{RD}$↓	$t_{WRHRDL1}$	$\overline{WR}$, $\overline{RD}$	80	—	ns
$\overline{WR}$↑→$\overline{RD}$↓ (Note)	$t_{WRHRDL2}$	$\overline{WR}$, $\overline{RD}$	160	—	ns

Note : Applies to access to an internal register of the IEEE 1394 block in forced sleep mode.

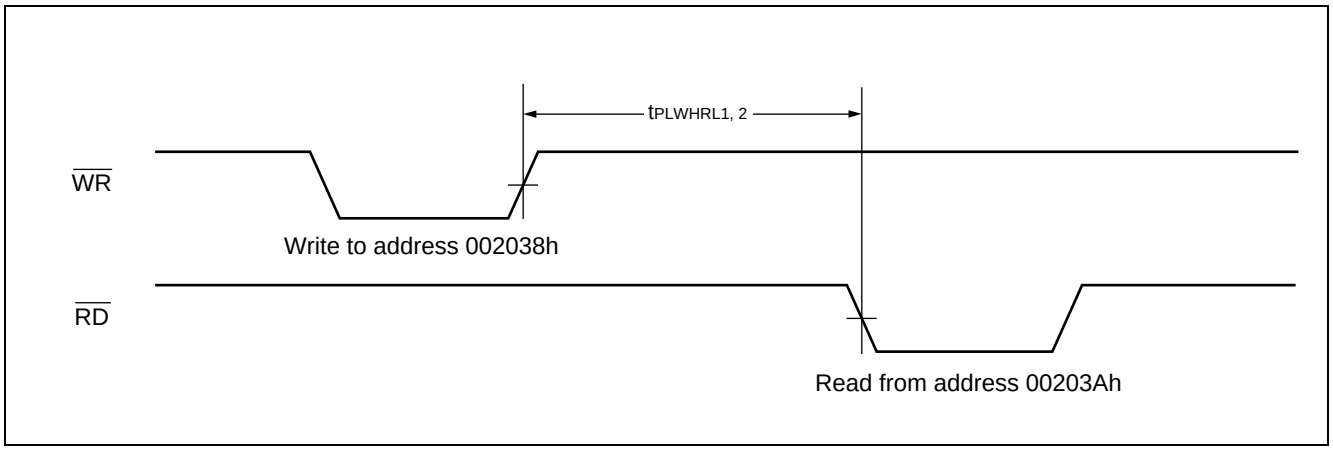


- **IEEE 1394 Block PHY/LINK Register Read Operation**

Shown below is the timing from writing the PHY/LINK register address set register (address 002038h) to reading the PHY/LINK access port (address 00203Ah) to access the PHY-LINK register in the IEEE 1394 block.

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{WR}\uparrow \rightarrow \overline{RD}\downarrow$	$t_{PLWHRL1}$	$\overline{WR}$, $\overline{RD}$	100	—	ns
$\overline{WR}\uparrow \rightarrow \overline{RD}\downarrow$ (Note)	$t_{PLWHRL2}$	$\overline{WR}$, $\overline{RD}$	200	—	ns

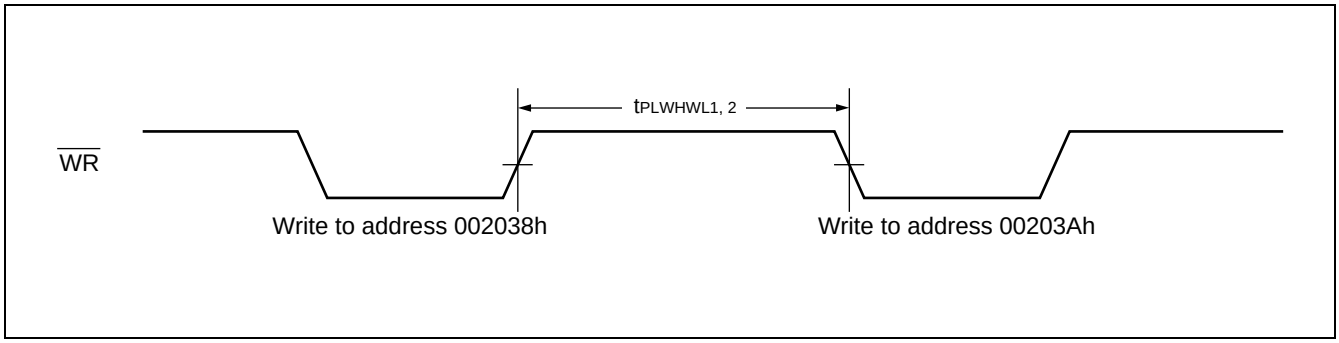
Note : Applies to access in forced sleep mode.



- **IEEE 1394 Block PHY/LINK Register Write Operation**

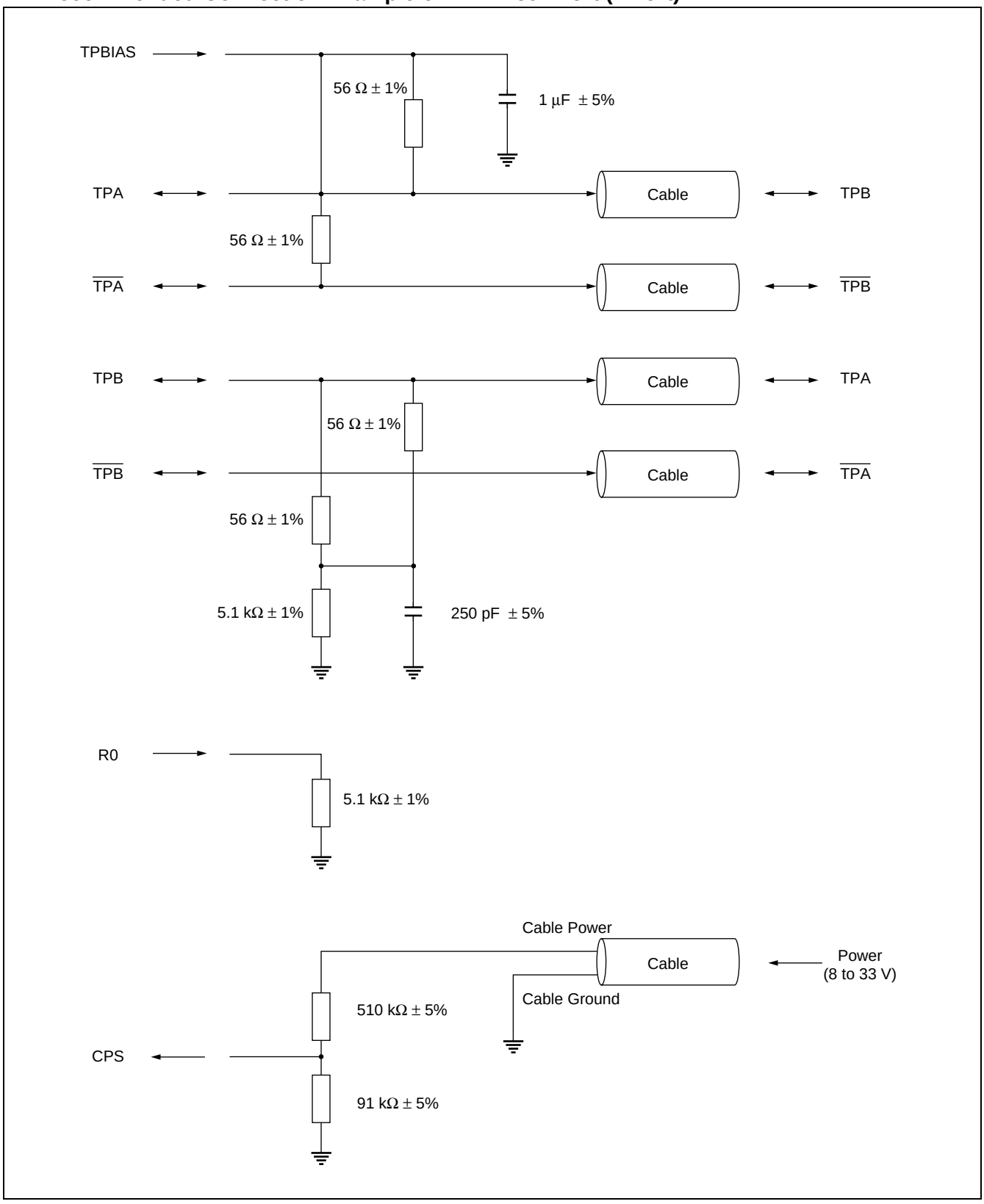
Shown below is the timing from writing the PHY/LINK register address set register (address 002038h) to writing the PHY/LINK access port (address 00203Ah) to access the PHY-LINK register in the IEEE 1394 block.

Parameter	Symbol	Pin name	Values		Unit
			Min.	Max.	
$\overline{WR}\uparrow \rightarrow \overline{WR}\downarrow$	$t_{PLWHWL1}$	$\overline{WR}$	100	—	ns

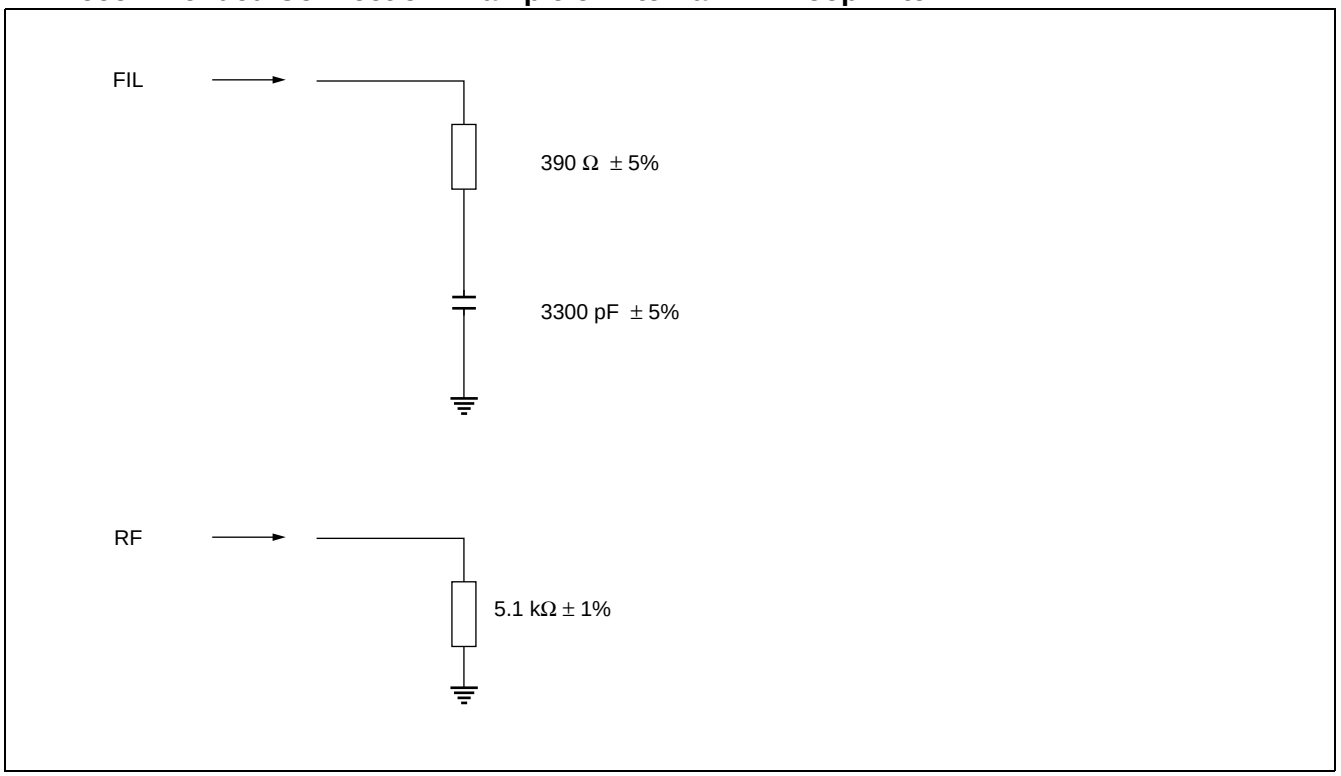


■ SYSTEM CONFIGURATION EXAMPLES

1. Recommended Connection Example of IEEE 1394 Port (1 Port)

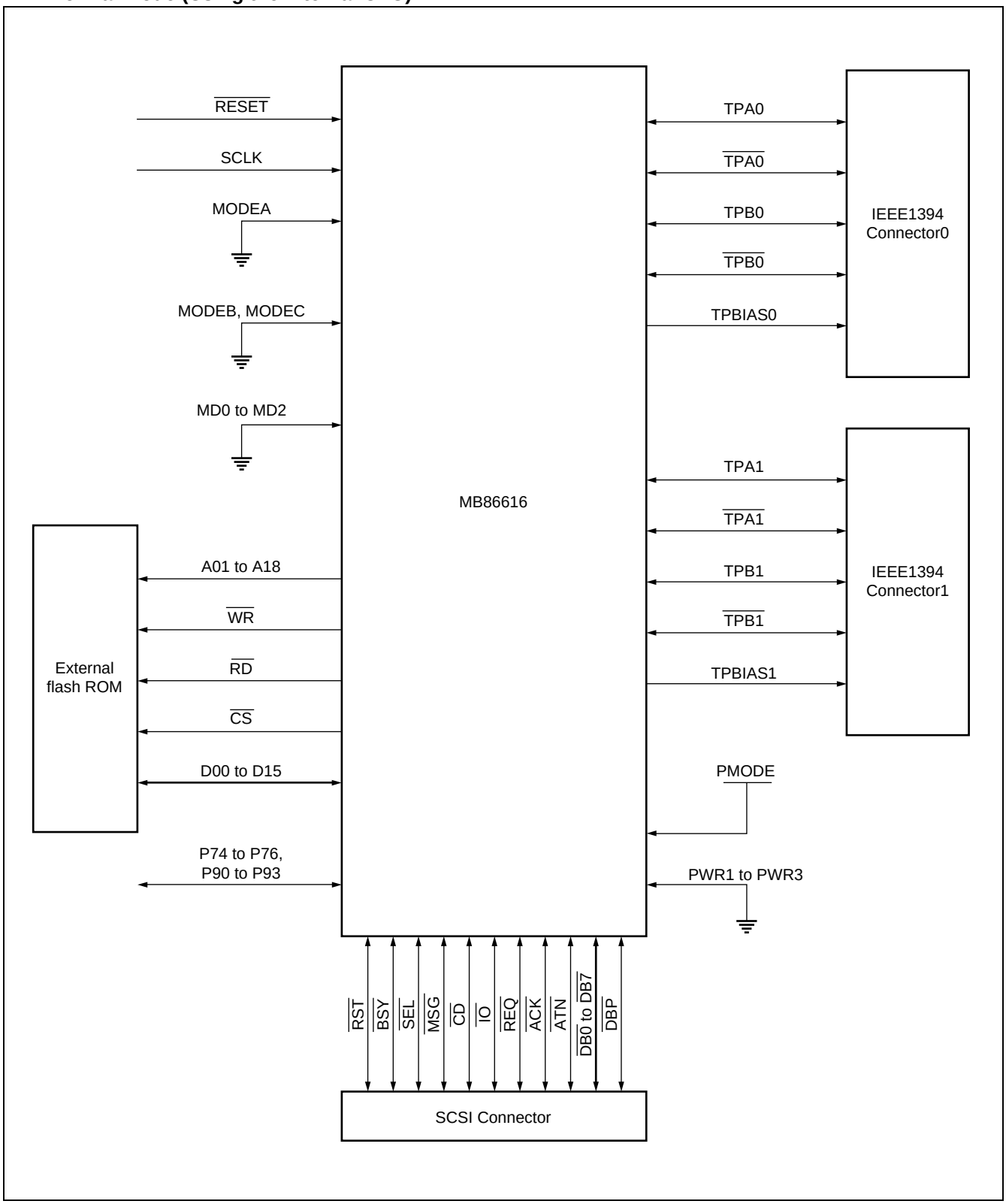


2. Recommended Connection Example of Internal PLL Loop Filter

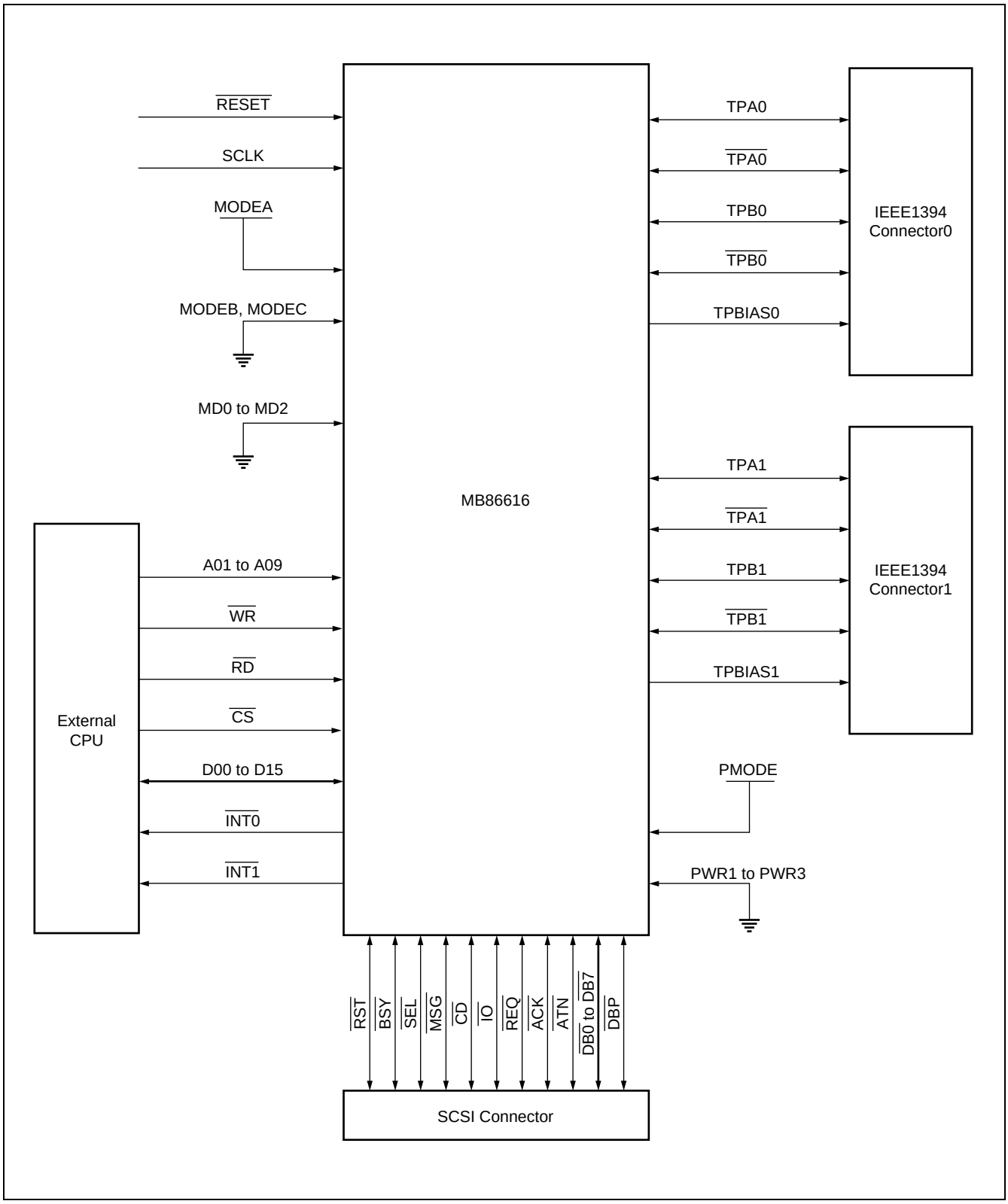


3. Sample System Configurations

- **Normal Mode (Using the Internal CPU)**



- **External CPU Mode**

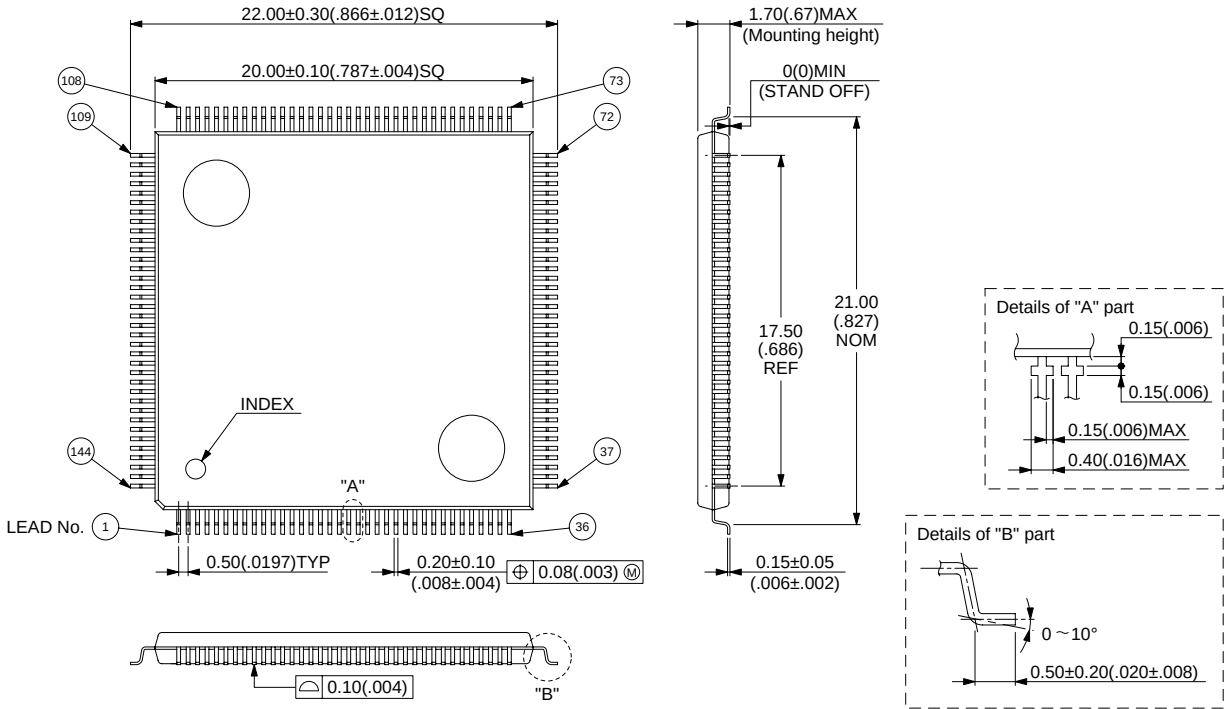


■ ORDERING INFORMATION

Part number	Package	Remarks
MB86616PFV-G-BND	144-pin Plastic LQFP (FPT-144P-M08)	

■ PACKAGE DIMENSION

144-pin Plastic LQFP
(FPT-144P-M08)



Dimensions in mm (inches)

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