February 1998
Edition 2.0

- PRELIMINARY -

DATA SHEET

MB86611A

IEEE 1394 Serial Bus Controller (DV-over-1394)

DESCRIPTION

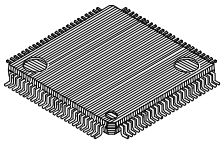
Fujitsu MB86611A is a high performance 1394 Serial Bus Controller LSI conforming to IEEE1394 standard draft (P1394; Rev.8.0 ver. 2). This controller LSI has two cable ports with on-chip differential transceivers and comparators for a network under the 1394 cable environment. For data rate, the MB86611A supports S100.

The 1394 physical layer and link layer are integrated into s single-chip for down-sizing and low power consumption.

Also, the device has a set of specific data ports for Isochronous data transfer making the isolation of header and data sections, and packetize automatically to achieve the consecutive data transfer.

Furthermore, since MB86611A has the DVC mode for the AV/C protocol to support the various automatic operations and CSR function, it is suitable for DVC use.

100-PIN PLASTIC LQFP
(FPT-100P-M05)

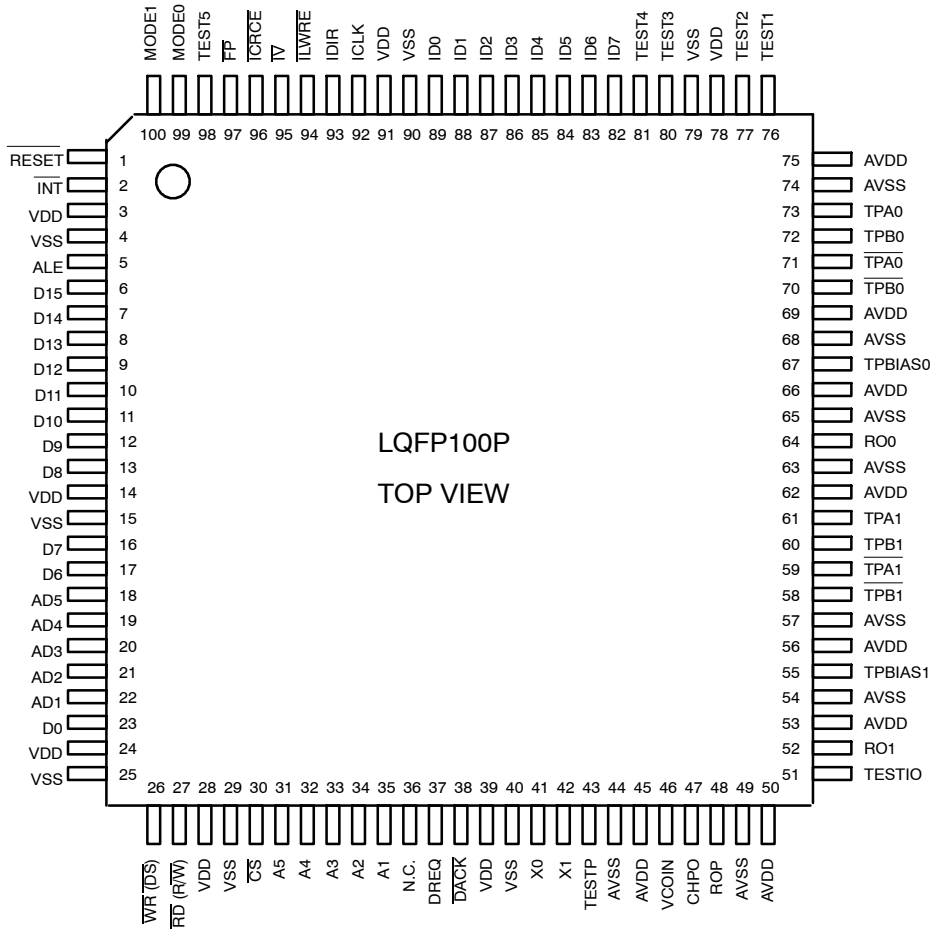


This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- Complies with IEEE 1394-1995 high-performance serial bus standard draft
- Integrates Physical layer and Link layer into a single-chip
- 2 cable ports (S100: 98.304Mbps data rate).
- 3.3V single power supply
- Internal clock generator by on-chip PLL (with crystal oscillator)
- Power Down Modes:
  1) Forced sleep by an instruction of external MPU
  2) Automatic sleep for non-connected ports
- Cycle master function
- On-chip various CSRs for Isochronous-Resource-Manager
- 32-bit CRC generation & check
- General-purpose ports for asynchronous transfer (16-bit MPU/DMA common bus)
- Isochronous-transfer ports (8-bit bus)
- On-chip Transaction sequencer
- 4-pin Cable Support
- Power supply voltage: Single +3.3 V
- Package: 100-Pin Plastic LQFP

MB86611A Pin Assignment



PIN LIST

Pin No.	I/O	80-MPU I/F Mode	68-MPU I/F Mode	Pin No.	I/O	80-MPU I/F Mode	68-MPU I/F Mode
		Pin Name	Pin Name			Pin Name	Pin Name
1	I	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	24	-	VDD	VDD
2	O	$\overline{\text{INT}}$	$\overline{\text{INT}}$	25	-	VSS	VSS
3	-	VDD	VDD	26	I	$\overline{\text{WR}}$	$\overline{\text{DS}}$
4	-	VSS	VSS	27	I	$\overline{\text{RD}}$	R/$\overline{\text{W}}$
5	I	ALE	ALE	28	-	VDD	VDD
6	IU/O	D15	D15	29	-	VSS	VSS
7	IU/O	D14	D14	30	I	$\overline{\text{CS}}$	$\overline{\text{CS}}$
8	IU/O	D13	D13	31	I	A5	A5
9	IU/O	D12	D12	32	I	A4	A4
10	IU/O	D11	D11	33	I	A3	A3
11	IU/O	D10	D10	34	I	A2	A2
12	IU/O	D9	D9	35	I	A1	A1
13	IU/O	D8	D8	36	-	N.C.	N.C.
14	-	VDD	VDD	37	O	DREQ	DREQ
15	-	VSS	VSS	38	I	$\overline{\text{DACK}}$	$\overline{\text{DACK}}$
16	IU/O	D7	D7	39	-	VDD	VDD
17	IU/O	D6	D6	40	-	VSS	VSS
18	IU/O	AD5	AD5	41	I/O	X0	X0
19	IU/O	AD4	AD4	42	I	X1	X1
20	IU/O	AD3	AD3	43	O	TESTP	TESTP
21	IU/O	AD2	AD2	44	-	AVSS	AVSS
22	IU/O	AD1	AD1	45	-	AVDD	AVDD
23	IU/O	D0	D0	46	I	VCOIN	VCOIN

(Continued)

Pin No.	I/O	80-MPU I/F Mode	68-MPU I/F Mode	Pin No.	I/O	80-MPU I/F Mode	68-MPU I/F Mode
		Pin Name	Pin Name			Pin Name	Pin Name
47	O	CHPO	CHPO	70	I/O	$\overline{\text{TPB0}}$	$\overline{\text{TPB0}}$
48	O	ROP	ROP	71	I/O	$\overline{\text{TPA0}}$	$\overline{\text{TPA0}}$
49	-	AVSS	AVSS	72	I/O	TPB0	TPB0
50	-	AVDD	AVDD	73	I/O	TPA0	TPA0
51	O	TESTIO	TESTIO	74	-	AVSS	AVSS
52	O	RO1	RO1	75	-	AVDD	AVDD
53	-	AVDD	AVDD	76	IU/O	TEST1	TEST1
54	-	AVSS	AVSS	77	IU/O	TEST2	TEST2
55	O	TPBIAS1	TPBIAS1	78	-	VDD	VDD
56	-	AVDD	AVDD	79	-	VSS	VSS
57	-	AVSS	AVSS	80	IU/O	TEST3	TEST3
58	I/O	$\overline{\text{TPB1}}$	$\overline{\text{TPB1}}$	81	IU/O	TEST4	TEST4
59	I/O	$\overline{\text{TPA1}}$	$\overline{\text{TPA1}}$	82	I/O	ID7	ID7
60	I/O	TPB1	TPB1	83	I/O	ID6	ID6
61	I/O	TPA1	TPA1	84	I/O	ID5	ID5
62	-	AVDD	AVDD	85	I/O	ID4	ID4
63	-	AVSS	AVSS	86	I/O	ID3	ID3
64	O	RO0	RO0	87	I/O	ID2	ID2
65	-	AVSS	AVSS	88	I/O	ID1	ID1
66	-	AVDD	AVDD	89	I/O	ID0	ID0
67	O	TPBIAS0	TPBIAS0	90	-	VSS	VSS
68	-	AVSS	AVSS	91	-	VDD	VDD
69	-	AVDD	AVDD	92	I	ICLK	ICLK

(Continued)

Pin No.	I/O	80-MPU I/F Mode	68-MPU I/F Mode	Pin No.	I/O	80-MPU I/F Mode	68-MPU I/F Mode
		Pin Name	Pin Name			Pin Name	Pin Name
93	I	IDIR	IDIR	97	I/O	$\overline{FP}$	$\overline{FP}$
94	O	$\overline{ILWRE}$	$\overline{ILWRE}$	98	O	TEST5	TEST5
95	I	$\overline{IV}$	$\overline{IV}$	99	I	MODE0	MODE0
96	O	$\overline{ICRCE}$	$\overline{ICRCE}$	100	I	MODE1	MODE1

PIN FUNCTION

1394 INTERFACE

Name of pin	I/O	Function
TPA0	I/O	TPA positive signal of cable port 0
$\overline{\text{TPA0}}$	I/O	TPA negative signal of cable port 0
TPB0	I/O	TPB positive signal of cable port 0
$\overline{\text{TPB0}}$	I/O	TPB negative signal of cable port 0
TPA1	I/O	TPA positive signal of cable port 1
$\overline{\text{TPA1}}$	I/O	TPA negative signal of cable port 1
TPB1	I/O	TPB positive signal of cable port 1
$\overline{\text{TPB1}}$	I/O	TPB negative signal of cable port 1
TPBIAS0	O	Reference voltage output pin for common voltage on cable port 0
TPBIAS1	O	Reference voltage output pin for common voltage on cable port 0
RO0	O	Ground this pin through a 4.8kΩ resistor.
RO1	O	Ground this pin through a 4.8kΩ resistor.

ISOCHRONOUS INTERFACE

Name of pin	I/O	Function
ICLK	I	Clock input pin for Isochronous-Data Interface. (4MHz to 16MHz)
IDIR	I	Data Direction Control pin for Isochronous transfer. When "0" is input, it clears FIFO and enters "Transmission" state. Data transmission starts after asserting $\overline{\text{ILWRE}}$ signal and receiving one packet data specified in the packet header setting register at address 10h of bank-0 registers. When "1" is input, it clears FIFO and enters "Receipt" state. However, when there are any packets in process (in transmission), the device will not be in "receipt" state until all the packet is transmitted. Receiving 1 packet asserts $\overline{\text{ILWRE}}$ signal. IDIR signal should normally be "1" ("H"), and should be "0" ("L") only when transmitting the data.
$\overline{\text{ILWRE}}$	O	Access Permission Signal output pin for Isochronous-FIFO. For Transmission state : It becomes "Active" if FIFO has a space. This signal is negated by the FIFO state "Full". At the negate state of this signal, the device receives the data for a rising edge of the next ICLK signal. When the Bus-Reset is detected, it is negated after receiving the data on packet boundary. After the bus reset, this signal is again asserted at the completion of transmitting one packet data from the FIFO. For Receipt state: This signal is asserted when one packet is completely received in the FIFO. It is once negated every time when one packet is read out from the FIFO. When the FIFO still has packets in it, the signal is again asserted.
ID7 - ID0	I/O	Data input/output pins for Isochronous transfer. (MSB:ID7, LSB:ID0)
$\overline{\text{IV}}$	I	Enable Signal Input pin for ID7-ID0. For Transmission state : While this signal is active, the data are fetched into FIFO at the rising edge of ICLK. For Receipt state : Making this signal state "Active" starts to send the data in FIFO to ID7-ID0. After that, the data changes synchronizing with the rising edge of ICLK.
$\overline{\text{ICRCE}}$	O	This signal indicates that data CRC error occurred in the received data.
$\overline{\text{FP}}$	I/O	Time-Stamp Trigger Signal input/output pin. For transmission state: This is a Time-Stamp Trigger input pin. The MB86611A fetches it's internal cycle timer register value by a falling edge of this signal. For Receipt state : This pin outputs the detection signal that Time-Stamp matched.

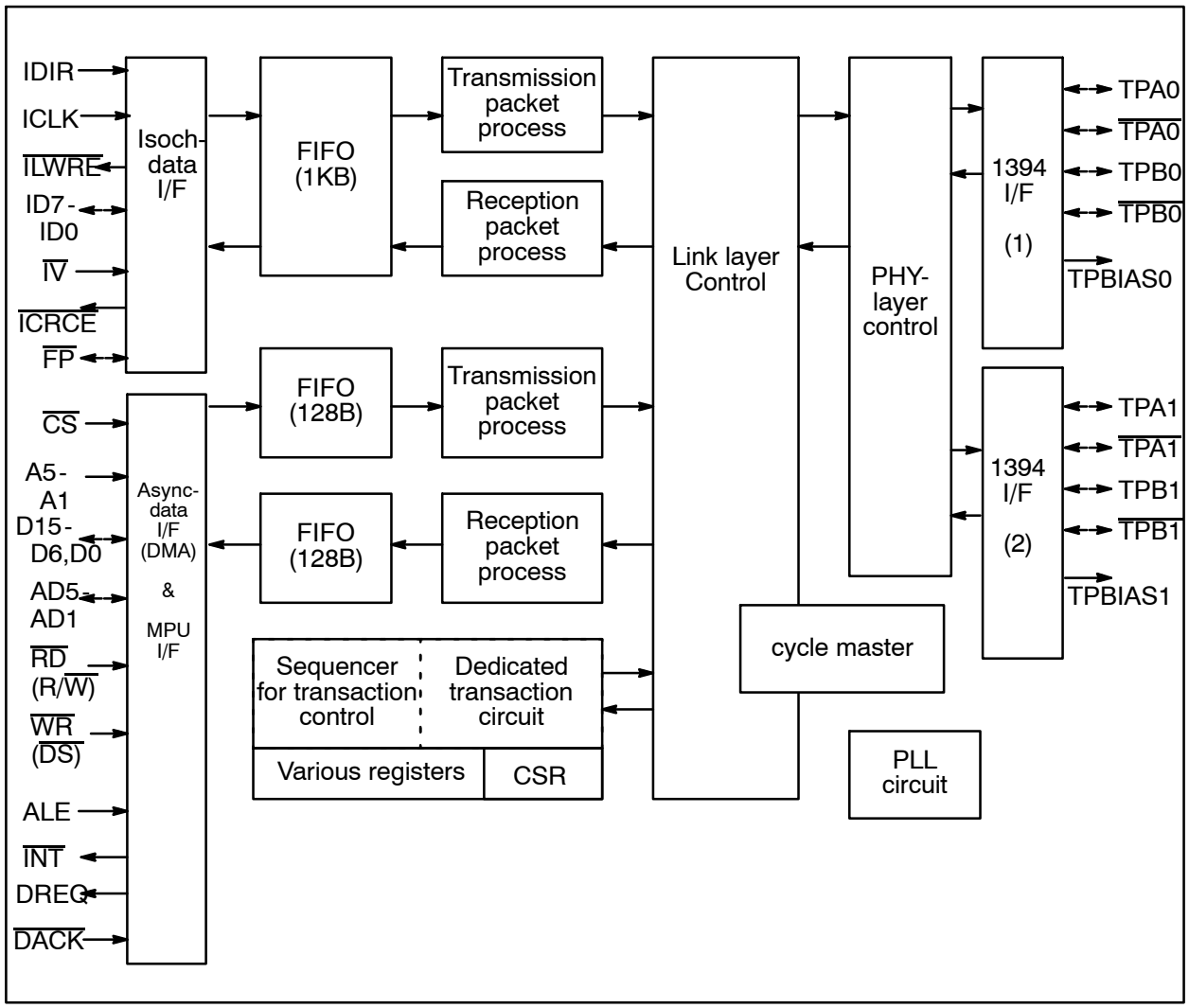
SYSTEM INTERFACE

Name of pin	I/O	Function
$\overline{CS}$	I	Chip Select signal Input pin for MPU to select this device as an I/O device
A5 to A1	I	Address input pin for selecting internal registers. These signals are valid only when the Non-multiplexed Mode is selected. This signal must be at ”0” for multiplexed mode.
D15 to D6, D0	I/O	16-bit data bus input/output pins. (MSB:D15, LSB:D0)
AD5 to AD1	I/O	16-bit data bus input/output pins. (MSBAD5, LSB:AD1) When address/data multiplexed mode is selected, these signals also serve as the address input pins.
$\overline{RD}$ (R/$\overline{W}$)	I	In 80-system mode: Input pin of read strobe signal for output data to data bus from this device In 68-system mode: Input pin of control signal R/W for output and input data from/to this device
$\overline{WR}$ ($\overline{DS}$)	I	In 80-system mode: Input pin for Write strobe signal for input data on data bus to this device In 68-system mode: Input pin of $\overline{DS}$ signal output when data bus enabled
ALE	I	This is a ALE signal input pin used to input ALE signal which is output while the specified address is valid in the Multiplexed mode. For the non-multiplexed mode, please input ”0” to this pin.
DREQ	O	DMA transfer request signal for DMAC during asynchronous transfer in DMA mode. DMA transfer is requested between this device and memory.
$\overline{DACK}$	I	DMA acknowledgement signal from DMA during asynchronous transfer in DMA mode
$\overline{INT}$	O	Interrupt output pin.

OTHERS

Name of pin	I/O	Function
X0	I/O	External crystal oscillator pins for oscillation circuit
X1	I	
VCOIN	I	VCO input pin for internal PLL
CHPO	O	Charge pump output pin for internal PLL
ROP	O	Ground this pin through a 4.8kΩ resistor.
$\overline{\text{RESET}}$	I	Reset signal input pin. By detecting the assertion of this signal, the device enters a Force-Sleep mode automatically.
MODE0	I	MPU Mode select pin. When ”0” : 80-system mode, and when ”1” : 68-system mode
MODE1	I	Address/Data Multiplexed Mode select pin. When ”0” : Non-multiplexed mode, and when ”1” : Multiplexed mode.
AVDD	-	Analog power supply pin
AVSS	-	Analog GND pin
VDD	-	Digital power supply pin
VSS	-	Digital GND pin
TEST1,2,3,4	IU/O	Device test pins. Do not connect with these pins.
TEST5	O	
TESTP, TESTIO	O	
NC	-	Non-connection pin. Do not connect.

BLOCK DIAGRAM



BLOCK FUNCTION

<Physical layer>

- Supports asynchronous transfer and isochronous transfer under IEEE 1394 cable environment
- 100 Mb/s transfer speed
- Two ports for analog transceiver/receiver, with bus status monitor, initialization, arbitration and encode/decode functions for data transmission/reception

<Link layer>

- Controls generation and transfer of standard packet in compliance with IEEE 1394
- Generates and checks 32-bits CRC for data and header
- Incorporates 32-bits cycle timer register and cycle master function

<Transmission/Receipt Packet Processing Unit>

- Transmission : Packetizes the header, data, and CRC sections. CRC is generated and added automatically.
- Receipt : Separates the 1394 packet into header and data sections and discards CRC section.

<Transmission/Reception FIFO>

- Incorporates 1KB FIFO for combined transmission/reception as isochronous transfer
- Incorporates 128B FIFO for both transmission/reception as asynchronous transfer

<Sequencer for Universal Transaction>

- Controls 1394 bus protocol by setting universal transfer command and transfer auxiliary command

<Dedicated Transaction Circuit>

- Packetizes the data dedicated to DVC format from data interface pin and reconstructs a receive data to data interface pin with transmission/reception packet processing unit for transfer

<Registers>

- MB86611A's own control registers, transfer parameter registers, DVC registers, and CSRs are built in. The built-in CSRs have the function required for Isochronous Resource Manager.

<PLL circuit>

- Generates internal operation clock and transfer clock from reference clock generated by crystal oscillator circuit. Reference oscillation frequency: 8.192 MHz

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Supply voltage	V_{DD}	V_{SS} - 0.5	+4.0	V
Input voltage	V_I	V_{SS} - 0.5	V_{DD} + 0.5	V
Output voltage	V_O	V_{SS} - 0.5	V_{DD} + 0.5	V
Operating ambient temperature*2	T_{OP}	-40	+85	°C
Storage temperature	T_{STG}	-55	+125	°C
Output current *3	I_O	-14	+ 14	mA
Overshoot *4	-	-	VDD+1.0	V
Undershoot *4	-	-	VSS-1.0	V

*1: The voltage ratings are based on VSS=0V.
*2: Operating ambient temperature rating does not guarantee the continuous chip operation.
*3: Output current rating is the output current that can be flown in steady. (Min.: at Vo=0V, Max.: Vo=VDD).
*4: Overshoot/Undershoot are within 50ns.

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value		Unit
			Min.	Max.	
Power-supply voltage		V_{DD}	3.0	3.6	V
Ambient temperature		T_A	0	70	°C
”H” level Input Voltage	CMOS Input	V_{IH}	V_{DD} x 0.65	V_{DD}	V
”L” level Input Voltage	CMOS Input	V_{IL}	V_{SS}	V_{DD} x 0.25	V
Differential Input Voltage @ data xfer	Cable Input	V_{ID}	142	260	mV
Differential Input Voltage @ arbitration	Cable Input	V_{IDA}	173	260	mV
Common Phase Input Voltage	Cable Input	V_{CM}	1.165	2.515	V
Receive Input Jitter	Cable Input	-	-	1.08	ns
Receive Input Skew	Cable Input	-	-	0.8	ns
Output Current	CMOS Output	I_{OL}/I_{OL}	-4	+4	mA
	TPBIAS	I_{OT}	-2	10	mA

*1: Voltage is based on VSS=0V.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

1394 INTERFACE

(1) Driver

(V_{DD} = +3 V to +3.6V, V_{SS} = 0V, T_A =0 to+70°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Differential Output voltage	V_{OD}	RI=55Ω	172	-	265	mV
Common Phase Current	I_{CM}	Driver enabled	-0.81	-	0.44	mA
Off-state Voltage	V_{OFF}	Driver disabled	-	-	20	mV
TPBIAS Output Voltage	V_O	-	1.665	-	2.015	V

(2) Comparator

(V_{DD} = +3 V to +3.6V, V_{SS} = 0V, T_A =0 to+70°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Common Phase Input Current	I_{IC}	Driver disabled	-20	-	20	μA
Rising Arbitration Comparator Threshold Voltage	V_{SCR}	-	89	-	168	mV
Falling Arbitration Comparator Threshold Voltage	V_{SCL}	-	-168	-	-89	mV
Cable Bias Detection Threshold Voltage / TPBx Input	V_{SD}	-	0.6	-	1.0	V

SYSTEM INTERFACE

(V_{DD} = +3 V to +3.6V, V_{SS} = 0V, T_A =0 to+70°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
”H” Level Input Voltage		V_{IH}	CMOS Input	V_{DD}x0.65	-	V_{DD}	V
”L” Level Input Voltage		V_{IL}	CMOS Input	V_{SS}	-	V_{DD}x0.25	V
”H” Level Output Voltage		V_{OH}	I_{OH}=-4mA	V_{DD}-0.5	-	V_{DD}	V
”L” Level Output Voltage		V_{OL}	I_{OL}=4mA	V_{SS}	-	0.4	V
Input Leakage Current	Input Pins	I_{LI}	V_I=0V to VDD	-5	-	5	mA
	Three-state input pins	I_{LZ}		-5	-	5	mA
Input Pull-up Resistor		R_P	V_{IH}=0V	25	50	200	kΩ
Supply Current	When 2 ports used.	I_{DD}	-	-	-	250	mA
	When 1 port used.	I_{DD1}	-	-	-	200	mA
	When port is not used.	I_{DD0}	-	-	-	180	mA
	Forced-sleep state	I_{DDS}	-	-	-	30	mA

AC CHARACTERISTICS

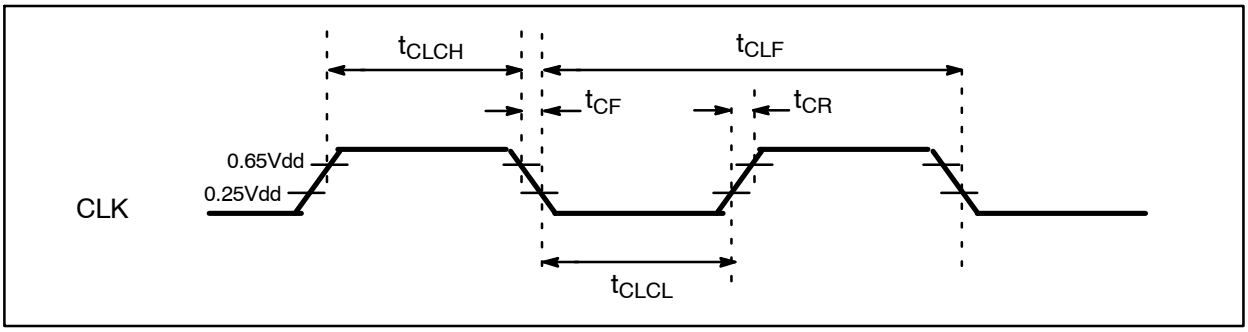
1394 DRIVER

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Transmit Jitter	t_{JT}	-	-	-	±0.8	ns
Transmit Skew	t_{SK}	-	-	-	±0.8	ns
Transmit Rising Time *	t_{DR}	C_L=10pF , R_L=55Ω	-	-	3.2	ns
Transmit Falling Time *	t_{DF}		-	-	3.2	ns

Note * : The levels are between 10% and 90%.

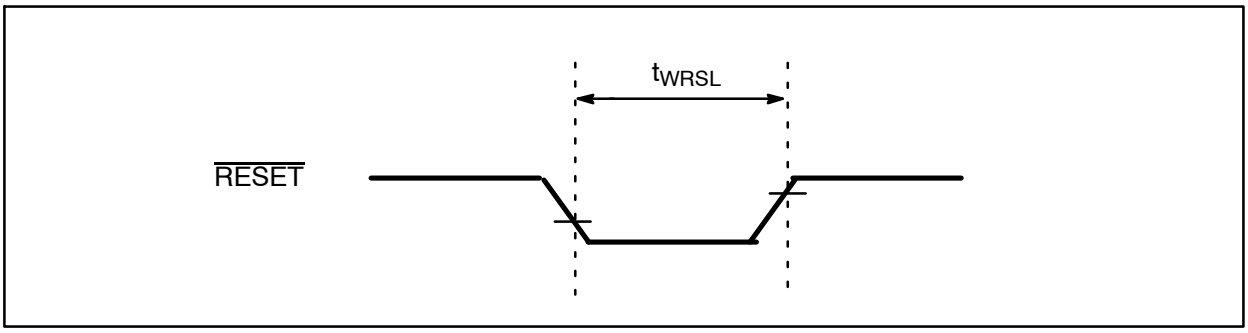
SYSTEM CLOCK

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Clock Frequency	f_C	-	-	8.192	-	MHz
Clock Cycle Time	t_{CLF}	-	-	1/fc	-	ns
Clock Pulse "H" Width	t_{CLCH}	-	50	-	-	ns
Clock Pulse "L" Width	t_{CLCL}	-	50	-	-	ns
Clock Rising Time	t_{CR}	-	-	-	5	ns
Clock Falling Time	t_{CF}	-	-	-	5	ns



SYSTEM RESET

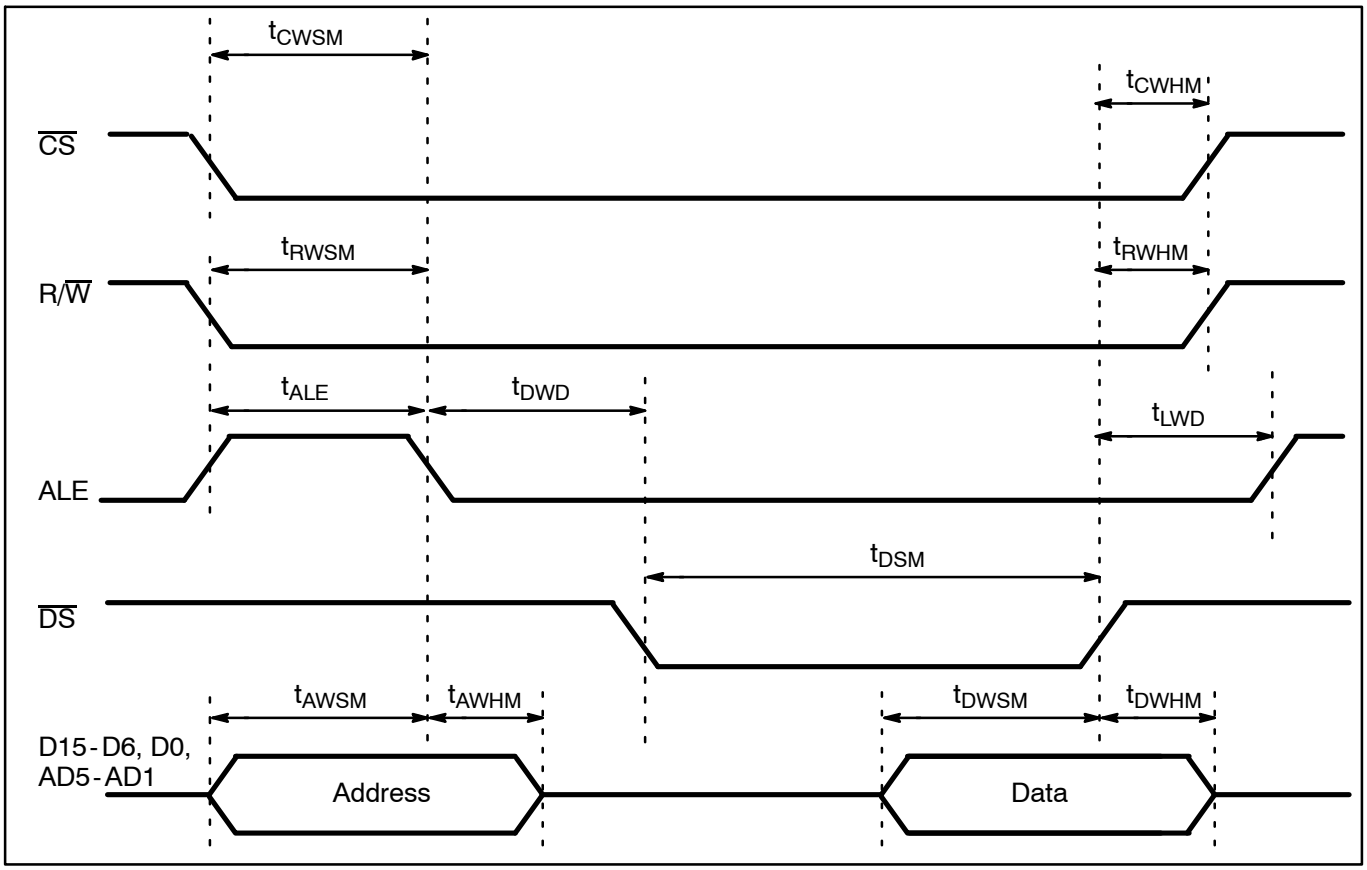
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Reset Signal ”L” level Pulse Width	t_{WRSL}	-	$4t_{CLF}$	-	-	ns



MPU INTERFACE

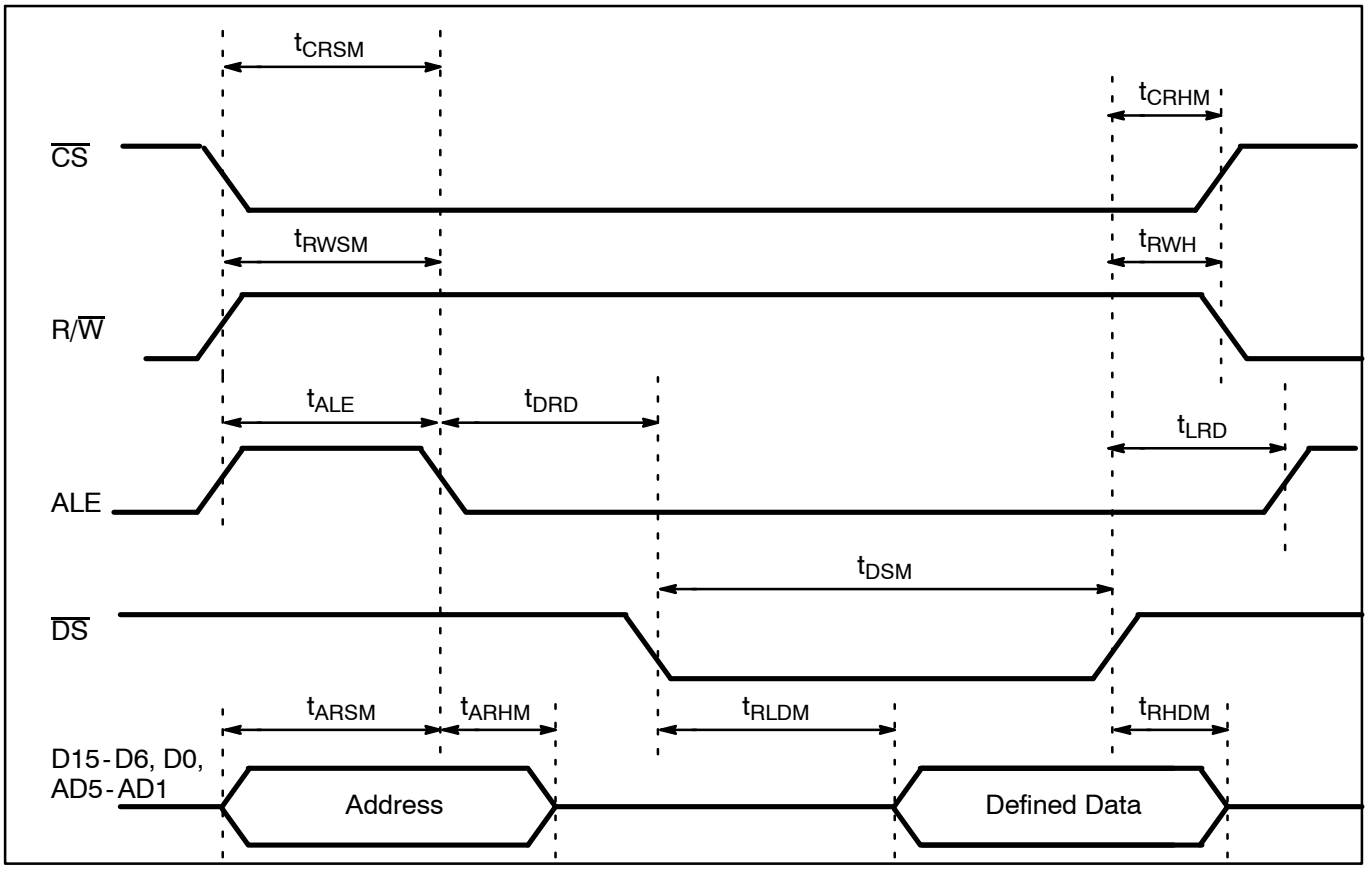
(1) 68-Series MPU Register Write Operation (Multiplex)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{AWSM}	-	10	-	-	ns
Address Hold Time	t_{AWHM}	-	10	-	-	ns
$\overline{CS}$ Setup Time	t_{CWSM}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CWHM}	-	10	-	-	ns
R/$\overline{W}$ Setup Time	t_{RWSM}	-	20	-	-	ns
R/$\overline{W}$ Hold Time	t_{RWHM}	-	10	-	-	ns
ALE "H" Level Pulse Width	t_{ALE}	-	15	-	-	ns
ALE Falling → $\overline{DS}$ Falling Time	t_{DWD}	-	15	-	-	ns
$\overline{DS}$ "L" Level Pulse Width	t_{DSM}	-	40	-	-	ns
Data Setup Time	t_{DWSM}	-	10	-	-	ns
Data Hold Time	t_{DWHM}	-	0	-	-	ns
$\overline{DS}$ Rising → ALE Rising Time	t_{LWD}	-	20	-	-	ns



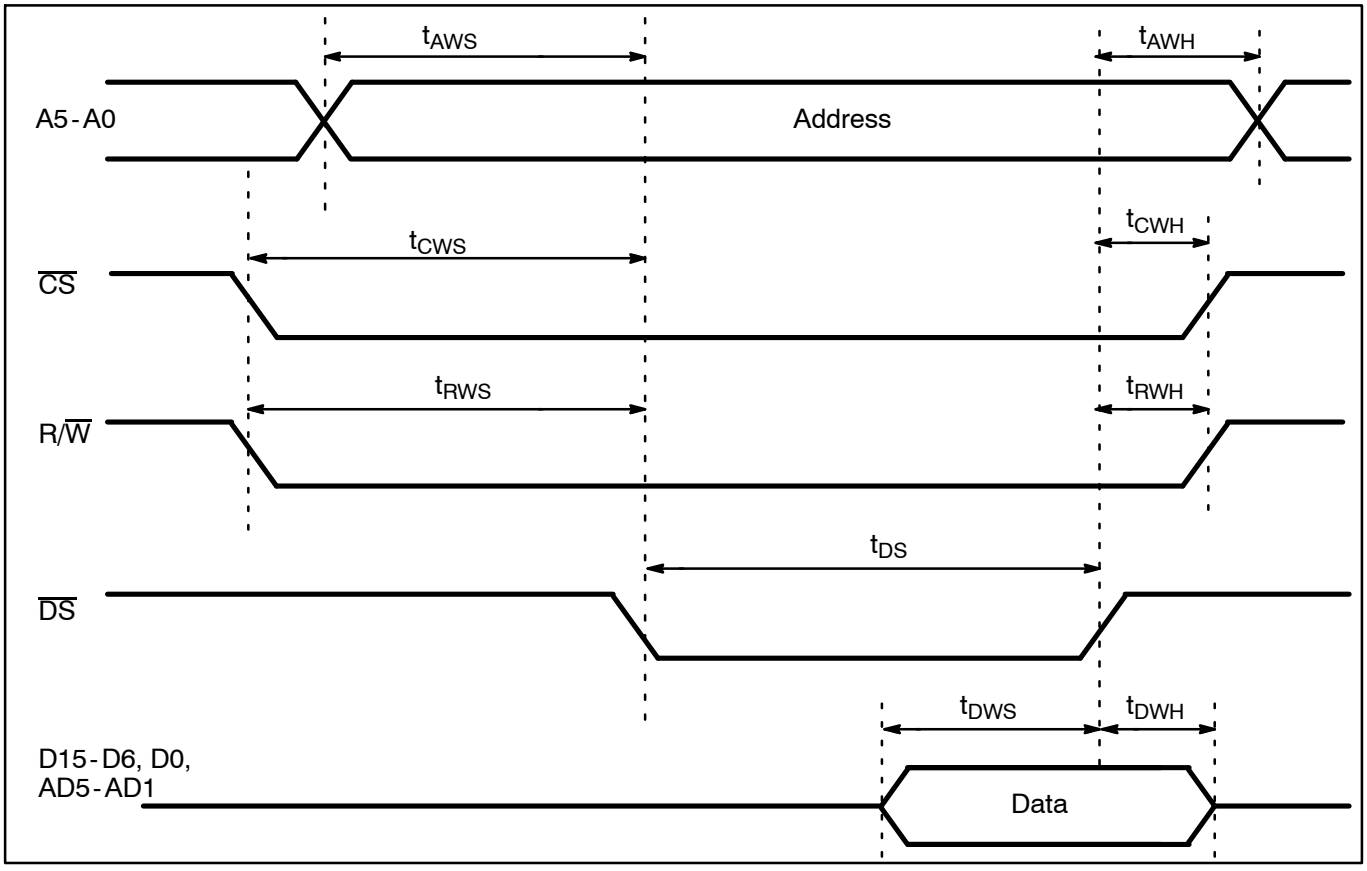
(2) 68-Series MPU Register Read Operation (Multiplex)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{ARSM}	-	10	-	-	ns
Address Hold Time	t_{ARHM}	-	10	-	-	ns
$\overline{CS}$ Setup Time	t_{CRSM}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CRHM}	-	10	-	-	ns
R/$\overline{W}$ Setup Time	t_{RWSM}	-	20	-	-	ns
R/$\overline{W}$ Hold Time	t_{RWH}	-	10	-	-	ns
ALE "H" Level Pulse Width	t_{ALE}	-	15	-	-	ns
ALE Falling → $\overline{DS}$ Falling Time	t_{DRD}	-	15	-	-	ns
$\overline{DS}$ "L" Level Pulse Width	t_{DSM}	-	40	-	-	ns
Data Output Defined Time	t_{RLDM}	-	-	-	40	ns
Data Output Disable Time	t_{RHDM}	-	5	-	-	ns
$\overline{DS}$ Rising → ALE Rising Time	t_{LRD}	-	20	-	-	ns



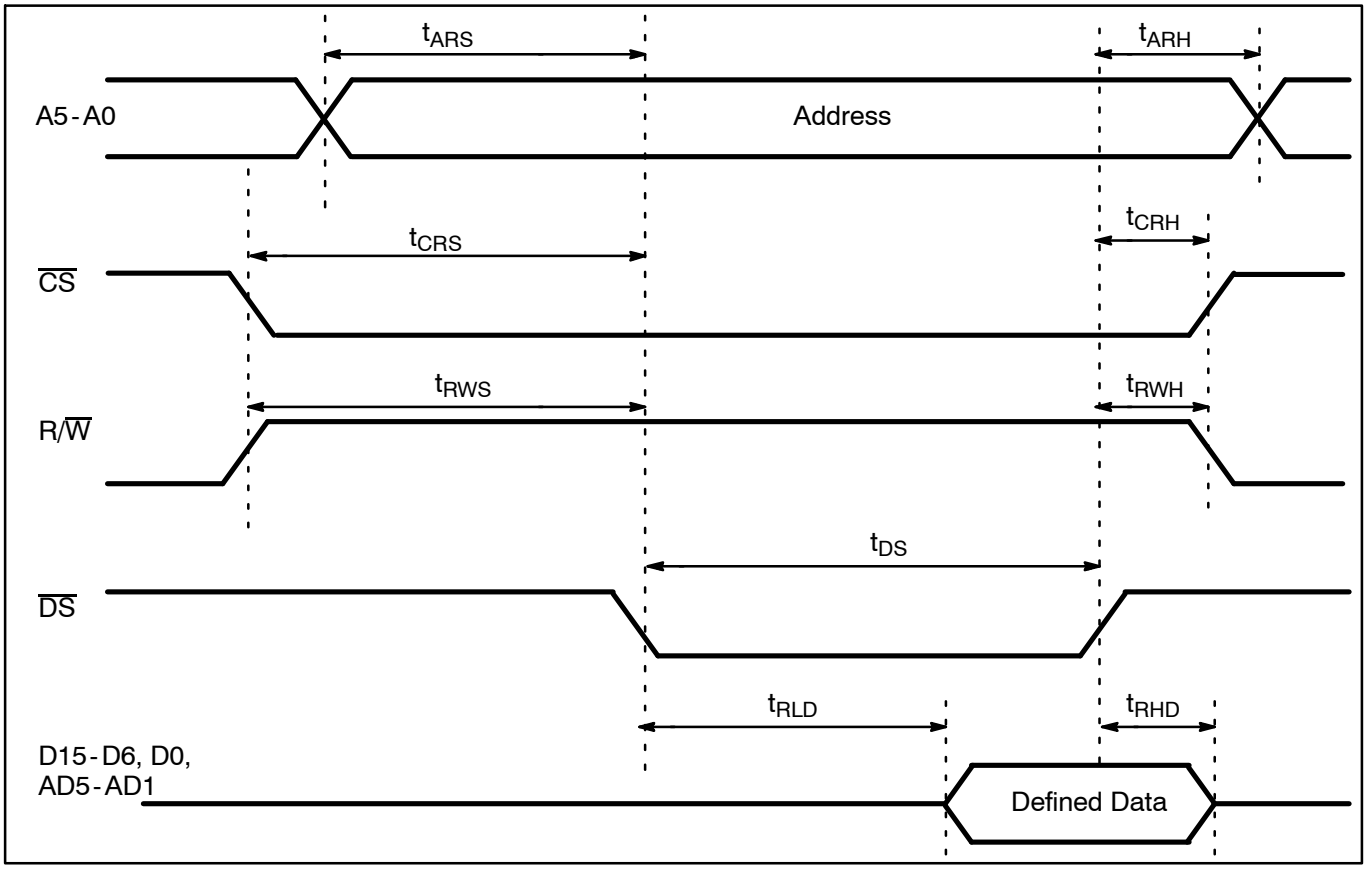
(3) 68-Series MPU Register Write Operation (Non-multiplex)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{AWS}	-	10	-	-	ns
Address Hold Time	t_{AWH}	-	20	-	-	ns
$\overline{CS}$ Setup Time	t_{CWS}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CWH}	-	10	-	-	ns
R/$\overline{W}$ Setup Time	t_{RWS}	-	20	-	-	ns
R/$\overline{W}$ Hold Time	t_{RWH}	-	10	-	-	ns
$\overline{DS}$ "L" Level Pulse Width	t_{DS}	-	40	-	-	ns
Data Setup Time	t_{DWS}	-	40	-	-	ns
Data Hold Time	t_{DWH}	-	0	-	-	ns



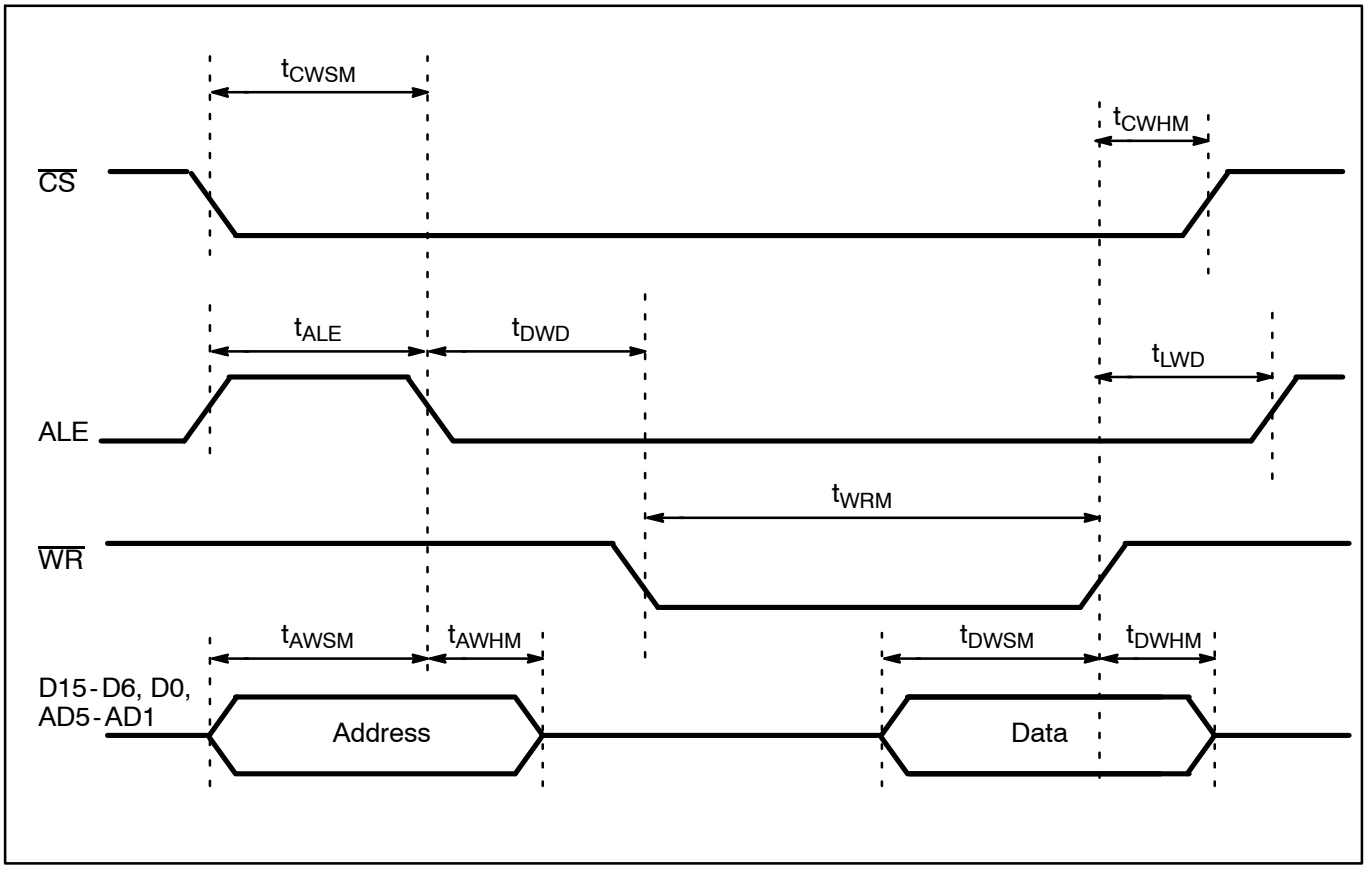
(4) 68-Series MPU Register Read Operation (Non-multiplex)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{ARS}	-	10	-	-	ns
Address Hold Time	t_{ARH}	-	20	-	-	ns
$\overline{CS}$ Setup Time	t_{CRS}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CRH}	-	10	-	-	ns
R/$\overline{W}$ Setup Time	t_{RWS}	-	20	-	-	ns
R/$\overline{W}$ Hold Time	t_{RWH}	-	10	-	-	ns
$\overline{DS}$ "L" Level Pulse Width	t_{DS}	-	40	-	-	ns
Data Output Defined Time	t_{RLD}	-	-	-	40	ns
Data Output Disable Time	t_{RHD}	-	5	-	-	ns



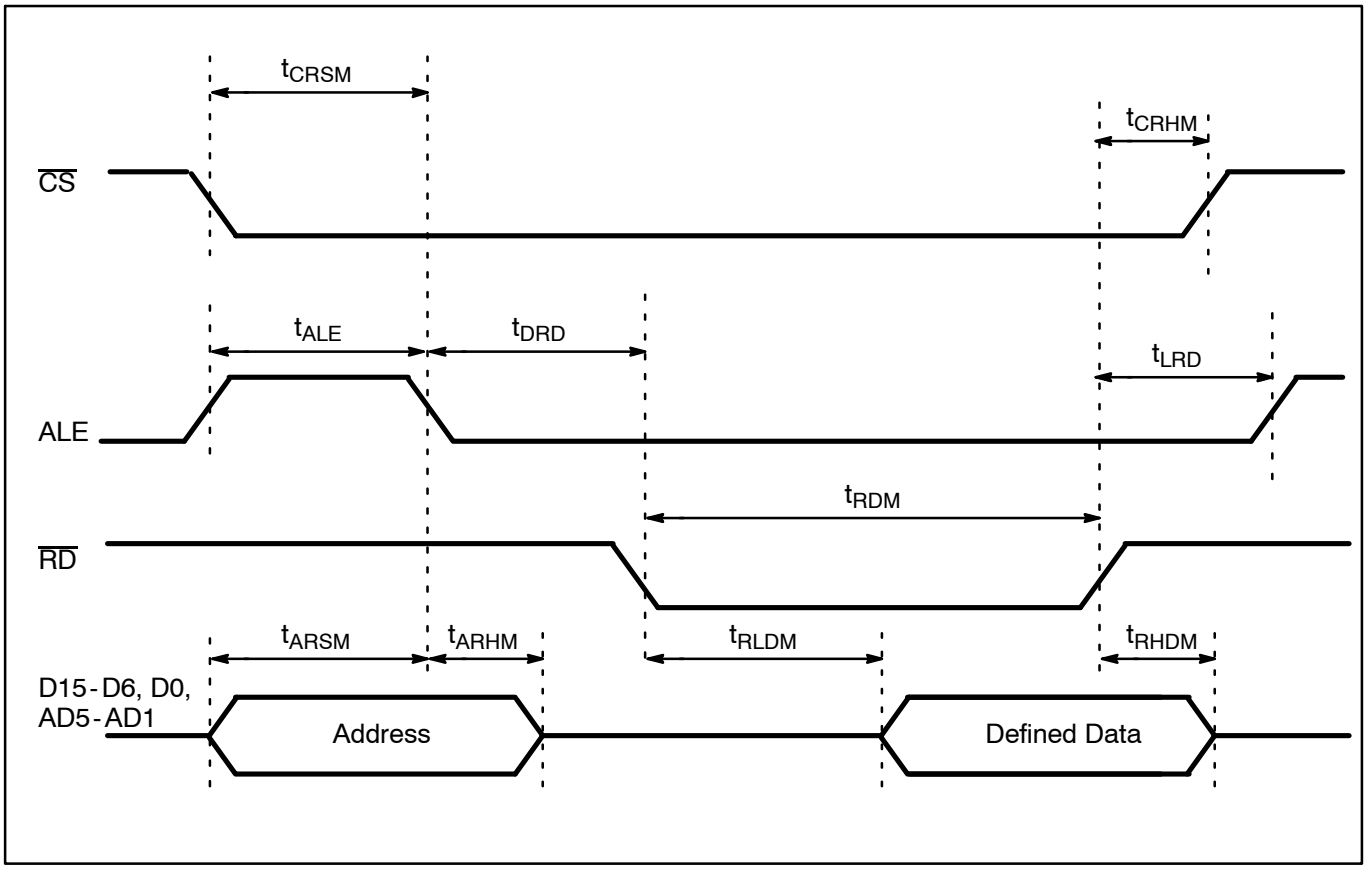
(5) 80-Series MPU Register Write Operation (Multiplex)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{AWSM}	-	10	-	-	ns
Address Hold Time	t_{AWHM}	-	10	-	-	ns
$\overline{CS}$ Setup Time	t_{CWSM}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CWHM}	-	10	-	-	ns
ALE "H" Level Pulse Width	t_{ALE}	-	15	-	-	ns
ALE Falling → $\overline{WR}$ Falling Time	t_{DWD}	-	15	-	-	ns
$\overline{WR}$ "L" Level Pulse Width	t_{WRM}	-	40	-	-	ns
Data Setup Time	t_{DWSM}	-	40	-	-	ns
Data Hold Time	t_{DWHM}	-	0	-	-	ns
$\overline{WR}$ Rising → ALE Rising Time	t_{LWD}	-	20	-	-	ns



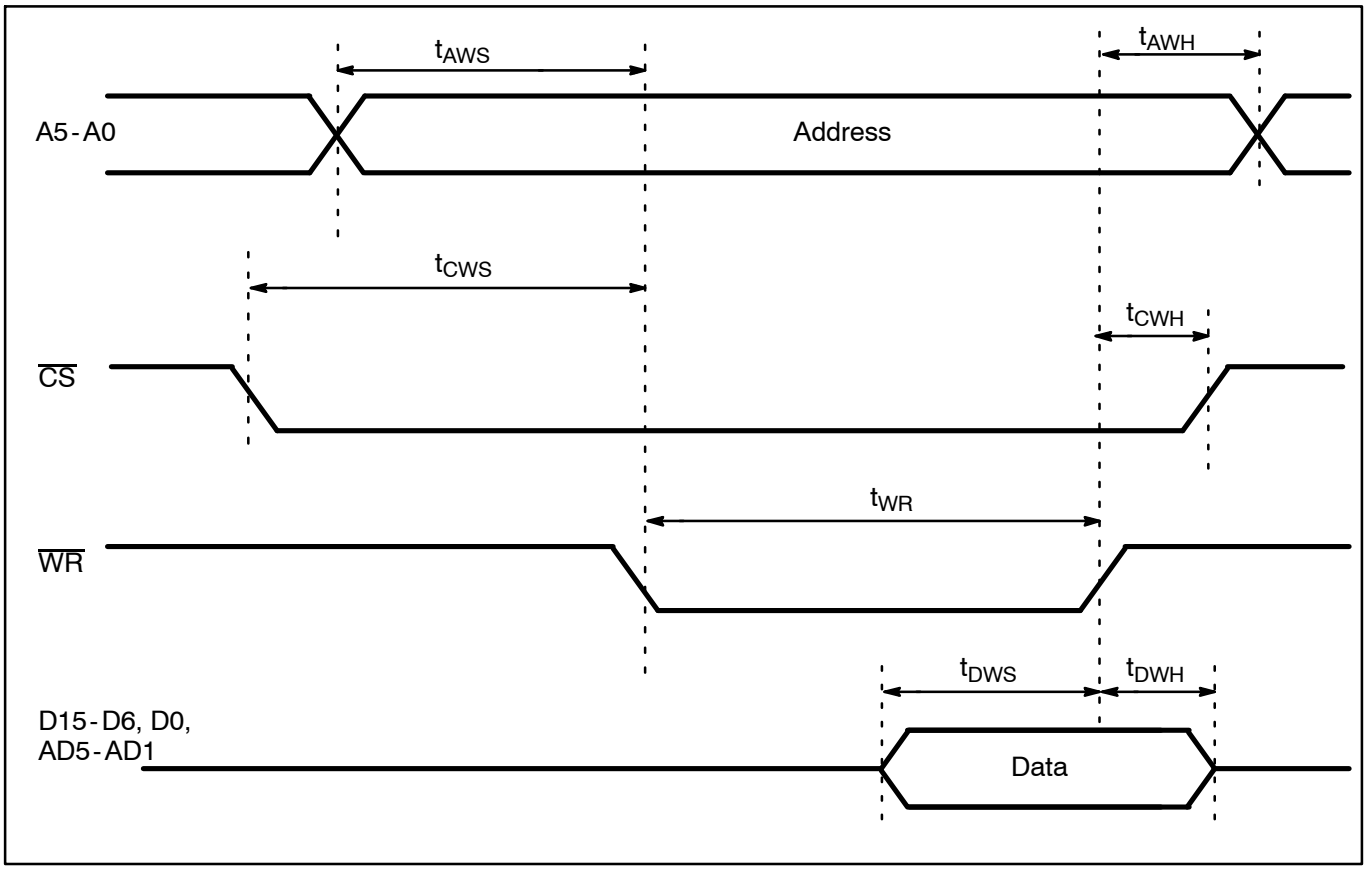
(6) 80-Series MPU Register Read Operation (Multiplex)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{ARSM}	-	10	-	-	ns
Address Hold Time	t_{ARHM}	-	10	-	-	ns
$\overline{CS}$ Setup Time	t_{CRSM}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CRHM}	-	10	-	-	ns
ALE "H" Level Pulse Width	t_{ALE}	-	15	-	-	ns
ALE Falling → $\overline{RD}$ Falling Time	t_{DRD}	-	15	-	-	ns
$\overline{RD}$ "L" Level Pulse Width	t_{RDM}	-	40	-	-	ns
Data Output Defined Time	t_{RLDM}	-	-	-	40	ns
Data Output Disable Time	t_{RHDM}	-	5	-	-	ns
$\overline{RD}$ Rising → ALE Rising Time	t_{LRD}	-	20	-	-	ns



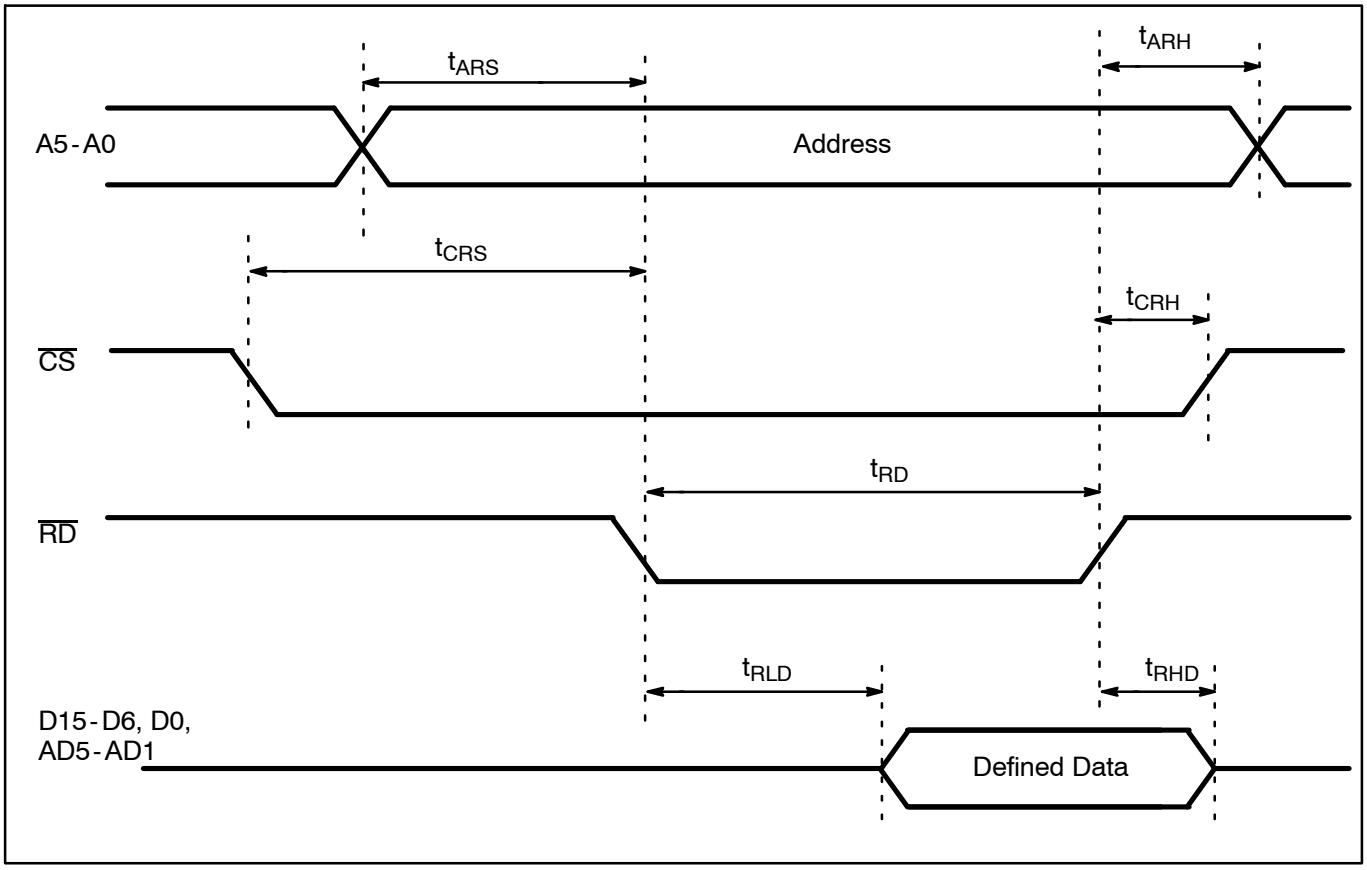
(7) 80-Series MPU Register Write Operation (Non-multiplex)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{AWS}	-	10	-	-	ns
Address Hold Time	t_{AWH}	-	20	-	-	ns
$\overline{CS}$ Setup Time	t_{CWS}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CWH}	-	10	-	-	ns
$\overline{WR}$ "L" Level Pulse Width	t_{WR}	-	40	-	-	ns
Data Setup Time	t_{DWS}	-	40	-	-	ns
Data Hold Time	t_{DWH}	-	0	-	-	ns



(8) 80-Series MPU Register Read Operation (Non-multiplex)

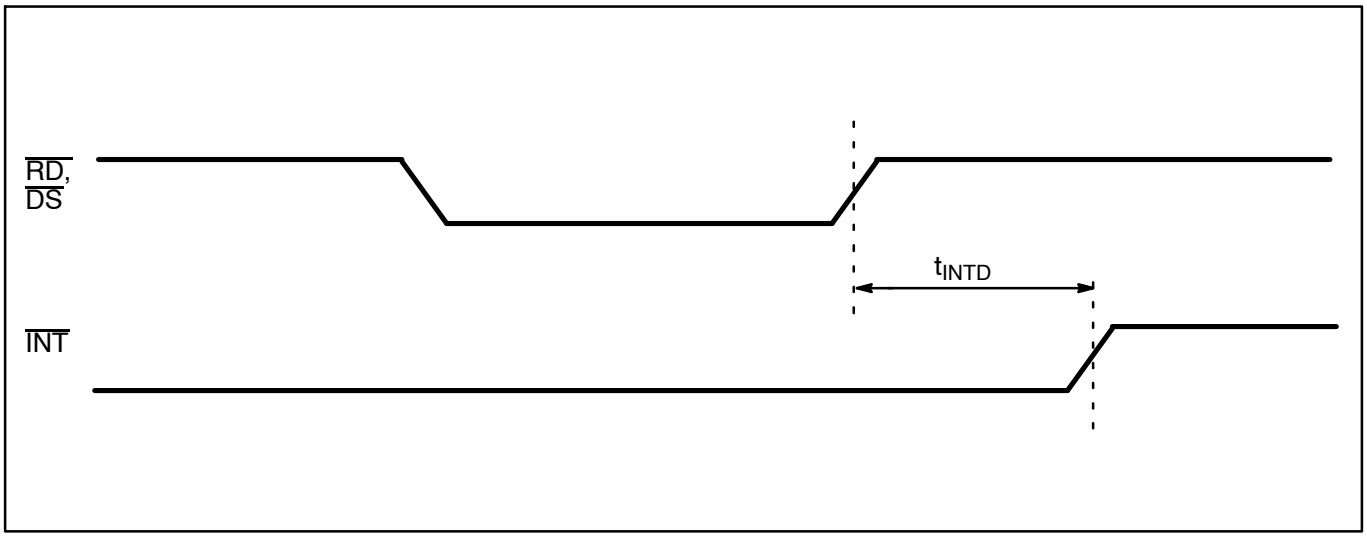
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address Setup Time	t_{ARS}	-	10	-	-	ns
Address Hold Time	t_{ARH}	-	20	-	-	ns
$\overline{CS}$ Setup Time	t_{CRS}	-	20	-	-	ns
$\overline{CS}$ Hold Time	t_{CRH}	-	10	-	-	ns
$\overline{RD}$ "L" Level Pulse Width	t_{RD}	-	40	-	-	ns
Data Output Defined Time	t_{RLD}	-	-	-	40	ns
Data Output Disable Time	t_{RHD}	-	5	-	-	ns



(9) INT Signal Timing

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
INT Read out → $\overline{INT}$ Signal Negation	t_{INTD}	-	100	-	-	ns

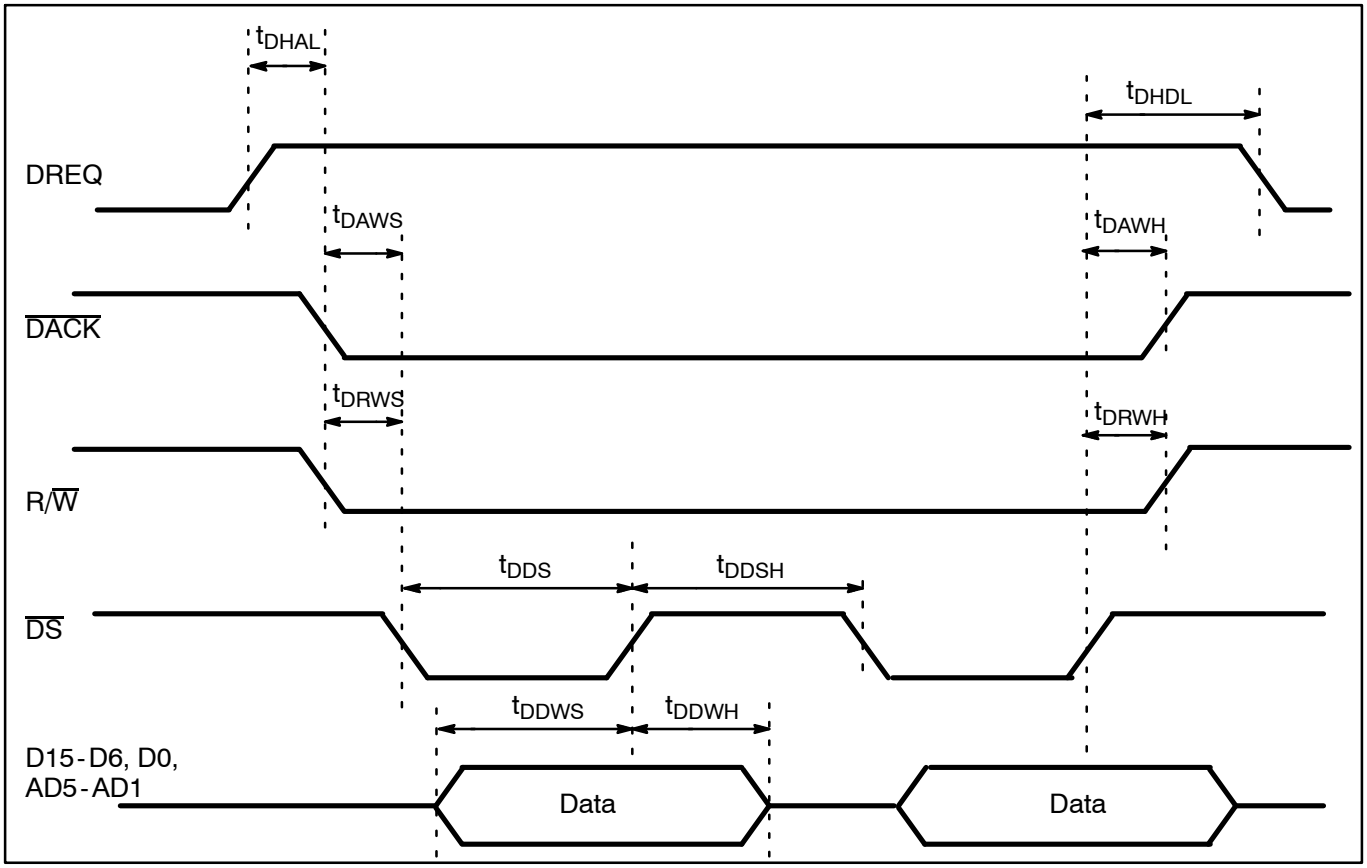
This AC timing is applicable to only when the last data is read out from the interrupt register. The other timing specifications for read operation follow the specification for each operation mode.



DMA ACCESS

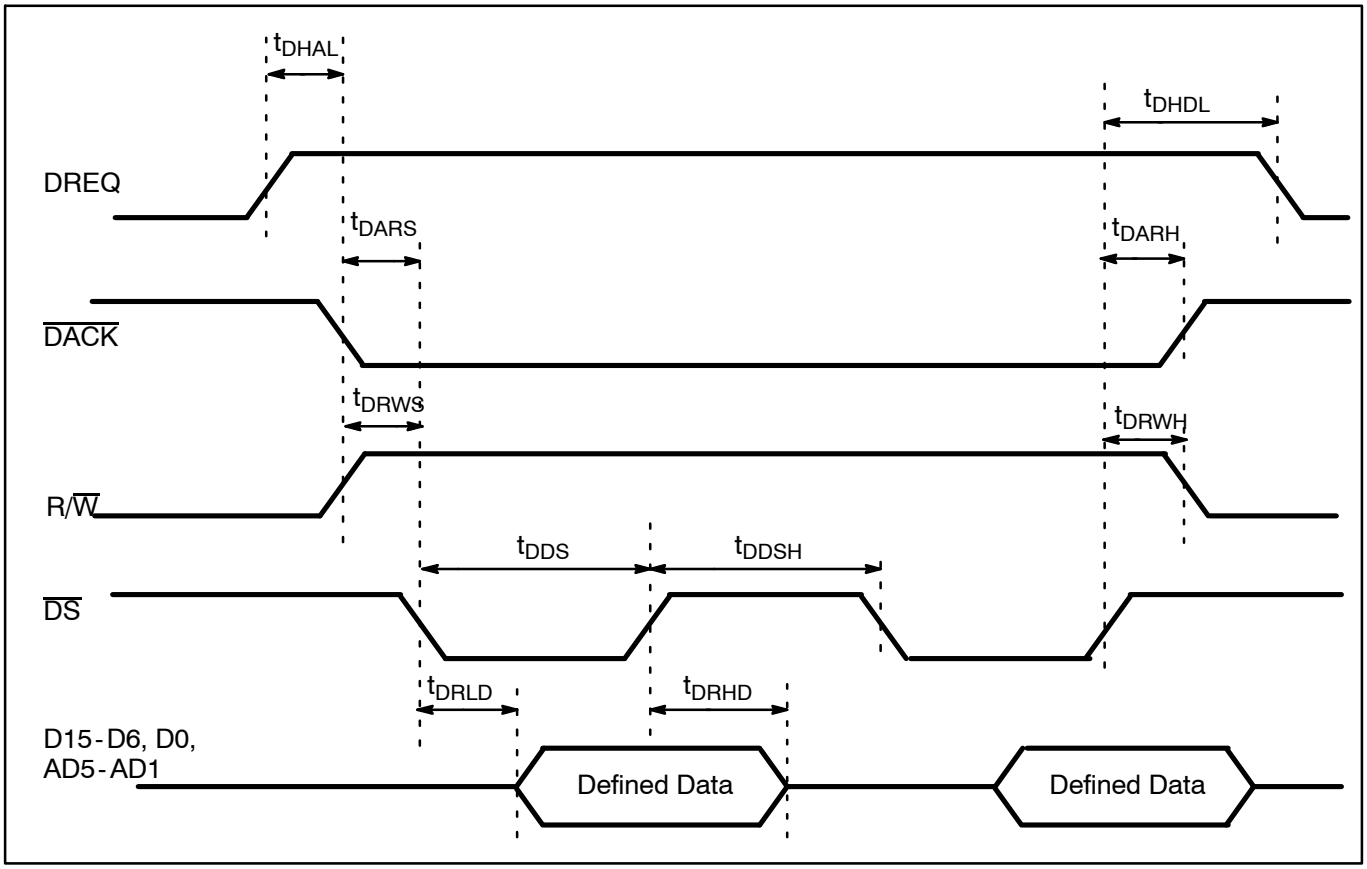
(1) 68-Series DMA Write Operation

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
DREQ "H" → $\overline{DACK}$ "L"	t_{DHAL}	-	0	-	-	ns
$\overline{DS}$ "H" → DREQ "L"	t_{DHDL}	-	-	-	30	ns
$\overline{DACK}$ Setup Time	t_{DAWS}	-	20	-	-	ns
$\overline{DACK}$ Hold Time	t_{DAWH}	-	0	-	-	ns
R/$\overline{W}$ Setup Time	t_{DRWS}	-	20	-	-	ns
R/$\overline{W}$ Hold Time	t_{DRWH}	-	10	-	-	ns
$\overline{DS}$ "L" Level Pulse Width	t_{DDS}	-	40	-	-	ns
$\overline{DS}$ "H" Level Pulse Width	t_{DDSH}	-	30	-	-	ns
Input Data Setup Time	t_{DDWS}	-	30	-	-	ns
Input Data Hold Time	t_{DDWH}	-	0	-	-	ns



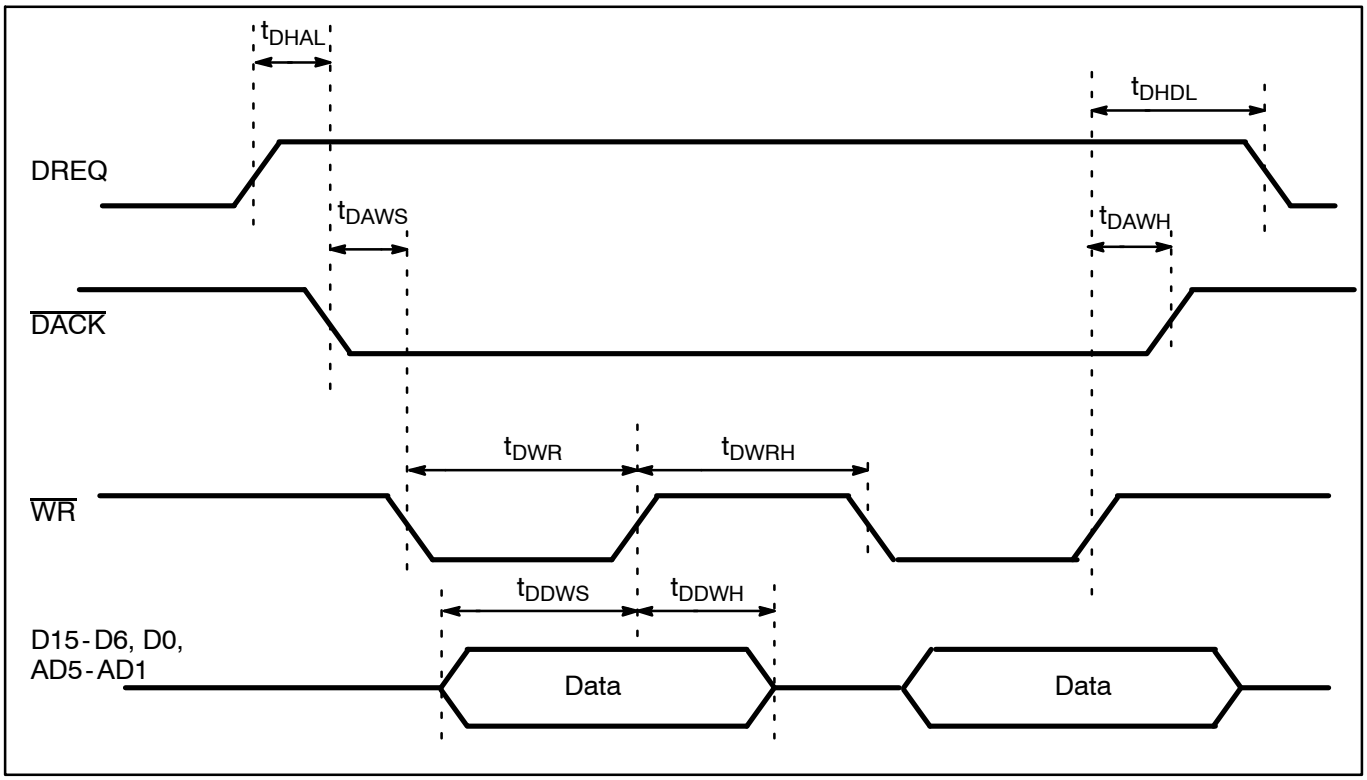
(2) 68-Series DMA Read Operation

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
DREQ "H" → $\overline{DACK}$ "L"	t_{DHAL}	-	0	-	-	ns
$\overline{DS}$ "H" → DREQ "L"	t_{DHDL}	-	-	-	30	ns
$\overline{DACK}$ Setup Time	t_{DARS}	-	20	-	-	ns
$\overline{DACK}$ Hold Time	t_{DARH}	-	0	-	-	ns
R/$\overline{W}$ Setup Time	t_{DRWS}	-	20	-	-	ns
R/$\overline{W}$ Hold Time	t_{DRWH}	-	10	-	-	ns
$\overline{DS}$ "L" Level Pulse Width	t_{DDS}	-	40	-	-	ns
$\overline{DS}$ "H" Level Pulse Width	t_{DDSH}	-	30	-	-	ns
Data Output Defined Time	t_{DRLD}	-	-	-	40	ns
Data Output Disable Time	t_{DRHD}	-	5	-	-	ns



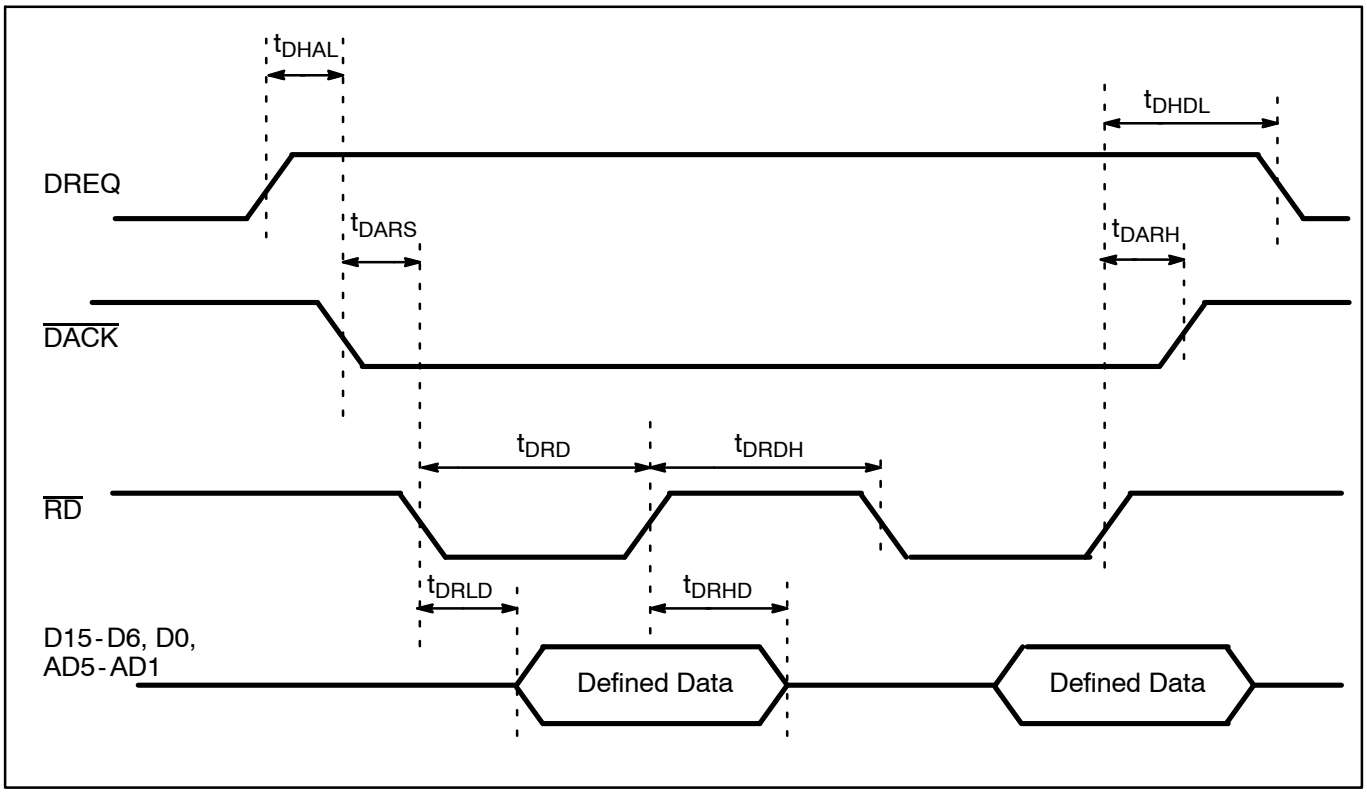
(3) 80-Series DMA Write Operation

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
DREQ "H" → $\overline{DACK}$ "L"	t_{DHAL}	-	0	-	-	ns
$\overline{WR}$ "H" → DREQ "L"	t_{DHDL}	-	-	-	30	ns
$\overline{DACK}$ Setup Time	t_{DAWS}	-	20	-	-	ns
$\overline{DACK}$ Hold Time	t_{DAWH}	-	0	-	-	ns
$\overline{WR}$ "L" Level Pulse Width	t_{DWR}	-	40	-	-	ns
$\overline{WR}$ "H" Level Pulse Width	t_{DWRH}	-	30	-	-	ns
Input Data Setup Time	t_{DDWS}	-	30	-	-	ns
Input Data Hold Time	t_{DDWH}	-	0	-	-	ns



(4) 80-Series DMA Read Operation

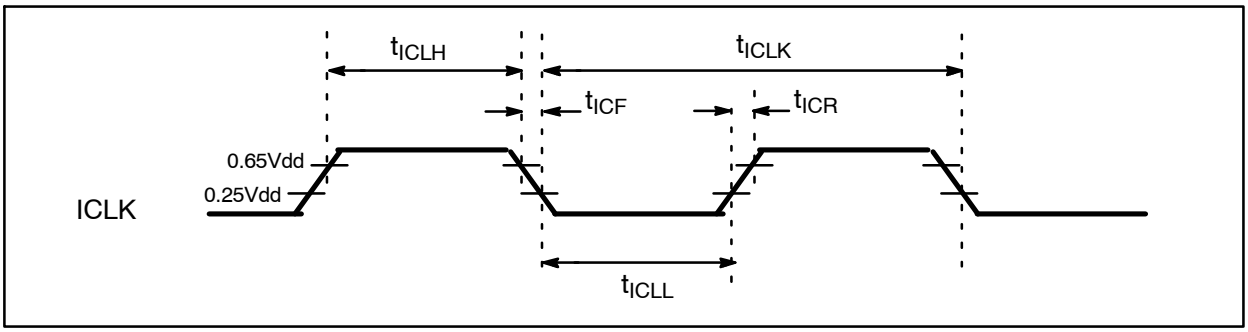
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
DREQ "H" → $\overline{DACK}$ "L"	t_{DHAL}	-	0	-	-	ns
$\overline{RD}$ "H" → DREQ "L"	t_{DHDL}	-	-	-	30	ns
$\overline{DACK}$ Setup Time	t_{DARS}	-	20	-	-	ns
$\overline{DACK}$ Hold Time	t_{DARH}	-	0	-	-	ns
$\overline{RD}$ "L" Level Pulse Width	t_{DRD}	-	40	-	-	ns
$\overline{RD}$ "H" Level Pulse Width	t_{DRDH}	-	30	-	-	ns
Data Output Defined Time	t_{DRLD}	-	-	-	40	ns
Data Output Disable Time	t_{DRHD}	-	5	-	-	ns



ISOCHRONOUS INTERFACE

(1) ICLK Timing

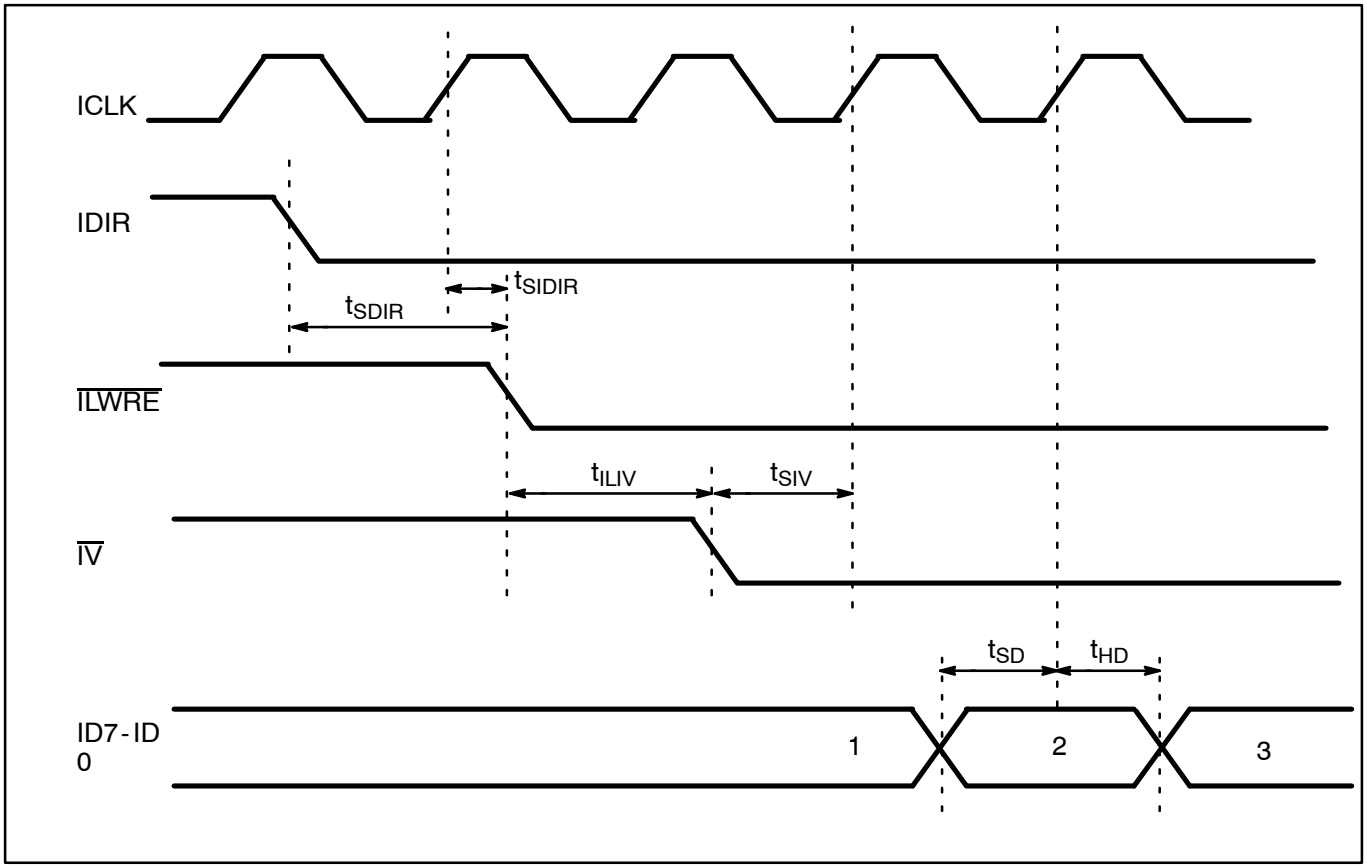
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Clock Frequency	f_{IC}	-	4	-	16	MHz
Clock Cycle Time	t_{ICLK}	-	62.5	-	250	ns
Clock Pulse ”H” Width	t_{ICLH}	-	20	-	-	ns
Clock Pulse ”L” Width	t_{ICLL}	-	20	-	-	ns
Clock Rising Time	t_{ICR}	-	-	-	7	ns
Clock Falling Time	t_{ICF}	-	-	-	7	ns



(2) Transmit Timing

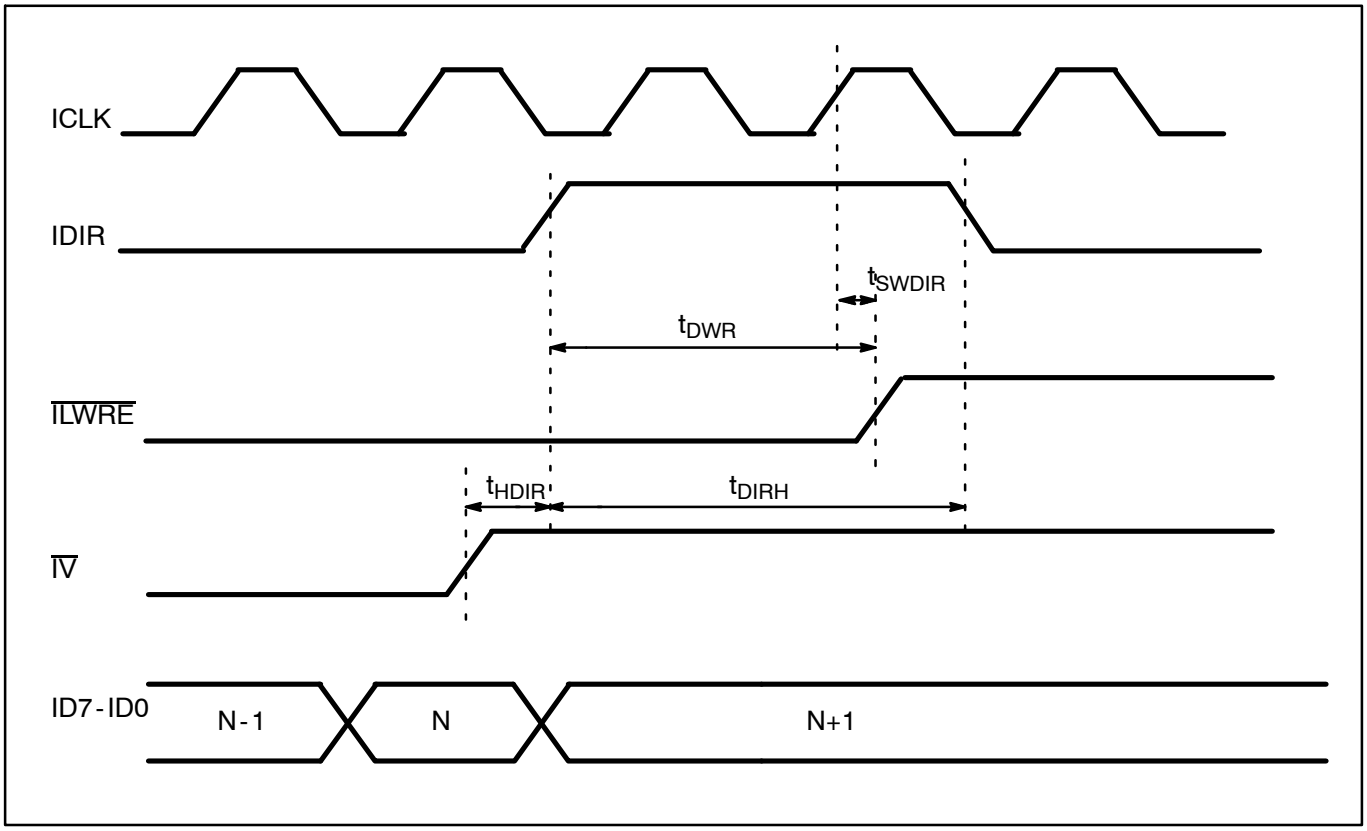
Xmit Activation

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
IDIR Falling → $\overline{\text{ILWRE}}$ Falling Time	t_{SDIR}	-	-	-	t_{ICLK}+125	ns
ICLK Rising → $\overline{\text{IV}}$ Falling Time	t_{SIDIR}	-	-	-	40	ns
$\overline{\text{ILWRE}}$ Falling → $\overline{\text{IV}}$ Falling Time	t_{ILIV}	-	0	-	-	ns
$\overline{\text{IV}}$ Setup Time	t_{SIV}	-	40	-	-	ns
Data Setup Time	t_{SD}	-	20	-	-	ns
Data Hold Time	t_{HD}	-	0	-	-	ns



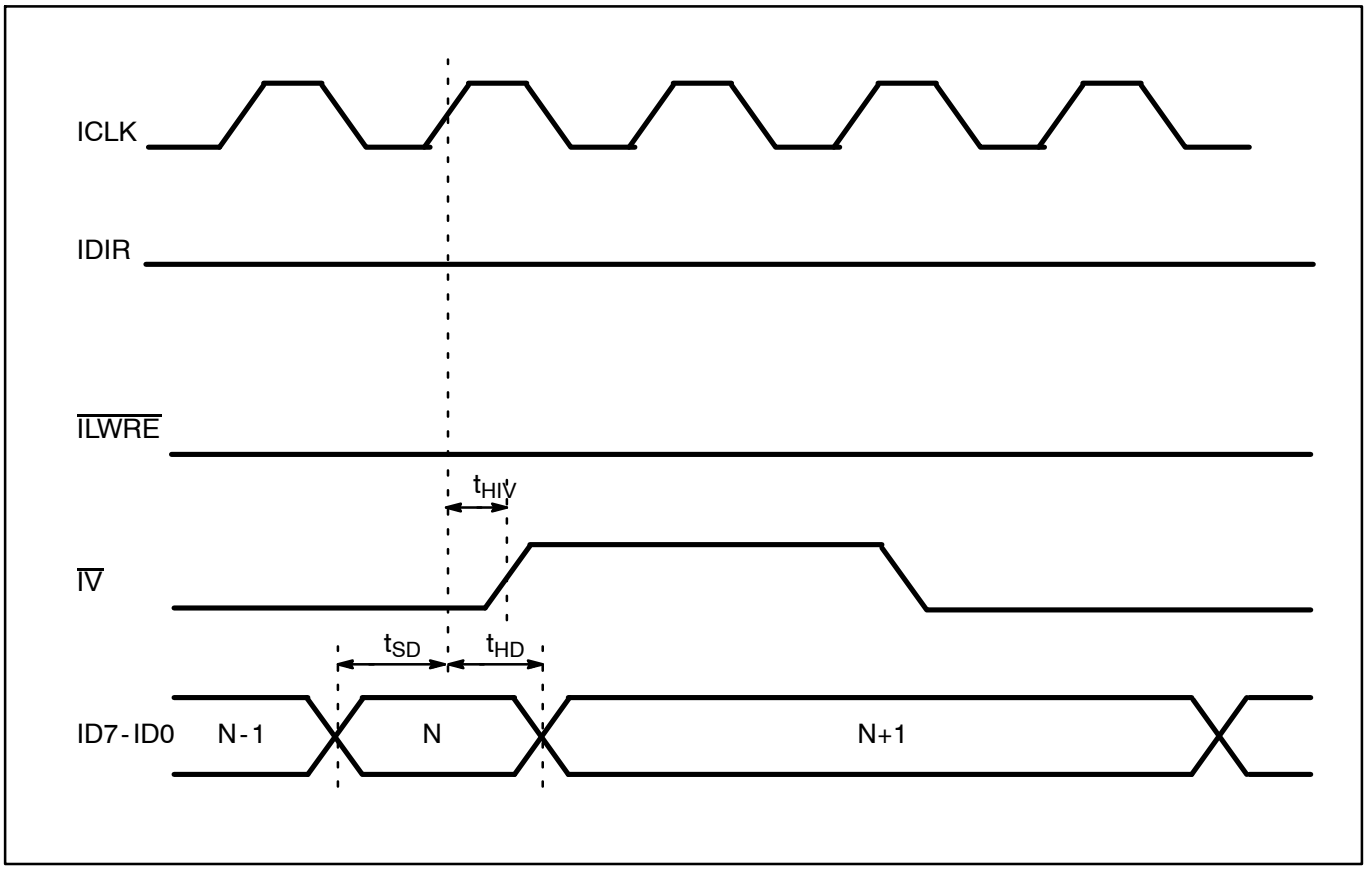
Xmit Termination

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
$\overline{IV}$ Rising → IDIR Rising Time	t_{HDIR}	-	0	-	-	ns
IDIR Rising → $\overline{ILWRE}$ Rising Time	t_{DWR}	-	-	-	$1t_{ICLK}+40$	ns
ICLK Rising → $\overline{ILWRE}$ Rising Time	t_{SWDIR}	-	-	-	40	ns
IDIR Rising → IDIR Falling Time	t_{DIRH}	-	250	-	-	µs



Transmission to $\overline{IV}$ Temporary Negation

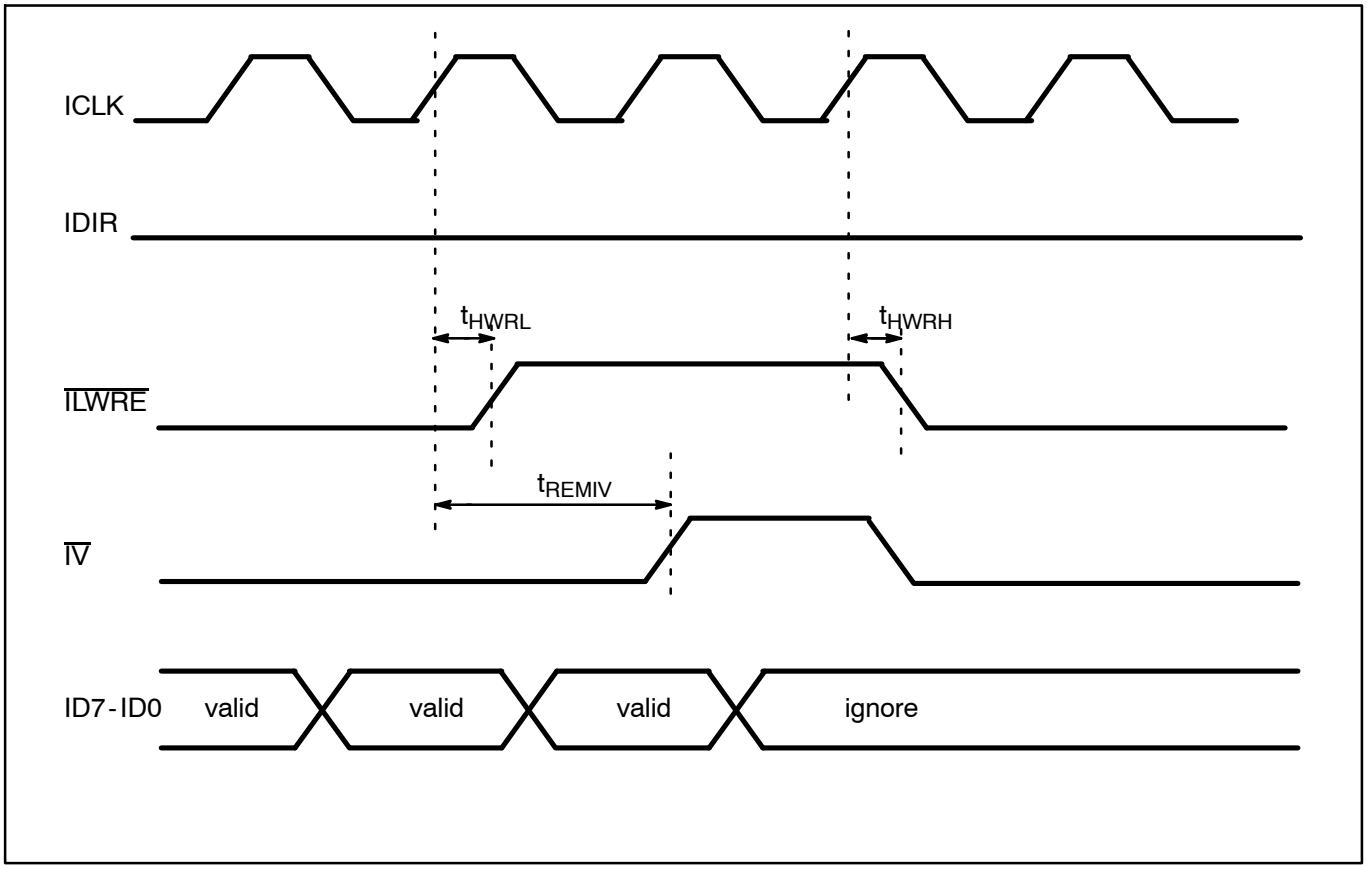
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
$\overline{IV}$ Hold Time	t_{HIV}	-	0	-	t_{ICLK}-40	ns
Data Setup Time	t_{SD}	-	20	-	-	ns
Data Hold Time	t_{HD}	-	0	-	-	ns



$\overline{\text{ILWRE}}$ Negation during Transmission (at Bus Reset detected or FIFO-full state)

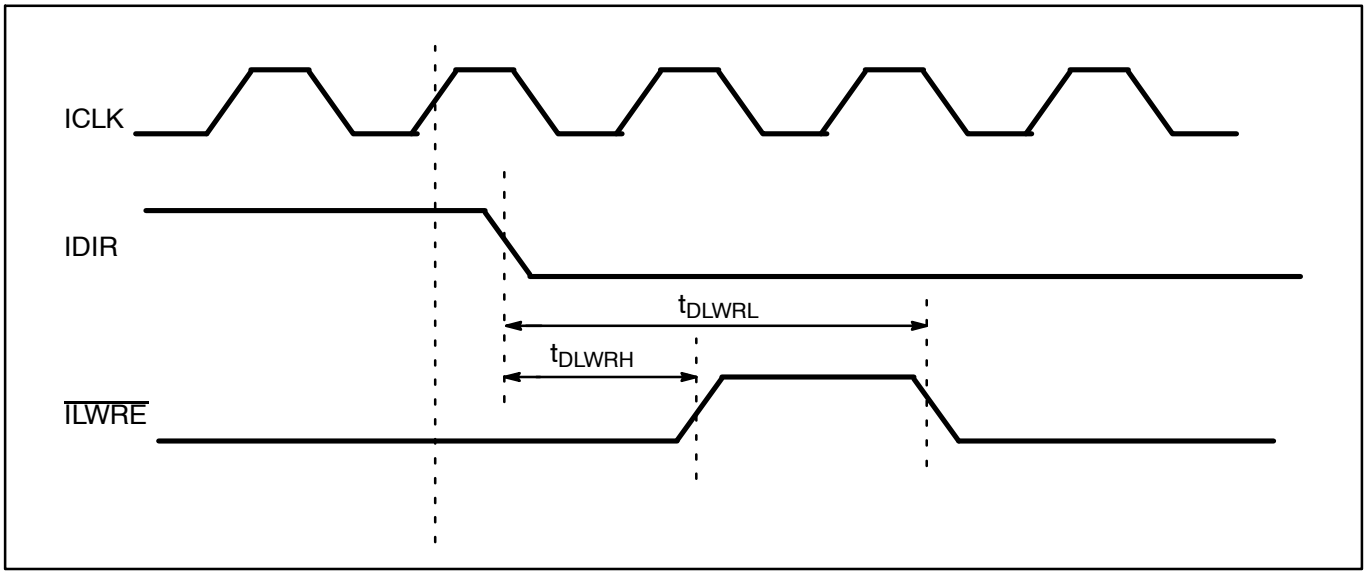
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
ICLK Rising → $\overline{\text{ILWRE}}$ Rising Time	t_{HWRL}	-	-	-	40	ns
$\overline{\text{ILWRE}}$ Rising → $\overline{\text{IV}}$ Rising Time	t_{REMIV}	-	t_{ICLK}	-	$2t_{ICLK}-40$	ns
ICLK Rising → $\overline{\text{ILWRE}}$ Falling Time	t_{HWRH}	-	-	-	40	ns

Because the MB86611A pauses the write operation for transmit data under the following conditions, it negates the $\overline{\text{ILWRE}}$ signal.
1) When the transmit Isochronous-FIFO is full. ($\overline{\text{ILWRE}}$ is negated synchronized with one ICLK before the FIFO is full.)
2) When bus reset is detected. (After the bus reset detected, $\overline{\text{ILWRE}}$ is negated synchronized with one ICLK before fetching 1 packet into the FIFO.)
Condition to resume the transmit: When 1 packet is transmitted.



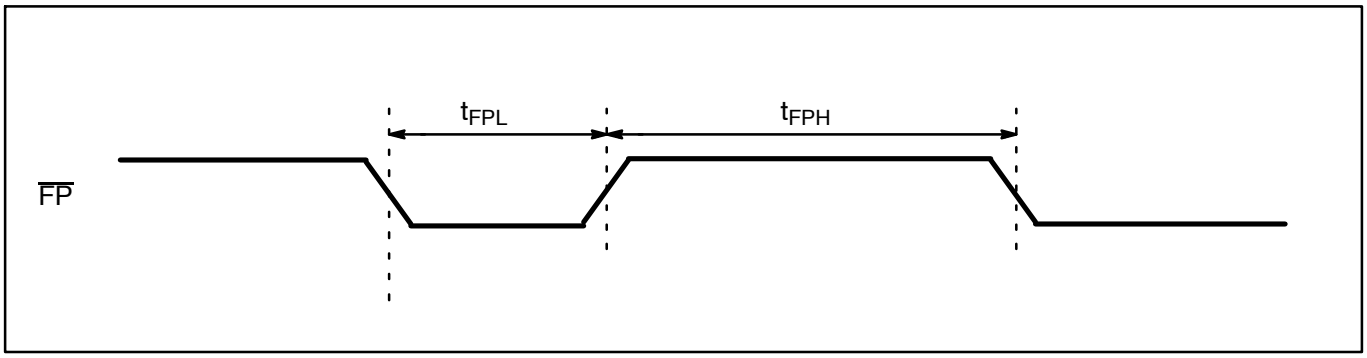
Switch to Transmission during Receive

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
IDIR Falling → $\overline{\text{ILWRE}}$ Rising Time	t_{DLWRH}	-	-	-	t_{ICLK}+40	ns
IDIR Falling → $\overline{\text{ILWRE}}$ Falling Time	t_{DLWRL}	-	-	-	$2t_{ICLK}$+40	ns



$\overline{FP}$ Input Timing

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
$\overline{FP}$ "L" Level Pulse Width	t_{FPL}	-	100	-	-	ns
$\overline{FP}$ "H" Level Pulse Width	t_{FPH}	-	125	-	-	µs
$\overline{FP}$ "L" Detected → CTR Value Fetch	t_{CTR}	-	80	-	150	ns

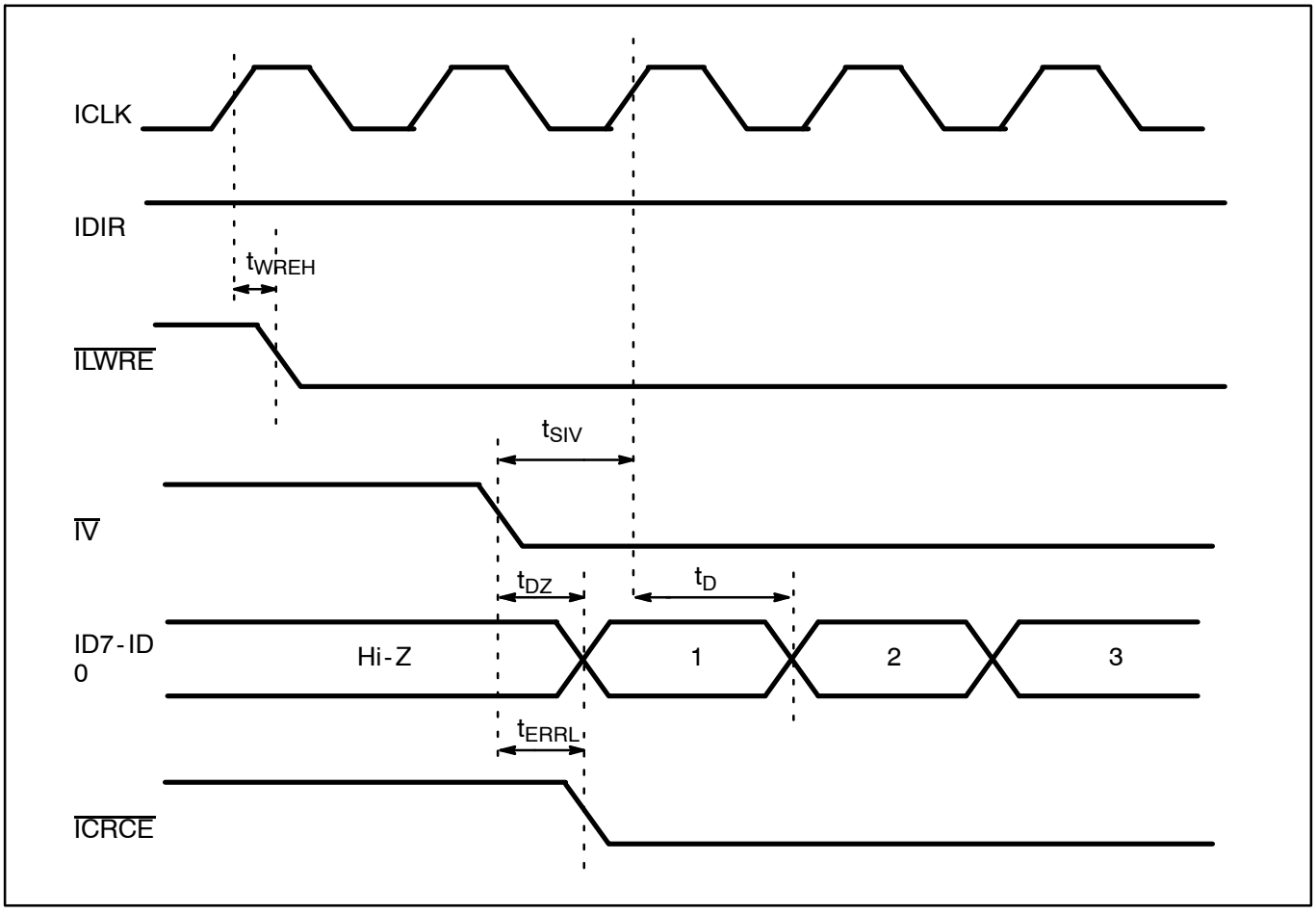


(2) Receive Timing

Rcv Activation

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
ICLK Rising → $\overline{\text{ILWRE}}$ Falling Time	t_{WREH}	-	-	-	40	ns
$\overline{\text{IV}}$ Setup Time	t_{SIV}	-	40	-	-	ns
Data Output Defined Time	t_{DZ}	-	-	-	40	ns
Data Output Disable Time	t_D	-	10	-	40	ns
$\overline{\text{IV}}$ Falling → $\overline{\text{ICRCE}}$ Falling Time *	t_{ERRL}	-	-	-	40	ns

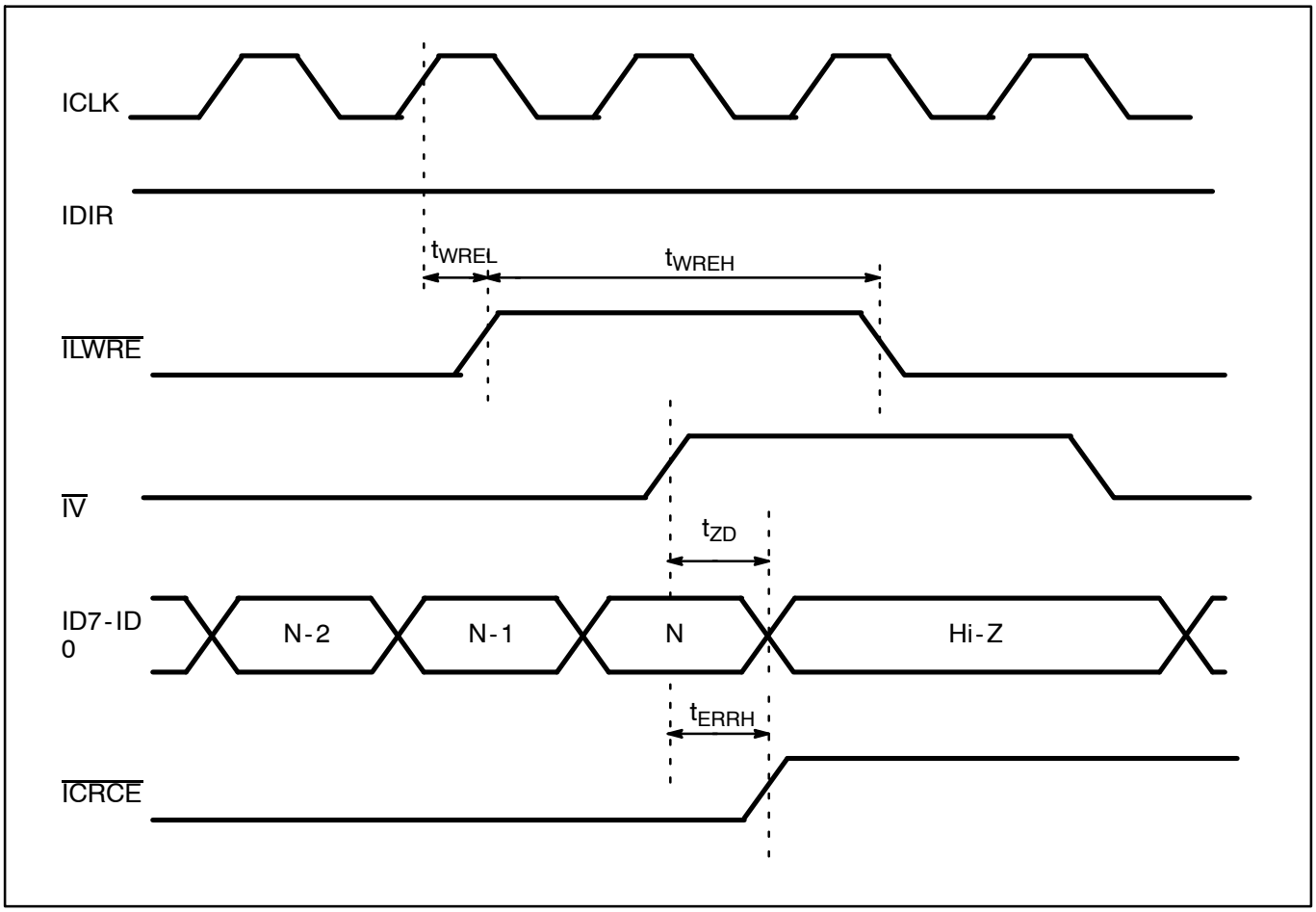
* : $\overline{\text{ICRCE}}$ signal is output only when there is an error on the received data.



Rcv Termination

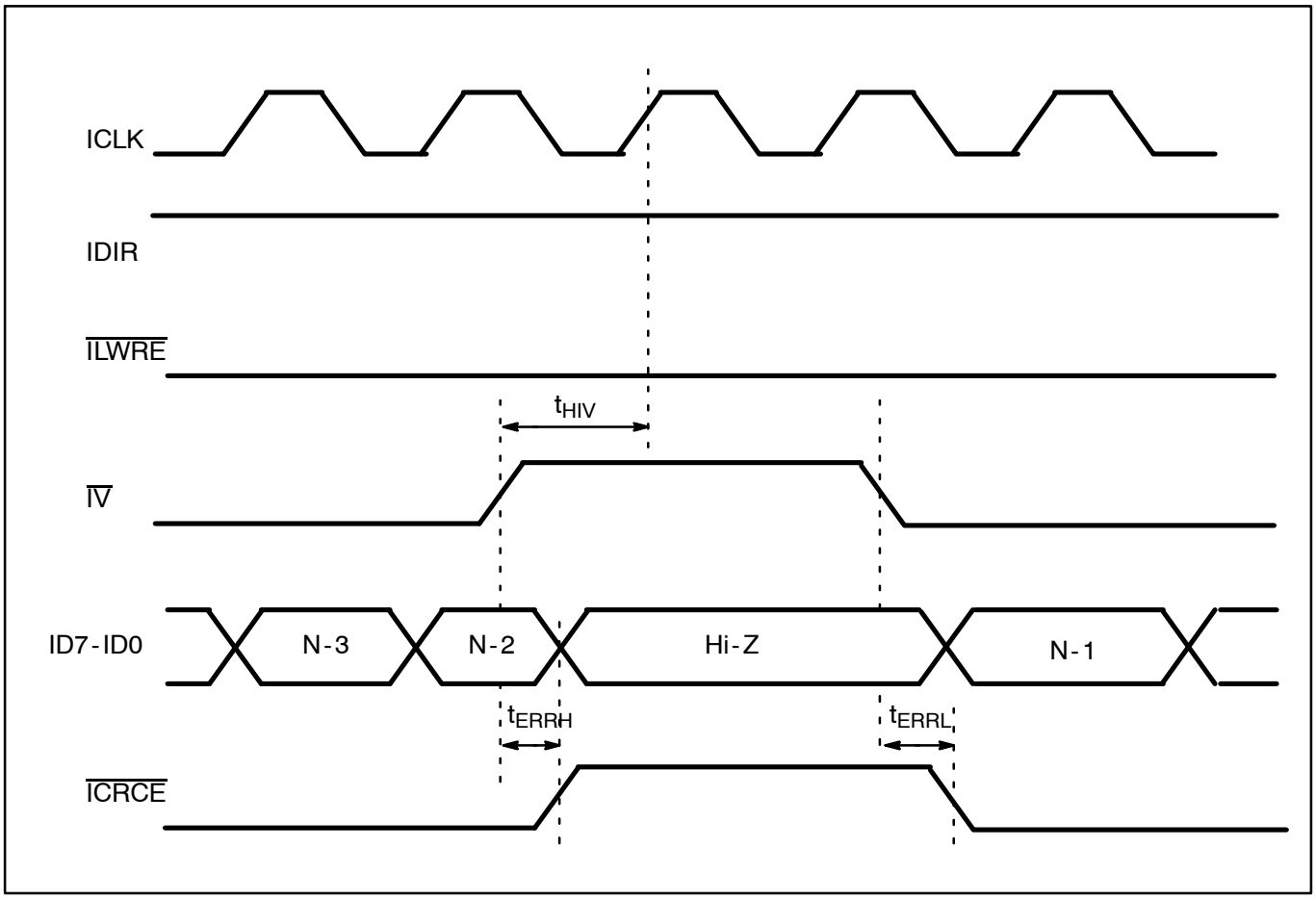
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
ICLK Rising → $\overline{\text{ILWRE}}$ Rising Time	t_{WREL}	-	-	-	40	ns
Data Output Disable Time	t_{ZD}	-	0	-	50	ns
$\overline{\text{ILWRE}}$ Negate Time *1	t_{WREH}	-	$6t_{ICLK}$	-	-	ns
$\overline{\text{IV}}$ Rising → $\overline{\text{ICRCE}}$ Rising Time *2	t_{ERRH}	-	-	-	40	ns

*1: MB86611A negates the $\overline{\text{ILWRE}}$ signal once every time 1 packet is read out.
*2 : $\overline{\text{ICRCE}}$ signal is output only when there is an error on the received data.



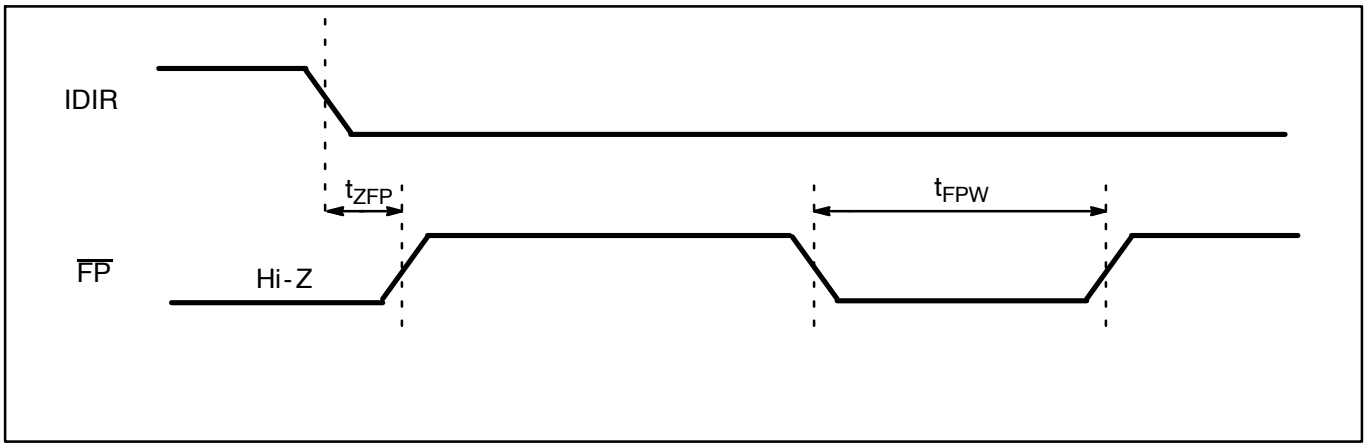
Receive to $\overline{IV}$ Temporary Negation

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
$\overline{IV}$ Rising → ICLK Rising Time	t_{HIV}	-	40	-	-	ns
$\overline{IV}$ Rising → $\overline{ICRCE}$ Rising Time	t_{ERRH}	-	-	-	40	ns
$\overline{IV}$ Falling → $\overline{ICRCE}$ Falling Time	t_{ERRL}	-	-	-	40	ns

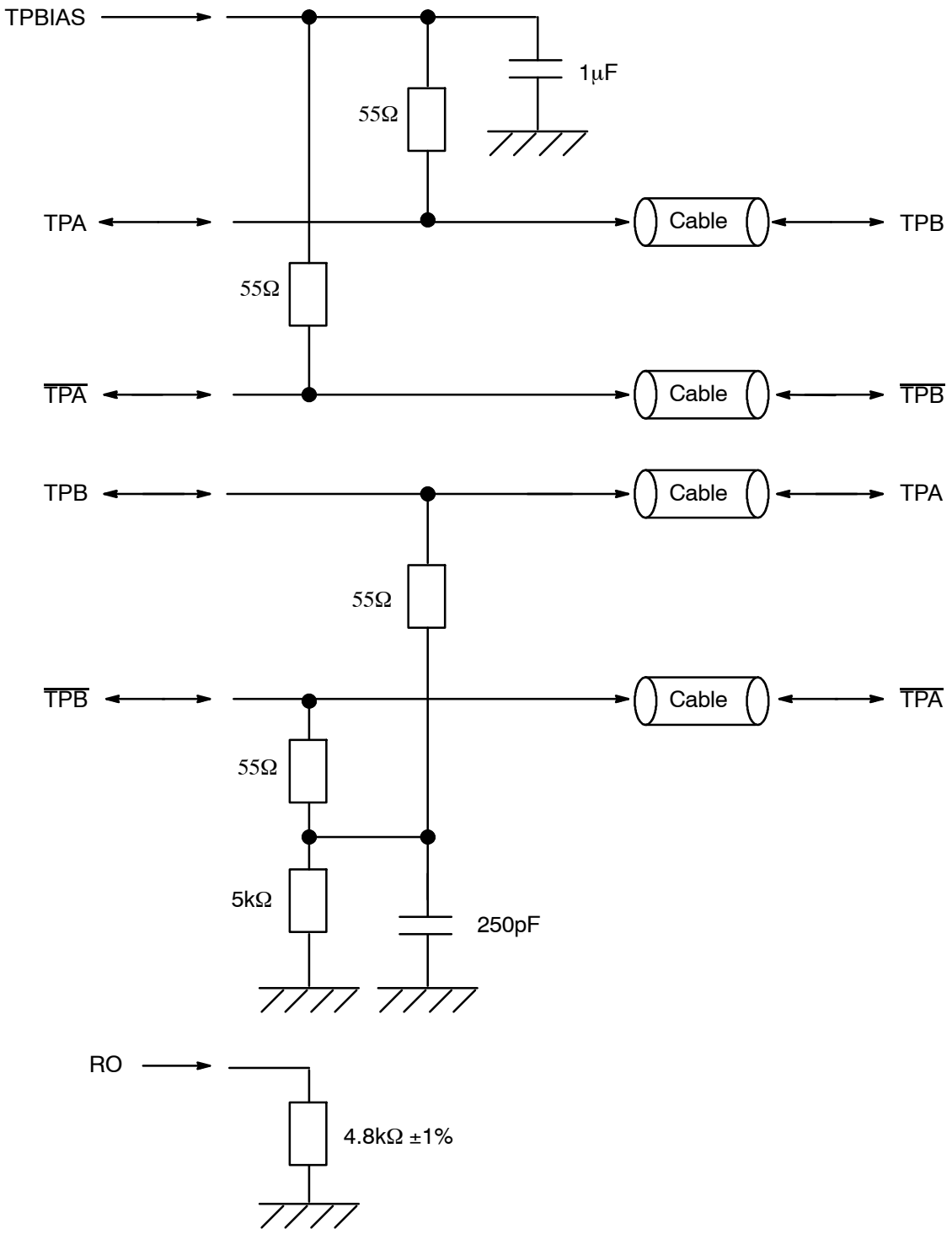


$\overline{FP}$ Signal Output Timing

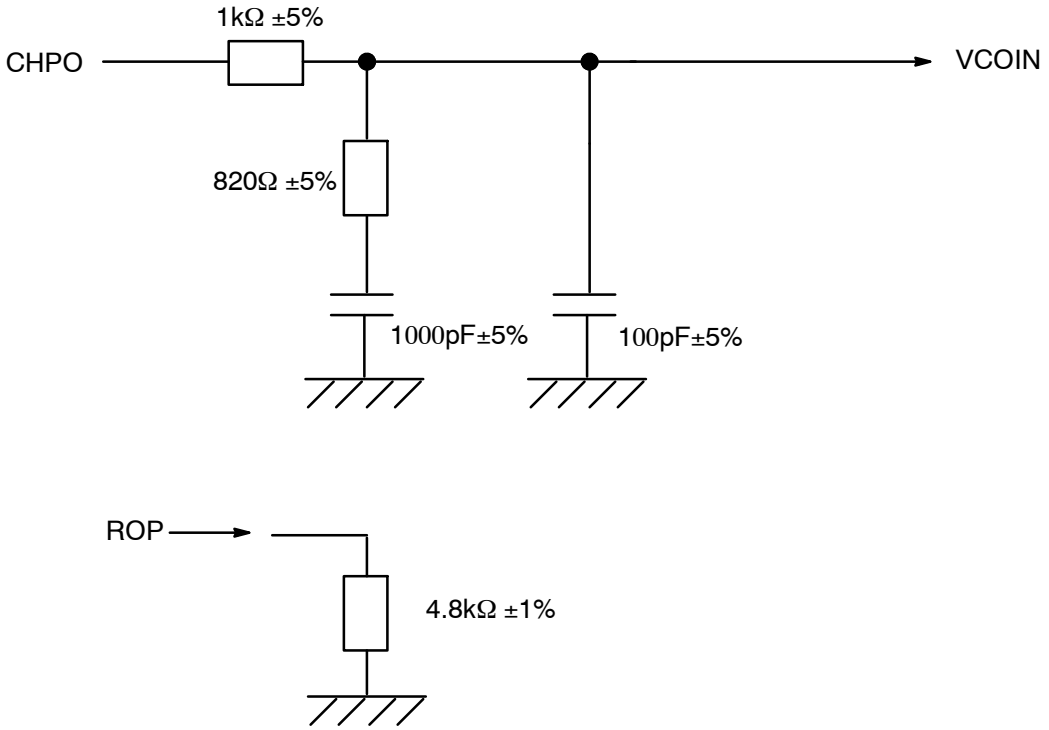
Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
IDIR Falling → $\overline{FP}$ Output Enable	t_{ZFP}	-	-	-	40	ns
$\overline{FP}$ "L" Level Pulse Width	t_{FPW}	-	600	-	730	ns
Timestamp Match → $\overline{FP}$ Output	t_{DTMP}	-	-	-	40	ns



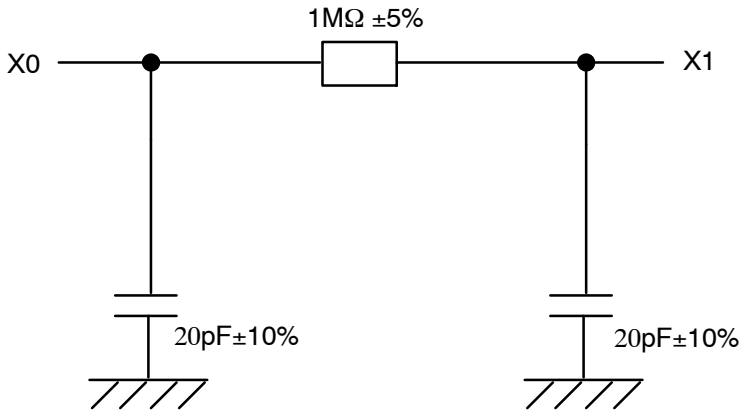
Recommended Connection Diagram for 1394 Port (Example)



Recommended Connection Diagram for On-chip PLL Loop Filter (Example)



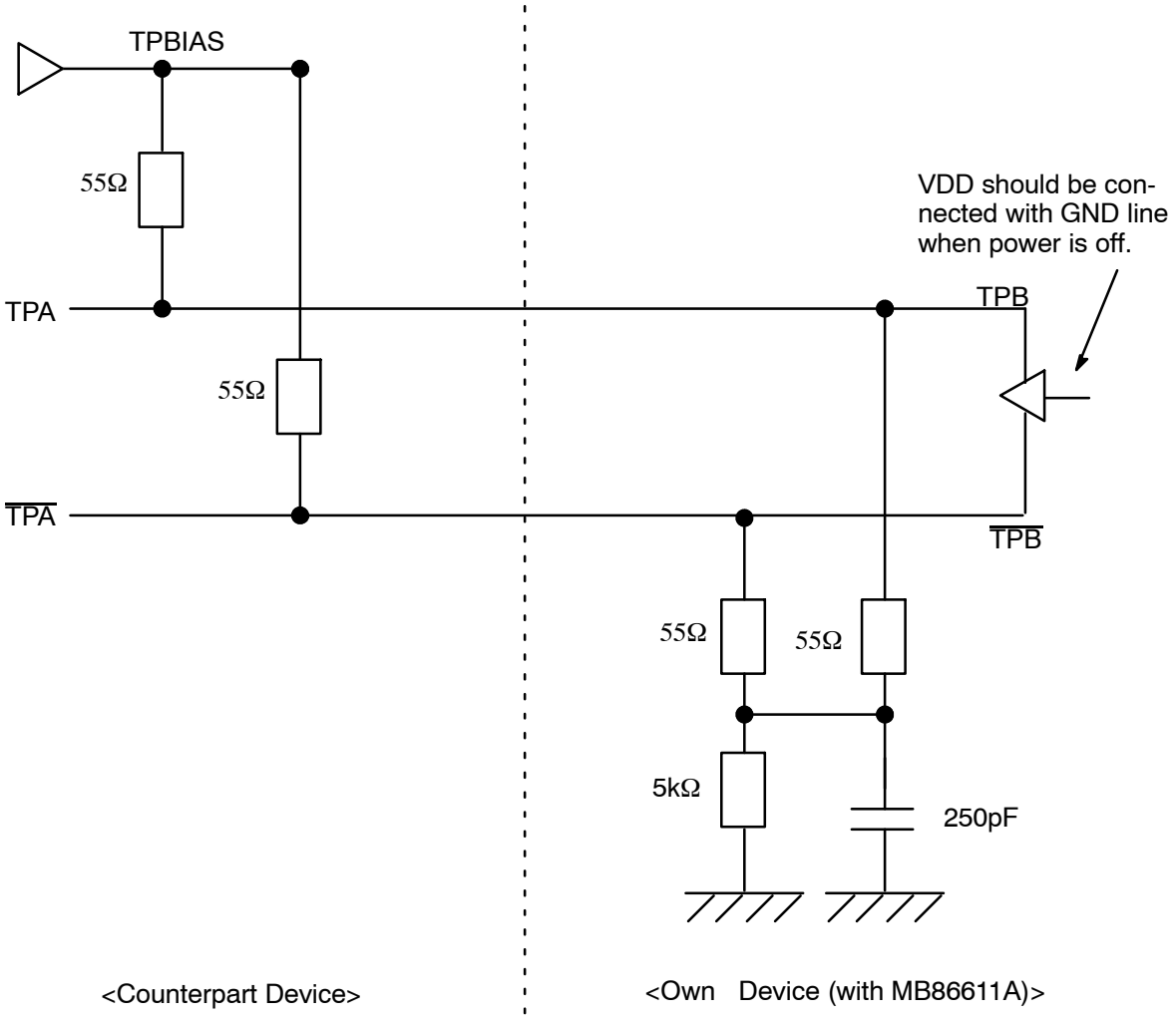
Recommended Connection Diagram for Crystal Oscillator (Example)



Notes on Use

Current Leak at the Power-Off

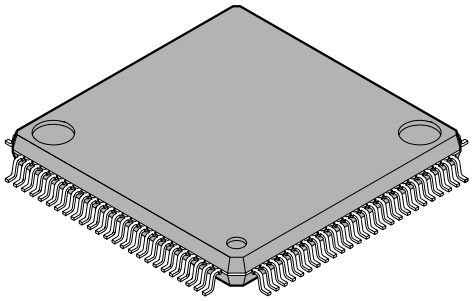
At the device powered-off, when the TP signal is biassed from the counterpart device via the 1394 cable, it is possible to flow overcurrent on the device via the TPB driver's current lines. Therefore, load components (14kΩ or greater is recommended) should be connected with the VDD lines.



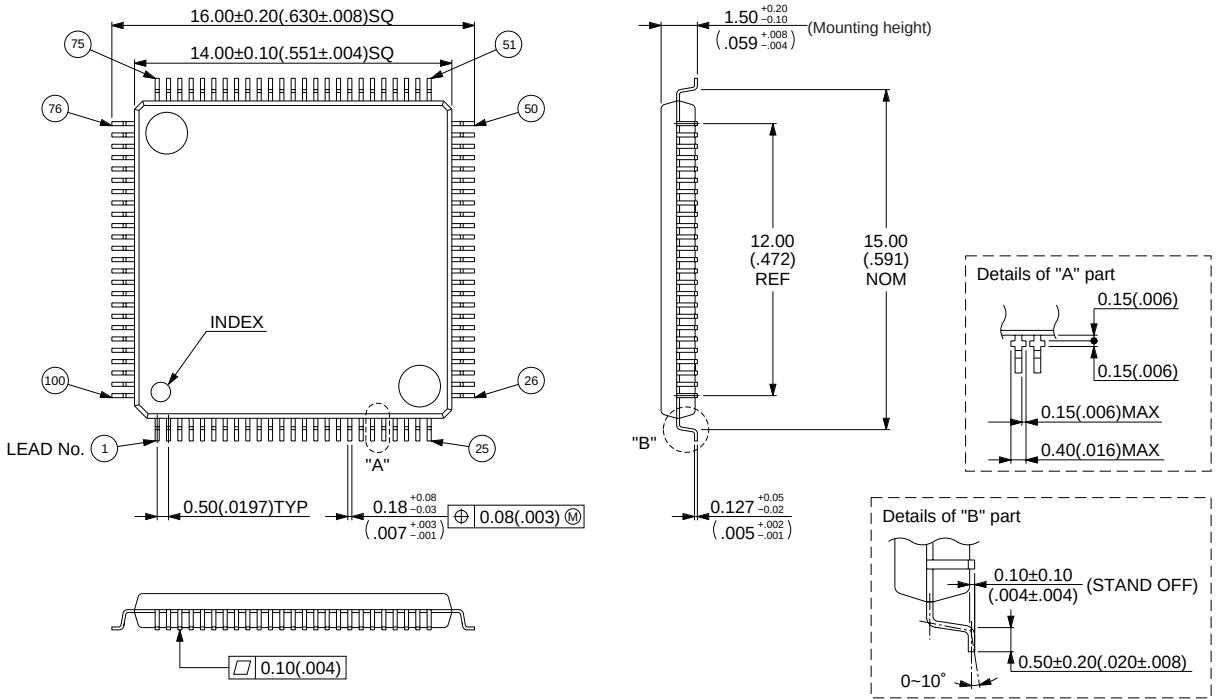
LOW PROFILE SHRINK QUAD FLAT L-LEADED PACKAGE
100 PIN PLASTIC

FPT-100P-M05

EIAJ code : ∗QFP100-P-1414-1

100-pin plastic LQFP  (FPT-100P-M05)	Lead pitch	0.50mm
	Package width × package length	14 × 14mm
	Lead shape	Gullwing
	Sealing method	Plastic mold

100-pin plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches).