FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11404-2E

MEMORY Mobile FCRAM™

CMOS

16 Mbit (1 M word × 16 bit)

Mobile Phone Application Specific Memory

MB82D01171A-80/80L/80LL/85/85L/85LL/90/90L/90LL

CMOS 1,048,576-WORD × 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface

■ DESCRIPTION

The Fujitsu MB82D01171A is a CMOS Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. This MB82D01171A is suited for low power applications such as Cellular Handset and PDA.

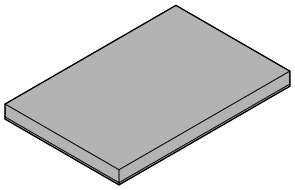
Note: FCRAM is a trademark of Fujitsu Limited, Japan.

■ PRODUCT LINEUP

Parameter	MB82D01171A								
	80	80L	80LL	85	85L	85LL	90	90L	90LL
Access Time (t_{AA} Max, t_{CE} Max)	80 ns			85 ns			90 ns		
Active Current (I_{DDA1} Max)	20 mA								
Standby Current (I_{DDS1} Max)	200 µA	100 µA	70 µA	200 µA	100 µA	70 µA	200 µA	100 µA	70 µA
Power Down Current (I_{DDP} Max)	10 µA								

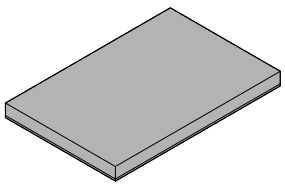
■ PACKAGES

48-ball plastic FBGA



(BGA-48P-M16)

48-ball plastic FBGA



(BGA-48P-M18)

FUJITSU

■ FEATURES

- Asynchronous SRAM Interface
- 1 M word × 16 bit Organization
- Fast Random Cycle Time : t_{RC} = 90 ns
- Fast Random Access Time : t_{AA} = t_{CE} = 80 ns, 85 ns, 90 ns
- Low Power Consumption : I_{DDS1} = 200 µA, 100 µA (L version) , 70 µA (LL version)
- Wide Operating Conditions : V_{DD} = +2.3 V to +2.7 V
  +2.7 V to +3.1 V
  +3.1 V to +3.5 V
  T_A = –30 °C to +85 °C
- Byte Write Control
- 4 words Address Access Capability
- Power Down Control by CE2

■ PIN ASSIGNMENTS

(TOP VIEW)

Flash Compatible FBGA
(suffix PBT)

	1	2	3	4	5	6
A	A4	A17	$\overline{UB}$	CE2	A8	A12
B	A3	A7	$\overline{LB}$	$\overline{WE}$	A9	A13
C	A2	A6	A18	NC	A10	A14
D	A1	A5	NC	A19	A11	A15
E	A0	DQ1	DQ3	DQ6	DQ8	A16
F	$\overline{CE}$1	DQ9	DQ11	DQ13	DQ15	NC
G	$\overline{OE}$	DQ10	DQ12	VDD	DQ14	DQ16
H	VSS	DQ2	DQ4	DQ5	DQ7	VSS

(BGA-48P-M16)

SRAM Compatible FBGA
(suffix PBN)

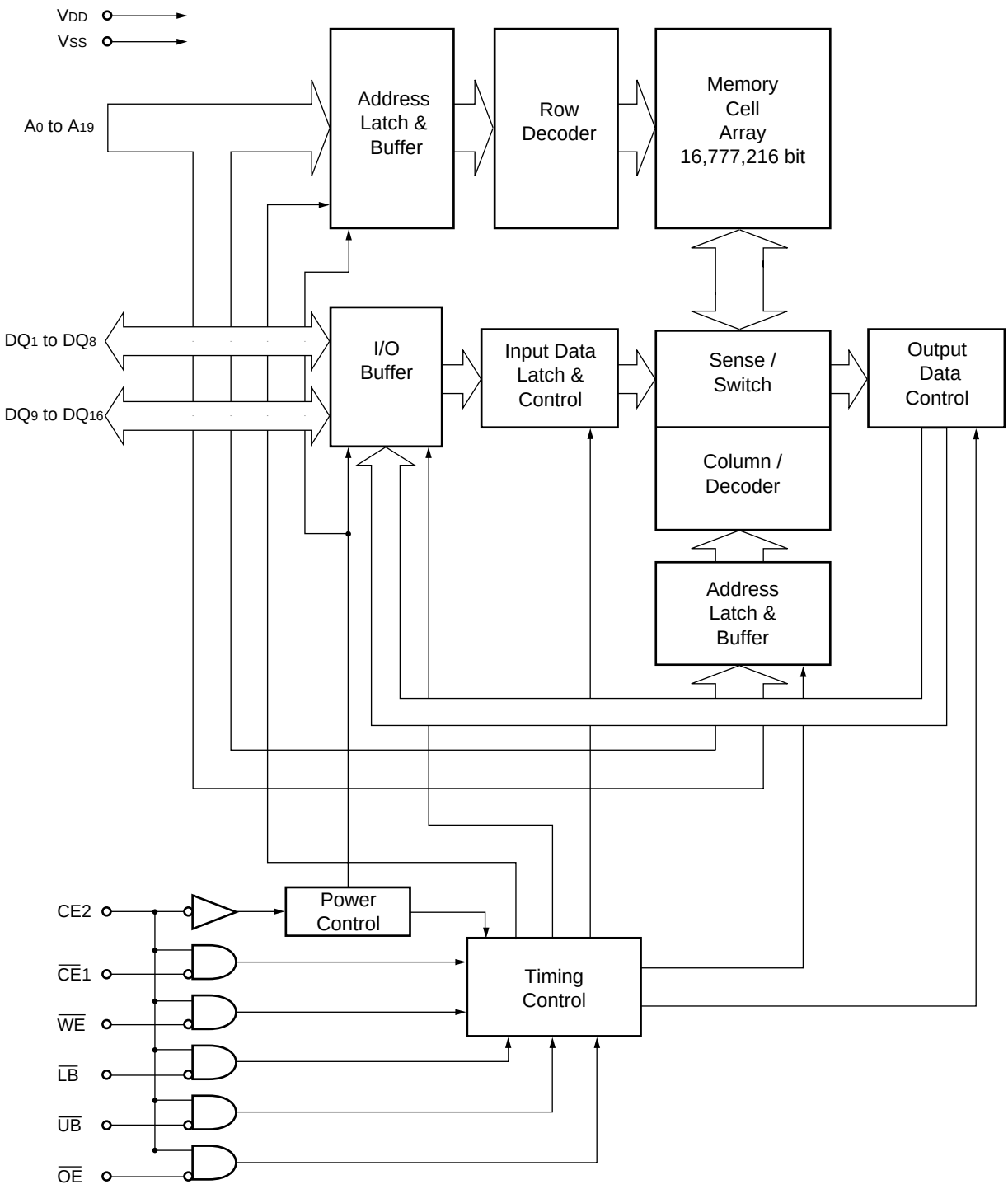
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	DQ9	$\overline{UB}$	A3	A4	$\overline{CE}$1	DQ1
C	DQ10	DQ11	A5	A6	DQ2	DQ3
D	VSS	DQ12	A17	A7	DQ4	VDD
E	VDD	DQ13	NC	A16	DQ5	VSS
F	DQ15	DQ14	A14	A15	DQ6	DQ7
G	DQ16	A19	A12	A13	$\overline{WE}$	DQ8
H	A18	A8	A9	A10	A11	NC

(BGA-48P-M18)

■ PIN DESCRIPTION

Pin Name	Description
A_0 to A_{19}	Address Input
$\overline{CE}$1	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Write Control (Low Active)
$\overline{UB}$	Upper Byte Write Control (Low Active)
DQ_1 to DQ_8	Lower Byte Data Input/Output
DQ_9 to DQ_{16}	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE *1

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ_1 to DQ_8	DQ_9 to DQ_{16}	I_{DD}	Data Retention
Power Down *2	X	L	X	X	X	X	High-Z	High-Z	I_{DDP}	No
Standby (Deselect)	H	H	X	X	X	X	High-Z	High-Z	I_{DDS}	Yes
Output Disable*3	L	H	H	H	X	X	High-Z	High-Z	I_{DDA}	Yes
Read*4	L	H	H	L	X	X	Output Valid	Output Valid	I_{DDA}	Yes
Write	L	H	L	H	L	L	Input Valid	Input Valid	I_{DDA}	Yes
Write (Lower Byte)	L	H	L	H	L	H	Input Valid	Invalid	I_{DDA}	Yes
Write (Upper Byte)	L	H	L	H	H	L	Invalid	Input Valid	I_{DDA}	Yes

*1 : V = Valid, L = Logic Low, H = Logic High, X = either “L” or “H”, High-Z = High Impedance

*2 : Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.

*3 : Output Disable mode should not be kept longer than 1 μs.

*4 : Byte control at Read mode is not supported.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	–0.5	+3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}	–0.5	+3.6	V
	V_{OUT}	–0.5	+3.6	V
Short Circuit Output Current	I_{OUT}	–50	+50	mA
Storage Temperature	T_{STG}	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Supply Voltage *1	V_{DD} (31)	3.1	3.5	V
	V_{DD} (27)	2.7	3.1	V
	V_{DD} (23)	2.3	2.7	V
	V_{SS}	0	0	V
High Level Input Voltage *1, *2	V_{IH} (31)	2.6	V_{DD} + 0.3 and ≤ 3.6	V
	V_{IH} (27)	2.2	V_{DD} + 0.3	V
	V_{IH} (23)	2.0	V_{DD} + 0.3	V
Low Level Input Voltage *1, *2	V_{IL} (31)	–0.3	0.5	V
	V_{IL} (27)	–0.3	0.5	V
	V_{IL} (23)	–0.3	0.4	V
Ambient Temperature	T_A	–30	85	°C

*1 : All voltages are referenced to V_{SS}.

*2 : Minimum DC voltage on input or I/O pins are –0.3 V. During voltage transitions, inputs may undershoot V_{SS} to –1.0 V for periods of up to 5 ns. Maximum DC voltage on input and I/O pins are V_{DD} + 0.3 V.
During voltage transitions, inputs may positive overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PIN CAPACITANCE

(f = 1.0 MHz, T_A = +25 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	C_{IO}	V_{IO} = 0 V	—	—	8	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter		Symbol	Conditions	Value		Unit
				Min	Max	
Input Leakage Current		I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	–1.0	+1.0	µA
Output Leakage Current		I_{LO}	0 V ≤ $V_{OUT} \le V_{DD}$, Output Disable	–1.0	+1.0	µA
Output High Voltage Level		$V_{OH(31)}$	$V_{DD} = V_{DD(31)}$, I_{OH} = –0.5 mA	2.4	—	V
		$V_{OH(27)}$	$V_{DD} = V_{DD(27)}$, I_{OH} = –0.5 mA	2.25	—	V
		$V_{OH(23)}$	$V_{DD} = V_{DD(23)}$, I_{OH} = –0.5 mA	1.8	—	V
Output Low Voltage Level		V_{OL}	I_{OL} = 1 mA	—	0.4	V
V_{DD} Power Down Current		I_{DDP}	$V_{DD} = V_{DD(31)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, CE2 ≤ 0.2 V	—	20	µA
			$V_{DD} = V_{DD(27, 23)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, CE2 ≤ 0.2 V	—	10	µA
V_{DD} Standby Current		I_{DDS}	$V_{DD} = V_{DD(31)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1$ = CE2 = V_{IH}, I_{OUT} = 0 mA	—	5.5	mA
	L Version			—	2.0	
	LL Version			—	1.5	
		I_{DDS}	$V_{DD} = V_{DD(27, 23)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1$ = CE2 = V_{IH}, I_{OUT} = 0 mA	—	5	mA
	L Version			—	1.5	
	LL Version			—	1	
		I_{DDS1}	$V_{DD} = V_{DD(31)}$ Max, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{DD} - 0.2$ V, $\overline{CE}1$ = CE2 ≥ V_{DD} – 0.2 V, I_{OUT} = 0 mA	—	250	µA
	L Version			—	150	
	LL Version			—	120	
		I_{DDS1}	$V_{DD} = V_{DD(27, 23)}$ Max, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{DD} - 0.2$ V, $\overline{CE}1$ = CE2 ≥ V_{DD} – 0.2 V, I_{OUT} = 0 mA	—	200	µA
	L Version			—	100	
	LL Version			—	70	

(Continued)

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Parameter	Symbol	Conditions		Value		Unit
				Min	Max	
V_{DD} Active Current	I_{DDA1}	$V_{DD(31)} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, I_{OUT} = 0 mA	t_{RC} / t_{WC} = Min	—	25	mA
		$V_{DD(27, 23)} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, I_{OUT} = 0 mA			20	
	I_{DDA2}	$V_{DD(31)} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, I_{OUT} = 0 mA	t_{RC} / t_{WC} = 1 µs	—	4.0	mA
		$V_{DD(27, 23)} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, I_{OUT} = 0 mA			3.0	

Notes:
- All voltages are referenced to Vss.
- DC Characteristics are measured after following POWER-UP timing.
- I_{OUT} depends on the output load conditions.

2. AC Characteristics

(1) Read Operation

Parameter	Symbol	-80/-80L/-80LL		-85/-85L/-85LL		-90/-90L/-90LL		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	90	—	90	—	90	—	ns	
Chip Enable Access Time	t_{CE}	—	80	—	85	—	90	ns	*1, *3
Output Enable Access Time	t_{OE}	—	45	—	45	—	45	ns	*1
Address Access Time	t_{AA}	—	80	—	85	—	90	ns	*1, *4
Output Data Hold Time	t_{OH}	5	—	5	—	5	—	ns	*1
$\overline{CE}1$ Low to Output Low-Z	t_{CLZ}	5	—	5	—	5	—	ns	*2
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	0	—	0	—	ns	*2
$\overline{CE}1$ High to Output High-Z	t_{CHZ}	—	30	—	30	—	30	ns	*2
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	25	—	25	—	25	ns	*2
Address Setup Time to $\overline{CE}1$ Low	t_{ASC}	–5	—	–5	—	–5	—	ns	*5
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	45	—	45	—	45	—	ns	*3, *6
	$t_{ASO[ABS]}$	10	—	10	—	10	—	ns	*7
Address Invalid Time	t_{AX}	—	5	—	5	—	5	ns	*4
$\overline{CE}1$ Low to Address Hold Time	t_{CLAH}	90	—	90	—	90	—	ns	*4
$\overline{OE}$ Low to Address Hold Time	t_{OLAH}	45	—	45	—	45	—	ns	*4, *8
$\overline{CE}1$ High to Address Hold Time	t_{CHAH}	–5	—	–5	—	–5	—	ns	
$\overline{OE}$ High to Address Hold Time	t_{OHAH}	–5	—	–5	—	–5	—	ns	
$\overline{CE}1$ Low to $\overline{OE}$ Low Delay Time	t_{CLOL}	45	1000	45	1000	45	1000	ns	*3, *6, *8, *9
$\overline{OE}$ Low to $\overline{CE}1$ High Delay Time	t_{OLCH}	45	—	45	—	45	—	ns	*8
$\overline{CE}1$ High Pulse Width	t_{CP}	20	—	20	—	20	—	ns	
$\overline{OE}$ High Pulse Width	t_{OP}	45	1000	45	1000	45	1000	ns	*6, *8, *9
	$t_{OP[ABS]}$	20	—	20	—	20	—	ns	*7

*1: The output load is 30 pF.

*2: The output load is 5 pF.

*3: The t_{CE} is applicable if $\overline{OE}$ is brought to Low before $\overline{CE}1$ goes Low and is also applicable if actual value of both or either t_{ASO} or t_{CLOL} is shorter than specified value.

*4: Applicable only to A_0 and A_1 when both $\overline{CE}1$ and $\overline{OE}$ are kept at Low for the address access.

*5: Applicable if $\overline{OE}$ is brought to Low before $\overline{CE}1$ goes Low.

*6: The t_{ASO}, t_{CLOL} (Min) and t_{OP} (Min) are reference values when the access time is determined by t_{OE}.
If actual value of each parameter is shorter than specified minimum value, t_{OE} become longer by the amount of subtraction actual value from specified minimum value.
For example, if actual t_{ASO}, t_{ASO} (actual) , is shorter than specified minimum value, t_{ASO} (Min) , during $\overline{OE}$ control access (i.e., $\overline{CE}1$ stays Low) , the t_{OE} become t_{OE} (Max) + t_{ASO} (Min) – t_{ASO} (actual) .

*7: The $t_{ASO[ABS]}$ and $t_{OP[ABS]}$ is the absolute minimum value during $\overline{OE}$ control access.

*8: If actual value of either t_{CLOL} or t_{OP} is shorter than specified minimum value, both t_{OLAH} and t_{OLCH} become t_{RC} (Min) – t_{CLOL} (actual) or t_{RC} (Min) – t_{OP} (actual) .

*9: Maximum value is applicable if $\overline{CE}1$ is kept at Low.

(2) Write Operation

Parameter	Symbol	-80/-80L/-80LL		-85/-85L/-85LL		-90/-90L/-90LL		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	90	—	90	—	90	—	ns	*1
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	*2
Address Hold Time	t_{AH}	45	—	45	—	45	—	ns	*2
$\overline{CE}1$ Write Setup Time	t_{CS}	0	1000	0	1000	0	1000	ns	
$\overline{CE}1$ Write Hold Time	t_{CH}	0	1000	0	1000	0	1000	ns	
$\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ Hold Time	t_{WH}	0	—	0	—	0	—	ns	
$\overline{LB}$ and $\overline{UB}$ Setup Time	t_{BS}	–5	—	–5	—	–5	—	ns	
$\overline{LB}$ and $\overline{UB}$ Hold Time	t_{BH}	–5	—	–5	—	–5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	0	1000	0	1000	0	1000	ns	*3
$\overline{OE}$ Hold Time	t_{OEH}	45	1000	45	1000	45	1000	ns	*3, *4
	$t_{OEH[ABS]}$	20	—	20	—	20	—	ns	*5
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time	t_{OHCL}	–3	—	–3	—	–3	—	ns	*6
Address Hold Time to $\overline{OE}$ High	t_{OHAH}	0	—	0	—	0	—	ns	*7
$\overline{CE}1$ Write Pulse Width	t_{CW}	60	—	60	—	60	—	ns	*1, *8
$\overline{WE}$ Write Pulse Width	t_{WP}	60	—	60	—	60	—	ns	*1, *8
$\overline{CE}1$ Write Recovery Time	t_{WRC}	15	—	15	—	15	—	ns	*1, *9
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	15	1000	15	1000	ns	*1, *3, *9
Data Setup Time	t_{DS}	20	—	20	—	20	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
$\overline{CE}1$ High Pulse Width	t_{CP}	20	—	20	—	20	—	ns	*9

*1: Minimum value must be equal or greater than the sum of actual t_{CW} (or t_{WP}) and t_{WRC} (or t_{WR}) .

*2: New write address is valid from either $\overline{CE}1$ or $\overline{WE}$ is brought to High.

*3: Maximum value is applicable if $\overline{CE}1$ is kept at Low and both $\overline{WE}$ and $\overline{OE}$ are kept at High.

*4: The t_{OEH} is specified from end of t_{WC} (Min) and is a reference value when access time is determined by t_{OE}.
If actual value is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value.

*5: The $t_{OEH[ABS]}$ is the absolute minimum value if write cycle is terminated by $\overline{WE}$ and $\overline{CE}1$ stays Low.

*6: t_{OHCL} (Min) must be satisfied if read operation is not performed prior to write operation.
In case $\overline{OE}$ is disabled after t_{OHCL} (Min) , $\overline{WE}$ Low must be asserted after t_{RC} (Min) from $\overline{CE}1$ Low.
In other words, read operation is initiated if t_{OHCL} (Min) is not satisfied.

*7: Applicable if $\overline{CE}1$ stays Low after read operation.

*8: t_{CW} and t_{WP} is applicable if write operation is initiated by $\overline{CE}1$ and $\overline{WE}$, respectively.

*9: t_{WRC} and t_{WR} is applicable if write operation is terminated by $\overline{CE}1$ and $\overline{WE}$, respectively.
The t_{WR} (Min) can be ignored if $\overline{CE}1$ is brought to High together or after $\overline{WE}$ is brought to High.
In such case, the t_{CP} (Min) must be satisfied.

(3) Power Down Parameters

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	100	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit	t_{CHH}	350	—	µs	
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	10	—	ns	

(4) Other Timing Parameters

Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	20	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	20	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	*2
CE2 High Hold Time after Power-up	t_{C2HL}	50	—	µs	*3
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	350	—	µs	*2
Input Transition Time	t_T	1	25	ns	*4

*1: It may write some data into any address location if t_{CHWX} is not satisfied.

*2: Must satisfy t_{CHH} (Min) after t_{C2LH} (Min) .

*3: Requires Power Down mode entry and exit after t_{C2HL}.

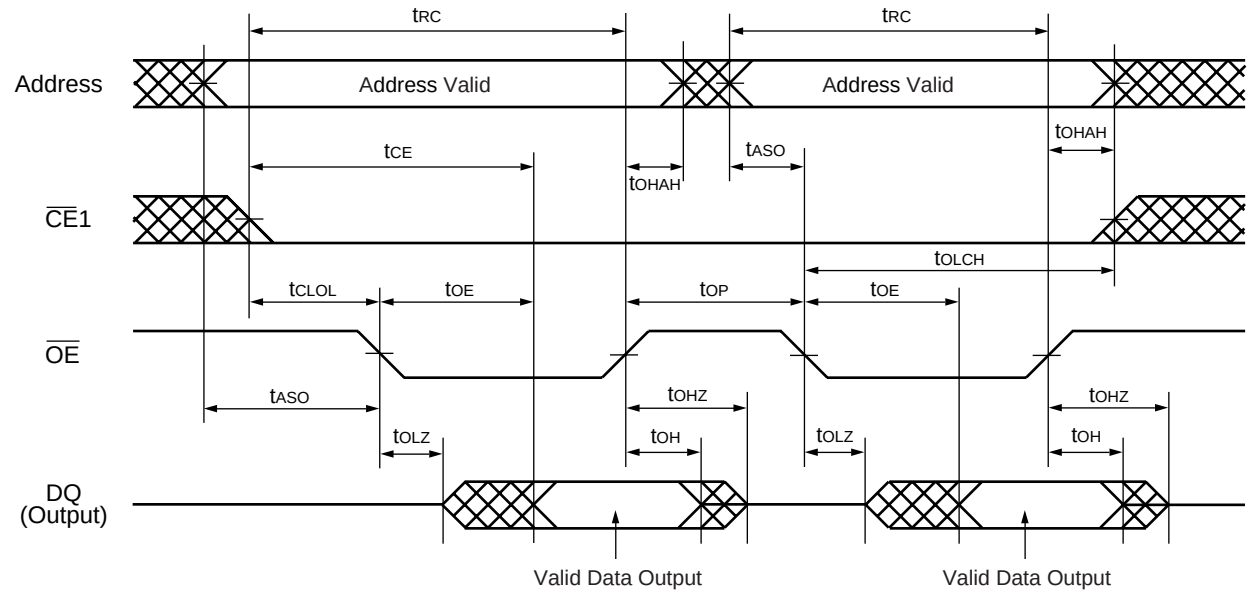
*4: The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate some timing parameters of AC specification.

(5) AC Test Conditions

Parameter	Symbol	Conditions	Measured Value	Unit	Note
Input High Level	V_{IH}	V_{DD} = 3.1 V to 3.5 V	2.6	V	
		V_{DD} = 2.7 V to 3.1 V	2.3	V	
		V_{DD} = 2.3 V to 2.7 V	2.0	V	
Input Low Level	V_{IL}	V_{DD} = 3.1 V to 3.5 V	0.5	V	
		V_{DD} = 2.7 V to 3.1 V	0.5	V	
		V_{DD} = 2.3 V to 2.7 V	0.4	V	
Input Timing Measurement Level	V_{REF}	V_{DD} = 3.1 V to 3.5 V	1.5	V	
		V_{DD} = 2.7 V to 3.1 V	1.3	V	
		V_{DD} = 2.3 V to 2.7 V	1.1	V	
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns	

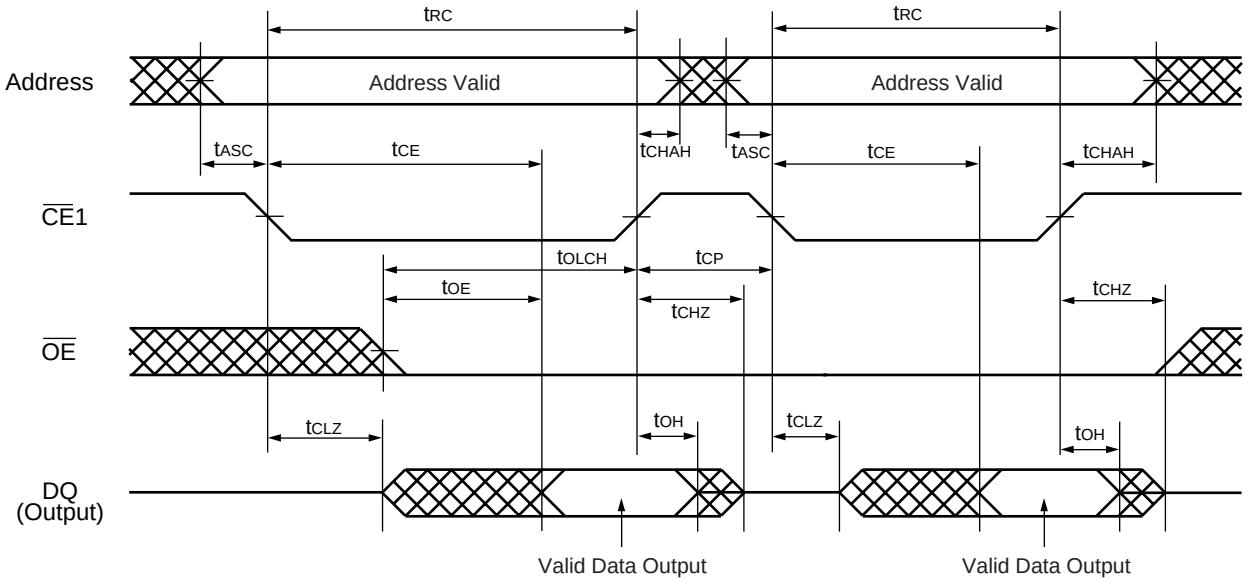
■ TIMING DIAGRAM

1. READ Timing #1 ($\overline{OE}$ Control Access)



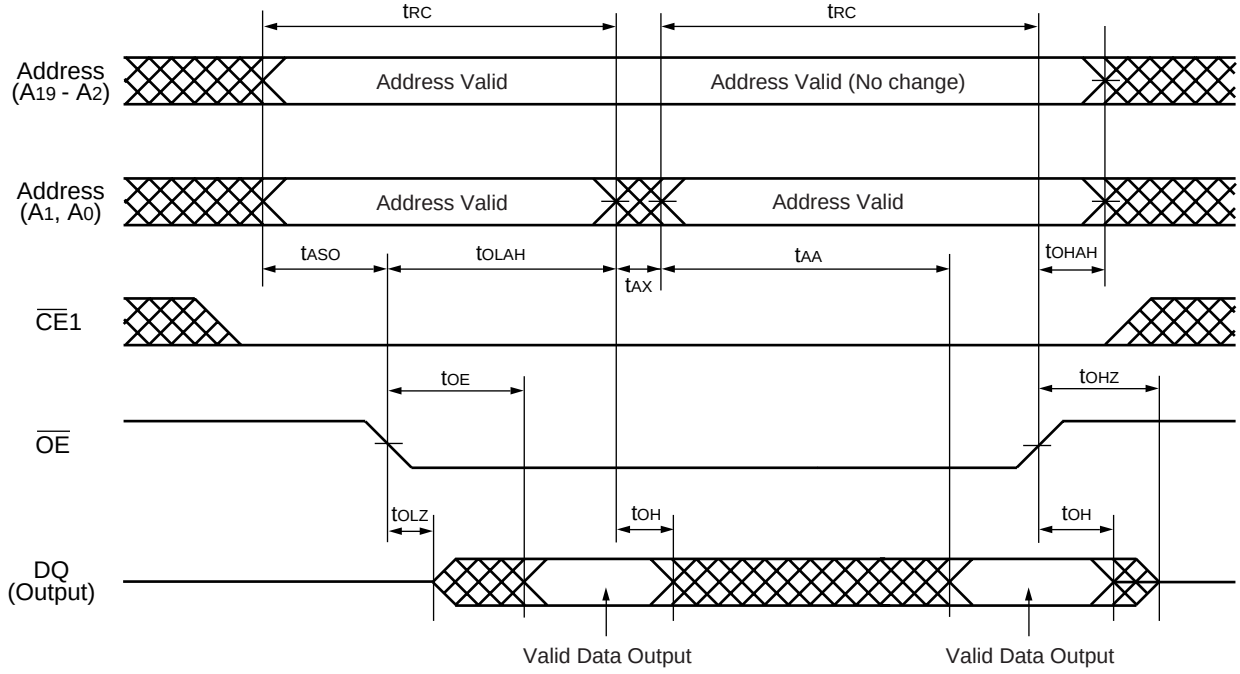
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

2. READ Timing #2 ($\overline{CE}$1 Control Access)



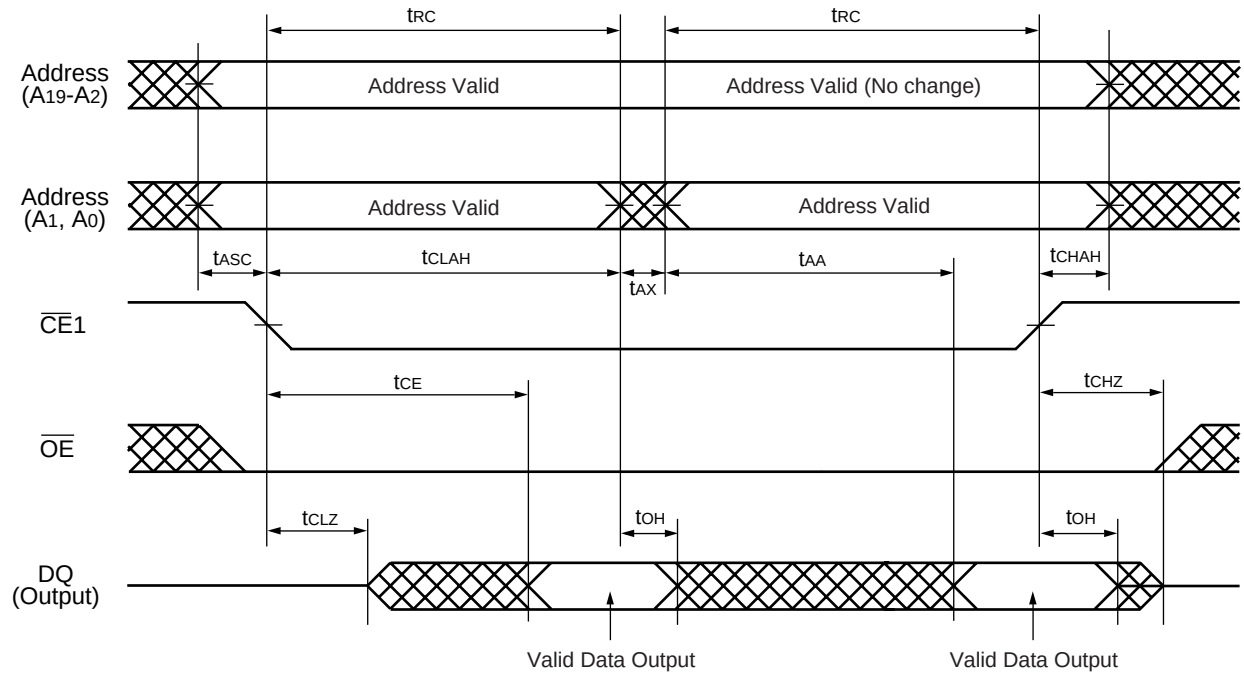
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

3. READ Timing #3 (Address Access after $\overline{OE}$ Control Access)



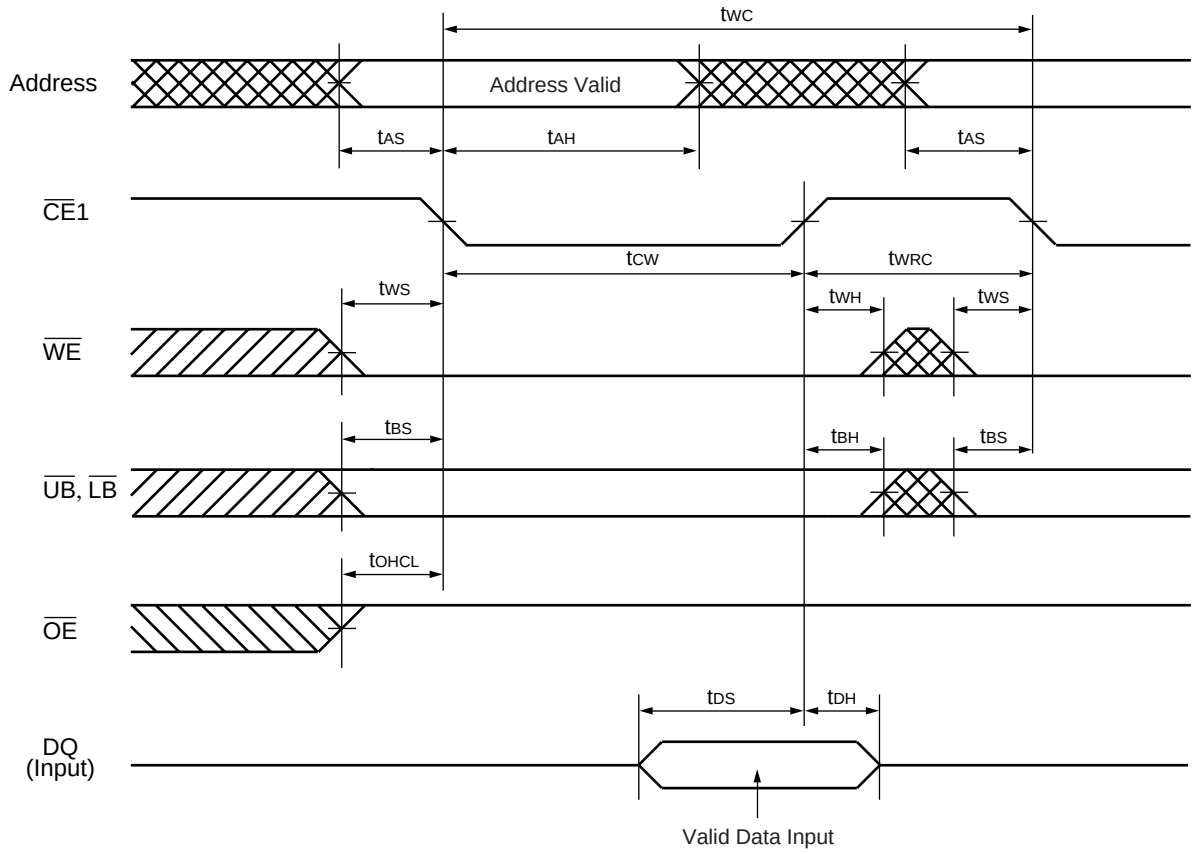
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

4. READ Timing #4 (Address Access after $\overline{CE}$1 Control Access)



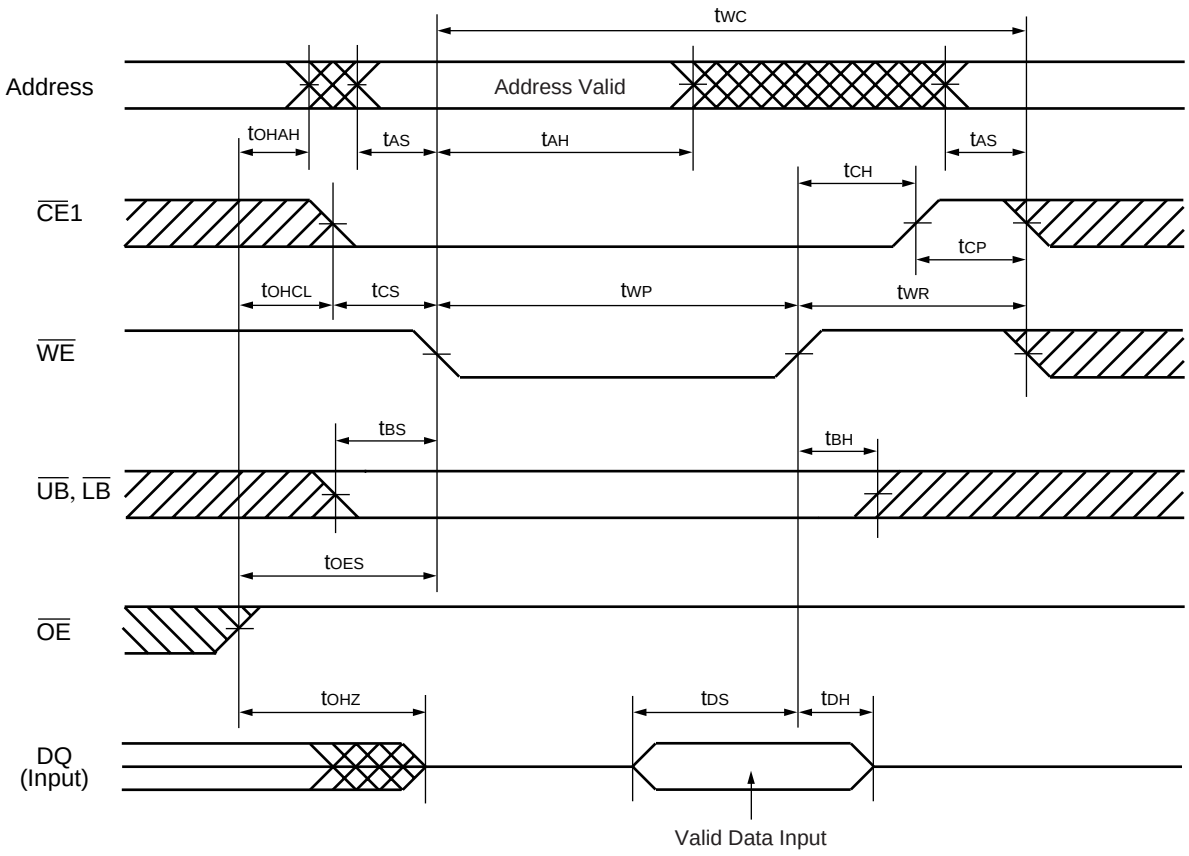
Note : CE2 and $\overline{WE}$ must be High for entire read cycle.

5. WRITE Timing #1 ($\overline{CE}$1 Control)



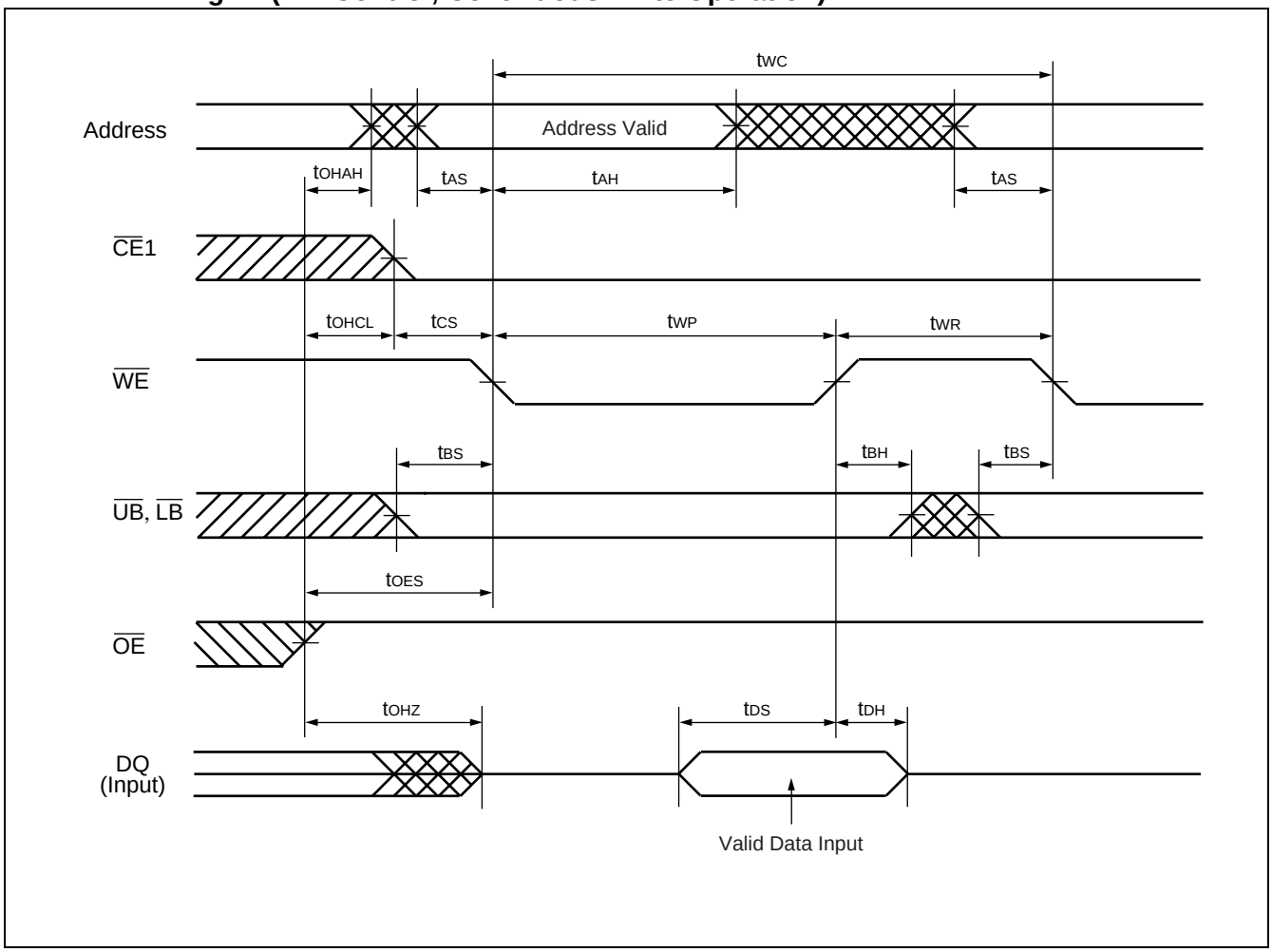
Note : CE2 must be High for write cycle.

6. WRITE Timing #2-1 ($\overline{WE}$ Control, Single Write Operation)

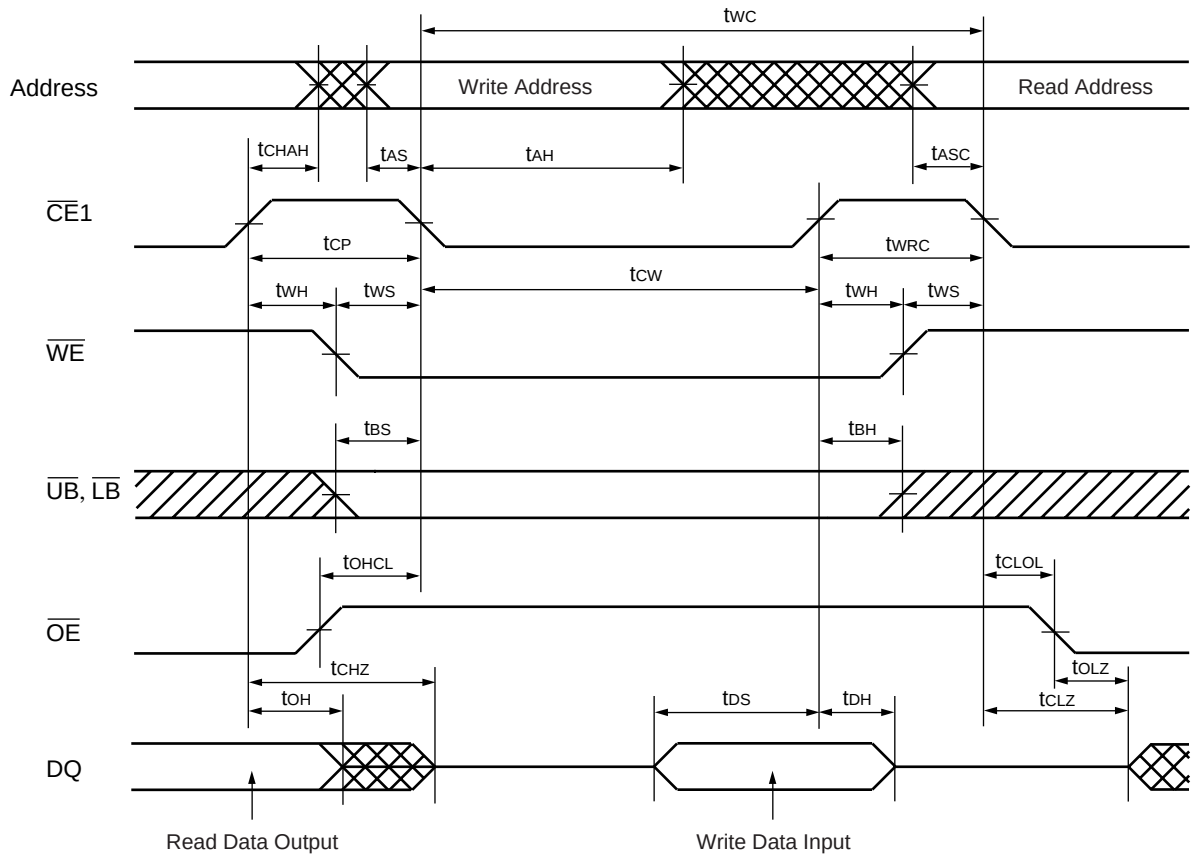


Note : CE2 must be High for write cycle.

7. WRITE Timing #2 ($\overline{WE}$ Control, Continuous Write Operation)

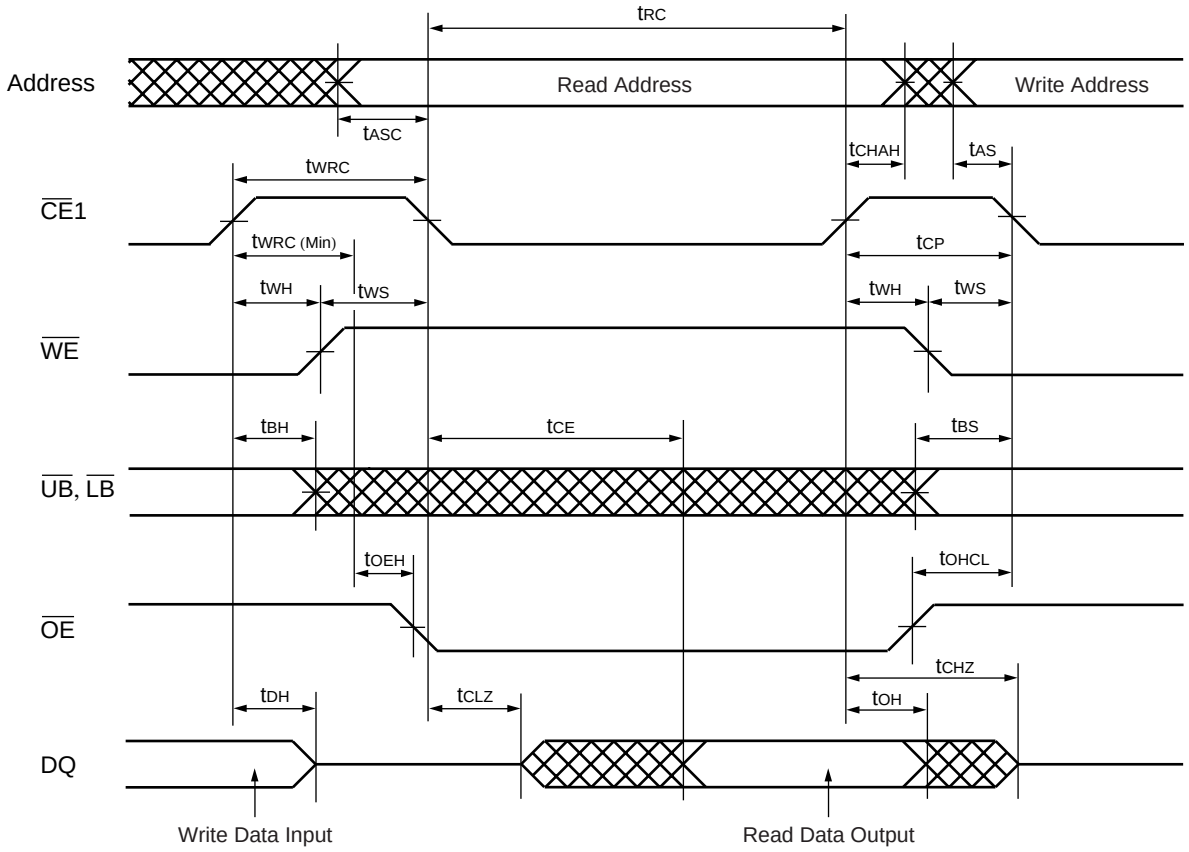


8. READ/WRITE Timing #1-1 ($\overline{CE}$1 Control)



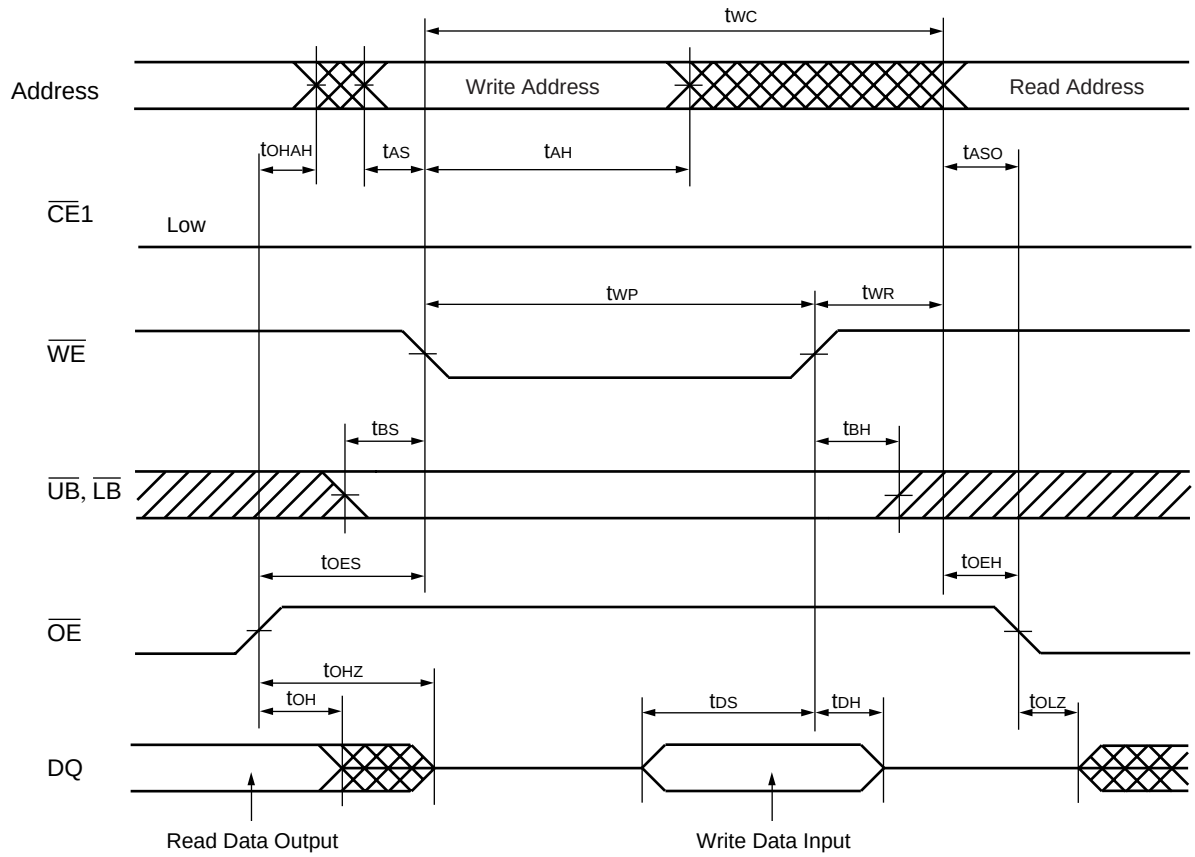
Note : Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

9. READ/WRITE Timing #1-2 ($\overline{CE}$1 Control)



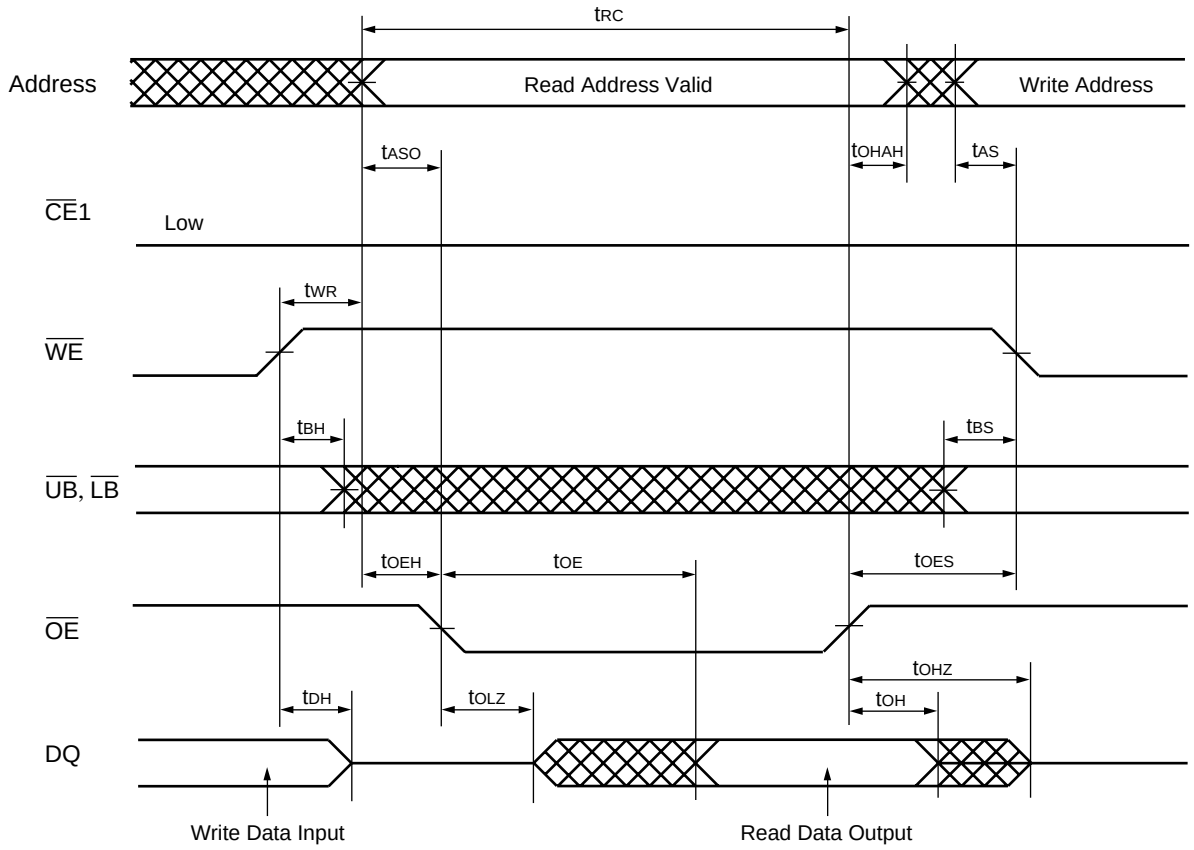
Note : The t_{OEH} is specified from the time satisfied both t_{WRC} and t_{WR} (Min) .

10. READ ($\overline{OE}$ Control) /WRITE ($\overline{WE}$ Control) Timing #2-1



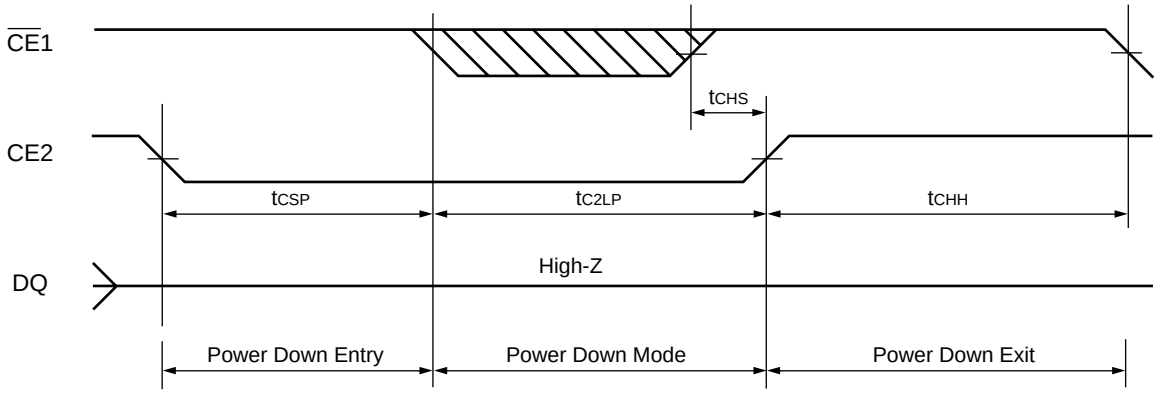
Note : $\overline{CE}1$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}1$ is tied to Low, output is exclusively controlled by $\overline{OE}$.

11. READ ($\overline{OE}$ Control) /WRITE ($\overline{WE}$ Control) Timing #2-2

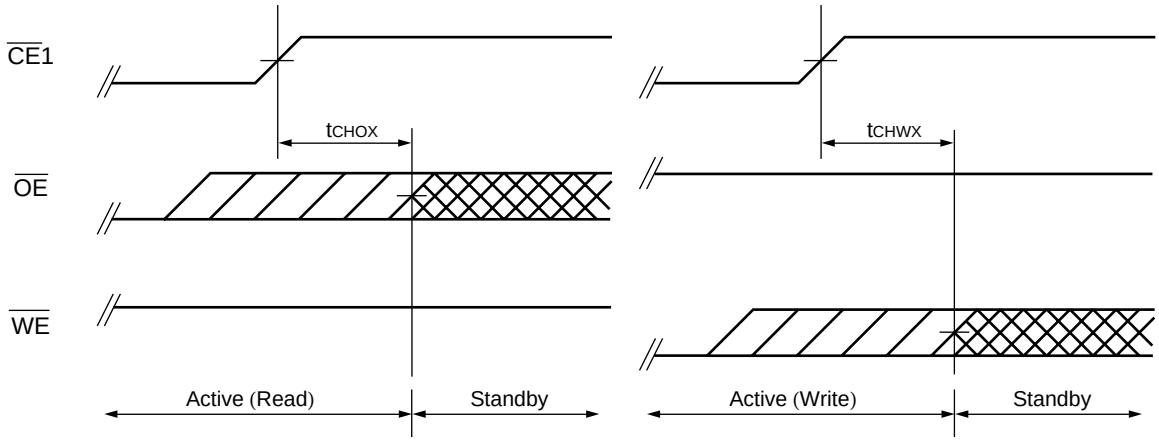


Note : $\overline{CE}1$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}1$ is tied to Low, output is exclusively controlled by $\overline{OE}$.

12. POWER DOWN Timing

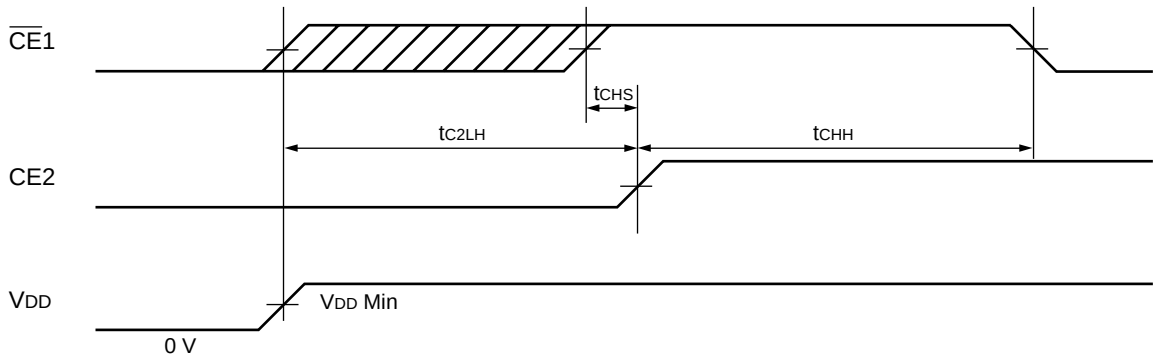


13. Standby Entry Timing after Read or Write



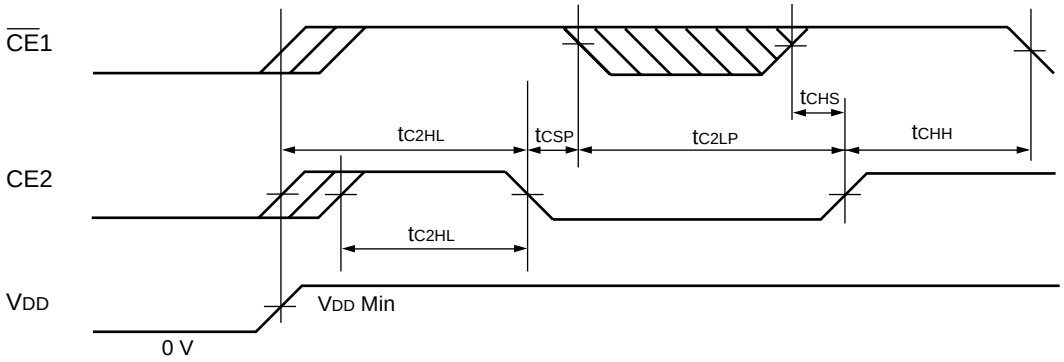
Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (Min) period from either last address transition of A_0 and A_1, or $\overline{CE}1$ Low to High transition.

14. POWER-UP Timing 1



Note : It is recommended to keep CE2 at Low during V_{DD} power-up.
The t_{C2LH} specifies after V_{DD} reaches specified minimum level.

15. POWER-UP Timing 2



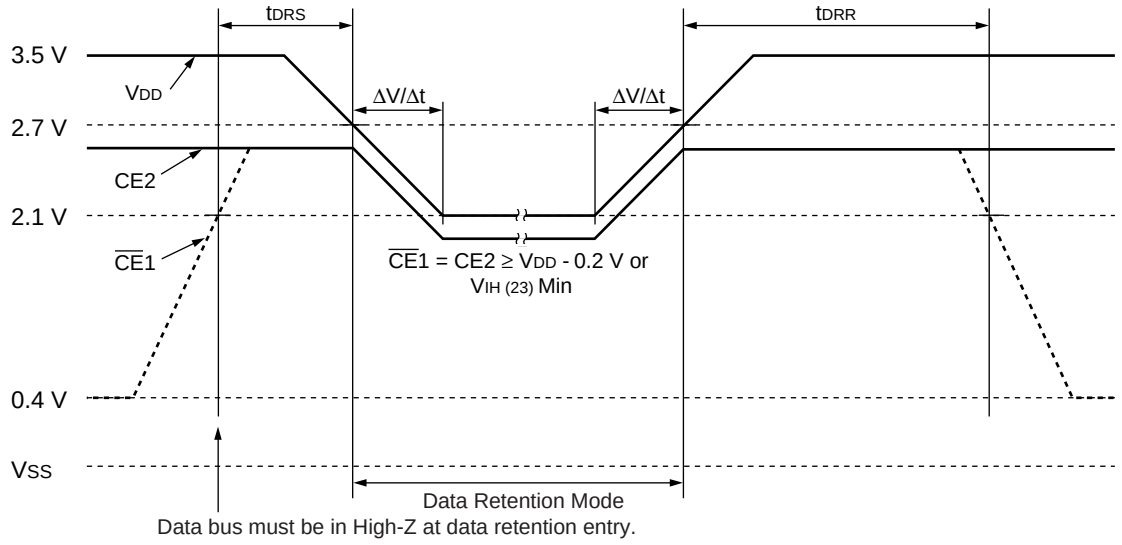
Note : The t_{C2HL} specifies from CE2 Low to High transition after V_{DD} reaches specified minimum level.
$\overline{CE1}$ must be brought to High prior to or together with CE2 Low to High transition.

■ DATA RETENTION

1. Low V_{DD} Characteristics

Parameter		Symbol	Test Conditions	Value		Unit
				Min	Max	
V_{DD} Data Retention Supply Voltage		V_{DR}	$\overline{CE}1 = CE2 \geq V_{DD} - 0.2$ V or, $\overline{CE}1 = CE2 = V_{IH}$,	2.1	3.5	V
V_{DD} Data Retention Supply Current		I_{DR}	$V_{DD} = V_{DD}$ (23) , $V_{IN} = V_{IH}$ (23) or V_{IL} $\overline{CE}1 = CE2 = V_{IH}$ (23) , I_{OUT} = 0 mA	—	5	mA
	L Version			—	1.5	
	LL Version			—	1	
		I_{DR1}	$V_{DD} = V_{DD}$ (23) , $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{DD} - 0.2$ V, $\overline{CE}1 = CE2 \geq V_{DD} - 0.2$ V, I_{OUT} = 0 mA	—	200	µA
	L Version			—	100	
	LL Version			—	70	
Data Retention Setup Time		t_{DRS}	$V_{DD} = V_{DD}$ (27) at data retention entry	0	—	ns
Data Retention Recovery Time		t_{DRR}	$V_{DD} = V_{DD}$ (27) after data retention	90	—	ns
V_{DD} Voltage Transition Time		ΔV/Δt	—	0.5	—	V/µs

2. Data Retention Timing

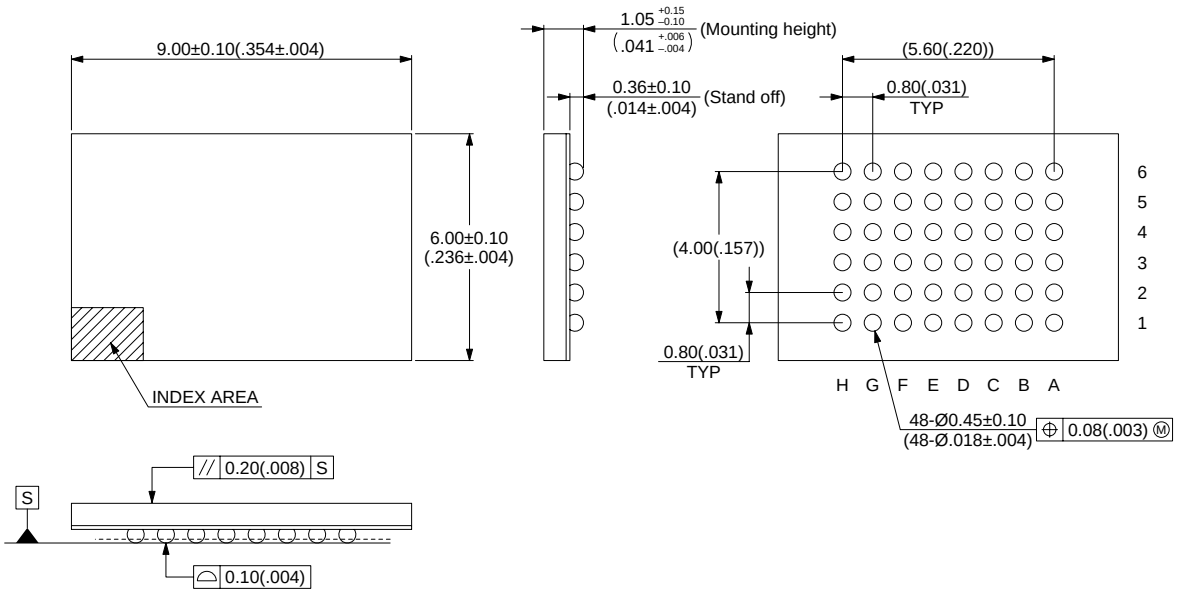


■ ORDERING INFORMATION

Part Number	Package	Remarks
MB82D01171A-80PBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 80 ns Max, I_{DDS1} = 200 µA Max Flash Compatible Package
MB82D01171A-80LPBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 80 ns Max, I_{DDS1} = 100 µA Max Flash Compatible Package
MB82D01171A-80LLPBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 80 ns Max, I_{DDS1} = 70 µA Max Flash Compatible Package
MB82D01171A-85PBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 85 ns Max, I_{DDS1} = 200 µA Max Flash Compatible Package
MB82D01171A-85LPBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 85 ns Max, I_{DDS1} = 100 µA Max Flash Compatible Package
MB82D01171A-85LLPBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 85 ns Max, I_{DDS1} = 70 µA Max Flash Compatible Package
MB82D01171A-90PBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 90 ns Max, I_{DDS1} = 200 µA Max Flash Compatible Package
MB82D01171A-90LPBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 90 ns Max, I_{DDS1} = 100 µA Max Flash Compatible Package
MB82D01171A-90LLPBT	48-ball plastic FBGA 0.8 mm pitch (BGA-48P-M16)	t_{CE} = 90 ns Max, I_{DDS1} = 70 µA Max Flash Compatible Package
MB82D01171A-80PBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 80 ns Max, I_{DDS1} = 200 µA Max SRAM Compatible Package
MB82D01171A-80LPBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 80 ns Max, I_{DDS1} = 100 µA Max SRAM Compatible Package
MB82D01171A-80LLPBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 80 ns Max, I_{DDS1} = 70 µA Max SRAM Compatible Package
MB82D01171A-85PBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 85 ns Max, I_{DDS1} = 200 µA Max SRAM Compatible Package
MB82D01171A-85LPBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 85 ns Max, I_{DDS1} = 100 µA Max SRAM Compatible Package
MB82D01171A-85LLPBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 85 ns Max, I_{DDS1} = 70 µA Max SRAM Compatible Package
MB82D01171A-90PBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 90 ns Max, I_{DDS1} = 200 µA Max SRAM Compatible Package
MB82D01171A-90LPBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 90 ns Max, I_{DDS1} = 100 µA Max SRAM Compatible Package
MB82D01171A-90LLPBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 90 ns Max, I_{DDS1} = 70 µA Max SRAM Compatible Package

■ PACKAGE DIMENSIONS

48-ball plastic FBGA
(BGA-48P-M16)

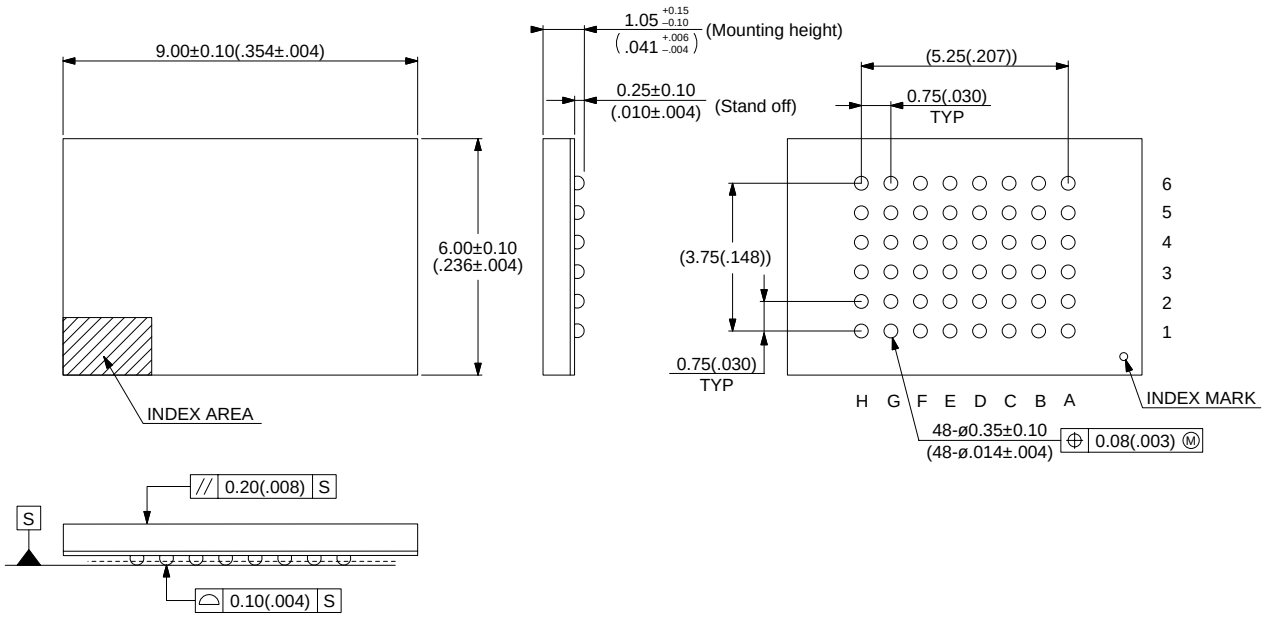


Dimensions in mm (inches)

(Continued)

(Continued)

48-ball plastic FBGA
(BGA-48P-M18)



Dimensions in mm (inches)

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