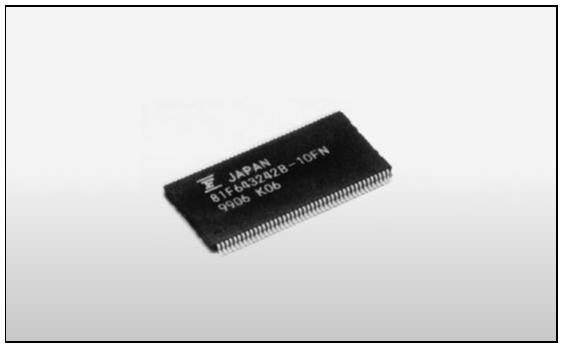
2M x 32-Bit Synchronous DRAM for Multimedia&Graphics: MB81F643242B MB811L643242B

The SDRAMs in a 32-bit I/O configuration can provide the effective solution for a wide range of applications, including multimedia and graphics applications. Also, these SDRAMs employ the new SCITT technology, thereby reducing the test time and cost.

Features

- ***64 M-bit SDRAM with a 32-bit I/O configuration***
- ***High performance series or low power consumption series***
- ***Introduction of a new test technology, SCITT***
- ***Reduced test time and cost using SCITT***
- ***Also available as extended operating-temperature components***
- ***JEDEC Standard 86-pin TSOP package***

Photo 1. MB81xx643242B Appearance



Overview

Synchronous DRAMs (SDRAMs) have been rapidly increasing in popularity since they were employed as main memory for personal computers. They have also been used not only for computer main memory, but also for various other applications, including communications equipment, consumer products, multimedia, graphics, and mobile products. It is expected that the 64 M-bit SDRAM with a 32-bit I/O configuration will be adopted as the preferred configuration for many of these applications.

FUJITSU has now developed two series of SDRAM with a 32-bit I/O configuration:

- The MB81F643242B is a high-performance version, operating at a maximum frequency of 143 MHz. This SDRAM is the second-generation product, based on the current mass-production 2M x 32-bit SDRAM.
- The MB811L643242B is a low-voltage, low power consumption version operating at 2.5V.

These products employ a new test technology, Static Component Interconnection Test Technology (SCITT), developed by a FUJITSU/Philips (Netherlands) collaboration. SCITT is a new XNOR circuit-based technology that is used for board-level interconnection testing. Using SCITT's simple method reduces the test time and cost required for board-level interconnection testing.

". . . reduces the test time and cost required for board-level interconnection testing."

Product Features

The MB81F643242B and MB811L643242B are SDRAMs in a "4 banks x 512K words x 32 bits" configuration, operating at supply voltages of 3.3V and 2.5V, respectively. These SDRAMs support the following settings:

- CAS latency: 2 or 3
- Burst length: 1, 2, 4, 8, or full page
- Burst type: Sequential or interleave

The package is an 86-pin TSOP with a pin pitch of 0.5 mm, fully conforming to JEDEC standards. The MB81F643242B Series consists of three speed versions: 143-MHz, 125-MHz, and 100-MHz. The MB811L643242B also consists of three speed versions: 100-MHz, 84-MHz, and 67-MHz. Also, a low power version is available.

FUJITSU also provides support for the SCITT functions and for optional, extended operating-temperature products for use in special environments.

Examples of applications for these SDRAMs are:

- High-speed model: Graphics card, digital TV, game equipment, etc.
- Low-voltage model: Portable video camera, digital camera, PDA, mobile computer, consumer product built-in device, etc.
- Extended operating-temperature models: Automotive equipment, such as a car navigation system, application-specific products, etc.
- Other applications: Copier, communications equipment, etc.

Table 1 lists the major characteristics of these SDRAMs and Figure 1 shows their pin assignments.

Table 1. MB81F643242B/MB811L643242B Major Characteristics

Part Number			MB81F643232B			MB811L643242B		
Speed Version			70/70L	80/80L	10/10L	10/10L	12/12L	15/15L
Clock Frequency		MHz	143	125	100	100	84	67
Clock Cycle Time	t_{CK} (min.)	ns	7	8	10	10	12	15
RAS Cycle Time	t_{RC} (min.)	ns	63	72	90	90	100	110
RAS-CAS Delay Time	t_{RCD}(min.)	ns	21	24	30	30	30	30
RAS Precharge Time	t_{RP} (min.)	ns	17	20	30	30	35	40
Clock Access Time	tAC (CL=2)	ns	6	6	7	8	8	8
	tAC (CL=3)	ns	6	6	7	8	8	8

Figure 1. MB81F643242B/MB811L643242B Pin Assignments

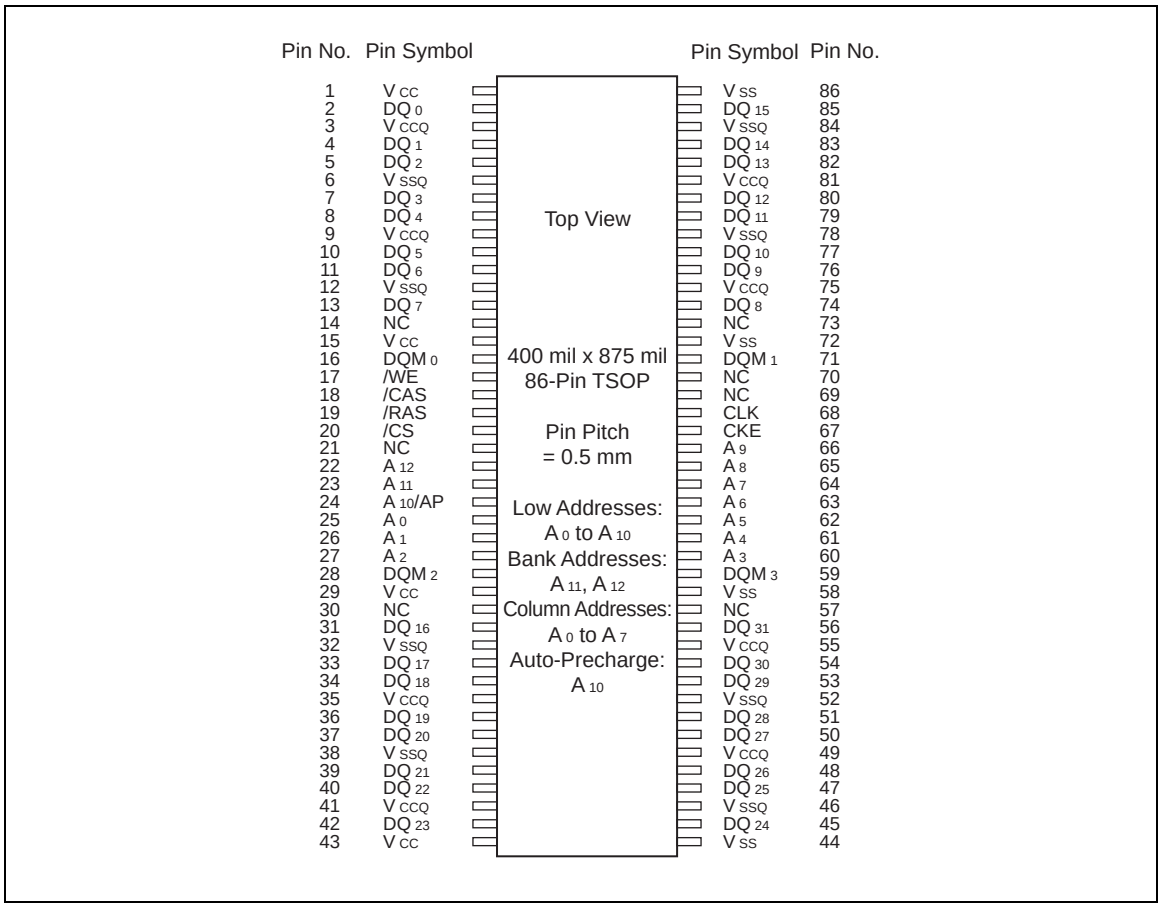
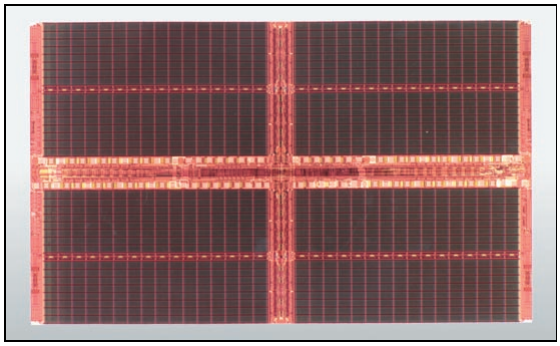


Photo 2. MB81xx643242B Chip

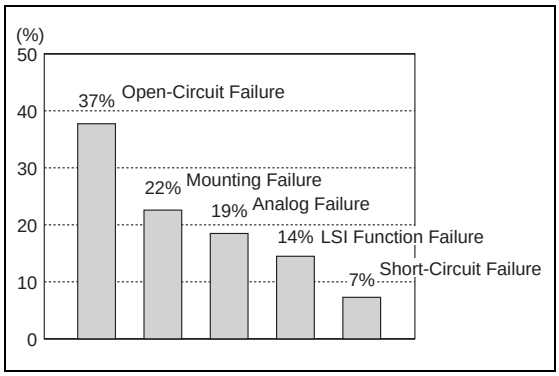


SCITT Functions

Most of the failures occurring after mounting LSIs on the board are attributable to open-circuit, mounting, or short-circuit faults. In addition, new packaging technologies make the post-mounting test more complicated. Considering these factors, FUJITSU, in collaboration with Philips, planned and developed the method for simply testing the mutual connection between LSIs mounted on the board.

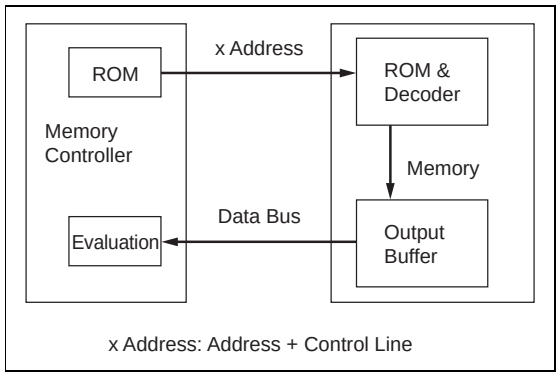
Figure 2 shows post-mounting fault ratios. Figure 3 illustrates the basic concept of SCITT technology, developed for detecting connection faults.

Figure 2. Post-Mounting Fault Ratios



The host controller outputs a test pattern on the address and control pins to memory. This test pattern had been stored in ROM in the host controller during controller design. The memory outputs a corresponding test pattern to the host controller via the I/O pins. The host side then checks the output pattern from the memory and compares the expected value and actual output value to detect open-circuit faults, short-circuit faults, missing LSIs, and mounting errors.

Figure 3. SCITT Technology Basic Concept



SCITT Advantages

The following features of SCITT can be listed as its advantages over the boundary scan method.

- No need for dedicated pins
- Short test time: 1/1,000 of the current test time or less
- Fault reject ratio: almost 100%
- Insignificant increase in chip size

Table 2 compares the interconnection tests by the SCITT and boundary scan methods.

SCITT Specifications for SDRAM

The SDRAM with SCITT functions has the following SCITT specifications.

Figure 4 shows the state diagram of SCITT mode. As shown in the figure, the SCITT functions are executed only before initialization after the supply voltage is applied. The SCITT functions are optional; the execution is not required.

The SCITT mode is controlled by the inputs from three pins: /CAS, /CS, and CKE. Each pin has the following functions:

- /CAS: For test mode entry/exit control
- /CS: For chip select control
- CKE: For test mode select control

Table 3 is the SCITT function table. Figure 5 shows the timings for entry to and exit from the SCITT mode. Figures 6 and 7 show test timings. Table 4 lists AC timing values.

Figures 8 and 9 show test patterns to be applied to 2M x 32-bit SDRAM. The applied test patterns consist of “walking-0,” “walking-1,” “all-0,” and “all-1.” Using these simple test patterns contributes to the significant reduction in test time.

Details on SCITT technology will be presented in collaboration with Philips in the International Test Conference to be held in October 1999.

“Using these simple test patterns contributes to the significant reduction in test time.”

The SCITT functions have been tested on actual applications and have verified the proof of concept and effectiveness. These functions are applicable not only to SDRAMs but also other devices. Following the accelerated trend of implementing equipment in digital form, multimedia products and consumer products will increasingly incorporate a mixture of Digital Signal Processors (DSPs), high-speed DRAMs, and flash memory. If the host processor can perform the SCITT type of interconnection test for each memory device, the efficiency of the test will be dramatically improved. ◆

Table 2. SCITT and Boundary Scan Method Comparison

Item		Boundary Scan		SCITT Technology	
Dedicated Pins Required		5 Pins		None	
Components		Shift Register/Pin TAP Controller Instruction Register Bypass Register IDCODE Register		ROM (or decoder) Comparator Circuit (controller side)	
Die Size Penalty		Yes		Negligible	
Test Items	Open-Circuit Fault	Yes	EX Test Feature Sample/Preload Feature Bypass Feature	Yes	
	Short-Circuit Fault	Yes		Yes	
	Missing IC	Yes		Yes	
	Mounting Error	Yes		Yes	
	Internal Logic Inspection	Yes	Run Test Feature IN Test Feature	No	Covered by Component Shipping Test
	ID Code Check	Yes	ID Code Feature	No	Covered by DIMM/SPD Function
	User Code Check	Yes	User Code Feature	No	

Table 3. SCITT Function Table

	/CAS	/OE	CKE	/WE	/RAS	ADD	DQM	CLK	DQ
Entry	H > L	L	L	X	X	X	X	X	X
Exit	L > H	X	X	X	X	X	X	X	X
Test Mode	L	L	H	V	V	V	V	V	V

L: Low Level
H: High Level
V: Valid Data
X: Don't Care (H or L)
cf1: First /CAS Falling Edge after Power-On Sequence

Table 4. AC Timing Values

Parameter	Description	Min. Value	Max. Value	Units
t_{TS}	Test Mode Entry Setup Time	0	—	ns
t_{TH}	Test Mode Entry Hold Time	5	—	
t_{EPD}	Test Mode to Power-On Sequence Delay Time	2	—	
t_{TLZ}	Test Mode Output in Low-Z Time	0	—	
t_{THZ}	Test Mode Output in High-Z Time	3	0	
t_{TIA}	Test Mode Input Access Time	—	20	
t_{ETD}	Test Mode Entry to Test Delay Time	5	—	

Figure 4. State Transition of SDRAM (with SCITT Functions)

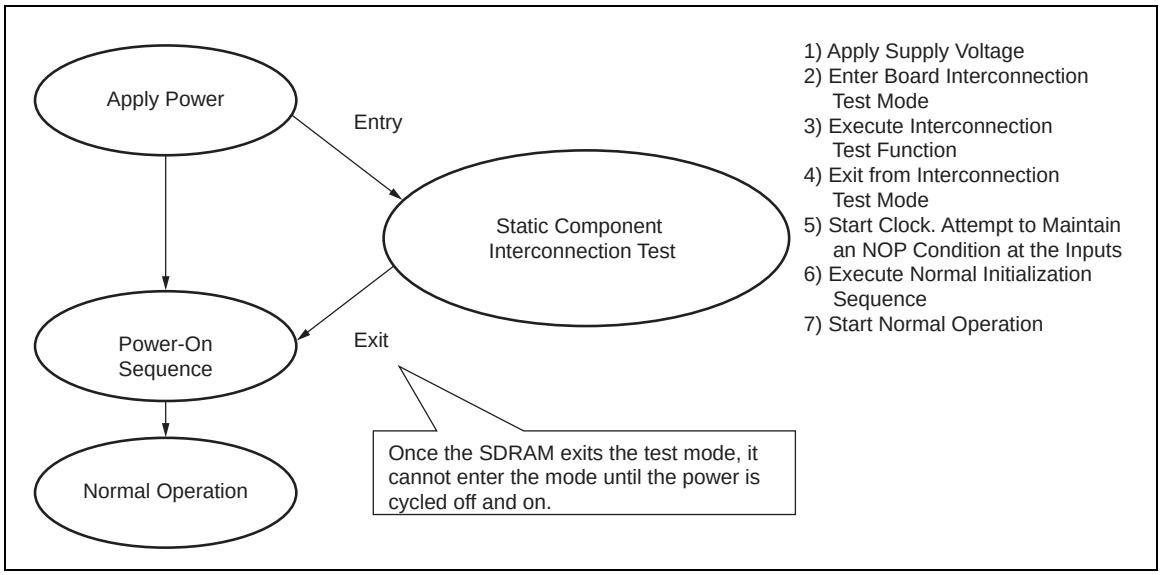
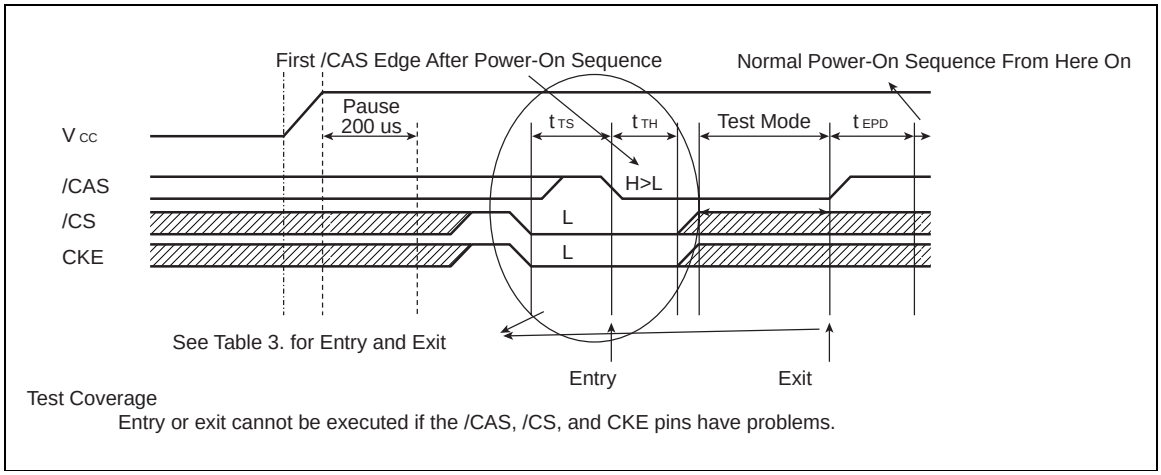


Figure 5. Entry to and Exit from SCITT Mode



Test Coverage

Entry or exit cannot be executed if the /CAS, /CS, and CKE pins have problems.

Figure 6. Test Timing (1)

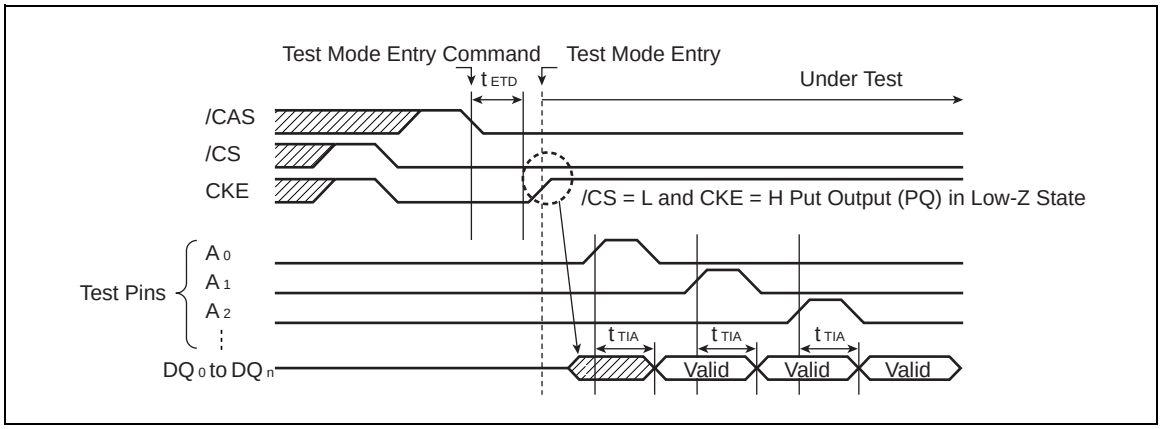


Figure 7. Test Timing (2)

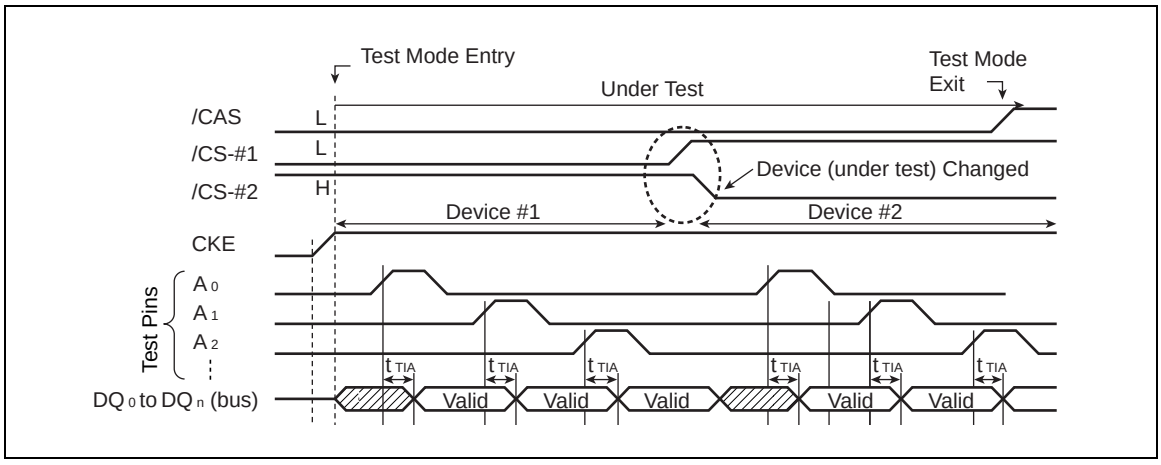


Figure 8. Test Pattern (1)

Input Bus																				Output Bus																															
/RAS	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	DQM_0	DQM_1	DQM_2	DQM_3	CLK	/WE	DQM_0	DQM_1	DQM_2	DQM_3	DQM_4	DQM_5	DQM_6	DQM_7	DQM_8	DQM_9	DQM_{10}	DQM_{11}	DQM_{12}	DQM_{13}	DQM_{14}	DQM_{15}	DQM_{16}	DQM_{17}	DQM_{18}	DQM_{19}	DQM_{20}	DQM_{21}	DQM_{22}	DQM_{23}	DQM_{24}	DQM_{25}	DQM_{26}	DQM_{27}	DQM_{28}	DQM_{29}	DQM_{30}	DQM_{31}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H

0 = Input Low, 1 = Input High, L= Output Low, H = Output High

Figure 9. Test Pattern (2)

Input Bus																				Output Bus																															
/RAS	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	DQM_0	DQM_1	DQM_2	DQM_3	CLK	/WE	DQM_0	DQM_1	DQM_2	DQM_3	DQM_4	DQM_5	DQM_6	DQM_7	DQM_8	DQM_9	DQM_{10}	DQM_{11}	DQM_{12}	DQM_{13}	DQM_{14}	DQM_{15}	DQM_{16}	DQM_{17}	DQM_{18}	DQM_{19}	DQM_{20}	DQM_{21}	DQM_{22}	DQM_{23}	DQM_{24}	DQM_{25}	DQM_{26}	DQM_{27}	DQM_{28}	DQM_{29}	DQM_{30}	DQM_{31}
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

0 = Input Low, 1 = Input High, L= Output Low, H = Output High