

# FUJI Power Supply Control IC

FA7703/04

## *Application Note*

June -2002  
Fuji Electric Co., Ltd.  
Matsumoto Factory

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**Note**

- Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and stable operation.

**Description**

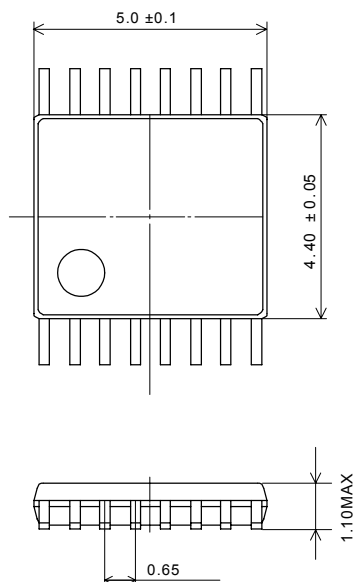
FA7703/04 are the PWM type DC-DC converter control ICs with 2ch output that can directly drive power MOSFETs. FA7703/04 feature CMOS devices with high breakdown voltage and also low power consumption are achieved. By means of their small and thin package (1.1mm max.), and high frequency operation (to 1MHz), FA7703/04 are completely suitable for the use of very small DC-DC converters. Besides, you can select a Pch or Nch type of MOSFET directly driven by FA7703/04, and also you can practically design any kind of DC-DC converter circuit like a boost converter, a buck converter, a inverting converter, a fly-back converter, and so on.

**1. Features**

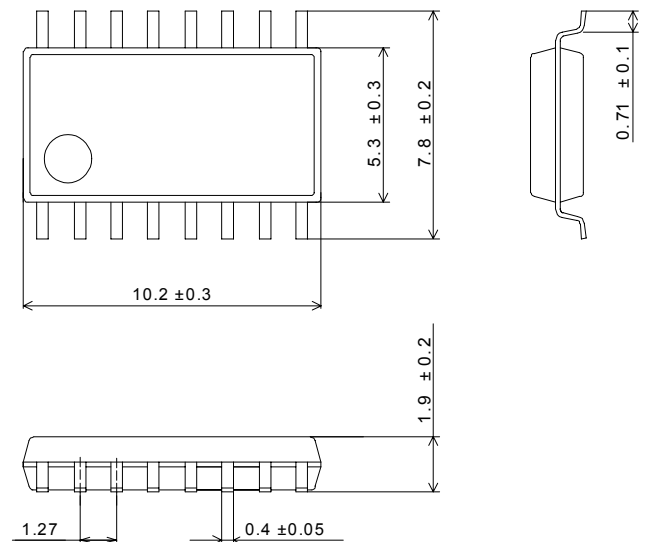
- Wide range of supply voltage:  $V_{CC}=2.5$  to  $20V$
- Direct driving of MOSFET
- Switching Pch/Nch driving is available (channel 1 only)
- Low current consumption is achieved by CMOS process:  
1.8mA (typ.) in operation
- 2ch PWM control IC
- High frequency operation is available: 50kHz to 1MHz
- Simple setting of operation frequency with a timing resistor
- Soft start setting is available
- Setting of the limitation of maximum output duty cycle is available in each channel
- Built-in protection function for undervoltage lockout
- Highly accurate reference voltage:  
 $V_{REF}: 1.00V \pm 1\%$ ,  $V_B: 1.00V \pm 2\%$ ,  $V_{REG}: 2.20V \pm 2\%$
- Built-in output timer latched short-circuit protection circuit
- Thin and small package: TSSOP-16, SOP-16

**2. Outline**

TSSOP-16 (V)

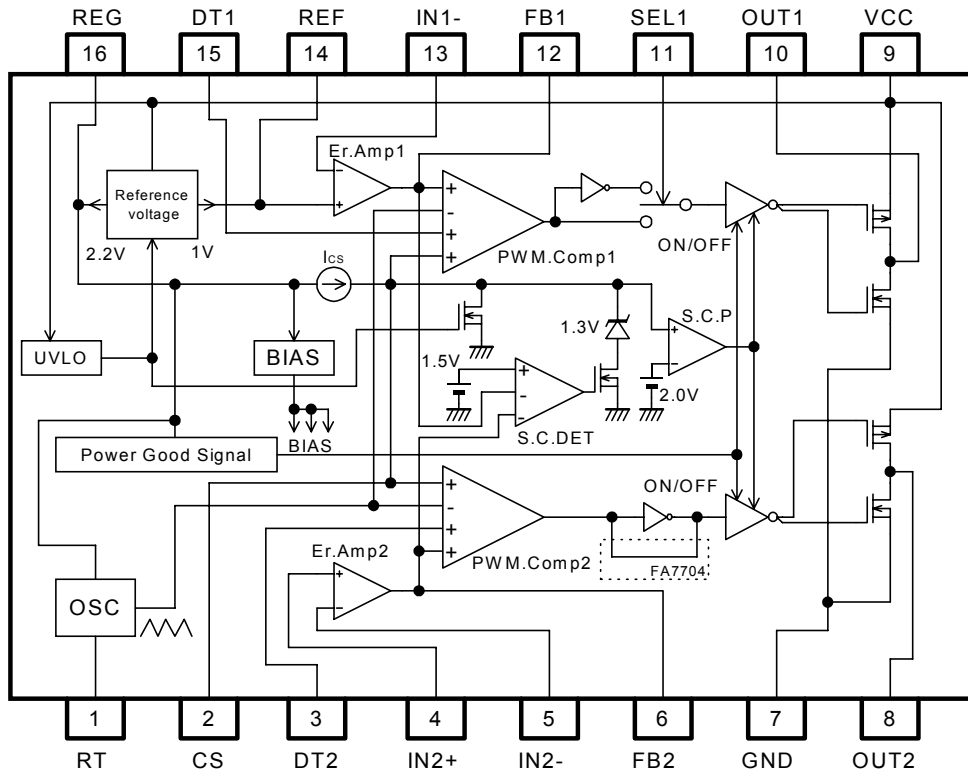


SOP-16 (M)



units:mm

**3. Block diagram**



**4. Selection Guide**

FA7703	Ch.1(OUT1)	Buck, Boost, Fly-back
	Ch.2(OUT2)	Buck, Inverting (Pch driven)
FA7704	Ch.1(OUT1)	Buck, Boost, Fly-back
	Ch.2(OUT2)	Boost, Fly-back (Nch driven)

**5. Pin assignment**

Pin No	Pin symbol	Description
1	RT	Oscillator timing resistor
2	CS	Soft start, Timer latched short circuit protection, ON/OFF control
3	DT2	Ch.2 Dead Time Adjustment
4	IN2+	Ch.2 non-inverting input to error amplifier
5	IN2-	Ch.2 inverting input to error amplifier
6	FB2	Ch.2 output o error amplifier
7	GND	Ground
8	OUT2	Ch.2 output
9	VCC	Power supply
10	OUT1	Ch.1 output
11	SEL	Selection of type of driven MOSFET (OUT1)
12	FB1	Ch.1 output o error amplifier
13	IN1-	Ch.1 inverting input to error amplifier
14	REF	Reference voltage
15	DT1	Ch.1 Dead Time Adjustment
16	REG	Regulated voltage output

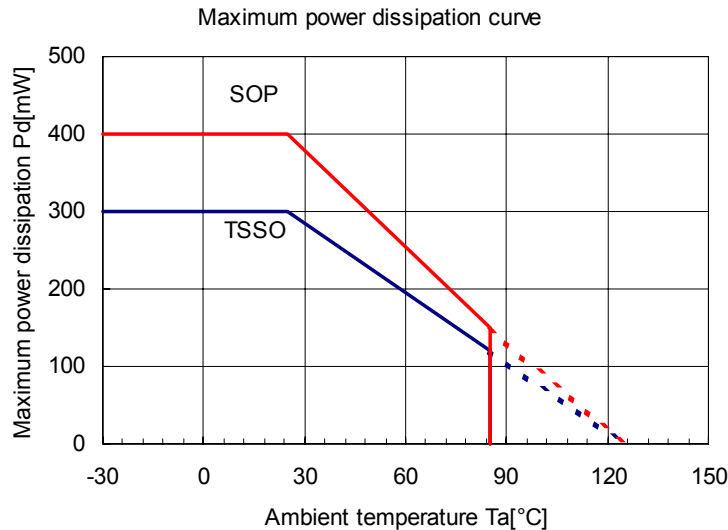
## 6. Ratings and characteristics

The contents are subject to change without notice. When using a product, be sure to obtain the latest specifications.

### (1) Absolute maximum ratings

Item	Symbol	Ratings	Units
Power supply voltage	VCC	20	V
REF Terminal output current	IREF	1	mA
REG Terminal output current	I <sub>REG</sub>	2	mA
OUT1, OUT2 Terminal source current	I <sub>SOpeak</sub>	-400(peak)	mA
	I <sub>SOcont</sub>	-50(continuous)	mA
OUT1, OUT2 Terminal sink current	I <sub>SIpeak</sub>	+150(peak)	mA
	I <sub>SIcont</sub>	+50(continuous)	mA
RT,CS,REG,REF,IN1-,IN2+,IN2-,FB1,FB2,DT1,DT2,SEL1 Terminal voltage	V <sub>LOGIC</sub>	+2.5(max.) -0.3(min.)	V
Power dissipation (T <sub>a</sub> ≤25°C)*	TSSOP	300	mW
	SOP	400	
Operating ambient temperature	T <sub>a</sub>	-30 to +85	°C
Operating junction temperature	T <sub>j</sub>	+125	°C
Storage temperature	T <sub>stg</sub>	-40 to +150	°C

\*:Maximum dissipation curve at T<sub>a</sub>≥25°C is shown under figure.



### (2) Recommended operating conditions

Item	Symbol	MIN.	TYP.	MAX.	Units
Supply voltage	V <sub>CC</sub>	2.5	6	18	V
DC feedback resistor of error amplifier	R <sub>NF</sub>	100			kΩ
VCC terminal capacitance*	C <sub>VCC</sub>	0.1			μF
REG terminal capacitance	C <sub>REG</sub>	0.047	0.1	1	μF
CS terminal capacitance	C <sub>CS</sub>	0.01		10	μF
Oscillation frequency	f <sub>OSC</sub>	50		1000	kHz
SEL1 terminal voltage	Pch,NPN driving	V <sub>SEL1L</sub>	Connect to GND		
	Nch,NPN driving	V <sub>SEL1H</sub>	Connect to REG terminal		

\*Please select the proper value by input-output conditions of power supply.

**(3)Electrical characteristics** [Unless otherwise standard, Ta=25°C, Vcc=6V, RT=22kΩ]

(1) Internal Bias Section (REF terminal voltage)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output Voltage	VREF	REF terminal load current IREF=0mA	0.990	1.000	1.010	V
Line Regulation	VLINEF	Vcc=2.5 to 18V, IREF=0mA		±1	±5	mV
Load Regulation	VLDF	IREF=0 to 1mA	-10	-3		mV
Variation with temperature	VTCF	Ta=-30 to +85°C Change rate for value at 25°C		-0.8 to +0.2		%

(2) Regulated Voltage for Internal Control Blocks Section (REG terminal voltage)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output Voltage	VREG	REG terminal load current IREG=0mA	2.156	2.200	2.244	V
Line Regulation	VLINEG	Vcc=2.5 to 18V, IREG=0mA		±4	±14	mV
Load Regulation	VLDG	IREG=0 to 2mA	-12	-2		mV
Variation with temperature	VTCG	Ta=-30 to +85°C Change rate for value at 25°C		-0.8 to +0.2		%

(3) Oscillator Section						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Oscillation frequency	fOSC	RT=22kΩ	160	190	220	kHz
Line Regulation	fLINE	Vcc=2.5 to 18V		±0.1		%
Variation with temperature	ftC1	Ta=+25 to -30°C, f=50k to 1MHz		±2		%
	ftC2	Ta=+25 to +85°C, f=50k to 1MHz		±3		%

(4) Error Amplifier Section (Input:IN1-,IN2+,IN2-,Output:FB1,FB2 terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Reference Voltage (ch1)	VB	IN1- terminal threshold voltage	0.980	1.000	1.020	V
Input offset (ch2)	VOFST	(IN2+) - (IN2-)	-	-	±10	mV
Common mode input voltage	VIN		0.3		1.4	V
Input Current	IIN		-100	0	+100	nA
Open Loop Gain	AVO		70			dB
Unity Gain Bandwidth	fT			1.5		MHz
Output Source Current	IOHE	FB1,2 terminal voltage=VREF-0.5V	-220	-160	-100	μA
Output sink Current	IOLE	FB1,2 terminal voltage=0.5V	3	6	12	mA

(5) Pulse Width Modulation Section (FB1,FB2 terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input threshold voltage	VFBO	Duty Cycle=0%	0.550	0.650	0.750	V
Input threshold voltage	VFB100	Duty Cycle=100%	1.000	1.100	1.200	V

(6) Dead Time Adjustment Circuit Section (DT1, DT2 terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input threshold voltage	VDT0	Duty Cycle=0%	0.550	0.650	0.750	V
Input threshold voltage	VDT100	Duty Cycle=100%	1.000	1.100	1.200	V

(7) Under Voltage Lock-Out Section (VCC terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
ON threshold	VCCON			2.00	2.25	V
OFF threshold	VCCOF		1.40	1.85		V
Hysteresis Voltage	VCCHY		0.05	0.15	0.35	V
Variation with temperature	VCCHY	Ta=-30 to +25°C		+0.3		mV/°C
		Ta=+25to +85°C		-0.1		mV/°C

(8) Soft Start Section (CS terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output source current	ICs	CS=0V	-2.8	-2.2	-1.6	μA
Threshold Voltage1	VCS0	Duty Cycle=0%	0.550	0.650	0.750	V
Threshold Voltage2	VCS50	Duty Cycle=50%		0.880		V

(9) Short circuit Protection Section (FB terminal, CS terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Short Detection Threshold Voltage	VFBTH	FB terminal voltage	1.350	1.500	1.650	V
Latched Mode Threshold Voltage	VCSTH	CS terminal voltage	1.900	2.000	2.100	V
Latched Mode Reset Voltage	VCSRE	CS terminal voltage		1.830		V
Latched Mode Hysteresis	VCSHY	CS terminal voltage	30	170	300	mV
CS terminal Clamped Voltage	VCSCL1	FB terminal voltage<1.35V	1.200	1.270	1.340	V
	VCSCL2	FB terminal voltage>1.65V	2.120	2.200	2.280	V

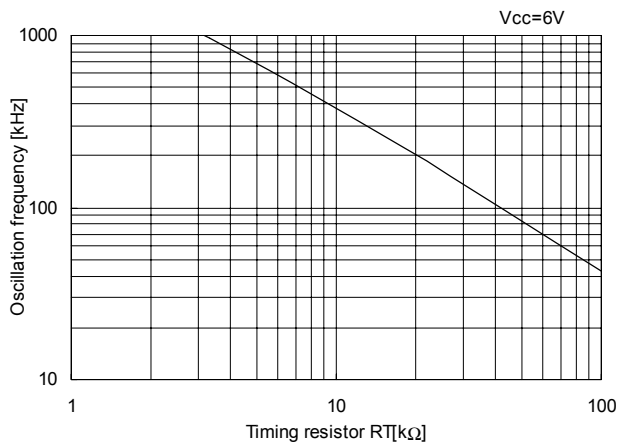
(10) Output Stage Section (OUT1,OUT2 terminal,SEL1 terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
High side on resistance	RONH	Vcc=6V,Source Current=-50mA		10	20	Ω
High side on resistance	RONH	Vcc=2.5V,Source Current=-50mA		18	36	Ω
Low side on resistance	RONL	Vcc=6V,Sink Current=+50mA		5	10	Ω
Low side on resistance	RONL	Vcc=2.5V,Sink Current=+50mA		5	10	Ω
Rise Time	trn	330pF Load to GND terminal		20		ns
	trp	330pF Load to VCC terminal		20		ns
Fall Time	tfn	330pF Load to GND terminal		35		ns
	tfp	330pF Load to VCC terminal		35		ns
SEL1 terminal Input Voltage	VSEL1L	Pch-MOSFET, PNP transistor driving	0		0.2	V
	VSEL1H	Nch-MOSFET, NPN transistor driving	VREG-0.2		VREG	V

(11) Overall Section (VCC terminal)						
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Operating mode Supply Current	ICC0	Duty Cycle=0%,OUT1/2:open CS=0V, FB1,FB2≈VREG RT=22kΩ,f≈190kHz		1.3	1.9	mA
	ICC1	Duty Cycle=80%,OUT1/2:open RT=22kΩ,f≈190kHz		1.8	2.7	mA
	ICC2	Duty Cycle=80%,OUT1/2:open RT=3kΩ,f≈1MHz		3.1	4.7	mA
Latched mode Supply Current	ICCLAT	CS>2.1V,FB1,FB2≈VREG, RT=22kΩ,f≈190kHz		1.3	1.9	mA

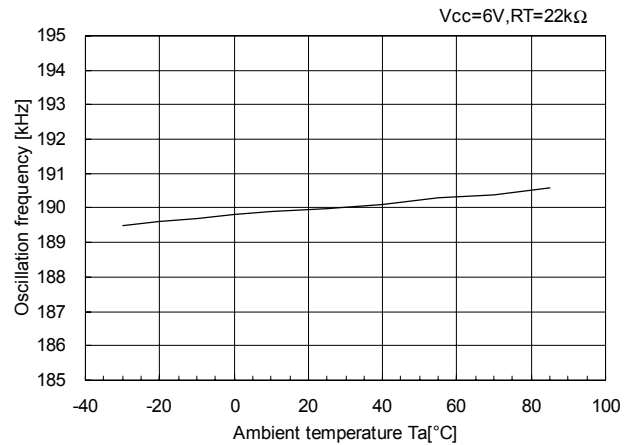


7. Characteristics curves

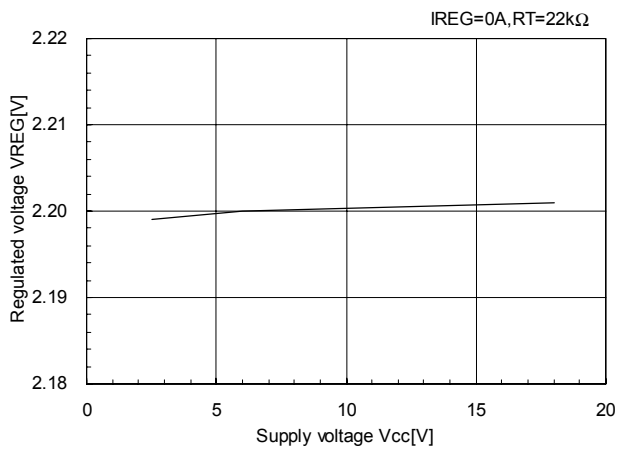
Timing resistor vs. Oscillation frequency



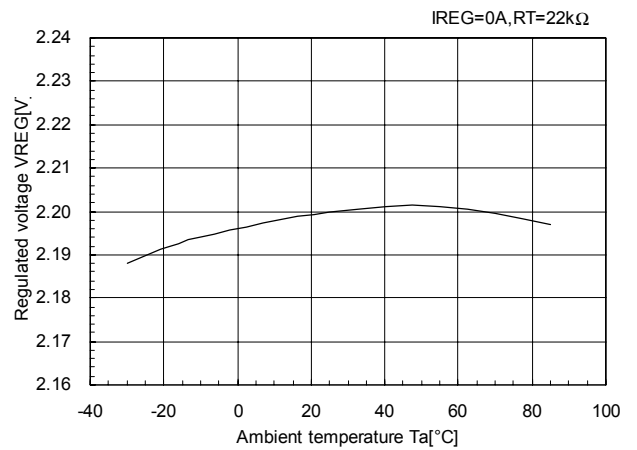
Oscillation frequency vs. ambient temperature



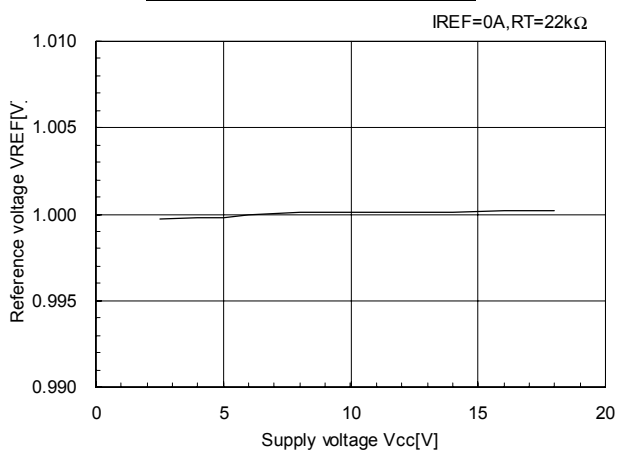
Regulated voltage vs. Supply voltage VCC



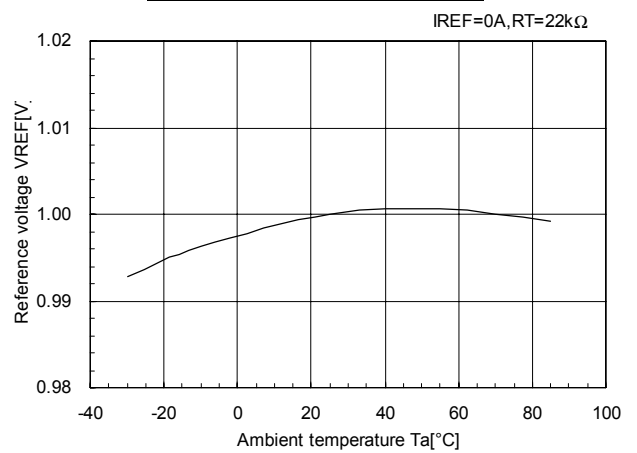
Regulated voltage vs. Ambient temperature

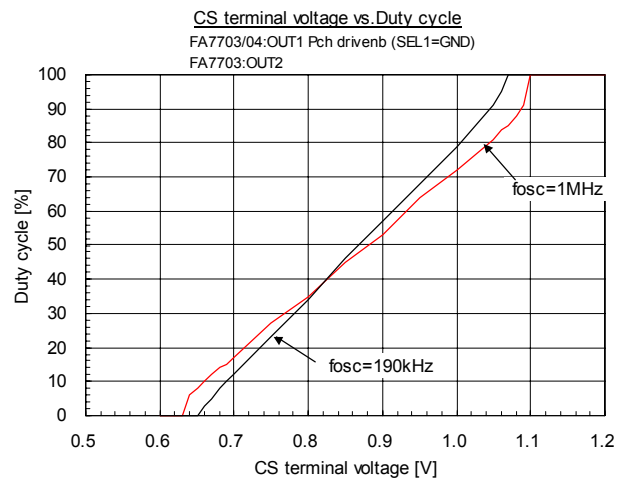
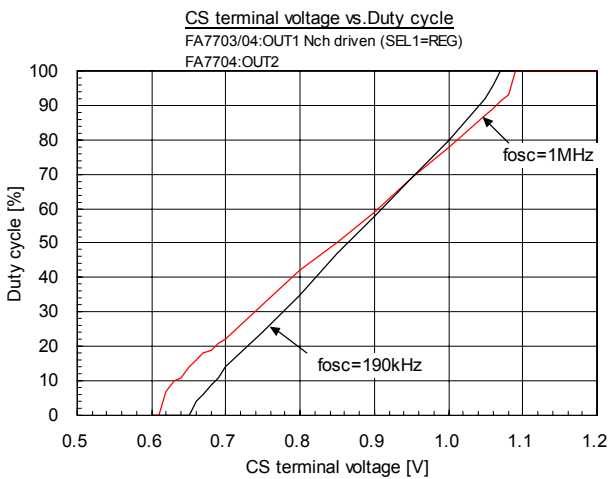
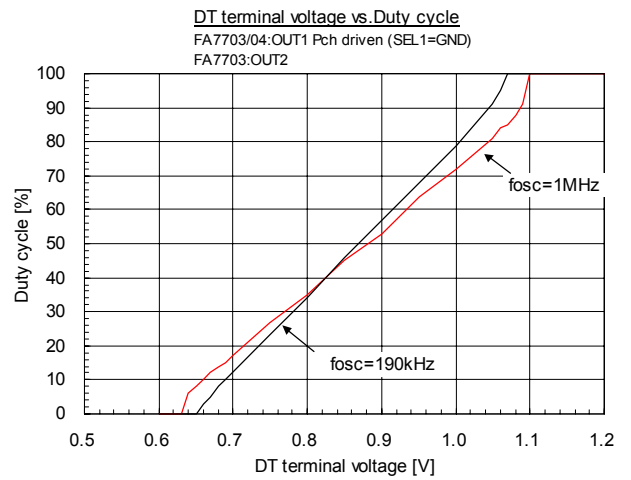
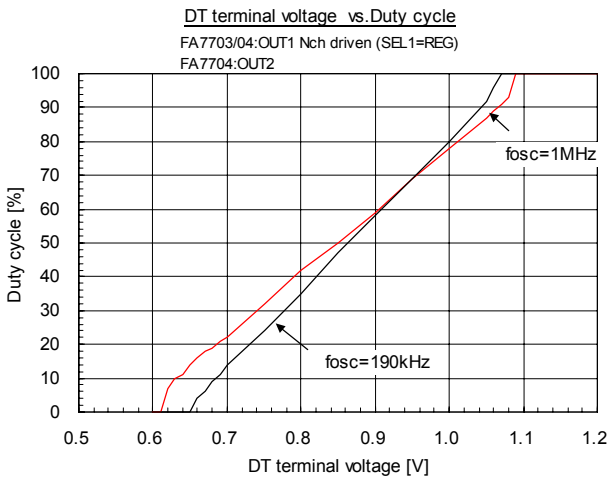
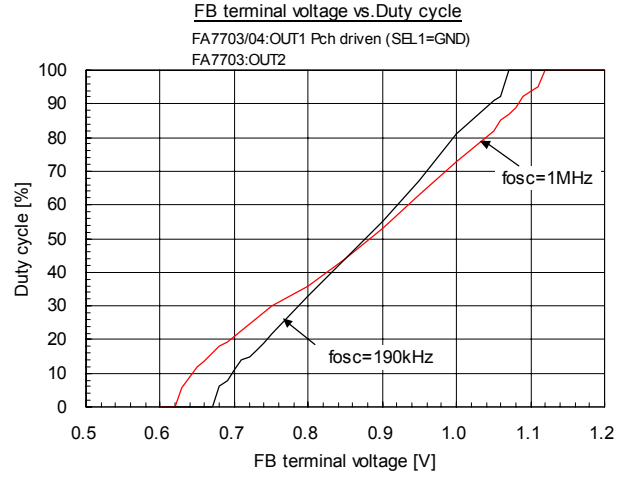
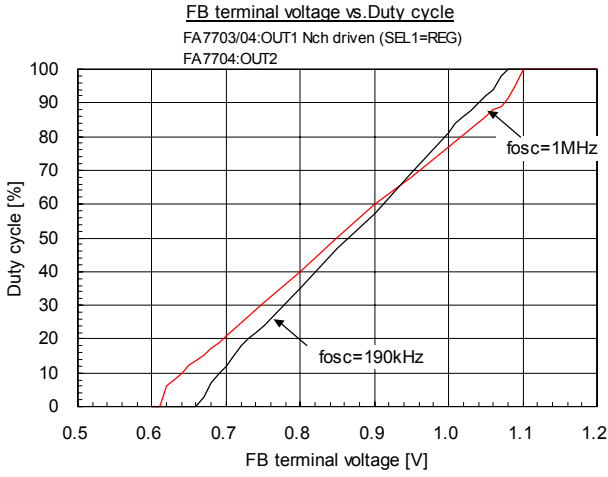


Reference voltage vs. Supply voltage VCC

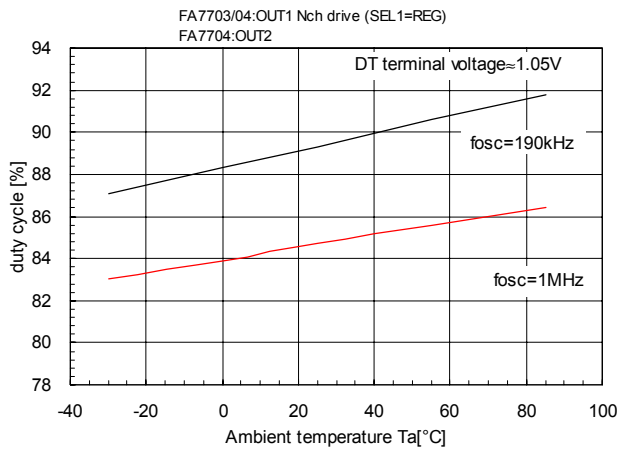


Reference voltage vs. Ambient temperature

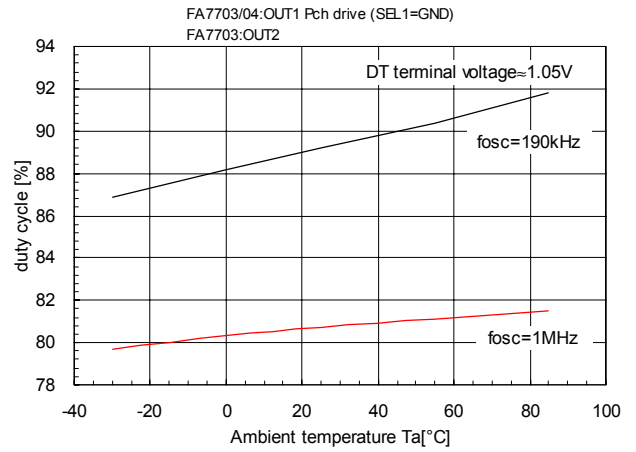




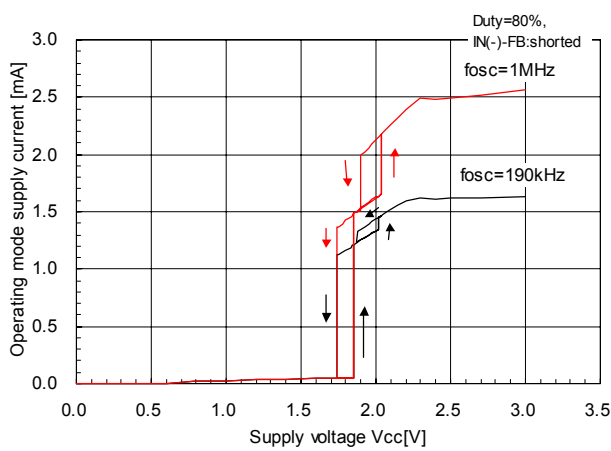
Duty cycle vs. Ambient temperature



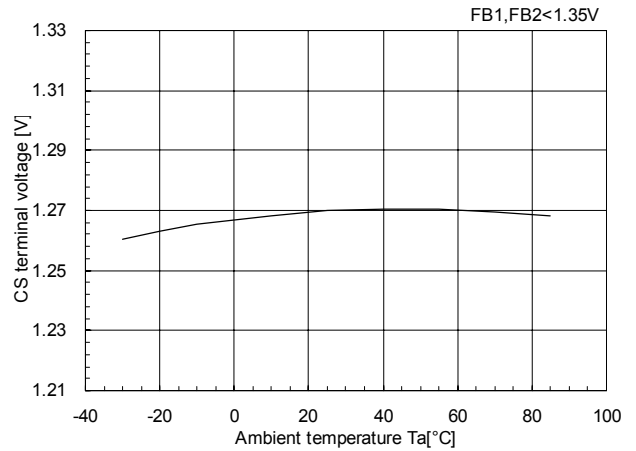
Duty cycle vs. Ambient temperature



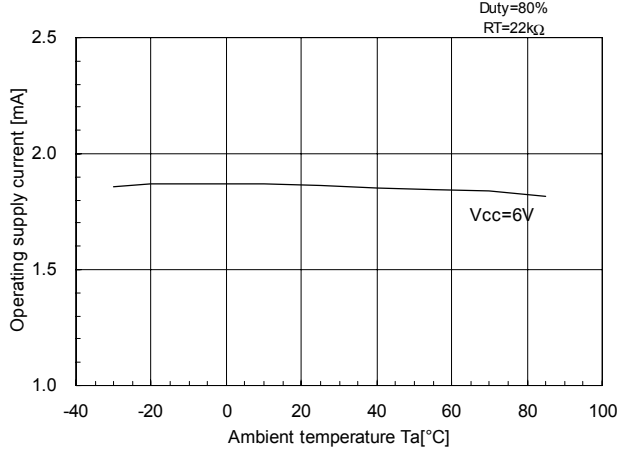
Operating mode supply current vs. Supply voltage



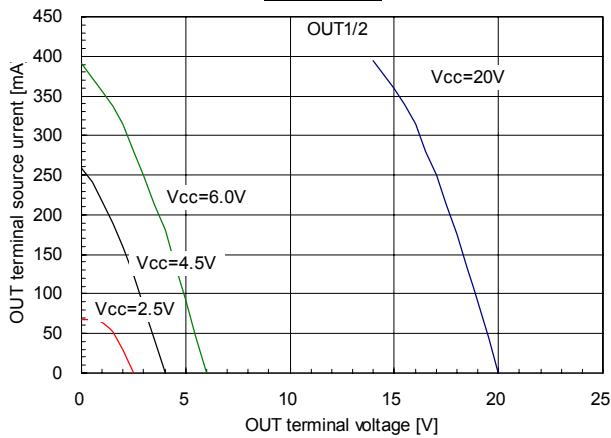
CS terminal voltage vs. Ambient temperature



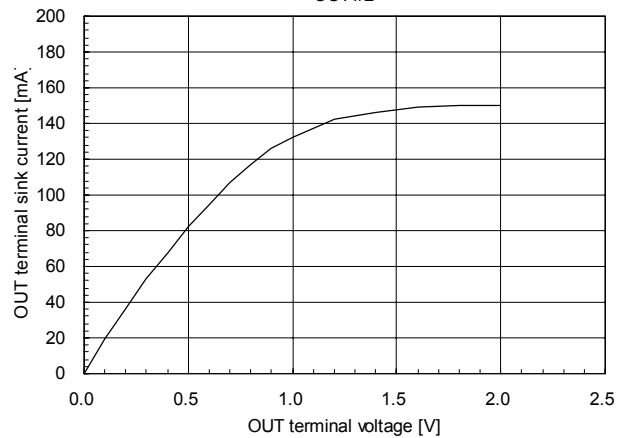
Operating supply current vs. Ambient temperature



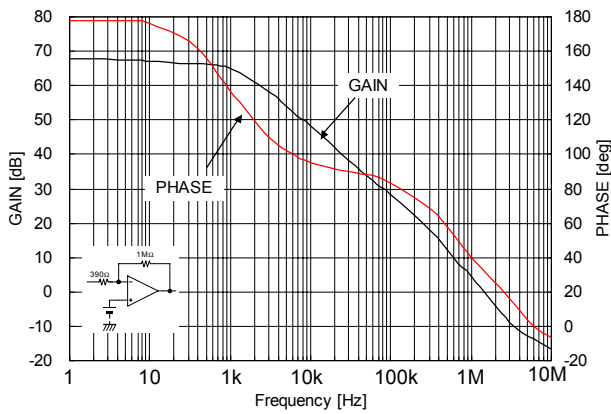
OUT terminal High side voltage vs. Source current



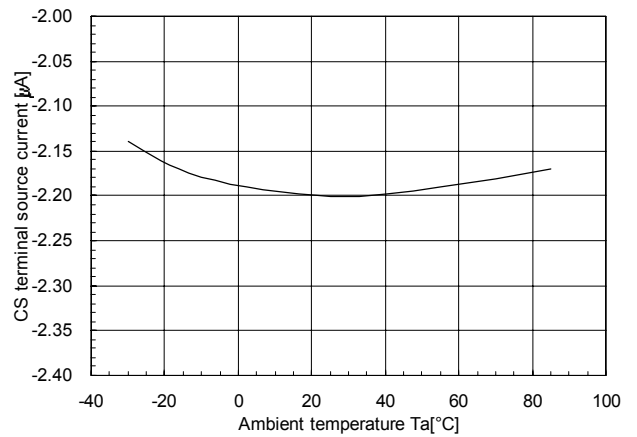
OUT terminal Low side voltage vs. Sink current



Error Amplifier gain and Phase vs. frequency



CS terminal source current vs. Ambient temperature



**8. Description of each circuit**

**(1)Reference Voltage Circuit**

The reference voltage circuit of FA7703/04 generates the reference voltage (VREF) of 1.00V±1% compensated in temperature from VCC voltage, and the regulated voltage (VREG) of 2.2V ±2% for internal controlling. These voltages start to output when the undervoltage lockout protection (UVLO) is cancelled, and they stabilize after the supply voltage (VCC) reaches up to approx. 2.4V or higher. The reference voltage (VREF) is connected to the non-inverting input of Error Amplifier 1 and serves as the reference voltage of Error Amplifier 1. Because of Error Amplifiers have offset voltage then, the precision of voltage in practical use is 1.00V±2%. The voltage (VREF) outputs externally from REF terminal, therefore, it can serve as a stabilized power source. When using it, be sure to set the output current 1mA or below.

The regulated voltage (VREG) for internal controlling serves as the stabilized power source for maximum output duty setting or the like. Be sure to set the output current 2mA or below in operation in this case. This voltage also serves as the control power source of all the internal circuits of FA7703/04. A capacitor for stabilization (CREG) is needed to be connected to the VREG terminal. See recommended operating conditions to determine capacitance.

**(2)Oscillator**

The oscillator of FA7703/04 generates triangular waveforms by charging and discharging the built-in capacitor. Any desired oscillation frequency can be obtained by setting the value of the resistor connected to RT terminal (Fig. 1).

The voltage oscillates between approximately 0.65V and 1.10V in charging and discharging with almost the same gradients (Fig. 2). Your desired oscillation frequency can be determined by changing the gradient using the resistor (RT) connected to RT terminal. (Large RT: Low frequency, small RT: High frequency) The waveforms of oscillator cannot be observed from the outside because a terminal for this purpose is not provided.

Approximately DC 1V is output to RT terminal.

The oscillator output is connected to PWM comparator.

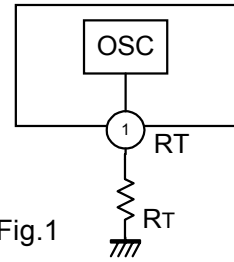


Fig.1

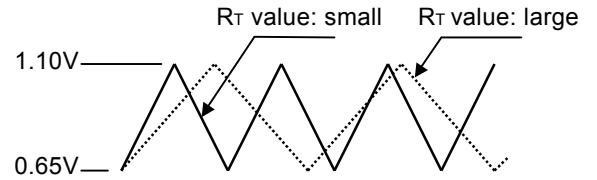


Fig.2

**(3)Error Amplifier Circuit**

Error Amplifier 1 of FA7703/04 has the inverting input IN1(-) terminal (Pin13). The non-Inverting input is internally connected to the reference voltage (VB) of 1.00V±2% at 25°C. Because error Amplifier 2 of FA7703/04 has the inverting input IN2(-) terminal (Pin5) and non-inverted input IN2(+) terminal (Pin4) outputting externally, various circuit can be designed by kinds of external circuit structures. FB terminals (Pin6, Pin12) are the outputs of Error Amplifiers. Voltage Gain and phase compensation can be set by connecting a capacitor (C) and a resistor (R) between FB terminal and IN(-) terminal.(Fig. 3) For more information about the connection for each output voltage of power supply, refer to Design Advice.

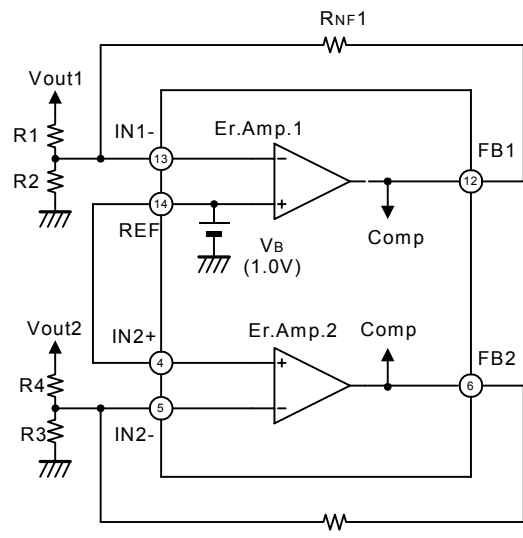


Fig.3

**(4) PWM comparator**

PWM comparator of FA7703/04 has 4 input terminals. (Fig. 4) The oscillator output ② is compared with the CS terminal voltage ①, the DT terminal voltage ③, and the Error Amplifier output ④. Among those 3 inputs of ①, ③, and ④, the one with the lowest voltage is chosen and given priority. While the value of the chosen voltage is lower than the value of the waveform of oscillator output, PWM comparator output is set to LOW. Similarly, while the value of the chosen voltage is higher than the waveform of oscillator output, PWM comparator output is set to HIGH. (Fig. 5)

When FA7703/04 are turning ON, the soft start function starts according to the CS terminal voltage ①, then the output pulses begin to widen gradually. The maximum pulse width is adjusted by changing the DT terminal voltage. In steady operation, the pulse width is determined with the condition of the Error Amplifier output ④, and then the output voltage of DC-DC converter is stabilized. The operation flow chart of PWM comparator and OUT terminal is shown in Fig. 5. The output polarity of OUT1 terminal changes according to the condition of SEL1 terminal. The polarity of OUT 2 terminal is different between FA7703 and FA7704; accordingly, select the type for your desired circuit design.

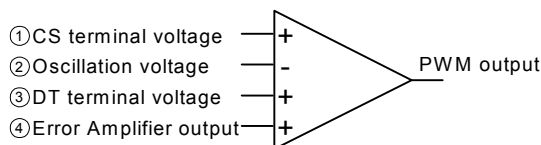


Fig.4

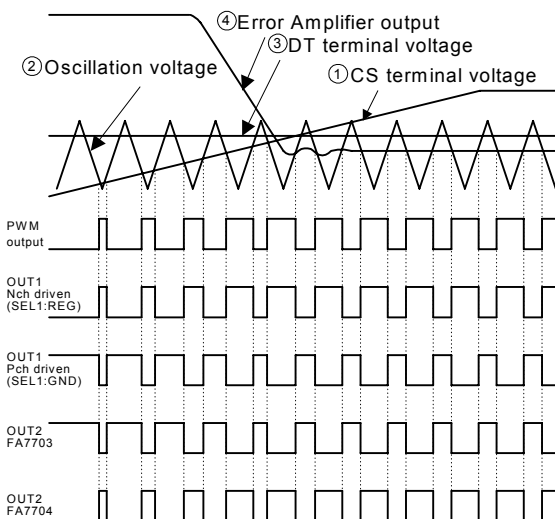


Fig.5

**(5) Soft start function**

As described in Fig. 6, a capacitor Ccs is connected to CS terminal. When the power supply of FA7703/04 starts and the undervoltage lockout protection circuit (UVLO) is cancelled, the capacitor Ccs is charged by the internal current source (2.2μA. typ.), and the voltage of CS terminal rises gradually. Since the voltage of CS terminal is connected to PWM comparator, the output pulses begin to widen gradually, and then the soft start function starts as a result. (Fig. 5)

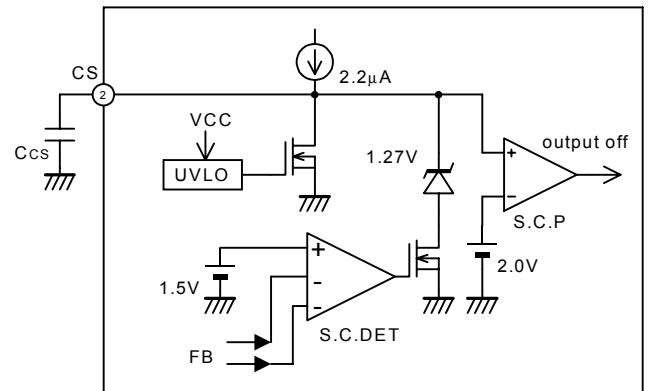


Fig.6

**(6) Timer latch short-circuit protection circuit**

The short-circuit protection circuit of FA7703/04 consists of two comparators. (S.C. DET comparator, S.C.P comparator) In steady operation, the output of Error Amplifier is approximately 1V, accordingly, the output of S.C.DET comparator is set to High, and the voltage of CS terminal is clamped at 1.27V. If the output voltage of Error Amplifiers exceeds 1.5V(typ.), the output of S.C.DET comparator is set to Low, and the clamp action at the CS terminal voltage of 1.27V is cancelled, then the voltage of CS terminal rises up to the VREG voltage. When the voltage of CS terminal exceeds 2.0V(typ.), the output of S.C.P comparator is set to High, accordingly, the output of FA7703/04 is shut off. In this case, FA7703/04 operate in OFF latch mode and the current consumption in this mode is 1.3mA(typ.). The operating waveform of the voltage of CS terminal is shown in Fig. 7.

The approximate time (tp) between the occurrence of a short-circuit in the output and the triggering of the short-circuit protection

function can be calculated with

$$t_p[s] \approx \frac{0.7 \times C_{cs}}{I_{cs}}$$

where,  $C_{cs}$ : Capacitance of CS terminal [ $\mu\text{F}$ ]

$I_{cs}$ : Output source current of CS terminal [ $\mu\text{A}$ ]

( $2.2\mu\text{A}$ , typ.)

You can reset the timer latch action for the short-circuit protection function by changing the voltage of either VCC terminal or CS terminal to the following values.

VCC terminal: below UVLO voltage (1.85V typ.)

CS terminal: below 1.83V(typ.)

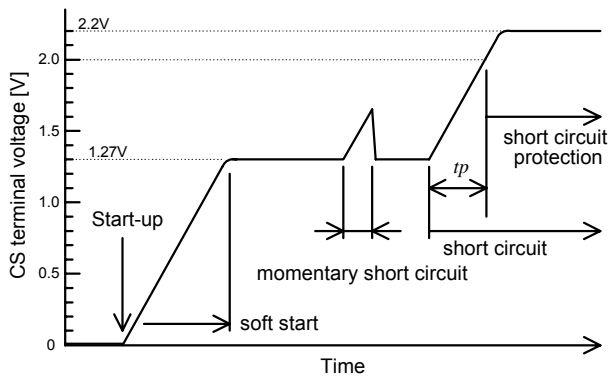


Fig.7

### (7)Output circuit

FA7703/04 contain a push-pull output stage and can directly drive MOSFETs. The peak current of OUT terminal is the maximum sink current of +150mA, and the source current of -400mA. FA7703/04 can also drive both NPN and PNP type transistors. And in such cases, the maximum continuous current is  $\pm 50\text{mA}$ . When designing the value of output current, be sure to consider the allowable loss accordingly. (See Design advice)

Ch1 of FA7703/04 is available for driving both types of MOSFETs and you can determine the type of MOSFET, which is connected externally by selecting the connection of SEL1 terminal (Pin11). If SEL terminal is connected to GND terminal, FA7703/04 can drive a Pch MOSFET. If SEL terminal is connected to REG terminal, they can drive Nch MOSFET.

You can accordingly design a buck converter circuit by Pch MOSFET driving, and a boost circuit or a fly-back converter circuit by Nch MOSFET driving.

DO NOT leave SEL1 terminal open in operation, and be sure to connect it to either GND terminal or REG terminal.

### (8)Power good signal/Undervoltage lockout protection circuit (UVLO)

To protect FA7703/04 from malfunction when the supply voltage drops, there is built-in undervoltage lockout as a protection circuit. When the supply voltage rises from 0V, the UVLO circuit is canceled at VCC of 2.0V(typ.). When the supply voltage drops, the UVLO circuit shuts off the output at VCC of 1.85V(typ.). In this case, CS terminal is reset to Low level.

Power good signal circuit monitors the voltage of REG terminal, and it stops the output of FA7703/04 until the voltage of REG terminal exceeds approximately 1.9V in order to protect the ICs from malfunction.

## 9. Design advice

### (1) Setting oscillation frequency

As described in “(2) Oscillator” of “Description of each circuit”, any desired oscillation frequency can be obtained by setting the value of the resistor connected to RT terminal. (Fig. 1) The desired oscillation frequency should be set between 50kHz and 1MHz. The oscillation frequency to RT can be obtained from the chart of “Oscillation frequency vs. timing resistor” characteristic curves or by calculating with the formulas below.

$$f_{osc} = 3 \times 10^3 \times R_T^{-0.907}$$

$$R_T = \left( \frac{3 \times 10^3}{f_{osc}} \right)^{1.1}$$

where,  $f_{osc}$ : Oscillation frequency [kHz]

$R_T$ : Timing resistor [kΩ]

These formulas can only be used for rough calculation; accordingly, be careful when designing, because the value obtained is not guaranteed. The operation frequency varies due to the conditions of the tolerance of IC influence for noises, or external discrete components etc. When determining the values, be sure to verify the effectiveness of the values you calculated in an actual circuit operation.

Because it is easily affected by noises by the high impedance, the resistor  $R_T$  should be connected as shortly as possible near RT terminal and GND terminal,

### (2) Operation around the maximum or the minimum output duty cycle

As described in the charts of “FB terminal voltage vs. output duty cycle”, “DT terminal voltage vs. output duty cycle”, “CS terminal voltage vs. output duty cycle” characteristic curves, the output duty of FA7703/04 changes sharply around the minimum and the maximum output duty. This phenomenon occurs more conspicuously when operating in a high frequency (i.e. when the pulse width is narrow). Cautious care must be taken when using high frequency.

### (3) Determining soft start period

The time from the start of charging CS terminal to n% output duty cycle can be roughly calculated by the following expression.

$$t_s[s] = \frac{V_{CSn} \times C_{CS}}{I_{CS}}$$

where,  $V_{CSn}$ : CS terminal voltage in the output duty of n% [V]

$C_{CS}$ : Capacitance of capacitor of CS terminal [ $\mu$ F]

$I_{CS}$ : Output source current of CS terminal [ $\mu$ A]  
2.2 $\mu$ A (typ.)

$V_{CSn}$  represents the voltage of CS terminal in the output duty of n%, and it changes according to the operation frequency. The value is obtained simply from the chart of “CS terminal voltage vs. output duty cycle” characteristic curves.

Since the output source current of CS terminal is 2.2 $\mu$ A, which it is rather small, if the capacitor has leak current, then the period of soft start ( $t_s$ ) is easily affected. Therefore, cautious care must be taken when determining the value.

Charging of CS terminal begins after UVLO is cancelled. Note that the time from power-on of Power supply to start of charging  $C_{CS}$  is  $t_0$  which is not zero as described in Fig. 8. be careful.

To reset the soft start function, the voltage of CS terminal is discharged with FA7703/04's internal switch triggered by lowering the voltage of Power supply below the voltage of UVLO (1.85V, typ.). If Power supply restarts before the voltage is sufficiently discharged, the soft start function might not properly operate. accordingly, cautious care must be taken about it.

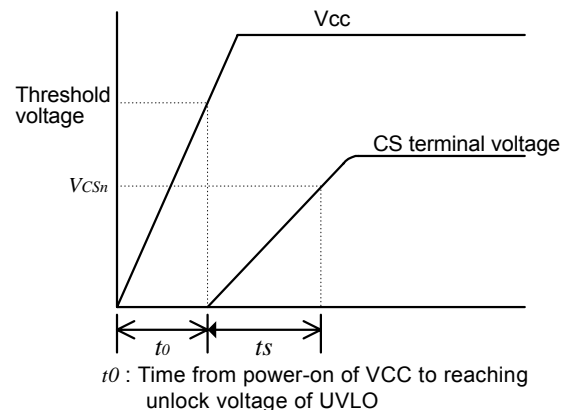


Fig.8



**(4)Setting the maximum output duty**

If you need to control the maximum output duty in the DC-DC converter circuit, you can control pulse width by connecting REG terminal to DT terminal divided with resistors R5 and R6, as described in Fig. 9. The output duty of the voltage of DT terminal in this case changes according to the operation frequency, as described in the chart of “DT terminal voltage vs. output duty cycle” characteristic curves. Set the output duty accordingly based on your required operation frequency. If the maximum output duty setting is not needed, be sure to connect DT terminal directly to REG terminal. In this case, the pulse width widens up to the output duty of 100%.

The voltage of DT terminal should be set in the range of 0.65V to 1.1V(typ.). There is a possibility of distortion of the output pulses if strong noises or the like are applied to DT terminal. When conducting pattern wiring, do it as close to each terminal of the IC as possible. Besides, it is strongly recommended to connect a capacitor CDT for a filter of noise prevention.

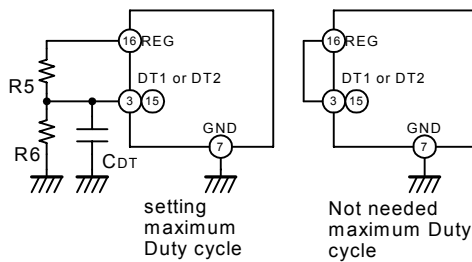


Fig.9

**(5)Pull-up/Pull-down resistor at the output section**

The power source of FA7703/04 to control the output section is supplied from the voltage of VREG, the voltage of this power source is accordingly not stationary below the UVLO voltage. On the other hand, OUT terminal becomes unsteady condition while Power supply voltage is below UVLO voltage. Be sure to connect a pull-up resistor/pull-down resistor according to Fig. 10. (See Fig. 10)

**(6)Restriction of external discrete components/Recommended operating conditions**

To achieve a stable operation of FA7703/04, the values of external discrete components connected to VCC, REF, and CS terminals of this IC should be within the range of recommended operating conditions. And also the voltage and the current applied to each terminal should be within the recommended operating conditions.

A Pch MOSFET is installed between VCC terminal and OUT1 terminal, and between VCC terminal and OUT2 terminal. Since the Pch MOSFET has a parasitic diode, if the voltage of OUT1 and OUT2 terminals becomes higher than the VCC terminal voltage, the current flows from each terminal to VCC terminal. Cautious care must be taken accordingly when designing.

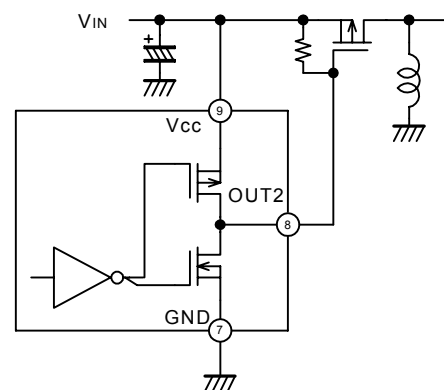
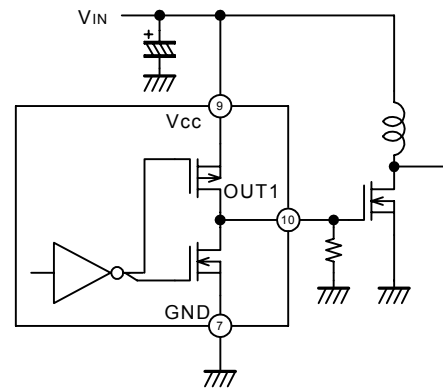


Fig.10



**(11)Setting of the output voltage of DC-DC converter**

**converter**

Figure 13 shows the ways to set each channel of the output voltage of DC-DC converter. The precision of output voltage based on FA7703/04's characteristics depends on the variation of the voltage of VB (±2%) and VREF (±1%), and also on offset voltage, and temperature characteristics.

selection Guide

FA7703	Ch1	Buck, Boost, Fly-back
	Ch2	Buck, Inverting (Pch driven)
FA7704	Ch1	Buck, Boost, Fly-back
	Ch2	Boost, Fly-back (Nch driven)

If using FA7703/04, and building:

In the case of a boost, a buck, or a fly-back circuit in ch1, the output voltage can be calculated with:

$$V_{out1} = \frac{R1 + R2}{R2} \times V_B$$

If using FA7703, and building:

A buck circuit in ch2, the output voltage can be calculated with:

$$V_{out2} = \frac{R3 + R4}{R3} \times V_{REF}$$

A inverting circuit in ch2, the output voltage can be calculated

with the following formula. (the output voltage is negative.)

$$V_{out2} = \frac{R3 + R4}{R3} \times V1 - \frac{R4}{R3} \times V_{REF}$$

,where  $V1 = \frac{R8}{R7 + R8} \times V_{REF}$

The ratio of resistance can be calculated with:

$$\frac{R3}{R4} = \frac{V_{REF} - V1}{V_{out2} + V1}$$

(Use the absolute value of Vout2 voltage)

If setting R7=R8, then,

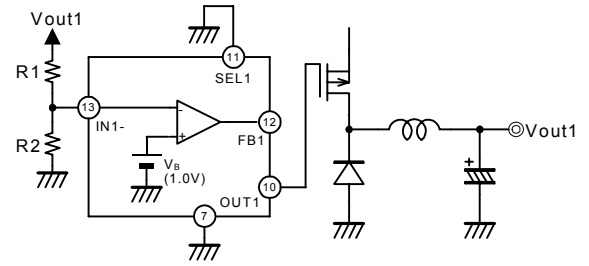
$$V_{out2} = V_{REF} \times \left( \frac{R3 - R4}{2R3} \right)$$

If using FA7704, and building:

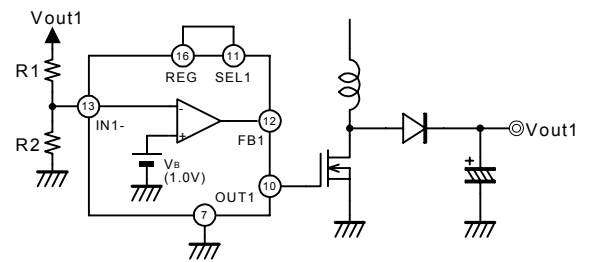
A boost, or fly-back circuit in ch2, the output voltage can be calculated with:

$$V_{out2} = \frac{R3 + R4}{R3} \times V_{REF}$$

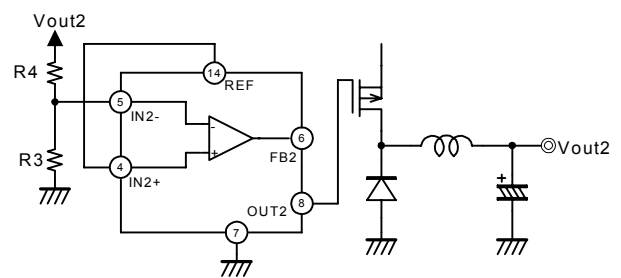
Ch1:Buck(FA7703/04)



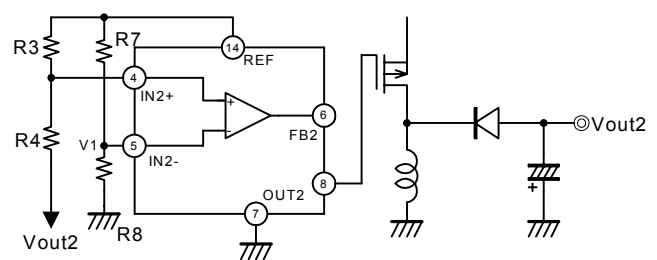
Ch1:Boost(FA7703/04)



Ch2:Buck(FA7703)



Ch2:Inverting(FA7703)



Ch2:Boost(FA7704)

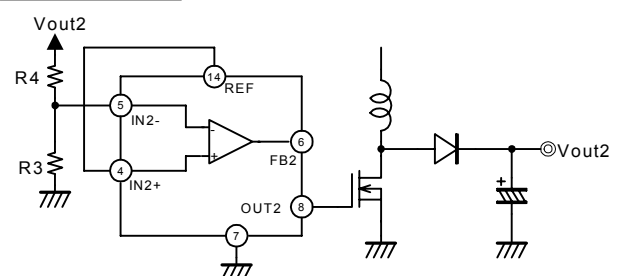


Fig.13

Please note that DO NOT leave SEL1 terminal open in operation, and be sure to connect it to GND or VREG terminal.

**(12) To protect FA7703/04 from application of negative voltage**

If rather large negative voltage is applied to any terminal of FA7703/04, then internal parasitic elements start operating, and they may cause malfunctions. Accordingly, the negative voltage, which is applied to each terminal of the ICs, must be kept above  $-0.3\text{V}$ .

In the case of OUT terminal, in particular, the oscillation of voltage occurring after MOSFET's turning off can be applied to OUT terminal through MOSFET's parasitic capacitance. As a result, there is a possibility that the negative voltage is applied to OUT terminal. If this negative voltage reaches  $-0.3\text{V}$  or below, connect an Schottky barrier diode between OUT terminal and GND terminal as shown in Fig. 14. The Schottky barrier diode's forward direction voltage clamps the voltage applied to OUT terminal. In this case, use the Schottky barrier diode with low voltage drop in forward direction. Other terminals should be kept above  $-0.3\text{V}$  also based on the same reasons.

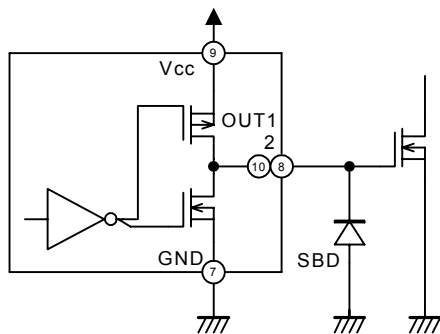


Fig.14

**(13) Forbidden use of external forcible latched operation for CS terminal**

If the external voltage of  $2.0\text{V}$  or more is forcibly applied to CS terminal in normal operation (clamped at  $1.2\text{V}$ ), the IC may be seriously damaged because the clamp circuit is not equipped with any resistor for limiter. Therefore, DO NOT apply external high voltage to CS terminal.

10. Application circuit

