

May 2000 Revised September 2003

NC7WB3306

TinyLogic® UHS 2-Bit Low Power Bus Switch

General Description

The NC7WB3306 is a 2-bit ultra high-speed CMOS FET bus switch with TTL-compatible active LOW control inputs. The low On Resistance of the switch allows inputs to be connected to outputs with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 2-bit switch with independent bus enable $\overline{(\text{OE})}$ controls. When $\overline{\text{OE}}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{\text{OE}}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports. Control inputs tolerate voltages up to 5.5V independent of V_{CC} .

Features

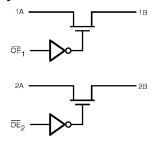
- Space saving US8 surface mount package
- MicroPak™ leadless package
- Typical 3Ω switch resistance at 5.0V V_{CC}
- Minimal propagation delay through the switch
- Power down high impedance input/output
- Zero bounce in flow through mode.
- TTL compatible active LOW control inputsControl inputs are overvoltage tolerant

Ordering Code:

		Product		
Order	Package	Code	Package Description	Supplied As
Number	Number	Top Mark		
NC7WB3306K8X	MAB08A	WB06	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WB3306L8X	MAC08A	U3	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

 $\label{eq:total_cond} \mbox{TinyLogio} \mbox{\mathbb{B} is a registered trademark of Fairchild Semiconductor Corporation.} \\ \mbox{MicroPak}^{\mbox{\mathbb{M}}} \mbox{\mathbb{M} is a trademark of Fairchild Semiconductor Corporation.} \\$

Logic Symbol



Pin Descriptions

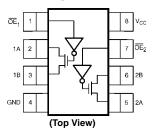
Pin Name	Description
Α	Bus A
В	Bus B
ŌĒ	Bus Enable Input

Function Table

Bus Enable Input OE	Function
L	B Connected to A
Н	Disconnected

H = HIGH Logic Level L = LOW Logic Level

Connection Diagrams



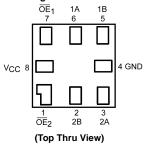
Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) -0.5V to +7.0V DC Switch Voltage (VS) -0.5V to +7.0V DC Output Voltage (V_{IN}) (Note 2) -0.5V to +7.0V

DC Input Diode Current

 $\begin{array}{ll} \text{(I}_{\text{IK}}\text{) V}_{\text{IN}} < 0\text{V} & -50\text{ mA} \\ \text{DC Output (I}_{\text{OUT}}\text{) Current} & 128\text{ mA} \end{array}$

DC V_{CC} or Ground Current (I_{CC}/GND)

 $\label{eq:Storage Temperature Range Temperature Range Temperature Under Bias Temperature$

Lead Temperature (T_L)

(Soldering, 10 seconds) $+260^{\circ}$ C Power Dissipation (P_D) @ +85°C 250 mW

Recommended Operating Conditions (Note 3)

 $\begin{array}{ll} \mbox{Supply Operating (V}_{\mbox{CC}}) & \mbox{4.0V to 5.5V} \\ \mbox{Control Input Voltage (V}_{\mbox{IN}}) & \mbox{0V to 5.5V} \end{array}$

Input Rise and Fall Time (t_r, t_f)

 Control Input
 0 ns/V to 5 ns/V

 Switch I/O
 0 ns/V to DC

Thermal Resistance (θ_{JA}) 250°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused logic inputs must be held HIGH or LOW. They may not float

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		°C	Units	Conditions	
- Cymbol	i didilictor	(V)	Min	Тур	Max	011110		
V _{IK}	Clamp Diode Voltage	4.5			-1.2	V	I _{IN} = -18 mA	
V _{IH}	HIGH Level Input Voltage	4.0 to 5.5	2.0			V		
V _{IL}	LOW Level Input Voltage	4.0 to 5.5			8.0	V		
V _{OH}	HIGH Level Output Voltage	4.5 to 5.5		see Figure 3		V	$V_{IN} = V_{CC}$	
I _{IN}	Input Leakage Current	5.5			±1.0	μΑ	0 ≤ V _{IN} ≤ 5.5V	
I _{OFF}	Switch OFF Leakage Current	5.5			±1.0	μΑ	0 ≤ A, B, ≤ V _{CC}	
R _{ON}	Switch On Resistance	4.5		3	7		V _{IN} = 0V, I _{IN} = 64 mA	
	(Note 4)	4.5		3	7	Ω	V _{IN} = 0V, I _{IN} = 30 mA	
		4.5		6	15	1 32	V _{IN} = 2.4V, I _{IN} = 15 mA	
		4.0		10	20		$V_{IN} = 2.4V$, $I_{IN} = 15 \text{ mA}$	
I _{CC}	Quiescent Supply Current	5.5			3	μΑ	$V_{IN} = V_{CC}$ or GND,	
							I _{OUT} = 0	
ΔI_{CC}	Increase in I _{CC} per Input	5.5		1	2.5	mA	$V_{IN} = 3.4V, I_{O} = 0,$	
	(Note 5)						Control Input Only	

±100 mA

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Per TTL driven input ($V_{IN} = 3.4V$, control input only). A and B pins do not contribute to I_{CC} .

AC Electrical Characteristics

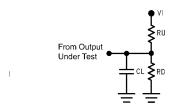
Symbol	Symbol Parameter		$T_{A} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} \qquad C_{L} = 50 \text{ pF, RU} = \text{RD} = 500\Omega$		Units	Conditions	Figure	
		(V)	Min	Тур	Max			Number
t _{PHL} ,	Propagation Delay Bus-to-Bus	4.0 to 5.5			0.25	ns	V _I = OPEN	Figures
t _{PLH}	(Note 6)							1, 2
t _{PZL} ,	Output Enable Time	4.5 to 5.5	0.8	2.5	4.2	ns	$V_I = 7V$ for t_{PZL}	Figures
t _{PZH}		4.0	0.8	3.0	4.6	115	$V_I = 0V$ for t_{PZH}	1, 2
t _{PLZ} ,	Output Disable Time	4.5 to 5.5	0.8	3.1	4.8		$V_I = 7V$ for t_{PLZ}	Figures
t _{PHZ}		4.0	0.8	2.9	4.4	115	$V_I = 0V$ for t_{PHZ}	1, 2

Note 6: This parameter is guaranteed. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance). The specified limit is calculated on this basis.

Capacitance

Symbol	Parameter	Тур	Typ Max Units		Conditions
C _{IN}	Control Pin Input Capacitance	2.5		pF	$V_{CC} = 0V$
C _{I/O} (OFF)	Port OFF Capacitance	6		pF	$V_{CC} = 5.0V = \overline{OE}$
C _{I/O} (ON)	Switch ON Capacitance	12		pF	$V_{CC} = 5.0V, \overline{OE} = 0V$

AC Loading and Waveforms



Input driven by 50 Ω source terminated in 50 Ω . C_L includes load and stray capacitance. Input PRR = 1.0 MHz t_w = 500 ns.

FIGURE 1. AC Test Circuit

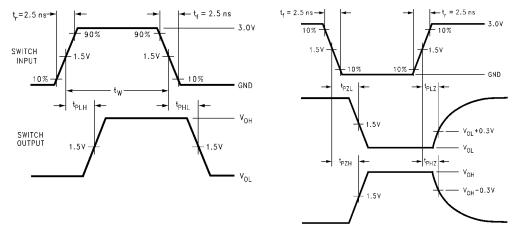
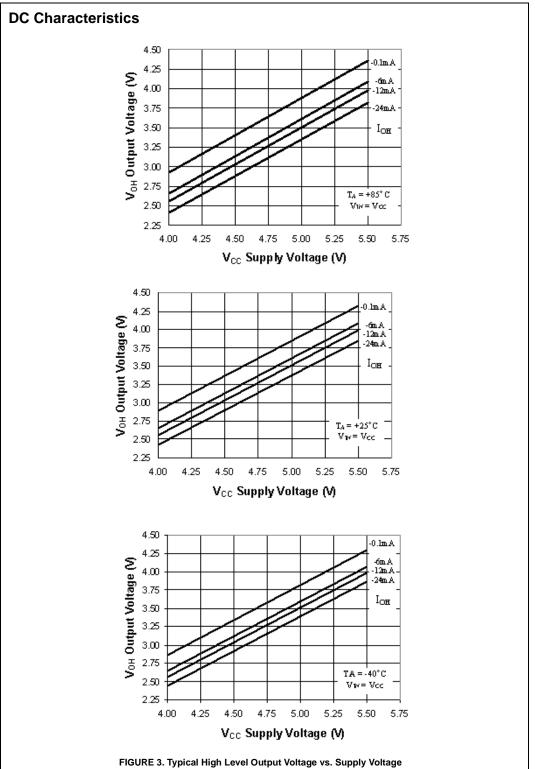


FIGURE 2. AC Waveforms

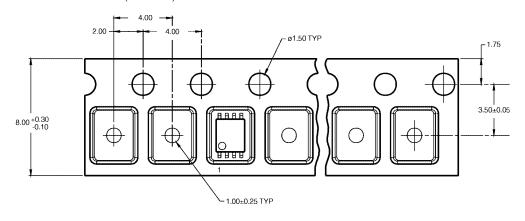


Tape and Reel Specification

TAPE FORMAT for US8

TALL FORMATION	700				
Package	Tape	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
K8X	Carrier	250	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

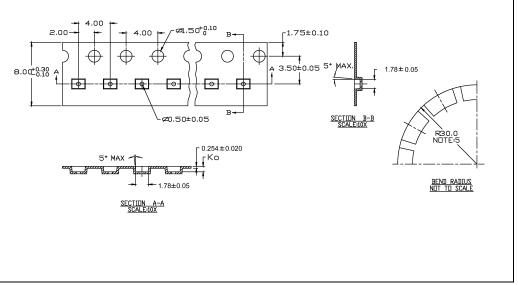
TAPE DIMENSIONS inches (millimeters)



TAPE FORMAT for MicroPak

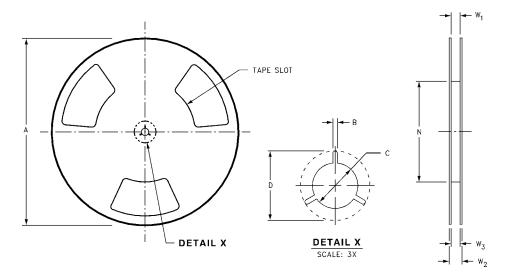
Package	Package Tape		Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
L8X	Carrier	250	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

TAPE DIMENSIONS inches (millimeters)



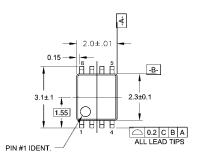
Tape and Reel Specification (Continued)

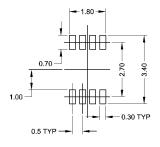
REEL DIMENSIONS inches (millimeters)



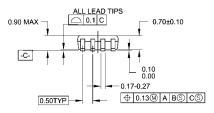
Tape Size	Α	В	С	D	N	W1	W2	W3
0	7.0	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1 + 0.078/-0.039
8 mm	(177.8)	(1.50)	(13.00)	(20.20)	(55.00)	(8.40 + 1.50/-0.00)	(14.40)	(W1 + 2.00/-1.00)

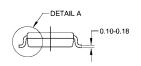
Physical Dimensions inches (millimeters) unless otherwise noted

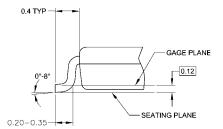




LAND PATTERN RECOMMENDATION







NOTES:

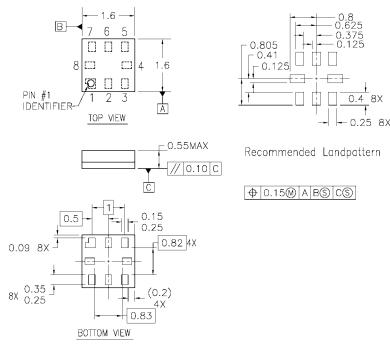
- CONFORMS TO JEDEC REGISTRATION MO-187
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

DETAIL A

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. PACKAGE REGISTRATION WITH JEDEC IS ANTICIPATED
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y.14M-1994

MAC08AREVB

8-Lead MicroPak, 1.6 mm Wide Package Number MAC08A

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