FAIRCHILD SEMICONDUCTOR™

April 2001
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FSTU16245
16-Bit Bus Switch with −2V Undershoot Protection

General Description

The Fairchild Switch FSTU16245 provides 16-bits of high-speed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 16-bit switch. There are two 8-bit switches with separate output enable inputs. When $\overline{OE}$ is LOW, the switch is ON and Port a is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OFF and a high impedance state exists between the A and B Ports. The A and B Ports are protected against undershoot to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHC™) senses undershoot at the I/O and responds by preventing voltage differentials from developing and turning the switch on. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

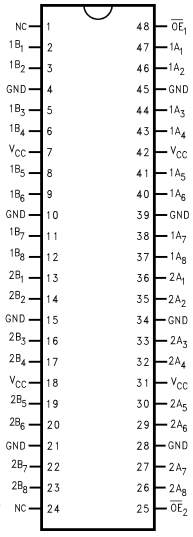
- Undershoot hardened to −2V (A and B Ports)
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- See Application Note AN-5008 for details

Ordering Code:

Order Number	Package Number	Package Description
FSTU16245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$1A_n$, $2A_n$, $3A_n$, $4A_n$	Bus A
$1B_n$, $2B_n$, $3B_n$, $4B_n$	Bus B
NC	No Internal Connection

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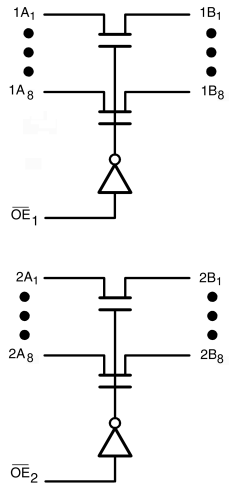
Logic Diagram



Truth Table

Inputs	Outputs
$\overline{OE}_x$	A, B
L	A Port = B Port
H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−2.0V to +7.0V
DC Input Voltage (V_{IN}) (Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output Current (I_{OUT})	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Min	Typ (Note 5)	Max	Units	Conditions
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64 mA
	(Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30 mA
		4.5		8	14	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA $\overline{OE}$ = 5.5V

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, RU = RD = 500Ω				Units	Conditions	Figure Number
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus-to-Bus (Note 7)		0.25		0.25	ns	V_I = OPEN	Figures 2, 3
t_{PZH}, t_{PZL}	Output Enable Time	1.0	6.5		6.9	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figures 2, 3
t_{PHZ}, t_{PLZ}	Output Disable Time	1.0	6.1		6.5	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figures 2, 3

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V, V_{IN} = 0V
$C_{I/O}$	Input/Output Capacitance "OFF State"	6		pF	V_{CC}, $\overline{OE}$ = 5.0V, V_{IN} = 0V

Note 8: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	V_{OH} - 0.3		V	Figure 1

Note 9: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

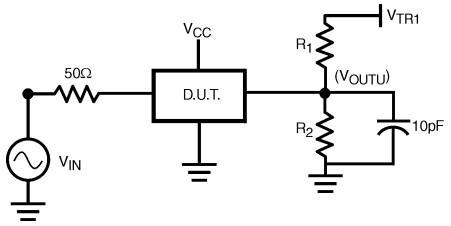
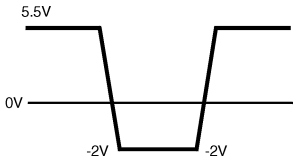


FIGURE 1.

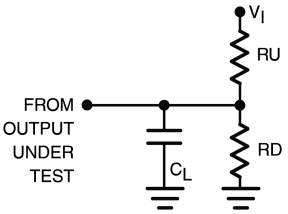
Device Test Conditions

Parameter	Value	Units
V_{IN}	see Waveform	V
$R_1 = R_2$	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 2. AC Test Circuit

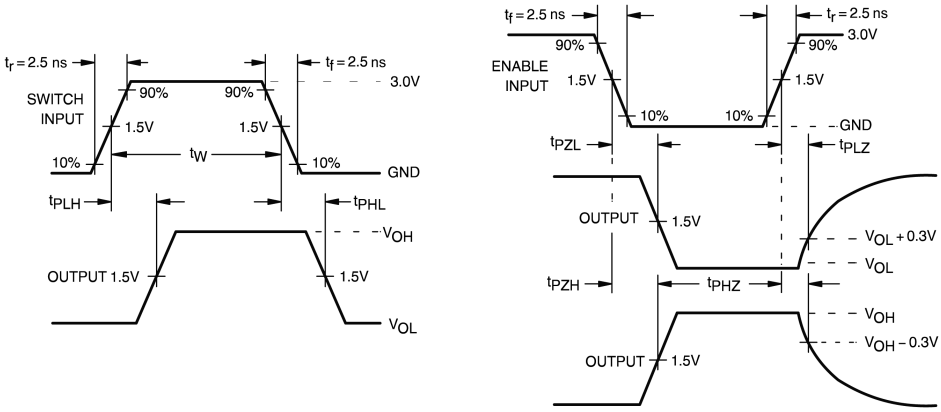
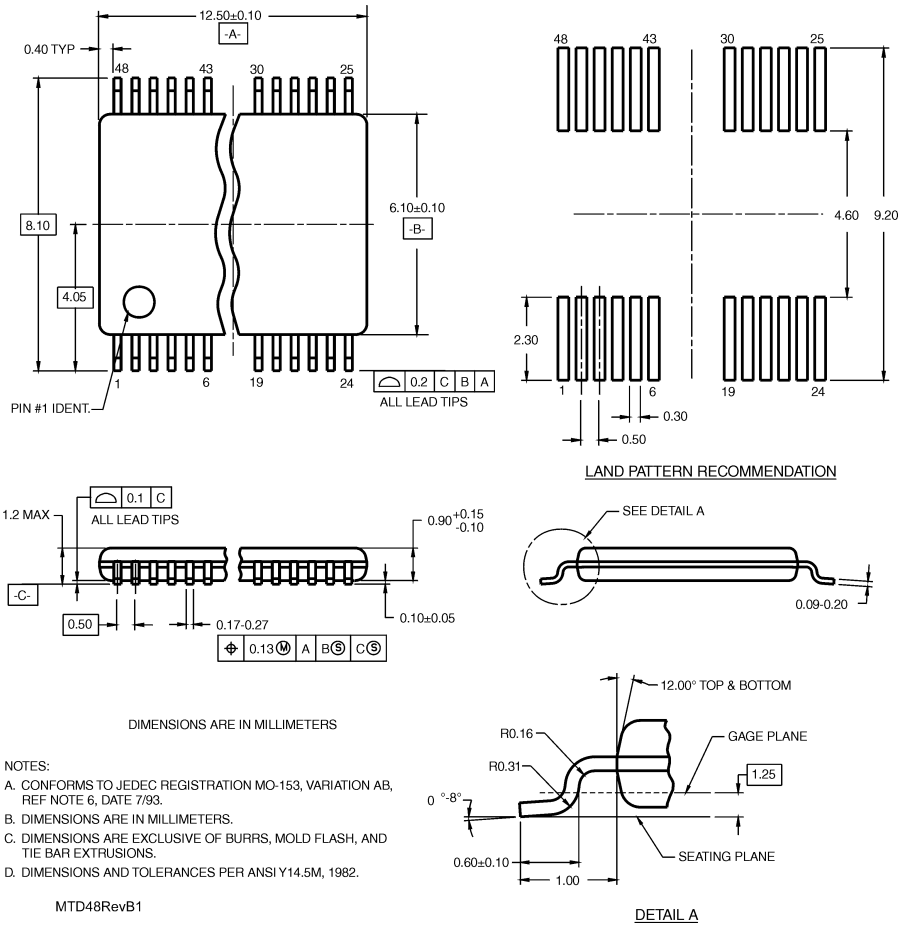


FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

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