

April 1984 Revised February 2000

DM74ALS533 Octal D-Type Transparent Latch with 3-STATE Outputs

General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the DM74ALS533 are transparent D-type latches. While the enable (G) is HIGH the Q outputs will follow the complement of the data (D) inputs. When the enable is taken LOW the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Features

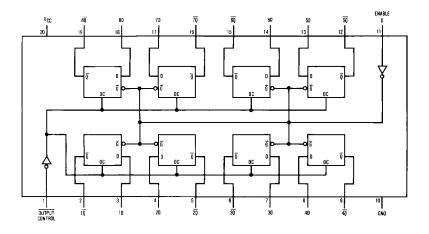
- Switching specifications at 50 pF
- \blacksquare Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS533WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74ALS533N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

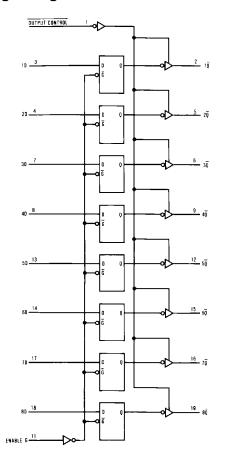


Function Table

Output	Enable	D	Output
Control	G		Q
L	Н	Н	L
L	Н	L	Н
L	L	X	\overline{Q}_0
Н	Х	Χ	Z
	Control L L	Control G L H L H L L	Control G L H H L L X

- L = LOW State
 H = HIGH State
 X = Don't Care
 Z = High Impedance State
- $\overline{\overline{Q}}_0 = \text{Previous Condition of } \overline{\overline{Q}}$

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage 7V Input Voltage 7V Voltage Applied to Disabled Output 5.5V Operating Free Air Temperature Range $0^{\circ}\text{C to } + 70^{\circ}\text{C}$

Storage Temperature Range -65°C to +150°C

Typical θ_{JA}

 N Package
 57.0°C/W

 M Package
 76.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	
V _{CC}	Supply Voltage	4.5	5	5.5	V	
V _{IH}	HIGH Level Input Voltage	2			V	
V _{IL}	LOW Level Input Voltage			0.8	V	
I _{OH}	HIGH Level Output Current			-2.6	mA	
I _{OL}	LOW Level Output Current			24	mA	
t _W	Width of Enable Pulse, HIGH or LOW	15			ns	
t _{su}	Data Setup Time (Note 2)	15↓			ns	
t _H	Data Hold Time (Note 2)	7↓			ns	
T _A	Free Air Operating Temperature	0		70	°C	

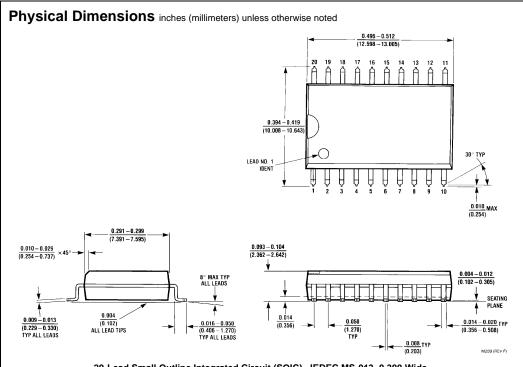
Note 2: The (\downarrow) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

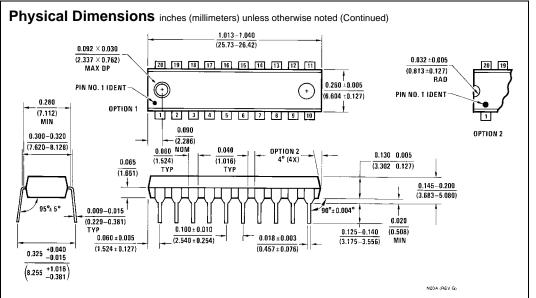
over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Symbol	Parameter	Conditions		Min	Тур	Max	Units
V _{IK}	Input Clamp Voltage	V _{CC} = 4.5V, I _I = -18 mA				-1.5	V
V _{OH}	HIGH Level	V _{CC} = 4.5V	$I_{OH} = -2.6 \text{ mA}$	2.4	3.3		V
	Output Voltage	V _{CC} = 4.5V to 5.5V	$I_{OH} = -400 \mu A$	V _{CC} - 2			V
V _{OL}	LOW Level	V _{CC} = 4.5V	I _{OL} = 12 mA		0.25	0.4	V
	Output Voltage		$I_{OL} = 24 \text{ mA}$		0.35	0.5	V
I _I	Input Current @ Maximum	V 55V V 7V				0.1	mA
	Input Voltage	$V_{CC} = 5.5V, V_{IH} = 7V$					
I _{IH}	HIGH Level Input Current	$V_{CC} = 5.5V, V_{IH} = 2.7V$			20	μΑ	
I _{IL}	LOW Level Input Current	$V_{CC} = 5.5V, V_{IL} = 0.4V$				-0.1	mA
Io	Output Drive Current	V _{CC} = 5.5V	$V_0 = 2.25V$	-30		-112	mA
I _{OZH}	OFF-State Output Current	V _{CC} = 5.5V			20	μА	
	HIGH Level Voltage Applied	$V_O = 2.7V$					
I _{OZL}	OFF-State Output Current	V _{CC} = 5.5V				-20	μА
	LOW Level Voltage Applied	$V_0 = 0.4V$					
I _{CC}	Supply Current	V _{CC} = 5.5V	Outputs HIGH		10	17	mA
		Outputs OPEN	Outputs LOW		17	26	mA
			Outputs Disabled		18.5	28	mA

Switching Characteristics over recommended operating free air temperature range Symbol Parameter Conditions From То Min Max Units V_{CC} = 4.5V to 5.5V Propagation Delay Time Data Any $\overline{\mathbf{Q}}$ 19 ns LOW-to-HIGH Level Output $R_L = 500\Omega$ Propagation Delay Time $C_L = 50 pF$ t_{PHL} Any $\overline{\mathbf{Q}}$ 4 13 Data ns HIGH-to-LOW Level Output Propagation Delay Time t_{PLH} Enable Any $\overline{\mathbf{Q}}$ 5 23 ns LOW-to-HIGH Level Output Propagation Delay Time t_{PHL} Enable Any $\overline{\mathbf{Q}}$ 18 ns HIGH-to-LOW Level Output t_{PZH} Output Enable Time Output Any Q ns to HIGH Level Output Control Output Enable Time Output t_{PZL} Any Q ns to LOW Level Output Control Output Disable Time Output t_{PHZ} Any $\overline{\mathsf{Q}}$ ns from HIGH Level Output Control Output Disable Time Output t_{PLZ} Any $\overline{\mathbf{Q}}$ 16 from LOW Level Output Control



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20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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