FAIRCHILD SEMICONDUCTOR™

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74FR16245
16-Bit Transceiver with 3-STATE Outputs

General Description

The 74FR16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B Ports. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The transmit/receive ($T/\overline{R}_n$) inputs determine the direction of data flow through the transceiver. The output enable ($\overline{OE}_n$) inputs disable both A and B Ports by placing them in an high impedance state.

Features

- Non-inverting buffers
- Bidirectional data paths
- A and B output sink capability of 64 mA, source capability of 15 mA
- Separate control pins for each byte
- Guaranteed pin-to-pin skew
- Low 3-STATE I_{IL}
- 16-Bit version of the 74F245 or 74F645

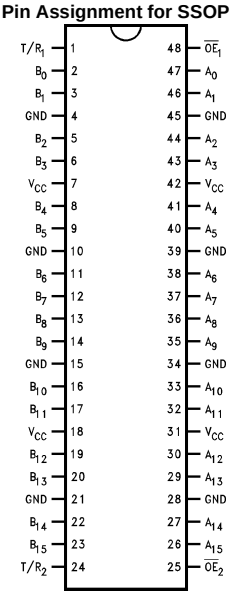
Ordering Code:

Order Number	Package Number	Package Description
74FR16245QC	V44A	44-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.650 Square
74FR16245SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

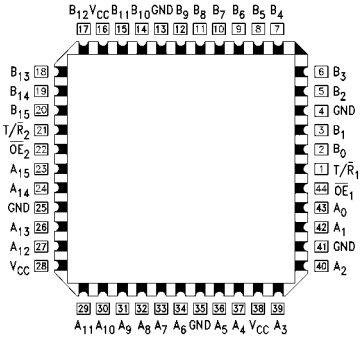
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

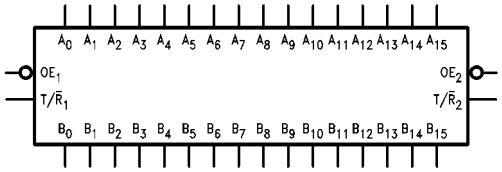
Pin Assignment for SSOP



Pin Assignment for PLCC



Logic Symbol



Pin Descriptions

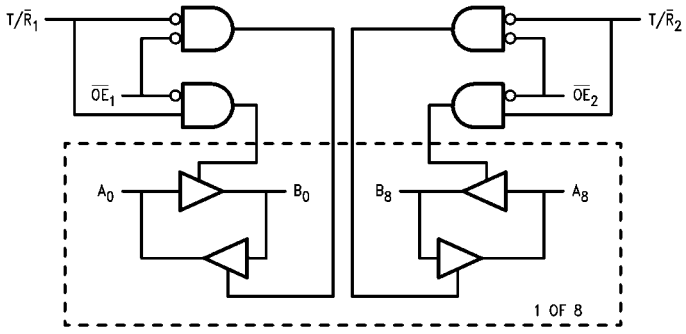
Pin Names	Description
$\overline{OE}_n$	Output Enable Input
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	A Bus Inputs/3-STATE Outputs
B_0–B_{15}	B Bus Inputs/3-STATE Outputs

Truth Table

Inputs				Output Operating Mode	
Byte1 (0:7)		Byte2 (8:15)			
$\overline{OE}_1$	$T/\overline{R}_1$	$\overline{OE}_2$	$T/\overline{R}_2$	Byte1 (0:7)	Byte2 (8:15)
L	L	H	X	Bus B Data to A	High Z State
L	H	H	X	Bus A Data to B	High Z State
H	X	L	L	High Z State	Bus B Data to A
H	X	L	H	High Z State	Bus A Data to B
L	L	L	L	Bus B Data to A	Bus B Data to A
L	H	L	H	Bus A Data to B	Bus A Data to B
H	X	H	X	High Z State	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	–0.5V to V_{CC}
3-STATE Output	–0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0	2.8 2.44		V	Min	I_{OH} = – 3 mA I_{OH} = – 15 mA (A_n, B_n)
V_{OL}	Output LOW Voltage		0.45	0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current			5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Break-Down Test			7.0	µA	Max	V_{IN} = 7.0V ($\overline{OE}_n$, T/$\overline{R}_n$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			0.1	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			–150 –100	µA µA	Max Max	V_{IN} = 0.5V (T/$\overline{R}_n$, A_n, B_n) V_{IN} = 0.5V ($\overline{OE}_n$)
I_{OS}	Output Short-Circuit Current	–100		–225	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{IH} + I_{OZH}	Output Leakage Current		0	25	µA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current		–20	–150	µA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Circuit Leakage Current			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	µA	0.0	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current		70	105	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		127	165	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		71	105	mA	Max	V_O = HIGH Z
C_{IN}	Input Capacitance		8.0		pF	5.0	$\overline{OE}$, T/$\overline{R}$
			17.0		pF	5.0	A_n, B_n

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Unit
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.3	2.7	4.3	1.3	4.3	ns
t_{PHL}	A_n to B_n or B_n to A_n	1.3	2.2	4.3	1.3	4.3	
t_{PZH}	Output Enable Time	3.9	6.9	13.9	3.9	13.9	ns
t_{PZL}		3.9	9.7	13.9	3.9	13.9	
t_{PHZ}	Output Disable Time	1.8	3.9	6.3	1.8	6.3	ns
t_{PLZ}		1.8	4.4	6.3	1.8	6.3	

Extended AC Characteristics

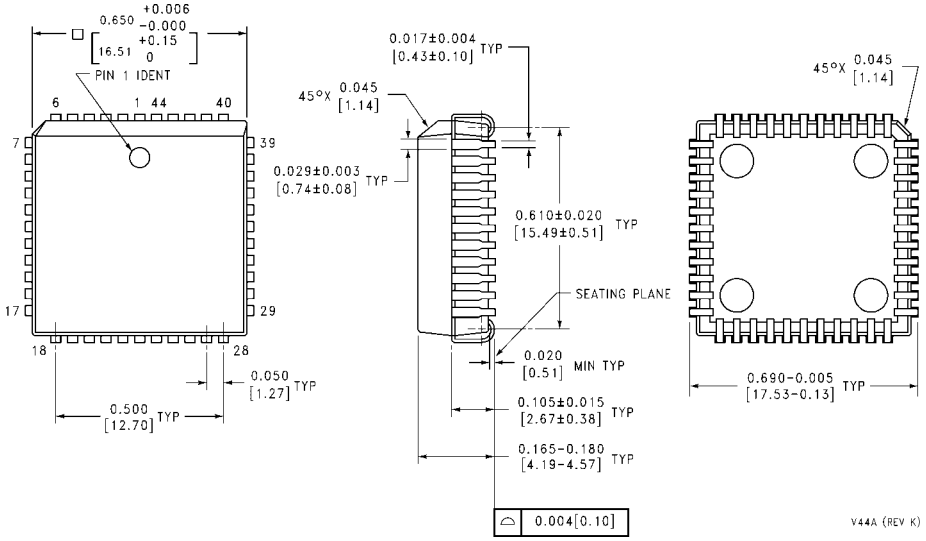
Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF, 16 Outputs Switching (Note 4)		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 250$ pF (Note 5)		Unit
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.3	5.8	3.2	8.2	ns
t_{PHL}	A_n to B_n or B_n to A_n	1.3	5.8	3.2	8.2	
t_{PZH}	Output Enable Time	3.9	14.6			ns
t_{PZL}		3.9	14.6			
t_{PHZ}	Output Disable Time	1.8	6.3			ns
t_{PLZ}		1.8	6.3			
t_{OSHL} (Note 3)	Pin-to-Pin Skew for HL Transitions		1.2			ns
t_{OSLH} (Note 3)	Pin-to-Pin Skew for LH Transitions		2.2			ns
t_{OST} (Note 3)	Pin-to-Pin Skew for HL/LH Transitions		2.5			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}) LOW-to-HIGH (t_{OSLH}), or HIGH-to-LOW and/or LOW-to-HIGH (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Note 4: This specification is guaranteed but not tested The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

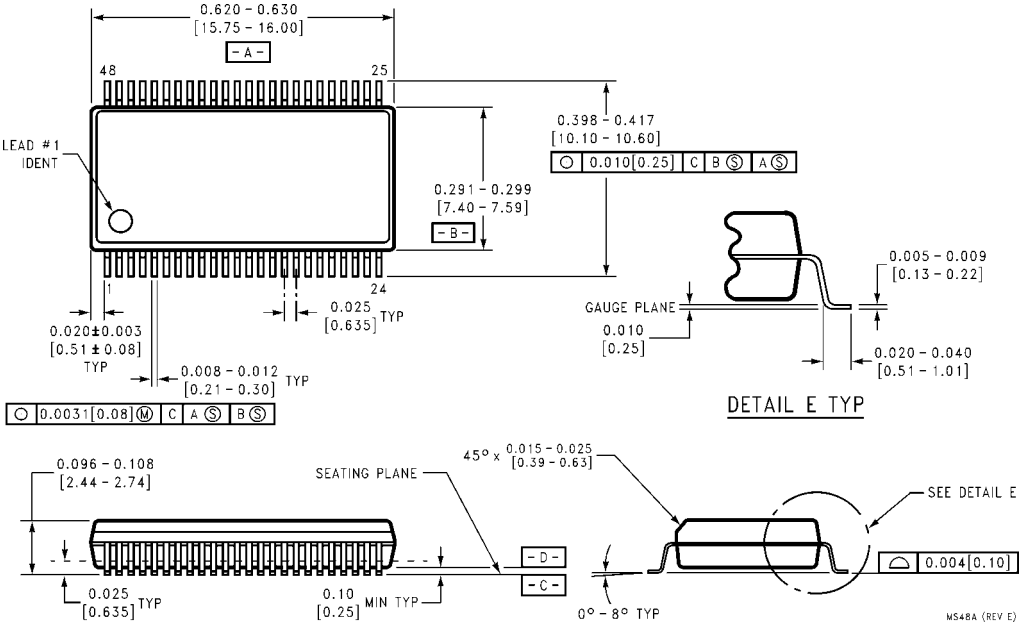
Note 5: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Physical Dimensions inches (millimeters) unless otherwise noted



44-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.650 Square
Package Number V44A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS48A

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