FAIRCHILD SEMICONDUCTOR™

April 1988
Revised August 1999

74F827 • 74F828
10-Bit Buffers/Line Drivers

General Description

The 74F827 and 74F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 74F828 is an inverting version of the 74F827.

Features

- 3-STATE output
- 74F828 is inverting

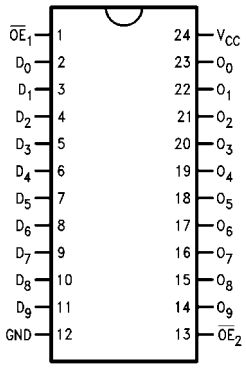
Ordering Code:

Order Number	Package Number	Package Description
74F827SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F827SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
74F828SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F828SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

74F827



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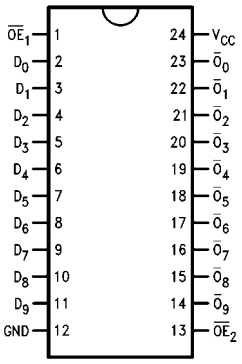
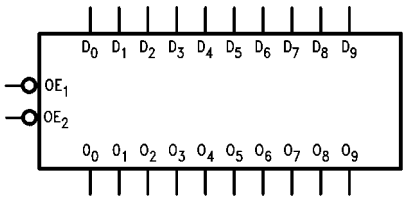


Logic Symbols

74F827



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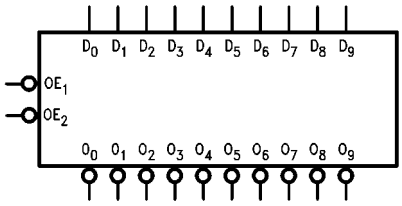
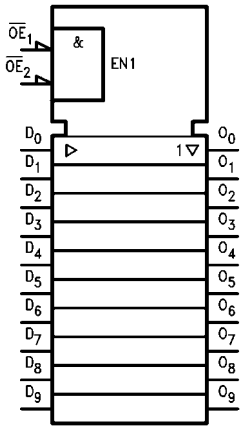
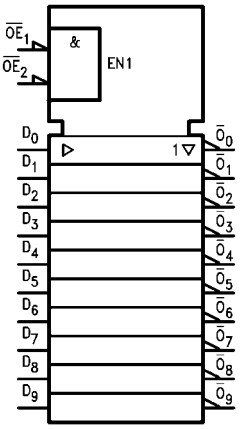


IEEE/IEC
74F827



IEEE/IEC
74F828



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input	1.0/1.0	20 µA/–0.6 mA
D_0–D_7	Data Inputs	1.0/1.0	20 µA/–0.6 mA
O_0–O_7	Data Outputs, 3-STATE	600/106.6 (80)	–12 mA/64 mA (48 mA)

Functional Description

The 74F827 and 74F828 are line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have 3-STATE outputs controlled by the Output Enable ($\overline{OE}$) pins. The outputs can sink 64 mA and source 15 mA. Input clamp diodes limit high-speed termination effects.

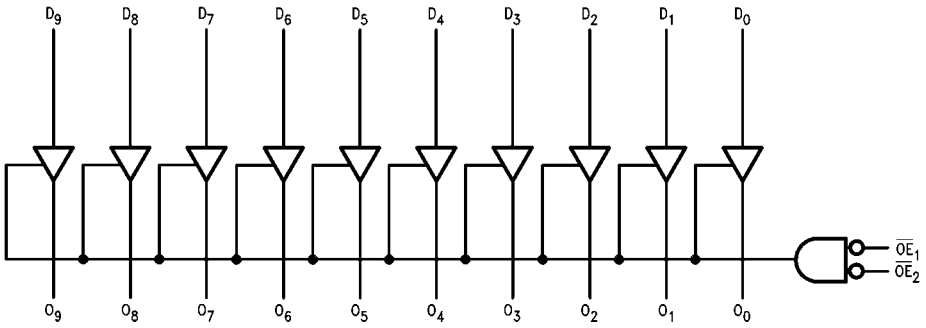
Function Table

Inputs		Outputs		Function
$\overline{OE}$	D_n	O_n		
		74F827	74F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

H = HIGH Voltage level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial

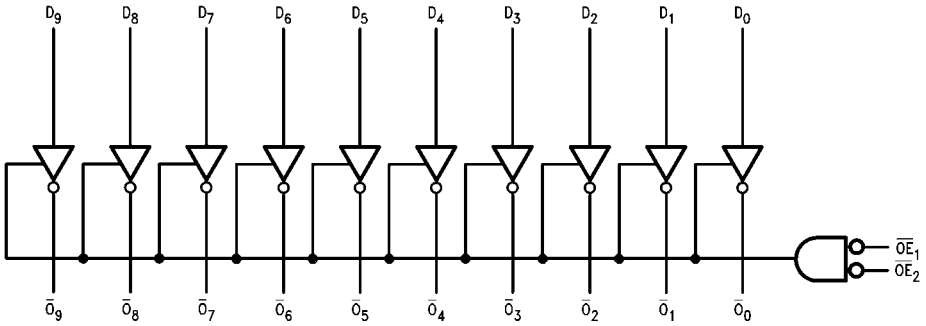
Logic Diagrams

74F827



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

74F828



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

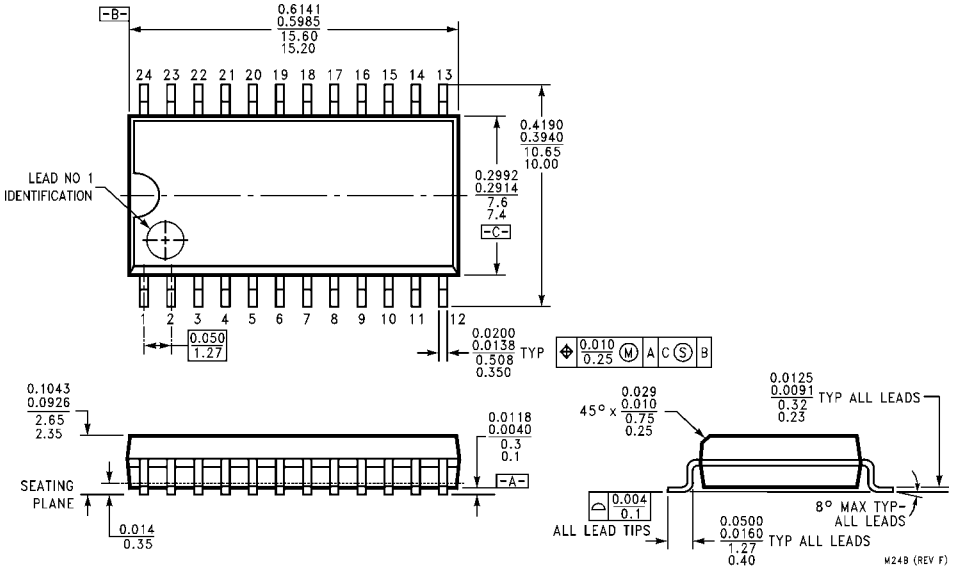
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.4			V	Min	I_{OH} = −3 mA
		10% V_{CC}	2.0					I_{OH} = −15 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current (74F827)			30	45	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current (74F827)			60	90	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current (74F827)			40	60	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current (74F828)			14	20	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current (74F828)			56	85	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current (74F828)			35	50	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

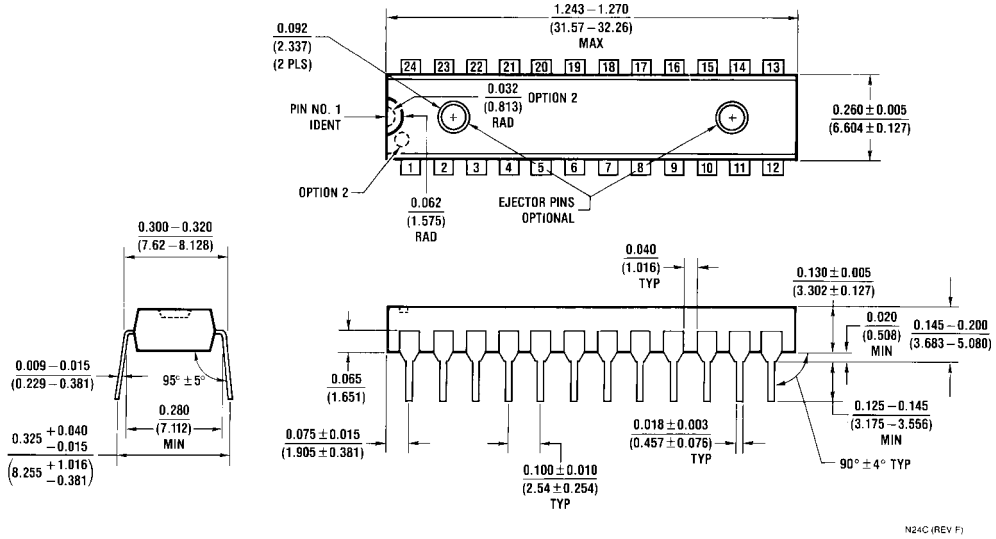
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0	3.0	5.5	1.0	7.5	1.0	6.5	ns
t_{PHL}	Data to Output (74F827)	1.5	3.3	5.5	1.5	7.0	1.5	6.0	
t_{PLH}	Propagation Delay	1.0	3.0	5.0			1.0	5.5	ns
t_{PHL}	Data to Output (74F828)	1.0	2.0	4.0			1.0	4.0	
t_{PZH}	Output Enable Time	3.0	5.7	9.0	2.5	10.0	2.5	9.5	ns
t_{PZL}	$\overline{OE}$ to O_n	3.5	6.8	11.5	3.0	12.5	3.0	12.0	
t_{PHZ}	Output Disable Time	1.5	3.3	8.0	1.5	9.0	1.5	8.5	ns
t_{PLZ}	$\overline{OE}$ to O_n	1.0	3.5	8.0	1.0	9.0	1.0	8.5	

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C