FAIRCHILD SEMICONDUCTOR™

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74ALVC16835
Low Voltage 18-Bit Universal Bus Driver with 3.6V Tolerant Inputs and Outputs

General Description

The ALVC16835 low voltage 18-bit universal bus driver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable ($\overline{OE}$), latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs (I_n) to Ouputs (O_n) on a Positive Edge Transition of the Clock. When $\overline{OE}$ is LOW, the output data is enabled. When $\overline{OE}$ is HIGH the output port is in a high impedance state.

The 74ALVC16835 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74ALVC16835 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- Compatible with PC100 DIMM module specifications
- 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (CLK to O_n)
  - 4.5 ns max for 3.0V to 3.6V V_{CC}
  - 5.5 ns max for 2.3V to 2.7V V_{CC}
  - 9.2 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

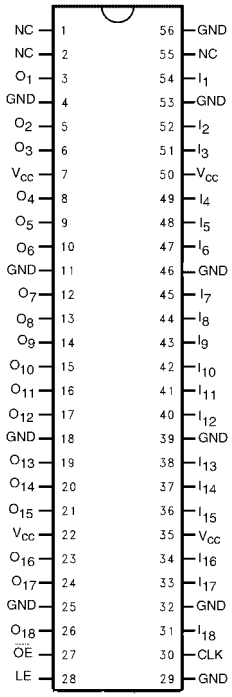
Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} (OE to GND) through a pulldown resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74ALVC16835MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input
CLK	Clock Input
I_1 - I_{18}	Data Inputs
O_1 - O_{18}	3-STATE Outputs
NC	No Connect

Truth Table

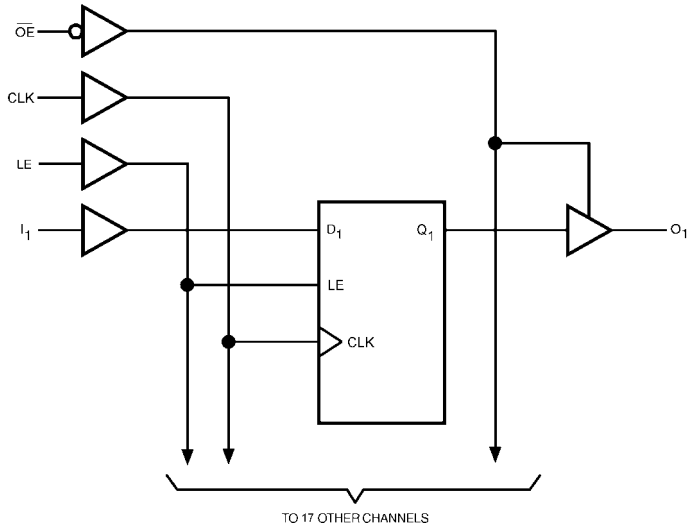
Inputs				Outputs
$\overline{OE}$	LE	CLK	I_n	O_n
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	O_0 (Note 2)
L	L	L	X	O_0 (Note 3)

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Clock Transition

Note 2: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

Note 3: Output level before the indicated steady-state input conditions were established.

Logic Diagram



Absolute Maximum Ratings (Note 4)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 5)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 6)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed, limited to 4.6V.

Note 6: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V_{CC}		V
			2.3 - 2.7	1.7		
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V_{CC}	V
			2.3 - 2.7		0.7	
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	1.65 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −4 mA	1.65	1.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.7		
			2.7	2.2		
			3.0	2.4		
		I_{OH} = −24 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 3.6		0.2	V
		I_{OL} = 4 mA	1.65		0.45	
		I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 12 mA	2.3		0.7	
			2.7		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V	3.6		±10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6		40	µA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	3 - 3.6		750	µA

AC Electrical Characteristics

Symbol	Parameter			$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
				$C_L = 50$ pF				$C_L = 30$ pF				
				$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
				Min	Max	Min	Max	Min	Max	Min	Max	
f_{CLOCK}	Clock Frequency				150		150		150		100	MHz
t_W	Pulse Width	LE High		3.3		3.3		3.3		4.0		ns
		CLK High or Low		3.3		3.3		3.3		4.0		
t_S	Setup Time	Data Before CLK ↑		1.7		2.1		2.2		2.5		ns
		Data Before LE ↓	CLK High	1.5		1.6		1.9				
			CLK Low	1.0		1.1		1.3				
t_H	Hold Time	Data After CLK ↑		0.7		0.6		0.6		1.0		ns
		Data After LE ↓	CLK High or Low	1.4		1.7		1.4				
f_{MAX}	Maximum Clock Frequency			150		150		150		100		MHz
t_{PHL}, t_{PLH}	Propagation Delay		I to O	1	3.6		4.2	1.0	4.2	1.5	8.4	ns
			LE to O	1.3	4.2		4.9	1.3	5.0	1.5	9.8	
			CLK to O	1.4	4.5		5.2	1.4	5.5	2	9.2	
t_{PZL}, t_{PZH}	Output Enable Time			1.1	4.6		5.6	1.4	5.5	1.5	9.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time			1.3	3.9		4.3	1.0	4.5	1.5	7.6	ns

AC Electrical Characteristics Over Load (Note 7)

Symbol	Parameter	$R_L = 500\Omega$, $V_{CC} = 3.3 \pm 0.15V$				Units
		$T_A = -0°C$ to $+85°C$		$T_A = -0°C$ to $+65°C$		
		$C_L = 0$ pF		$C_L = 50$ pF		
		Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus	0.9	2.0	1.0	4.0	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Bus	1.5	2.9	1.7	4.5	ns

Note 7: This parameter is guaranteed by characterization but not tested.

Capacitance

Symbol	Parameter		Conditions	$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance	Control	$V_I = 0V$ or V_{CC}	3.3	3	pF
		Data	$V_I = 0V$ or V_{CC}	3.3	6	
C_{OUT}	Output Capacitance		$V_I = 0V$ or V_{CC}	3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, $C_L = 0$ pF	3.3	31	pF
				2.5	26	
		Outputs Disabled	f = 10 MHz, $C_L = 0$ pF	3.3	14	
				2.5	12	

I_{OUT} - V_{OUT} Characteristics

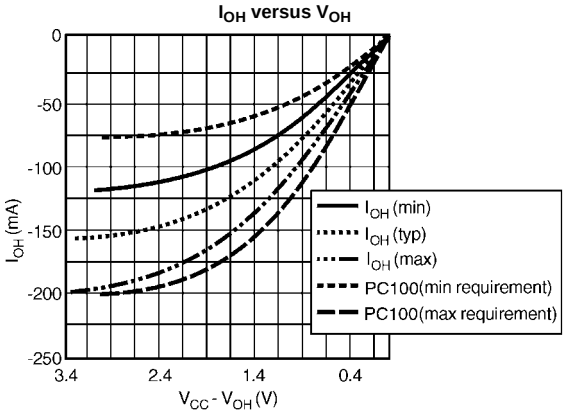


FIGURE 1. Characteristics for Output - Pull Up Driver

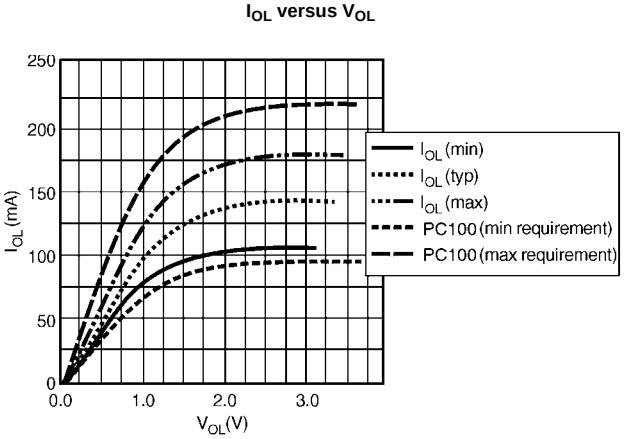


FIGURE 2. Characteristics for Output - Pull Down Driver

AC Loading and Waveforms

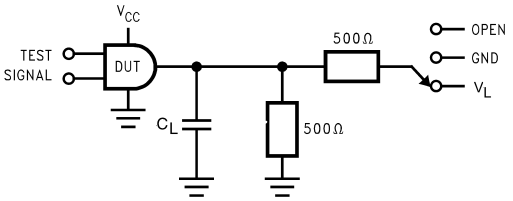


FIGURE 3. AC Test Circuit

TABLE 1.

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: f = 1MHz; $t_r = t_f$ = 2ns; Z_0 = 50Ω)

Symbol	V_{CC}			
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**	**1.8 ± 0.15V**
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V
V_L	6V	6V	V_{CC}/*2	V_{CC}/*2

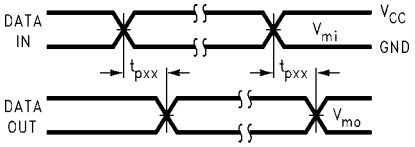


FIGURE 4. Waveform for Inverting and Non-inverting Functions
$t_r = t_f \leq$ 2.0ns, 10% to 90%

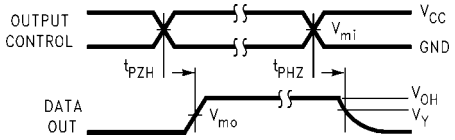


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic
$t_r = t_f \leq$ 2.0ns, 10% to 90%

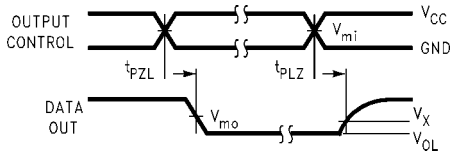
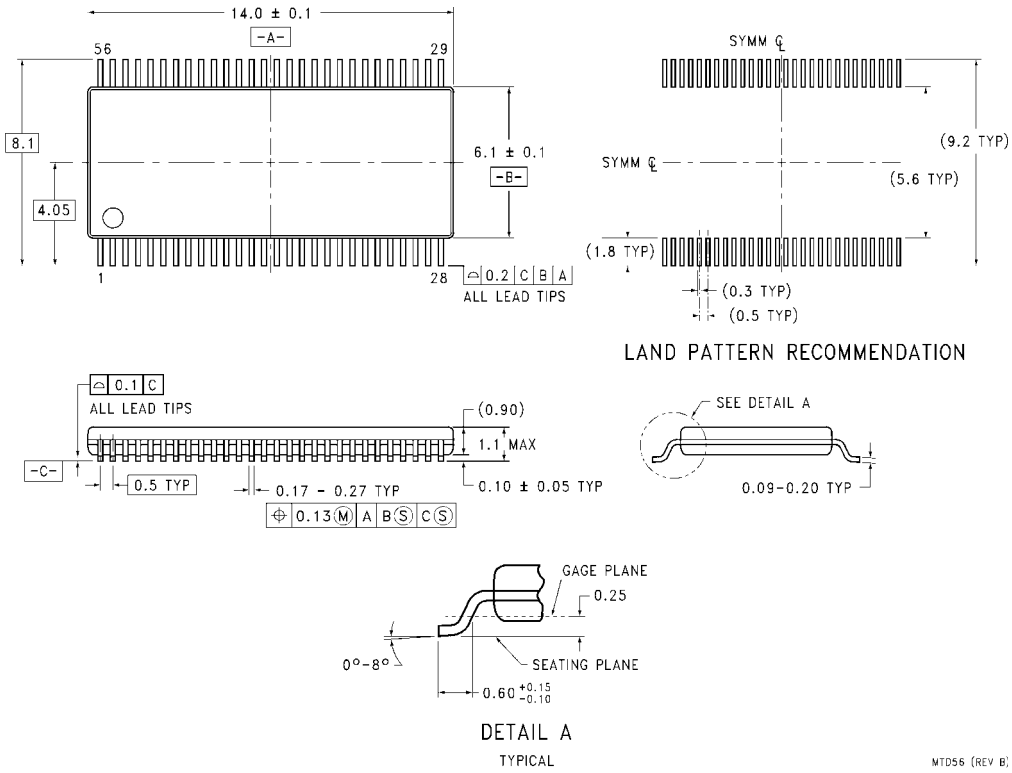


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic
$t_r = t_f \leq$ 2.0ns, 10% to 90%

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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