1 INTRODUCTION

The SiW1750 Baseband Processor is part of Silicon Wave's second-generation solutions for Bluetooth™ wireless communications. The SiW1750 provides the essential Bluetooth baseband link control and link management that meets Bluetooth 1.1 specification in a digital system-on-chip (SoC) with integrated firmware up to the HCI. Combined with the SiW1701 or SiW1502 Radio Modem ICs, it provides a complete and cost effective hardware solution to integrate into products.

2 FEATURES

- Small footprint 132-pin BGA package (8 x 8 mm).
- Fully compliant Bluetooth 1.1 component.
- Low power 1.8 V core with flexible 1.8 V or 3.3 V I/O voltage.
- Full piconet with 7 slaves support.
- Scatternet support.
- Full speed Bluetooth operation.
- HCI UART and USB transport support.
- CODEC interface for audio applications.
- External flash memory interface.
- Easy migration to cost-reduced ROM device.
- ARM7 TDMI® industry standard processor.
- Support for low power sleep modes.

3 APPLICATIONS

The SiW1750 Baseband Controller is ideally suited for high performance systems with fast data transfer and multiple device connectivity requirements. When combined with the SiW1701 or SiW1502 Radio Modem IC, a low power and cost effective integrated Bluetooth system can be easily integrated into the following products:

- Bluetooth enabled printers for home or office.
- Built-in or add-on accessory options for notebook PCs.
- PDAs (personal digital assistant) and palmtop computers.
- Bluetooth enabled network access stations.
- Audio applications such as headsets and mobile phones.

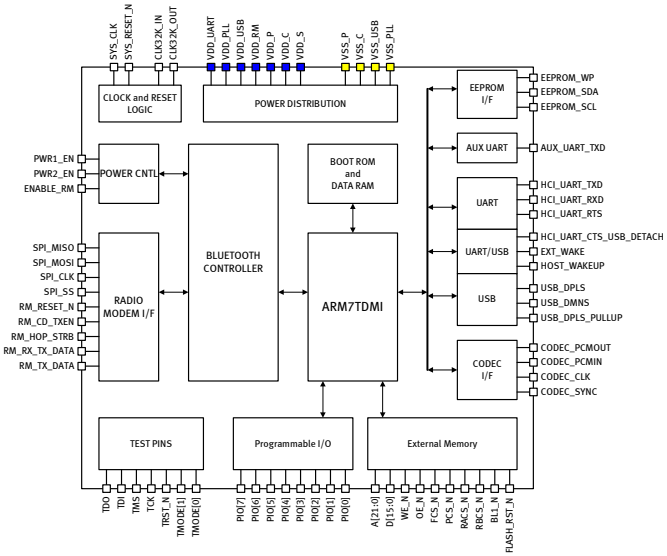


Figure 1: SiW1750 Baseband Processor IC Block Diagram

A typical design of a Bluetooth compliant product consists of the SiW1701 Radio Modem and the SiW1750 Baseband Processor. The Bluetooth link manager firmware is stored in external flash memory. Figure 2 illustrates the connection flow between the system's main components for designs using the SiW1750.

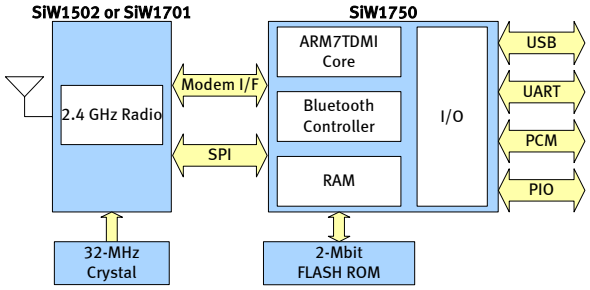


Figure 2: Bluetooth Subsystem

4 Bluetooth Subsystem

4.1 Overview

Adding Bluetooth connectivity to a system is as simple as including the Bluetooth radio, baseband, and link manager firmware. The host system then interfaces to the Bluetooth subsystem via the host controller interface (HCI) transport. The host system can also execute the Bluetooth protocol stack and application software.

Silicon Wave's chip set provides the required Bluetooth connectivity to a system. Starting with the SiW1701 radio modem chip that provides the industry's highest integrated functions and the best RF performance, to the SiW1750 baseband chip with integrated ARM processor core for the execution of Bluetooth firmware, Silicon Wave provides the most efficient solution to enable an OEM project. At the heart of the solution is the SiW1750 baseband hardware and link manager firmware.

4.2 SiW1750 Hardware and Firmware Features

The Bluetooth baseband and link manager firmware provide the essential functions of Bluetooth physical and logical connectivity. The link manager firmware resides in external flash memory. In conjunction with the baseband hardware, the ARM7TDMI processor and the necessary peripherals, the solution provides the following features:

- Supports Bluetooth specification version 1.1 defined connections, links and packet types:
  - **FEC**–forward error correction.
  - **Whiten/De-whiten**–scramble/unscramble.
  - **Encrypt/Decrypt**–apply/remove encryption.
  - **CRC**–cyclic redundancy check.
  - **HEC**–header error correction.
  - **Tx/Rx Buffers**–storage for received packets and packets to be transmitted.
- ACL and SCO links supported for data and voice applications.
- Point-to-point and point-to-multipoint (with 7 active and 7 parked slaves) connections.
- HCI UART (H:4) and USB (H:2) transports.
- Multi-slot packets minimize packet overhead and maximize data throughput.
- Encryption, authentication, and pairing provide secure data transfer between devices.
- Hold, sniff, and park modes maximize device connectivity and battery life.
- Bluetooth test modes facilitate production testing of the system.

4.3 SiW1750 Audio Features

The SiW1750 incorporates dedicated audio processing circuits to convert audio data between CVSD, linear PCM, and log PCM (A-law or μ-law). The CVSD circuit is useful during SCO connections where data is being transmitted over the air in CVSD format. The converted data can then be directed to an external audio CODEC via the CODEC interface on the SiW1750.

5 External System Interfaces

5.1 Radio Interface

The external radio interface provides control and data transfer capabilities to and from the radio chip. To minimize the power consumption, the interface is designed to operate at 1.8 or 3.0 V. The link manager firmware controls the radio interface at all times so customer intervention is not required.

5.2 Host HCI Transport (H:4 UART)

The high speed UART interface provides the physical transport between the SiW1750 and the application host for the transfer of Bluetooth control signals and data compliant to the Bluetooth section H:4 specification. Table 1 shows the supported bit rates. The default baud rate is 115,200, but can be configured depending on the application.

SiW1750 HCI UART Parameters	Required Host Setting
Number of data bits	8
Parity bit	No parity
Stop bit	1 stop bit
Flow control	RTS/CTS
Host flow-off response requirement from SiW1750	8 bytes
SiW1750 flow-off response requirement from host	2 bytes
Supported baud rates	9.6k, 19.2k, 38.4k, 57.6k, **115.2k**[1], 230.4k, 460.8k, 500k, 921.6k, 1M

Table 1: Host HCI Transport

[1] Default baud rate.

5.3 Host HCI Transport (H:2 USB)

The USB transport is compliant to USB 1.1 specification and the HCI transport specification within Section H:2 of the Bluetooth specification with all end points supported. The SiW1750 USB interface encompasses three I/O signals: USB_DPLS, USB_DMNS, and USB_DPLS_PULLUP. The USB_DPLS_PULLUP signal is used to control the state of pull-up on the USB_DPLS signal. There are two additional signals, EXT_WAKE and HOST_WAKE, which can be used as signals for power management of the SiW1750 device from the USB host.

A separate sideband signal, HCI_UART_CTS_USB_DETACH, is used to force the USB controller to detach from the USB bus. This input to the SiW1750 is optional and should be pulled low when not used.

5.4 Audio CODEC Interface

The SiW1750 supports direct interface to an external audio CODEC. The interface is configurable to support:

- Standard 64-KHz PCM clock rate.
- Up to 2-MHz clock rates with support for multi-slot handshakes and synchronization.
- Either master or slave (Motorola SSI) mode.

Configuration of the CODEC interface is done by the firmware during boot-up by reading non-volatile memory (NVM) parameters.

The following are examples of supported CODEC modes:

- Generic 64-kHz audio CODEC, such as the OKI MSM-7702.
- Motorola MC145481 or similar CODEC as master.
- Motorola SSI mode as slave device.

5.5 Programmable I/O (PIO)

Eight (8) programmable IO PIO ports are available for customer use in the SiW1750. The PIO ports can be set to input or output. Reading, writing, and controlling the PIO pins by the host application software can be done via vendor specific HCI commands.

5.6 External Memory/Peripheral Interface

An external memory and peripheral interface is available in the SiW1750. Using the external memory interface permits direct connection to memory devices such as flash (recommended flash part: Am29LV200B, part number DS42615), SRAM, and other memory mapped I/O devices such as bridge chips. The interface contains a 22-bit address bus and 16-bit data bus and either 16-bit or 8-bit devices are supported, with four (4) chip-select signals to select the target device. The control of the external memory interface such as timing/wait states is done within the configuration firmware of the boot memory.

5.7 External EEPROM Controller and Interface

The EEPROM interface is not required for configurations with external flash and is not used with the SiW1750. This interface is intended for use with ROM-based solutions. In this case, the EEPROM is the non-volatile memory (NVM) in the system and contains many system configuration parameters such as the Bluetooth device address, the CODEC type, as well as other system related parameters. These default parameters are set at the factory, and some parameters will change depending on the system configuration. Please consult the Silicon Wave application support team for details.

6 Configuration Selection During Boot Up

6.1 HCI Transport Interface Selection

The HCI transport (USB or UART) is selected on power up by sampling PIO2.

Value	Description
0	UART
1	USB

6.2 Firmware Boot Memory Selection

Programmable IO (PIO) pins are sampled at power-on-reset to provide control signals that are required before firmware code is executed. The values on the PIO[0] and PIO[1] pins are sampled when the SYS_RESET_N signal transitions from 0 to 1. After this point, the values on the pins may change to suit any desired application without affecting the captured values. Table 2 shows the pins that are captured and how the captured data is used.

PIO[0]	PIO[1]	Definition
0	0	Boot from internal ROM.
0	1	Reserved.
1	0	Boot from 16-bit external flash (chip select FCS_N).
1	1	Reserved.

Table 2: PIO Pins

7 On-Chip Memory

20 KB of synchronous static RAM is included on the chip. The SRAM memory is used by the link manager firmware for data storage and is not accessible by the host/application.

Boot ROM is included on the chip and serves to control the boot sequence as well as to direct the execution to the appropriate place for further operation. Further operation may be one of the following:

- Execution of code in off-chip flash
- Flash code download/update utility

8 Power Management

8.1 General System Power Management Control

EXT_WAKE and HOST_WAKEUP are used by the host and the SiW1750 to signal to each other the status of the power management. These signals are used in both the USB and UART HCI systems.

The active level for both EXT_WAKE and HOST_WAKEUP may be either a low or high voltage level depending on the user configuration. This polarity defaults to "active low" that wakes up the respective device, but it is programmable through an NVM parameter.

EXT_WAKE From Host to SiW1750. The polarity of this signal is programmable via an NVM parameter; the default is active low. When this signal is asserted, it causes the SiW1750 to remain awake and ready to communicate with the host. When this signal is de-asserted, it allows the SiW1750 to enter its lowest power consumption state.

HOST_WAKEUP From SiW1750 to Host. The polarity of this signal is programmable via an NVM parameter; the default is active low. When this signal is asserted, the host must remain awake and ready to communicate with the SiW1750. When this signal is de-asserted, it allows the host to optionally shut down the HCI and enter a low power state.

EXT_WAKE and HOST_WAKEUP are on the HCI UART power rail. In UART HCI operational modes this power rail may be either 1.8 V or 3.0 V depending on the voltage of the host/transceiver. In the USB HCI operational mode, this power rail is connected to the USB regulated voltage of 3.2 V.

9 Power Supply Requirements

There are multiple power requirements in the SiW1750 that need to be supplied with the proper voltage. Depending on the type of device connected and the desired power management control, various configurations are possible.

Pin	Usage	Voltage
VDD_RM	I/O voltage for radio interface.	3.3 V ± 10%, 3.0 V ± 10%, 1.8 V ± 10%.
VDD_USB	I/O PAD voltage for USB transceiver.	3.1 V to 3.6 V.
VDD_UART	I/O PAD voltage for UART HCI transport.	3.3 V ± 10%, 3.0 V ± 10%, 1.8 V ± 10%.
VDD_P	I/O PAD voltage for all other I/O's.	3.3 V ± 10%, 3.0 V ± 10%, 1.8 V ± 10% 3.3 V with AMD flash.
VDD_C	Core digital voltage.	1.8 V ± 10%.
VDD_S	Core digital supply for ROM memory.	1.8 V ± 10%.
VDD_PLL	Power for 32.768-kHz oscillator circuit and PLL for the USB controller.	1.8 V ±10%.
VSS_X (all pins)	Ground.	Common ground.

Table 3: Power Requirements

10 Clocking Requirements

10.1 System Clock

The SiW1750 uses a 16-MHz system clock as the reference clock rate for internal system functions.

The USB logic has its own PLL circuit to generate the required 48-MHz clock from the 16-MHz main system clock. This 48-MHz clock is used exclusively for the USB controller logic. This 48-MHz clock is internal to the SiW1750 is not available to the host or application software.

10.2 Low Power Clock

For the Bluetooth low power clock, a 32.768-kHz crystal may be used to drive the SiW1750 oscillator circuit, or alternatively, a 32.768-kHz reference clock signal can be used instead of a crystal. If lowest power consumption is not required during low-power modes such as sniff, hold, park, and idle modes, the 32.768-kHz crystal may be omitted in the design.

11 JTAG and Test Interface

11.1 Boundary Scan

There is an implementation of IEEE 1149.1 JTAG on the SiW1750. It supports only the mandatory instructions.

The IDCODE for the device is formed from the 8-bit JEDEC code for Silicon Wave and the version register.

Bits	Field	Value	Comment
31:28	HW version register.	0x02	
27:24	Unused.	0x0	Reserved for future use.
23:18	Product code.	0x02	Identification of the SiW1750.
17:12	Major features.	0x03	CVSD accelerator and USB port present.
11:1	Manufacturer.	0x17C	See below.
0	LSB.	0x1	Fixed value of 1.

Table 4: JTAG and Test Interface[1]

[1] The manufacturer code is formed from the Silicon Wave JEDEC code of 0x7C0 bank 3 in the manner described.

12 PINOUT

12.1 Pin Diagram

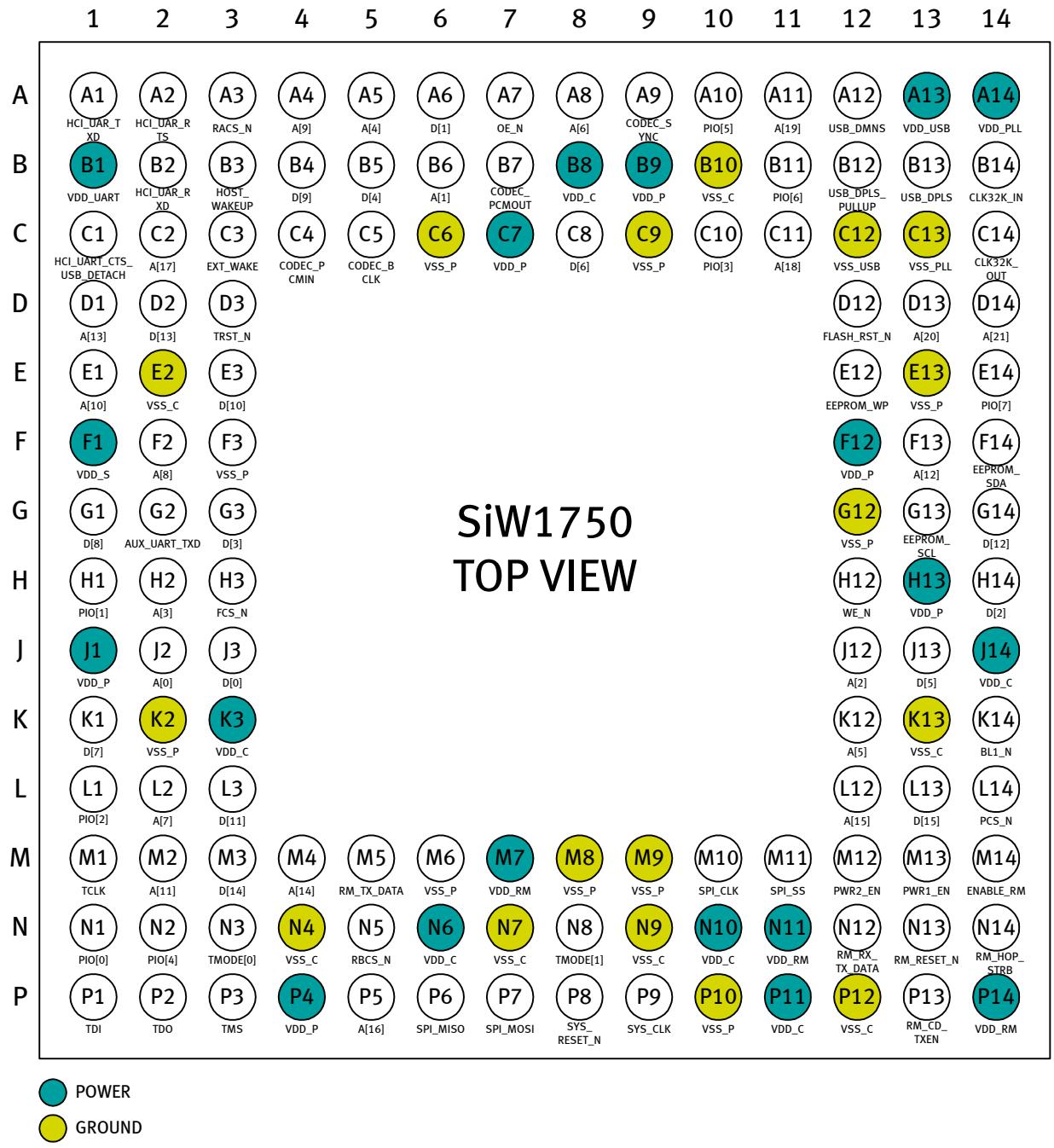


Figure 3: SiW1750 Pin Diagram

12.2 Pin List

Table 5 shows a complete list of the pins on the SiW1750.

Name	I/O Type	Ball	Comment	Reset Direction and Output Value
System Clock and Reset (Power from VDD_RM)				
SYS_CLK	CMOS Input	P9	System clock input at 16 MHz.	–
SYS_RESET_N	CMOS Input	P8	Power-up reset for the chip. Active low.	–
Crystal Oscillator (Power from VDD_PLL)				
CLK32K_IN	Analog	B14	For crystal or external clock input (32.768 kHz).	–
CLK32K_OUT	Analog	C14	Drive for crystal.	–
Power Control Interface (Power from VDD_RM)				
PWR2_EN	CMOS Output	M12	Enable for optional external switch to control power to VDD_S power pad (internal ROM).	In
PWR1_EN	CMOS Output	M13	Enable for optional external switch to control power to VDD_P power pad (external flash and CODEC).	In
ENABLE_RM	CMOS Output	M14	Enable for the radio modem. Forced high during reset. Active high.	"1"
Radio Modem Interface (Power from VDD_RM)				
SPI_MISO	CMOS Input	P6	SPI port serial data.	–
SPI_MOSI	CMOS Output	P7	SPI port serial data.	"0"
SPI_CLK	CMOS Output	M10	SPI port clock for serial data.	"0"
SPI_SS	CMOS Output	M11	SPI port slave select signal.	"1"
RM_RESET_N	CMOS Output	N13	Reset control for the radio modem. Active low.	"0" then "1"
RM_CD_TXEN	Bi-directional with internal pull-down	P13	Carrier detect from radio modem during receive slots and transmit enable control during transmit slots.	In
RM_HOP_STRB	CMOS Output	N14	Hop strobe signal for radio modem.	"0"
RM_RX_TX_DATA	Bi-directional with internal pull-down	N12	Normally bi-directional, but may also be used as receive data from radio modem.	In
RM_TX_DATA	CMOS output	M5	Transmit data to radio modem.	"0"
Peripheral Interface (Power from VDD_P)				
PIO[7]	Bi-directional	E14	Programmable input/output.	"0"
PIO[6]	Bi-directional	B11	Programmable input/output.	"0"
PIO[5]	Bi-directional	A10	Programmable input/output.	"0"
PIO[4]	Bi-directional	N2	Programmable input/output. Sampled following reset. PIO[4] = 0, execute ROM application. PIO[4] = 1, execute flash application.	"0"
PIO[3]	Bi-directional	C10	Programmable input/output	"1"
PIO[2]	Bi-directional	L1	Programmable input/output. Sampled following reset. PIO[2] = 0, selects UART transport. PIO[2] = 1, selects USB transport.	In

Table 5: SiW1750 Pin List

Name	I/O Type	Ball	Comment	Reset Direction and Output Value
PIO[1] PIO[0]	Bi-directional Bi-directional	H1 N1	Programmable input/output sampled following reset to select firmware boot. PIO[0] / PIO[1] / Definition 0 / 0 / Boot from internal ROM. 0 / 1 / Reserved. 1 / 0 / Boot from 16-bit external flash (chip select FCS_N). 1 / 1 / Reserved.	In In
EEPROM_SCL	Bi-directional if used as PIO and Output if EEPROM	G13	EEPROM interface SCL clock line. Reserved for future use.	"1"
EEPROM_SDA	Bi-directional with internal pull-up	F14	EEPROM interface SDA data line. Reserved for future use.	In
EEPROM_WP	Bi-directional if used as PIO and Output if EEPROM	E12	EEPROM interface write protect line. Reserved for future use.	"1"
AUX_UART_TXD	CMOS Output	G2	Auxiliary UART transmit data used for debugging purposes.	"1"
CODEC_PCMOUT	CMOS Input	B7	CODEC PCM data input.	In
CODEC_PCMIN	CMOS Output	C4	CODEC PCM data output.	–
CODEC_BCLK	CMOS Output	C5	CODEC PCM clock. Input for Motorola SSI slave mode.	-
CODEC_SYNC	CMOS Output	A9	CODEC PCM synchronization signal. Input for Motorola SSI slave mode.	In
HCI Transport Interface (Power from VDD_UART)				
EXT_WAKE	CMOS Input	C3	Wake up signal from host.	–
HOST_WAKEUP	CMOS Output	B3	Wake up signal to host.	"0"
HCI_UART_RXD	CMOS Input	B2	HCI UART receive data.	–
HCI_UART_TXD	CMOS Output	A1	HCI UART transmit data.	"1"
HCI_UART_CTS_ USB_DETACH	CMOS Input	C1	HCI UART flow control "Clear to send" for UART transport and USB sideband "Detach" when USB for USB transport.	–
HCI_UART_RTS	CMOS Output	A2	HCI UART flow control "Ready to send."	"1"
USB_DPLS	Analog	B13	USB differential pair positive signal.	–
USB_DMNS	Analog	A12	USB differential pair negative signal.	–
USB_DPLS_ PULLUP	Bi-directional	B12	Output signal for controlling the on/off of the pull-up of the USB_DPLS line.	In
Test Pins (Power from VDD_P)				
TMODE[0]	CMOS Input with internal pull-down	N3	Reserved for chip-level production testing. Leave unconnected.	–
TMODE[1]	CMOS Input with internal pull-down	N8	Reserved for chip-level production testing. Leave unconnected.	–
TRST_N	CMOS Input with internal pull-up	D3	Reserved for chip-level production testing and available as IEEE 1149.1 pins for board testing. If not implemented, connect to ground.	–
TCK	CMOS Input with internal pull-up	M1	Reserved for chip-level production testing and available as IEEE 1149.1 pins for board testing. If not implemented, leave unconnected.	–

Table 5: SiW1750 Pin List (Continued)

Name	I/O Type	Ball	Comment	Reset Direction and Output Value
TMS	CMOS Input with internal pull-up	P3	Reserved for chip-level production testing and available as IEEE 1149.1 pins for board testing. If not implemented, leave unconnected.	–
TDI	CMOS Input with internal pull-up	P1	Reserved for chip-level production testing and available as IEEE 1149.1 pins for board testing. If not implemented, leave unconnected.	–
TDO	CMOS Output, tri-statable	P2	Reserved for chip-level production testing and available as IEEE 1149.1 pins for board testing. If not implemented, leave unconnected.	"Z"
External Memory Interface Pins (power from VDD_P)				
A[21] A[20] A[19] A[18] A[17] A[16] A[15] A[14] A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1]	CMOS Output	D14 D13 A11 C11 C2 P5 L12 M4 D1 F13 M2 E1 A4 F2 L2 A8 K12 A5 H2 J12 B6	Address bus for external flash. Every bit except A[0] is a forcing zero at reset to ensure that there are no un-driven addresses to external memory devices; bit zero is a forcing one at reset because it might be being used as a low byte signal.	"0"
A[0]		J2		"1"
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	Bi-directional with internal pull-down	L13 M3 D2 G14 L3 E3 B4 G1 K1 C8 J13 B5 G3 H14 A6 J3	Data bus for external flash. Every bit becomes an input at reset to ensure that there are no conflicts with external memory devices.	In

Table 5: SiW1750 Pin List (Continued)

Name	I/O Type	Ball	Comment	Reset Direction and Output Value
OE_N	CMOS Output	A7	Output enable for controlling read data from external devices. Active low.	"1"
WE_N	CMOS Output	H12	Write enable for controlling write data to external devices. Active low.	"1"
RACS_N	CMOS Output	A3	RAM A chip select. Active low. Reserved for debug use only.	"1"
RBCS_N	CMOS Output	N5	RAM B chip select. Active low. Reserved for debug use only.	"1"
FCS_N	CMOS Output	H3	Flash chip select. Active low.	"1"
PCS_N	CMOS Output	L14	Peripheral chip select. Active low. Reserved for debug use only.	"1"
BL1_N	CMOS Output	K14	Byte lane 1 for 16-bit flash with low and high byte enables. Active low. Byte lane 0 is overlaid on with A[0].	"1"
FLASH_RST_N	CMOS Output	D12	Reset for flash (if required). Active low.	"1"
Power and Ground Pins				
VDD_RM	Power	N11 M7 P14	Pad ring V_{dd} supply for the section that tracks the voltage of the radio modem IC.	–
VDD_P	Power	P4 F12 B9 J1 H13 C7	Pad ring V_{dd} supply for the section that may either track the radio modem IC voltage or be supplied by an external regulator.	–
VDD_C	Power	N6 N10 P11 K3 J14 B8	V_{dd} supply for those sections of the core that must always be powered up.	–
VDD_S	Power	F1	Independent, switchable V_{dd} supply for sections of the core that can be powered down to save current.	–
VDD_UART	Power	B1	V_{dd} supply for section of the power ring that includes the HCI UART and associated sleep signals.	–
VDD_USB	Power	A13	USB transceiver cell V_{dd} supply.	–
VDD_PLL	Power	A14	PLL and 32.768-kHz oscillator V_{dd} supply.	–
VSS_P	Ground	F3 M6 M8 P10 G12 C9 K2 M9 E13 C6	Pad ring V_{SS} supply.	–

Table 5: SiW1750 Pin List (Continued)

Name	I/O Type	Ball	Comment	Reset Direction and Output Value
VSS_C	Ground	N7 N9 P12 E2 N4 K13 B10	Core cell V_{SS} supply.	–
VSS_USB	Ground	C12	USB transceiver cell V_{SS} connection.	–
VSS_PLL32K	Ground	C13	PLL and 32.768-kHz oscillator V_{SS} connection.	–

Table 5: SiW1750 Pin List (Continued)

12.3 Special Pins

Table 6 shows a list of pins on the SiW1750 that need special consideration on the board.

Pin	Function	Comment
CLK32K_IN	Pull-down	If no external 32.768-kHz crystal is needed, pull this pin low.
CLK32K_OUT	Float	If no external 32.768-kHz crystal is needed, leave this pin unconnected.
RM_CD_TXEN	Pull down	A pull-down resistor of 1.5 kΩ is recommended on this pin.
PIO[N]	Pull down	PIO bits 0, 1, and 2 may be left as inputs and pulled to ground to avoid floating, or they may be made outputs and driven low. PIO bits 3, 4, 5, 6, and 7 reset as outputs and should be left unconnected if not used.
HCI_UART_RXD	Pull down	If no device is connected to the HCI UART port, pull this pin to ground.
HCI_UART_CTS_USB_DETACH	Pull down	If no device is connected to the HCI UART port, or if flow control is not being used, pull this pin to ground.
CODEC_PCMOUT	Pull down	If no device is connected to the CODEC port, pull this pin to ground.
EXT_WAKE	Pull down	If no external host is present, or if wake up from the host is not required, pull this pin to ground.
USB_DPLS and USB_DMNS	Float	If no device is connected to the USB port, leave the differential data pair unconnected.
TRST_N	Ground	This pin should be connected to ground.
TDI	Float	This pin has an internal pull-up and may be left unconnected.
TCK	Float	This pin has an internal pull-up and may be left unconnected.
TMS	Float	This pin has an internal pull-up and may be left unconnected.
D[N] (all data bits D[0] through D[15])	Float	If not all external data bus bits are required (for example, if only 8-bit memory is being used), leave the unused bits unconnected since the pins have internal pull-downs.
TMODE[0] TMODE[1]	Float	These pins have internal pull-downs and may be left unconnected.

Table 6: Special Pins

13 Electrical Specifications

13.1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
T_{ST}	Storage temperature.	-55	+125	°C
V_{ddmax}	Supply voltage.	-0.3	+4.0	V
I_{in}	Input current.	-10	+10	mA

13.2 ESD Rating

Symbol	Description	Rating
ESD	ESD protection - all pins.	2000 V

Note: This device is a high performance integrated circuit with an ESD rating of 2,000 volts (HBM conditions per Mil-Std-883, Method 3015). Handling and assembly of this device should only be done using appropriate ESD controlled processes.

13.3 Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
T_{OP}	Operating temperature (industrial).	-40	+85	°C

13.4 Supply Voltage DC Parameters (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power supply V_{dd_p}	V_{vdd_p}	V_{dd_p} = 3.3 V	2.97	3.3	3.63	V
Power supply V_{dd_p}	V_{vdd_p}	V_{dd_p} = 3.0 V	2.70	3.0	3.30	V
Power supply V_{dd_p}	V_{vdd_p}	V_{dd_p} = 1.8 V	1.62	1.8	1.98	V
Power supply V_{dd_rm}	V_{vdd_rm}	V_{dd_rm} = 3.3 V	2.97	3.3	3.63	V
Power supply V_{dd_rm}	V_{vdd_rm}	V_{dd_rm} = 3.0 V	2.70	3.0	3.30	V
Power supply V_{dd_rm}	V_{vdd_rm}	V_{dd_rm} = 1.8 V	1.62	1.8	1.98	V
Power supply V_{dd_uart}	V_{vdd_uart}	V_{dd_uart} = 3.3 V	2.97	3.3	3.63	V
Power supply V_{dd_uart}	V_{vdd_uart}	V_{dd_uart} = 3.0 V	2.70	3.0	3.30	V
Power supply V_{dd_uart}	V_{vdd_uart}	V_{dd_uart} = 1.8 V	1.62	1.8	1.98	V
Power supply V_{dd_usb}	V_{vdd_usb}	–	3.10	3.2	3.60	V
Power supply V_{dd_pll32k}	V_{vdd_pll32k}	–	1.62	1.8	1.98	V
Power supply V_{dd_c}	V_{vdd_c}	–	1.62	1.8	1.98	V
Power supply V_{dd_s}	V_{vdd_s}	–	1.62	1.8	1.98	V

13.5 I/O DC Parameters (T_{OP} = 25°C, V_{dd} = 3.0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input low voltage	V_{il}	V_{dd} = 3.0 V	-0.3	–	0.8	V
Input high voltage	V_{ih}	V_{dd} = 3.0 V	2.0	–	V_{dd} + 0.5	V
Output low voltage	V_{ol}	V_{dd} = 3.0 V I_{ol} = 2 mA	GND	0.2	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output high voltage	V_{oh}	V_{dd} = 3.0 V, I_{oh} = -2 mA	V_{dd} - 0.5	–	V_{dd}	V
Input high current	I_{ih}	–	–	75	–	µA
Input low current	I_{il}	–	–	-15	–	µA
Input capacitance	C_i	All inputs.	–	–	TBD	pF
Output capacitance	C_o	All outputs.	–	–	TBD	pF

13.6 I/O DC Parameters (T_{op} = 25°C, V_{dd} = 1.8 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input low voltage	V_{il}	V_{dd} = 1.8 V	-0.3	–	V_{dd} * 0.3	V
Input high voltage	V_{ih}	V_{dd} = 1.8 V	V_{dd} · 0.7	–	V_{dd} + 0.3	V
Output low voltage	V_{ol}	V_{dd} = 1.8 V I_{ol} = 1 mA	GND	0.2	0.4	V
Output high voltage	V_{oh}	V_{dd} = 1.8 V I_{oh} = -1mA	V_{dd} - 0.5	–	V_{dd}	V
Input high current	I_{ih}	–	–	25	–	µA
Input low current	I_{il}	–	–	-5	–	µA

13.7 Current Consumption (T_{op} = 25°C, V_{dd} = 1.8 V)

Symbol	Description	Typ	Unit
I_{DD}(sleep)	Current during sleep with low power 32.768KHz crystal option.	40	µA
I_{DD}(idle) UART	Current in active mode (USB not included). SYS_CLK is running, but there is no Bluetooth activity.	7	mA
I_{DD}(idle) USB	Current for USB controller and transceiver when using USB transport.	9	mA
I_{DD}(active) UART	Average current in a typical full-duplex Bluetooth connection state (UART transport).	12	mA
I_{DD}(active) USB	Average current in a typical full-duplex Bluetooth connection state (USB transport).	14	mA

14 Package Specification

The packaging diagrams for the 132-pin BGA package are shown below.

14.1 132-Pin BGA (8-mm x 8-mm Body)

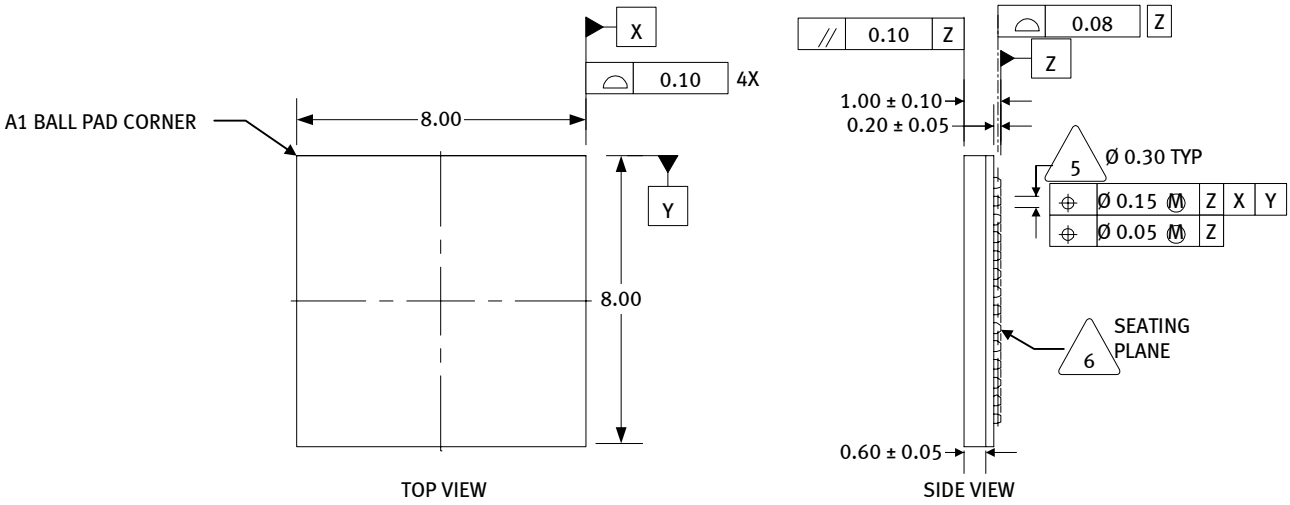


Figure 4: 132-Pin BGA Package

Notes: Unless otherwise specified:

1. All dimensions and tolerances conform to ASME Y14.5M-1994.
2. The basic solder ball grid pitch is 0.50.
3. The maximum solder ball matrix size is 14 x 14.
4. The maximum allowable number of solder balls is 132.
5. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
6. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
7. Reference specifications:
   A.AAWW SPEC #001-0531-2234: Packing Operation Procedure.
   B.AAWW SPEC #001-0519-2062: Marking.

15 I/O Assignment

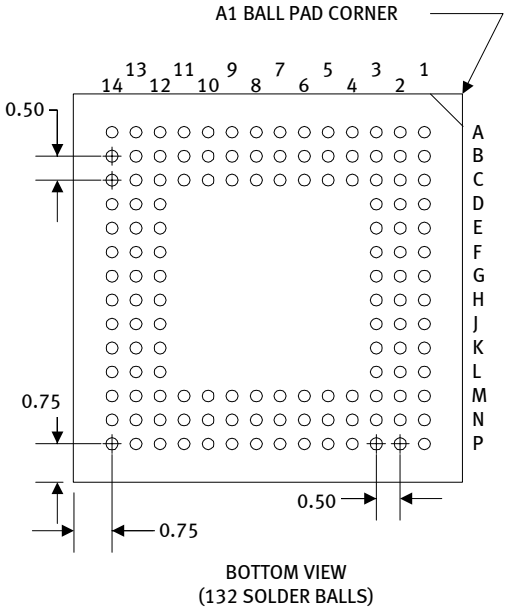


Figure 5: 132-Pin BGA I/O Pad

16 SiW1750 Product Marking

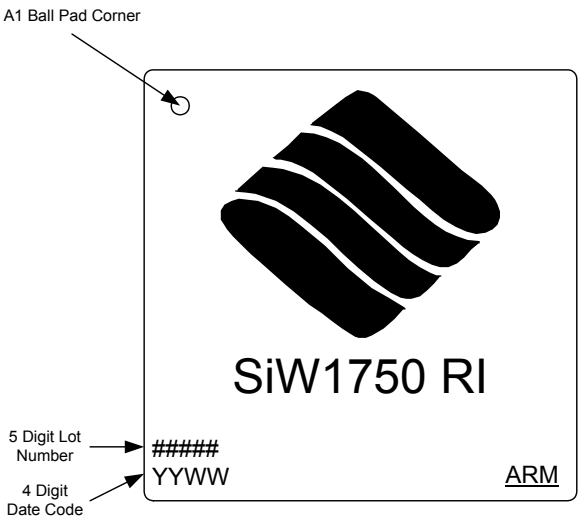
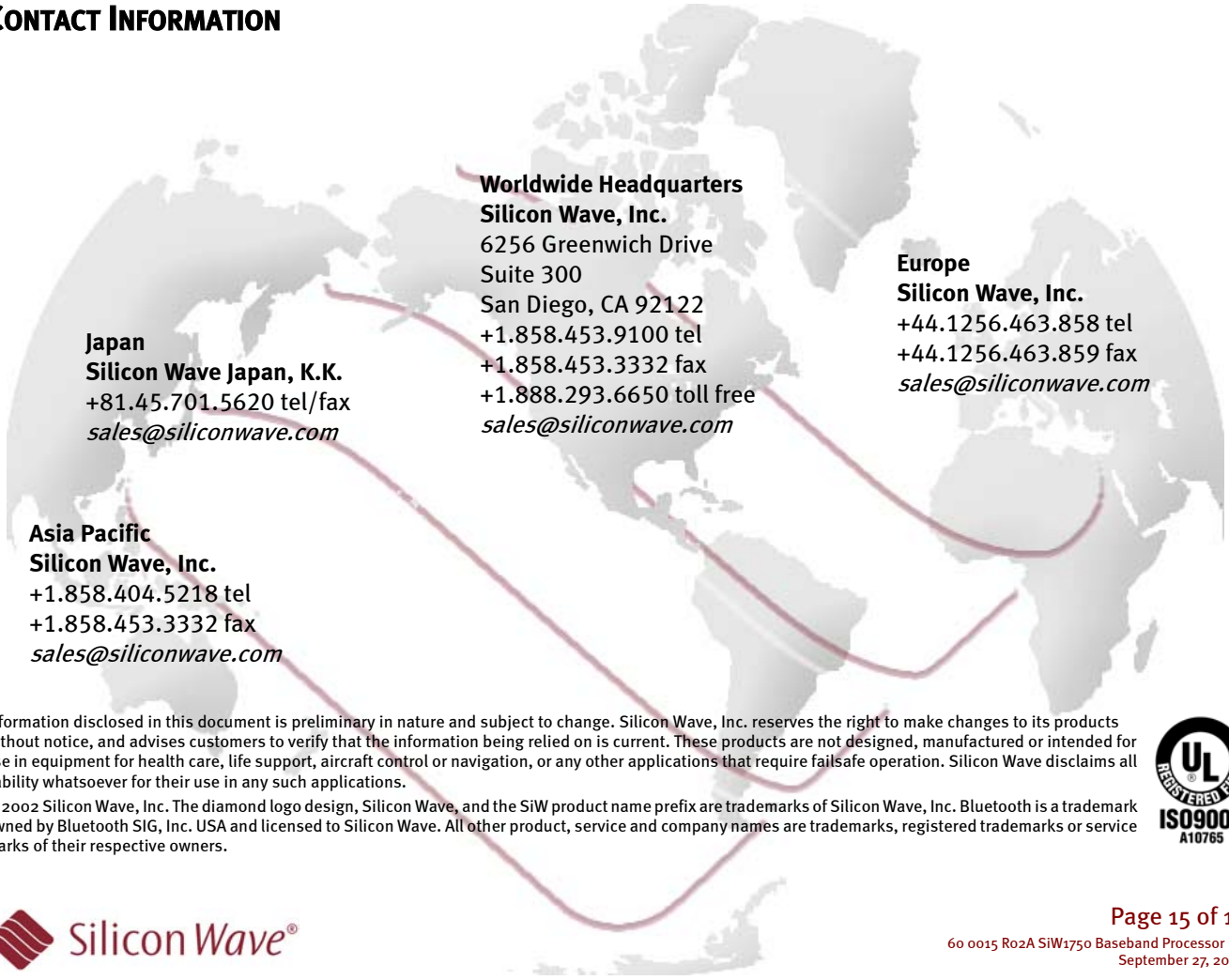


Figure 6: SiW1750 Product Marking

17 Ordering Information

Part Number	Operational Temperature Range	Package	Ordering Quantity
SiW1750RI	Industrial.	BGA-132	360 pcs. per tray.
SiW1750RI-TR13	Industrial.	BGA-132	2500 pcs. per reel.

Contact Information



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