Ulysses™ SGN3100 Bluetooth™ Baseband IC

PRELIMINARY SPECIFICATION

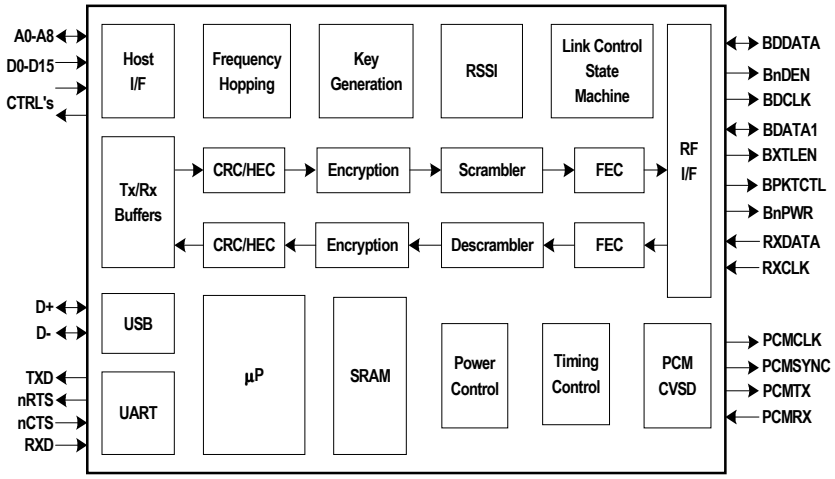
Product Description:

The Ulysses™ SGN3100 provides Bluetooth™ Link Control and Link Management functions that support up to 8 data/3 voice channels compliant with the Bluetooth™ Specification 1.1. The SGN3100 contains a 32 bit RISC microprocessor and a large 80 kB on-chip SRAM for easy implementation into notebook PCs, PDAs, internet appliances and other devices requiring low power, cost effective Bluetooth™ functionality. In addition to USB and UART interfaces, the SGN3100 implements a parallel host interface that can be connected to a wide variety of buses such as PCMCIA™, CompactFlash, and microprocessor buses, eliminating the need for glue logic components.

The SGN3100 is optimized to work with Signia's Ulysses™ SGN5010 transceiver for use in Bluetooth™ applications through a 7-pin BlueRF™ interface. This interface allows interoperability with the BlueRF™ compliant transceivers. The interface consists of a bi-directional transmit and receive data line, three SGN3100-to-SGN5010 uni-directional control lines for power and timing control, and a 3-wire serial data bus for accessing SGN5010's internal registers.

The SGN3100 is available in two low cost, small footprint, industry standard packages: LQFP-80 and LFBGA-81.

Block Diagram:



Key Features:

- Parallel host interface connects directly to PCMCIA™, CompactFlash, and many microprocessor buses.
- Full-speed USB device compliant to USB 1.1.
- High-speed UART up to 1.843 Mbits/sec.
- Large on-chip SRAM.
- Hardware implemented Bluetooth™ FEC, Data Scrambling, CRC/HEC, encryption/decryption, and authentication key generation
- Fully support point-to-multipoint, 3 SCO or 7 ACL traffic channels
- Support RSSI channel quality measurement for each link in a pico-net
- Support for transmit power control
- Support for PCM A-law/µ-law and CVSD codec
- Compliant to Bluetooth™ specification version 1.1 and BlueRF™ interface
- A component of Signia's Ulysses™ family of complete hardware and software Bluetooth™ solutions, optimized for use with Signia's SGN5010 transceiver

Applications:

- Battery Powered Portable and Handheld Devices
- Laptop Computers
- PDAs
- Modems and Internet Access Points
- Cordless and Cellular Phones
- PCMCIA™ or CompactFlash

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Ratings

Absolute Maximum Ratings					
Parameter	**Symbol**	**Rating**			**Unit**
		Min	**Typ**	**Max**	
Operating Temperature	T_{OP}	-0		+85	°C
Supply Voltage to Core	V_{DD}	+2.25	+2.50	+2.75	V
Supply Voltage to I/O	V_{DD_IO}	+3.0	+3.3	+3.6	V
Supply Voltage to RF I/O	V_{DD_RF}	+2.5	+3.3	+3.6	V

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.
2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover work benches with grounded conductive mats.
3. Information given in this data sheet is believed to be accurate and reliable at the time of printing. However, Signia reserves the right to make changes to products and specifications without notice.

Electrical Characteristics

The following specifications are guaranteed for T_A = 25 °C, V_{DD} = 2.5V**,** unless otherwise noted

Parameter	**Symbol**	**Specification**			**Unit**	**Condition**
		Min	**Typ**	**Max**		
DC Specifications						
V_{DD} supply Voltage - Core	V_{DD}	2.25	2.5	2.75	V	
V_{DD_IO} supply Voltage - IO	V_{DD_IO}	3.0	3.3	3.6	V	
V_{DD_RF} supply Voltage - RF	V_{DD_RF}	2.5	2.5	3.6	V	
Current Consumption - Connection	I_{DD_CONN}		45.0		mA	V_{DD}=2.5V, V_{DD_IO}=3.3V, V_{DD_RF}=2.5V
Current Consumption - Peak	I_{DD_PEAK}		75.0		mA	V_{DD}=2.5V, V_{DD_IO}=3.3V, V_{DD_RF}=2.5V
Current Consumption - Standby	I_{DD_SB}		0.8		mA	V_{DD}=2.5V, V_{DD_IO}=3.3V, V_{DD_RF}=2.5V
Digital Inputs						
Logic input high	V_{IH}				V	
Logic input low	V_{IL}				V	
Input pin capacitance	C_I		7.213		pF	
I/O pin capacitance	$C_{I/O}$		7.461		pF	
Digital Outputs						
Logic output high	V_{OH}		V_{DD_IO}		V	
Logic output low	V_{OL}		0		V	
Input Leakage Current	I_{iL}		1		uA	
Output Leakage Current	I_{OL}		10		uA	

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Functional Description

The SGN3100 provides all the Bluetooth™ Link Control (LC), Link Management (LM) and Host Communication Interface (HCI) functions in a single chip for a hosted Bluetooth™ application. All the channel related coding and decoding such as the forward error correction (FEC), the scrambling, the cyclic redundancy check (CRC), and the optional data encryption are implemented directly in hardware. This is in addition to the PCM/CVSD audio transcoder function, which are also implemented in hardware.

To avoid missing real-time events, timing critical operations such as RF synthesizer on/off and timing control, receive data symbol clock recovery, TX/RX frequency hopping calculation, master/slave TDD switch, etc. are also supported directly in hardware. Also provided in the SGN3100 hardware are the power-management and link quality measurement supports.

To facilitate the communication with the host, the SGN3100 implements a full-speed USB 1.1-compliant device interface, a high-speed UART interface (for communication speed up to 1.8432 Mbit/sec), and a parallel host interface. In addition, an I^2C interface allows the SGN3100 to store configuration parameters in a small-footprint serial E^2PROM. The same E^2PROM can also store the HCI firmware that the SGN3100 will automatically upload into its internal SRAM upon reset.

PHY I/F – Physical Layer Interface

The SGN3100 supports the bi-directional BlueRF™ interface protocol with the RXMODE2 in receive mode. When it interfaces with a BlueRF™-compatible PHY device, the SGN3100 sends/receives data at the 1MHz symbol rate over the same piece of wire. The direction of the data is controlled by an internal state machine, which is synchronized with the PHY device over 3 control signals. These 3 control signals also provide the crucial packet timing information as well as the power-down, sleep mode control to the PHY device.

To access the internal registers of the PHY device, the BlueRF™ interface defines a 3-wire SPI-like serial interface (DBus). Through this 3-wire DBus, the SGN3100 retrieves the RSSI information from the PHY device as well as provides fine-grain control, such as synthesizer programming and DC-offset tuning, to the PHY device.

In addition to the BlueRF™ interface, the SGN3100 can also be programmed to receive the recovered symbol clock and demodulated data directly from the Bluetooth™ PHY device during the receive slot. This allows the SGN3100 to provide better receive performance when linked up with Signia's own SGN5010 PHY device.

CRC/HEC – Cyclic Redundancy Check/Header Error Check

To protect data from transmission error, all Bluetooth™ packet headers are encoded with a header-error-check and all ACL packets payloads are encoded with a CRC. If either the HEC error or CRC error is detected on the receive side, the packet must be re-transmitted. The CRC is automatically disabled for all SCO and AUX packets per Bluetooth™ specification.

Scrambler/De-scrambler

The main purpose of data scrambling is to randomize the transmit data so as to avoid the long sequences of 0's and 1's, which can cause un-wanted DC-offset in the receive circuit. The randomized data, with the frequent transitions between 0 and 1, can also help the symbol clock tracking performance.

FEC – Forward Error Correction

After a packet is CRC/HEC-encoded, scrambled, and optionally encrypted (see below), it is further encoded with the forward error correction code. Depending on the packet type and field, either 1/3 or 2/3 FEC is applied. The FEC code provides another layer of protection over channel noise. The results of FEC error checking can be used for measuring the link quality.

Authentication/Encryption Key Generation

In order to establish a secure communication link, the Bluetooth™ specification defines a process for the authentication/encryption key generation. This process is implemented entirely in the SGN3100. During the connection establishing states or any time during the connection state, the SGN3100 firmware can invoke the key generation hardware to generate the keys, and then exchange the keys with the peer through the LMP messages.

Encryption/Decryption

With the authentication/encryption keys, a secure communication link can then be established by encrypting and decrypting the out-going and incoming messages with the keys. The SGN3100 implements an encryption/decryption engine in hardware to ensure all encryption and decryption are done in real-time. Once a

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channel is enabled for secure communication, the encryption/decryption engine automatically engages during transmit/receive operation. The encryption is applied after the CRC/HEC coding and before the scrambling.

Frequency Hopping

The Bluetooth™ standard uses frequency hopping spread spectrum technique to avoid channel congestion. The hopping sequences are computed from the device address and the clock of a node or its master, and can vary between 79-hop or 23-hop depending on the region where the device resides. The SGN3100 implements this hopping frequency computation directly in hardware to avoid confusion and to release the firmware from tedious but timing critical operations.

Timing Control

The SGN3100 implements programmable hardware to keep track of the critical timing events in a Bluetooth™ piconet. This hardware allows the SGN3100 to control the timing of many Bluetooth-specific operations down to the sub-microsecond level. For example, the SGN3100 can be programmed to accommodate different delays through the RF circuits as well as different timing requirement for the RF synthesizer to stabilize. This allows the firmware to fine-tune the RF interface for better RF performance. The SGN3100 receive logic can automatically re-adjust the estimated master timing upon the detection of every master transmit, whether the transmission is heading its way or not. This ensures a slave device is always in sync with the master as long as the master is transmitting. The SGN3100 can compute the slot-offset between the master and the native clock, saves the off-set, and later restores the timing from the saved offset; a crucial operation for scatter-net implementation.

Power Management

The SGN3100 currently supports the Bluetooth™ sniff and hold mode (and will support the park mode when demand picks up). During these two modes, both the SGN3100 and the companion SGN5010 chips can be shut down to save power. The SGN3100 wakes up after a specified amount of time when a programmable counter expires. This counter can be clocked either by the main crystal or by a second optional, low-power, low frequency crystal, which is activated during the low-power sleep mode.

During normal connection when the device is not in sleeping mode, the SGN3100 can be programmed to shut down all the non-essential blocks, including the on-chip microprocessor, on a per-cycle based to conserve the power.

PCM/CVSD Encoding/Decoding

For audio data, the SGN3100 implements both the PCM A-law/μ-law and the CVSD transcoding functions in hardware to support the Bluetooth™ audio requirements. Both the PCM and the CVSD encoding provide audio-data compression for better sound quality over the linearly sampled data.

Host Processor Interface

For high-speed communication with the host, the SGN3100 implements a parallel host-processor interface. This interface can be hooked up to PCMCIA™, CompactFlash, and many microprocessor memory buses directly. And, since it is a parallel bus, it provides virtually un-limited bus bandwidth for Bluetooth™ transport-layer communication.

USB/UART

In addition to the parallel Host Processor Interface, two separate USB and UART interfaces are also provided. The USB interface follows the standard USB v1.1 device specification.

The UART interface implements a 4-wire interface with an optional automatic nCTS/nRTS flow control to avoid losing data due to overrun. The implementation supports baud rate up to 1.8432 Mbauds per second.

I^2C Interface

The SGN3100 implements an I^2C master interface for communication with I^2C slave devices such as the serial E^2PROM. This I^2C interface allows the SGN3100 to store Bluetooth™ specific configuration data such as the device address and authentication keys between power-on. It also provides a source for the SGN3100 to boot from. Currently, the SGN3100 can automatically up-load the HCI firmware upon power-on from either the I^2C interface or the parallel host interface.

On-Chip Microprocessor/SRAM

To enable the implementation of the full Host Control Interface (HCI), the SGN3100 includes an on-chip, 32-bit RISC microprocessor and an 80kByte on-chip SRAM. Among many things, the firmware, running on the microprocessor, implements all the data buffering and controls the flow of the data between various hardware modules in the SGN3100. In addition, the firmware also implements all the algorithmic/heuristic logic that otherwise cannot be easily done in hardware.

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GPIO

For generic I/O operations, up to 24 GPIO pins are provided. These pins are organized into 3 groups of 8 pins. Each pin can be individual configured as input, output, or open-drain pin. When configured as input or open-drain pin, an optional filter can be applied before the value is sampled. Once sampled, the pin values can be read off a register directly by the embedded MPU. Or, the values can be watched by a monitoring logic, which looks for combination of pin values or edges and triggers interrupts to the MPU. Due to limited number of available pins, the GPIO module shares pins with other functional modules. Upon power-on, the GPIO has control over all the shared pins and the embedded MPU needs to disable the GPIO function of a pin to restore the specially assigned function.

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PIN Descriptions

PHY Device Interfaces

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
1	A2	BDATA1	-	I/O-U	In transmit mode, this pin receives transmit data from the baseband at a 1MHz data rate. In receive mode, this pin sends receive data to the baseband at a 1MHz data rate.
2	A3	BnPWR	-	O	This is basically the reset pin to the PHY. When asserted (low), the PHY should be in lower-power mode.
3	A4	BDCLK	-	O	The Dbus serial clock at 12 MHz.
5	B1	BDDATA	-	I/O-U	Serial data port. This pin provides a variety of control data to the RF chip, including TX_ON, RX_ON, SYNTH_ON, ACG_CTRL, and PLL_CTRL. It also passes RSSI data from the RF chip to the baseband. Data is transferred on the rising edge of BDCLK.
6	B3	BnDEN	-	O	The 3-wire Dbus enable pin. The BDDATA pin should only wiggle when the BnDEN pin is held low.
8	B4	BXTLEN	-	O	This pin is to shut down the clock logic in PHY for power-saving sleep mode.
11	C3	BPKTCTL	-	O	In transmit mode, this pin turns signals the start of transmit data. This should be after the PHY has tuned the synthesizer to the new hopping frequency. In receive mode, this pin controls the DC estimation in two different states: a low state is used to set the DC estimation for fast acquisition and a high state is used for slower DC estimation.
9	C1	RXCLK	GPIO2[3]	I/O	Recovered 1MHz receive clock.
10	C2	RXDATA	GPIO2[2]	I/O	Recovered data input at 1MHz symbol rate.

Host Processor Interfaces

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
48, 47, 46, 45, 44, 42, 41, 40	G3, G4, G5, G6, G7, G8, G9, H9	HADDR[7:0]	-	I-U	Address from the host processor
64	F5	HADDR[8]	GPIO2[7]	I/O	
23, 22, 19, 18, 17, 16, 15, 14	J6, J5, J3, J2, H1, G2, G1, F1	HDATA[7:0]	-	I/O-U	16-bit parallel to and from the host
39, 38, 37, 36, 35, 34, 33, 32	H8, H7, H6, H5, H3, J9, J8, J7	HDATA[15:8]	GPIO1[7:0]	I/O	
49	E9	HnCE	-	I-U	Active low chip select
50	F6	HnOE	-	I-U	Active low output enable for memory read operation
52	F7	HnWR	-	I-U	Active low write enable for memory write operation
53	E7	HnIOWR	-	I-U	Active low IO write
54	E8	HnIORD	-	I-U	Active low IO read

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LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
63	C6	HnREG	-	I-U	Select between config and memory space
65	B9	HRESET	-	I-D	Reset from the host processor
66	D7	HnINPACK	GPIO2[6]	I/O	Acknowledge for IO operation
67	C7	HnINT	GPIO2[5]	I/O	Active low interrupt to host processor
68	B1	HnWAIT	-	O	Active low wait for SGN3100 to hold the bus

USB Interfaces

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
25	E2	D+	-	U-I/O	USB data +
26	E1	D-	-	U-I/O	USB data -

UART Interfaces

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
28	F3	nCTS	GPIO0[0]	I/O	UART clear to send
29	D3	nRTS	GPIO0[1]	I/O	UART request to send
30	E3	TXD	GPIO0[2]	I/O	UART transmit data
31	F2	RXD	GPIO0[3]	I/O	UART receive data

PCM Interfaces

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
55	D9	PCMCLK	GPIO0[4]	I/O	PCM 256KHz data clock output
56	D8	PCMSYNC	GPIO0[5]	I/O	PCM frame strobe output
57	C9	PCMRX	GPIO0[6]	I/O	PCM serial data input
58	C8	PCMTX	GPIO0[7]	I/O	PCM serial data output

I^2C Interfaces

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
71	E6	SCL	-	O	I^2C serial clock
72	D6	SDA	-	OD-U	I^2C serial data

Miscellaneous Interfaces

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
59	D5	TESTMD	-	I-D	Test mode enable
62	C4	TESTSE	-	I-D	Test scan enable
74	B5	nRESET	-	I-US	Hardware Reset
78	A8	XTLIN	-	XI	Crystal input (10 - 20MHz)
77	A7	XTLOUT	-	XO	Crystal Output
12	E4	XTLOUT2	GPIO2[1]	I/O	Low frequency crystal out

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LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
13	F4	XTLIN2	GPIO2[0]	I/O	Low frequency crystal in (32K, 32.768K, or 40KHz)
75	C5	XBYPASS	-	I-D	Disable and bypass the internal PLL.
76	B6	XOUT/BCFG	-	I/O-D	In test mode, this pin outputs the synthesized clock from the PLL. In normal mode, this pin determines the power-on boot configuration.
70	D4	nRSTO	GPIO2[4]	I/O	Watch-dog timer reset output

Power

LQFP-80	LFBGA-81	Pin Name	GPIO	Type	Description
20, 61, 79	A6, B8, H2	VDD_CORE	-	P	VDD for CORE (2.5v)
4	B2	VDD_RFIO	-	P	VDD for RF I/O pins (3.3v or 2.5v)
24, 43, 69	D2, F8, H4	VDD_IO	-	P	VDD for the rest I/O pins (3.3v)
7, 21, 27, 51, 60, 73, 80	A1, A5, A9, D1, F9, J1, J4	VSS	-	P	VSS for both CORE and I/O

Pin Type Description

O Output pin

OD-U Open-drain input/output pin with a 50kOhm internal pull-up to 2.5v

I-U Input pin with a 50kOhm internal pull-up to 2.5v

I-D Input pin with a 50kOhm internal pull-down to GND

I-US Schmitt-triggered Input pin with a 50kOhm internal pull-up to 2.5v

I/O Input/output pin

I/O-U Input/output pin with a 50kOhm internal pull-up to 2.5v

I/O-D Input/output pin with a 50kOhm internal pull-down to GND

U-I/O Differential USB input/output pin

XI Crystal input or single-ended clock input

XO Crystal output

P Power pin

Except for P, XI, and I-US type pins, which must be appropriately connected on the board, all the other pins can be left floating if not used.

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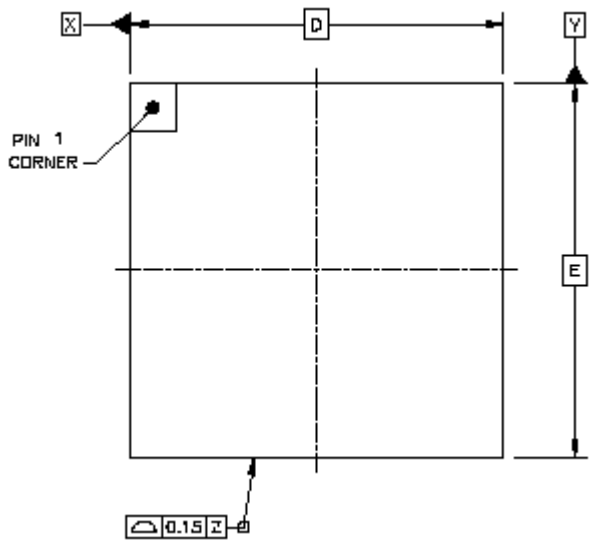
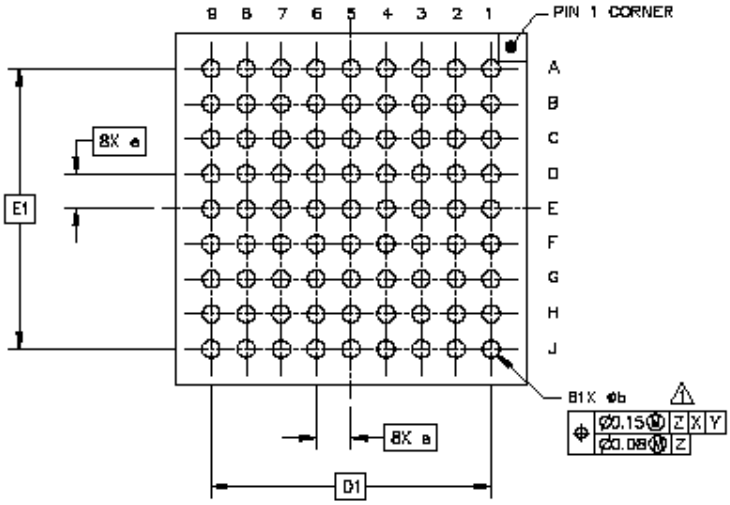
Package Outline

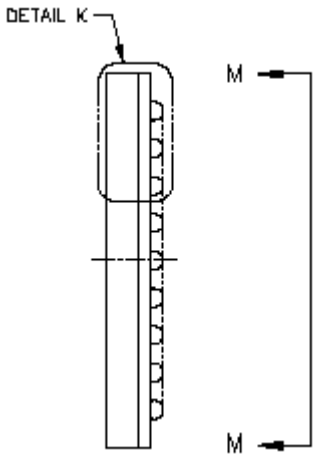
LFBGA-81

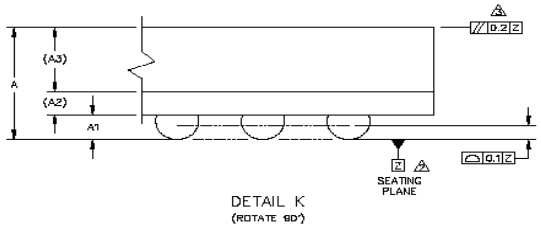


DIM	Min	Nom	Max
A	-		1.4
A1	0.3		0.4C
A2		0.26 REF	
A3		0.7 REF	
b	0.35	0.4	0.45
D		8 BSC	
E		8 BSC	
e		0.8 BSC	
D1		6.4 BSC	
E1		6.4 BSC	

All dimensions are in mm







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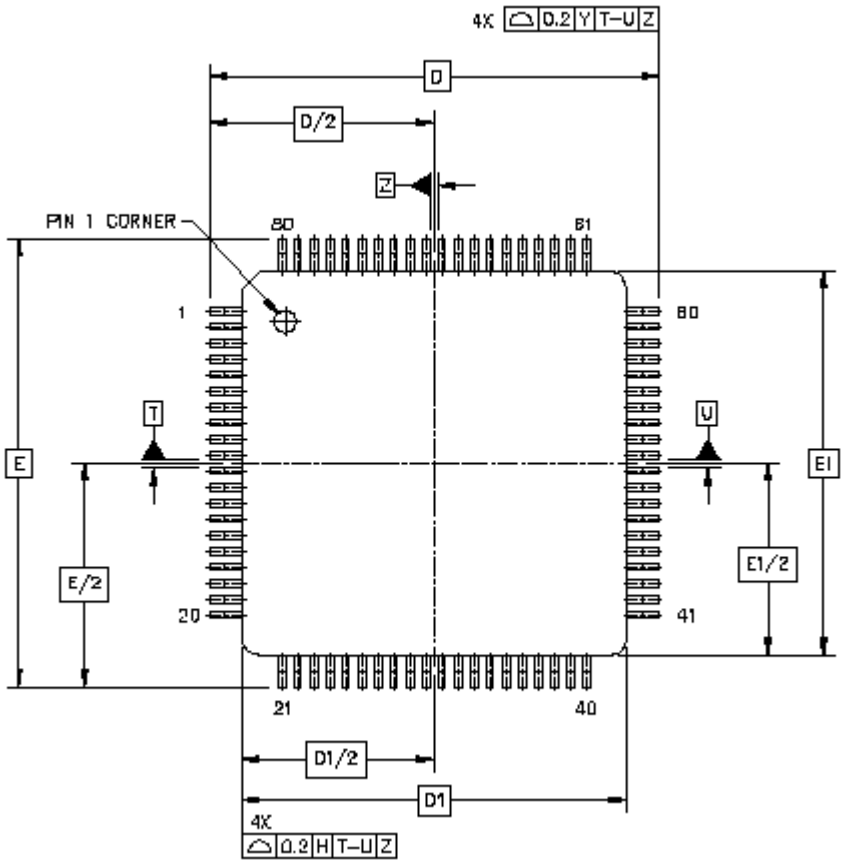
LQFP-80



DIM	Min	Nom	Max
A	---		1.6
A1	0.05		0.15
A2	1.35		1.45
b	0.17		0.27
D		14 BSC	
D1		12 BSC	
e		0.5 BSC	
E		14 BSC	
E1		12 BSC	
L	0.45		0.75
L1		1 REF	
R1/R2		0.2 REF	
S		0.17 REF	
θ	0°		7°
θ1	0°		---
θ2	10°		14°

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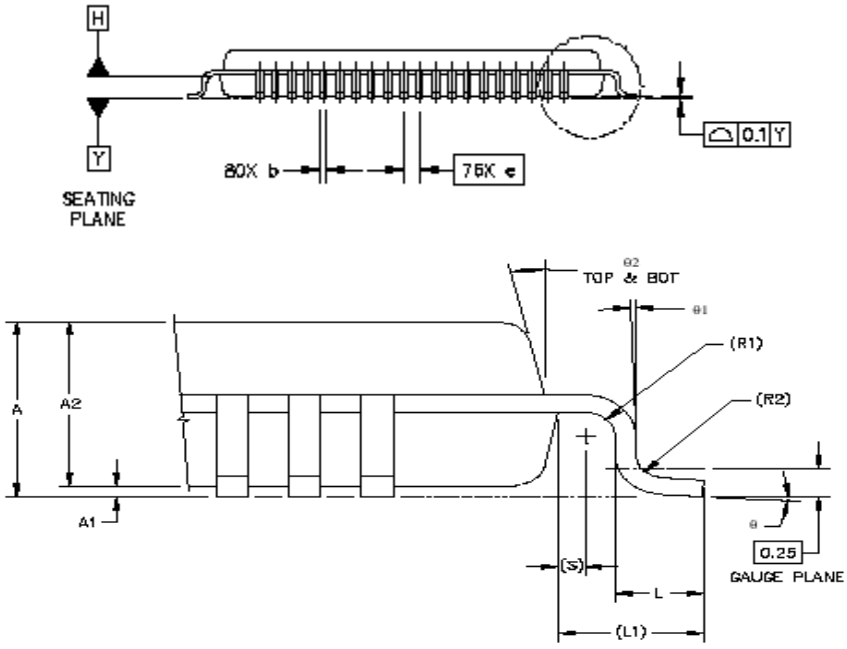

DETAIL F

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