

SELP

Technical Specifications

Via Giuntini 25 – 56023 – frazione Navacchio Cascina (PI) - ITALIA
Capitale sociale : 350.000 int. vers.
Registro delle imprese di Pisa n° 2819/1998 REA 127299 C.F. P.I. n° 01428250508

SELP Preliminary Datasheet		v1.0	03/06/02	Page 1/15
---------------------------------------	--	-------------	-----------------	----------------------

INDEX

INDEX.....2

1 INTRODUCTION.....3

 1.1 Features.....3

2 FUNCTIONAL DESCRIPTION.....3

 2.1 Functional description during Normal Operation.....3

 2.2 Current limitation at power on.....4

 2.3 Programmability of overcurrent level, filtering time and soft start time.....4

 2.4 Selp used with an External Power p-mos Switch.....4

 2.5 Stby mode and STBY and ALARM pins.....4

3 APPLICATION CIRCUIT.....6

4 SELP PIN.....7

 4.1 Pin Count.....7

 4.2 Package.....8

 4.3 Block Diagram.....9

5 ABSOLUTE MAXIMUM RATINGS.....10

6 ELECTRICAL CHARACTERISTICS.....11

7 **APPLICATION NOTE.....13**

8 **CONTACT US.....15**

1 INTRODUCTION

1.1 Features

-SELP IS REALIZED IN DMILL BiCMOS 0.8UM LATCH UP FREE TECHNOLOGY

-IT PROVIDES THE POWER SUPPLY TO OTHER NOT-LACH-UP-FREE CHIPS.

-IT CONTAINS AN INTELLIGENT 1 ohm MAX. P-MOS POWER WITH ITS DRIVER

-THE CURRENT ACROSS AN EXTERNAL RESISTOR CONNECTED BETWEEN THE SUPPLY PIN OF SELP AND THE SOURCE TERMINALS OF THE INTERNAL POWER SWITCH IS MONITORED AND, IF IT IS ABOVE A CERTAIN THRESHOLD FOR A CERTAIN PROGRAMMABLE FILTERING TIME, THE POWER SWITCH IS TURNED OFF

-THE OVERCURRENT SHUTDOWN EVENT PROVIDES A WARNING ON DEDICATED PIN ALARM

-AT POWER-ON LINEAR CURRENT LIMITATION IS PROVIDED (SOFT START)

-THE SOFT START TIME IS PROGRAMMABLE BY AN EXTERNAL CAPACITOR

-WHEN THE SUPPLIED CHIP REQUIRES MORE THAN 300mA, IT IS POSSIBLE TO USE AN EXTERNAL pMOS POWER DRIVEN BY THE DRIVER INTERNAL TO THE SELP

-BOTH POWER SUPPLY OF 5V AND 3.3V ARE SUPPORTED (see User's Manual at the end)

2 FUNCTIONAL DESCRIPTION

2.1 Functional Description during

Normal Operation

SELP is a device realized in BiCMOS 0.8um 5V rad hard DMILL technology which protects not-rad hard devices from dangerous latch up events. It contains a p-mos power switch with a R_{dson}MAX of 1 ohm, typycal 0.5 ohm, which provides the power supply to another device. The current across the power switch, which supplies the other device, is internally monitored. This current is sensed as a voltage drop on an external resistor connected in series with the pmos power switch. When the drop becomes higher than a certain threshold of typ 120mV, the latch up event on the serviced device is recognised, and, if the overcurrent condition remains for a certain filter time of typ 25us, the power switch is switched off and the logical bit on pin ALARM is set. Every time the pin ALARM is set, it remains set until the falling edge on the STBY pin: every time the power switch is turned off, it remains off until the next rising edge on pin STBY.

The logic input pin STBY has a pull down. This pin, when its voltage is low, puts the p-mos power switch in the OFF condition and it puts the device in stby mode: to make the power switches ON and the overcurrent monitor

SELP Preliminary Datasheet		v1.0	03/06/02	Page 3/15
----------------------------	--	------	----------	-----------

goes active, a rising edge on the logical input pin STBY has to be sensed.

2.2 Current limitation at power on

During power on, the device is protected against false overcurrent alarms induced by capacitor charges which require peaks of current. In fact, for a certain time between the rising edge on pin STBY occurs and an external capacitor is charged, a linear current limitation is internally provided on the power switch, providing the soft start. The level of this current limitation is just the normal operation threshold that causes ALARM pin is set and the p-mos power switch is switched off.

2.3 Programmability of overcurrent level, filtering time and soft start time

The overcurrent level at which the latch up event is sensed – the p-mos power switch is switched off and the pin ALARM is set – is adjustable by adjusting the external sense resistor: Obviously this affects the drop between the power supply and the power voltage supplied to the serviced device.

Any way, the maximum DC power dissipation allowed for the chip is 500mwatt and the maximum value for the resistance of the internal power p-mos switch is 1 ohm at 300mA.

The filter time for the overcurrent switch off is programmable by the external capacitor connected between pin FILT and ground.

The soft start time during which the linear current limitation is active is programmable by the external capacitor connected between pin SOFT and ground.

2.4 Selp used with an External Power p-mos Switch

The internal p-mos power switch has a R_{dson} of 1 ohm max at 300mA. Sometimes, the serviced device or devices have a total current consumption exceeding this current. In this cases it does not help to decrease the external sense resistor to obtain an higher overcurrent, because of the higher drop across the internal power switch, which reduces drastically the voltage level of the power supply furnished to the serviced devices. Than, the possibility to use an external power switch has been added. All the terminals of the internal power switch are bonded on pins, including the gate: than, an external p-mos power device can be connected between these pins. The functionality of the device in this condition is exactly the same as in the case the internal power switch is used.

2.5 Stby mode and STBY and ALARM pins

- **stby mode** is active when the logical input pin STBY is low.

Stby mode is low consumption mode: the current consumption during this mode of operation is less than 10uA. The power p-mos

switch is off during this condition, no current monitor is made, and the serviced device is also in stby mode. Pin ALARM is kept in high impedance and it is pull upped high by the external resistor.

- the **STBY** logic input pin has a pull down. On the low level of this pin, the device is put into the low consumption state (stand by): the current consumption in stand by mode is less than 10uA.

During the stby mode the power is switched off, and no current monitor is made.

The stby mode ends on the rising edge of STBY signal (normal operation mode), which causes the power p-mos switch is turned ON (with current limitation during the soft start time).

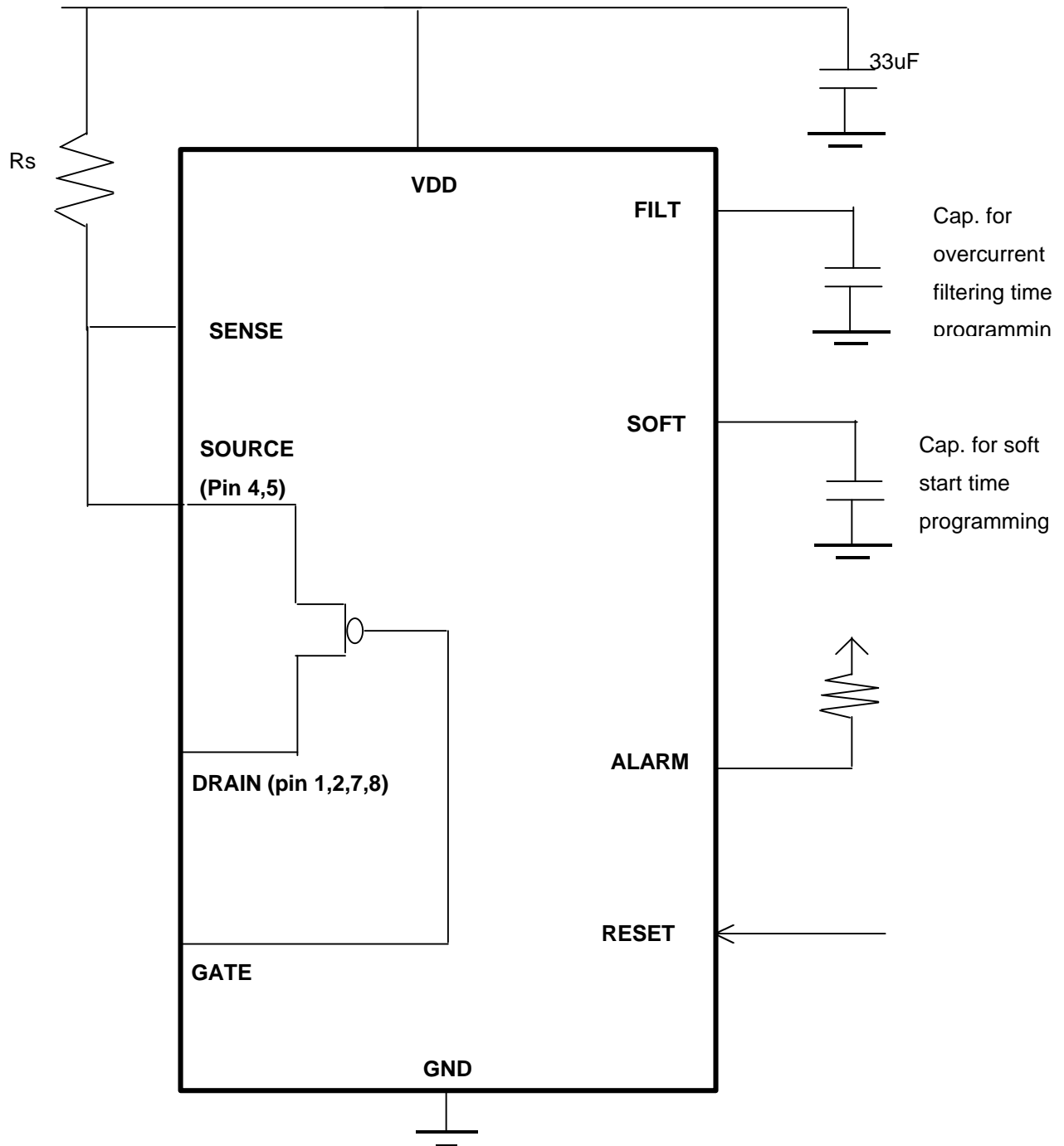
If, during the normal operation mode, an overcurrent event is sensed , the power is switched off and the ALARM pin goes active – low: The condition on pin ALARM is kept until the next falling edge on STBY pin, the off condition for the power switch is kept until the next rising edge on pin STBY.

- the **ALARM** pin is an open drain pin. An

external pull up resistor has to be connected between ALARM pin and VDD pin. This allows multiple wired open drain connections on the same net, in the case multiple SELP devices are used to protect a certain number of devices. Taking into account that the leakage current to ground for the ALARM pin is 5uA max, depending from the number of Selp devices have the pin ALARM connected together, one can calculate the value for the pull up resistor, taking into account the Rdson of the ALARM pin (see the specifications) when the internal pull down is active.

The internal pull down on the ALARM pin goes active (pin ALARM set low by the internal pull down n-mos transistor) whenever an overcurrent switch off occurs. This condition on the ALARM pin will be kept until the stby signal on STBY pin is high. On the next falling edge on the stby signal the internal n-mos transistor goes inactive and the ALARM pin is pull upped high by the external resistor. The device enter in the stby mode. On the next rising edge of the stby signal the device re-enters in normal operation mode, the power switch is turned on and current monitor is made.

3 APPLICATION CIRCUIT



4 SELP PIN

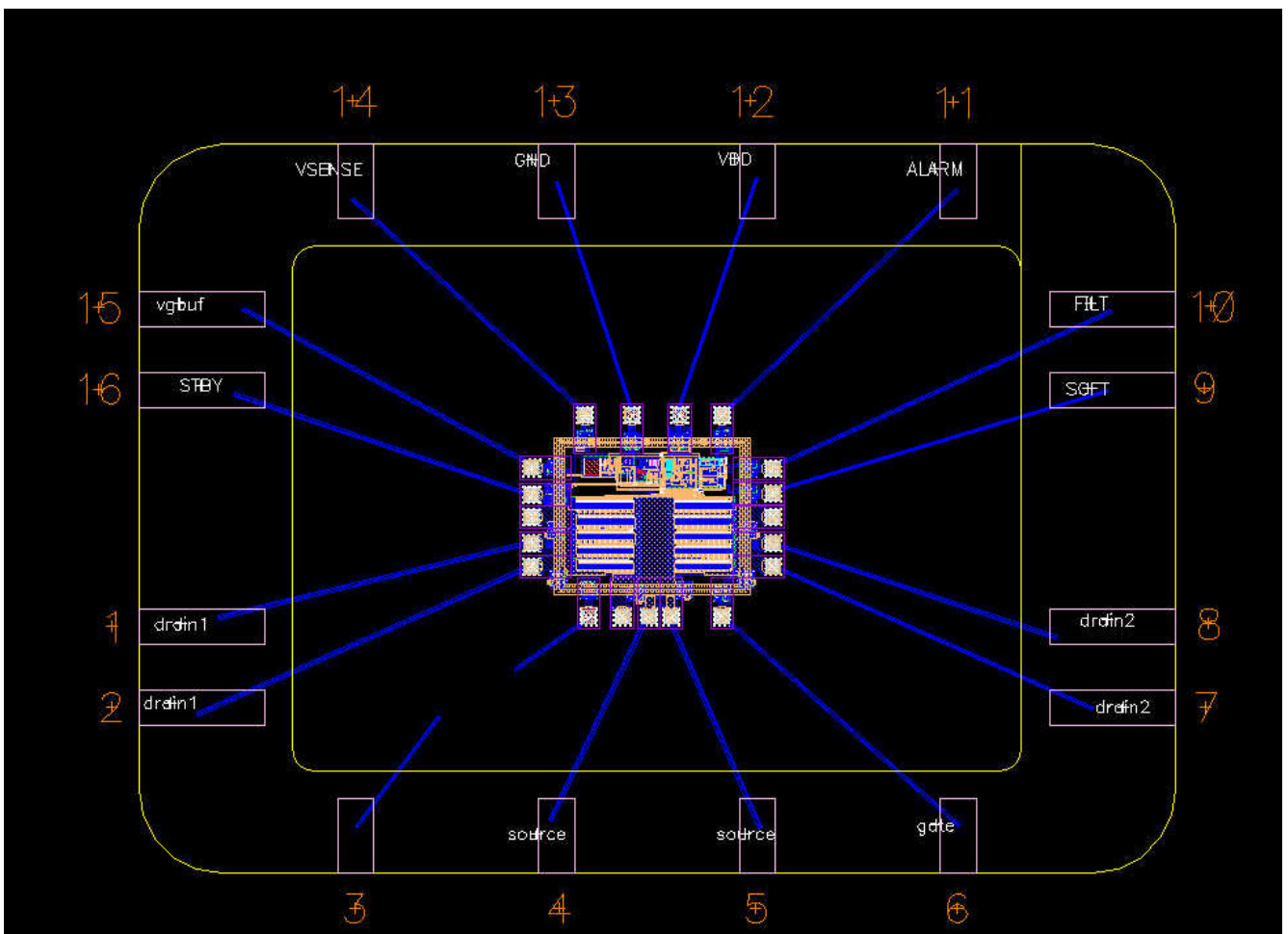
4.1 Pin Count

Pin Name	Pin Number	Description	Type
ALARM	11	Open Drain Logic Output pin. When low, an alarm is put (low active)	Open drain logic output. Low active.
STBY	16.	Logic low active signal to put the device in stby mode	Logic input pin, with pull down. When low, the device is put into the stby mode. Low active
DRAIN1	1	Drain Connection for the Internal Power Switch to be connected together with the other DRAIN pins	Power pin.
DRAIN1	2	Drain Connection for the Internal Power Switch to be connected together with the other DRAIN pins	Power pin.
DRAIN2	7	Drain Connection for the Internal Power Switch to be connected together with the other DRAIN pins	Power pin.
DRAIN2	8	Drain Connection for the Internal Power Switch to be connected together with the other DRAIN pins	Power pin.
SOURCE	4	Source Connection for the Internal Power Switch to be connected together with the other SOURCE pins	Power pin.
SOURCE	5	Source Connection for the Internal Power Switch to be connected together with the other SOURCE pins	Power pin.
GATE	6	Gate of the internal power p-mos switch. It has to be connected with the gate of the external p-mos power switch when used.	Analog pin: high impedance
VDD	12	Power supply for the device. It is also the upper sense pin for the overcurrent monitor	Analog and Logic Supply
GND	13	Ground Connection for the device	Analog and Logic Ground

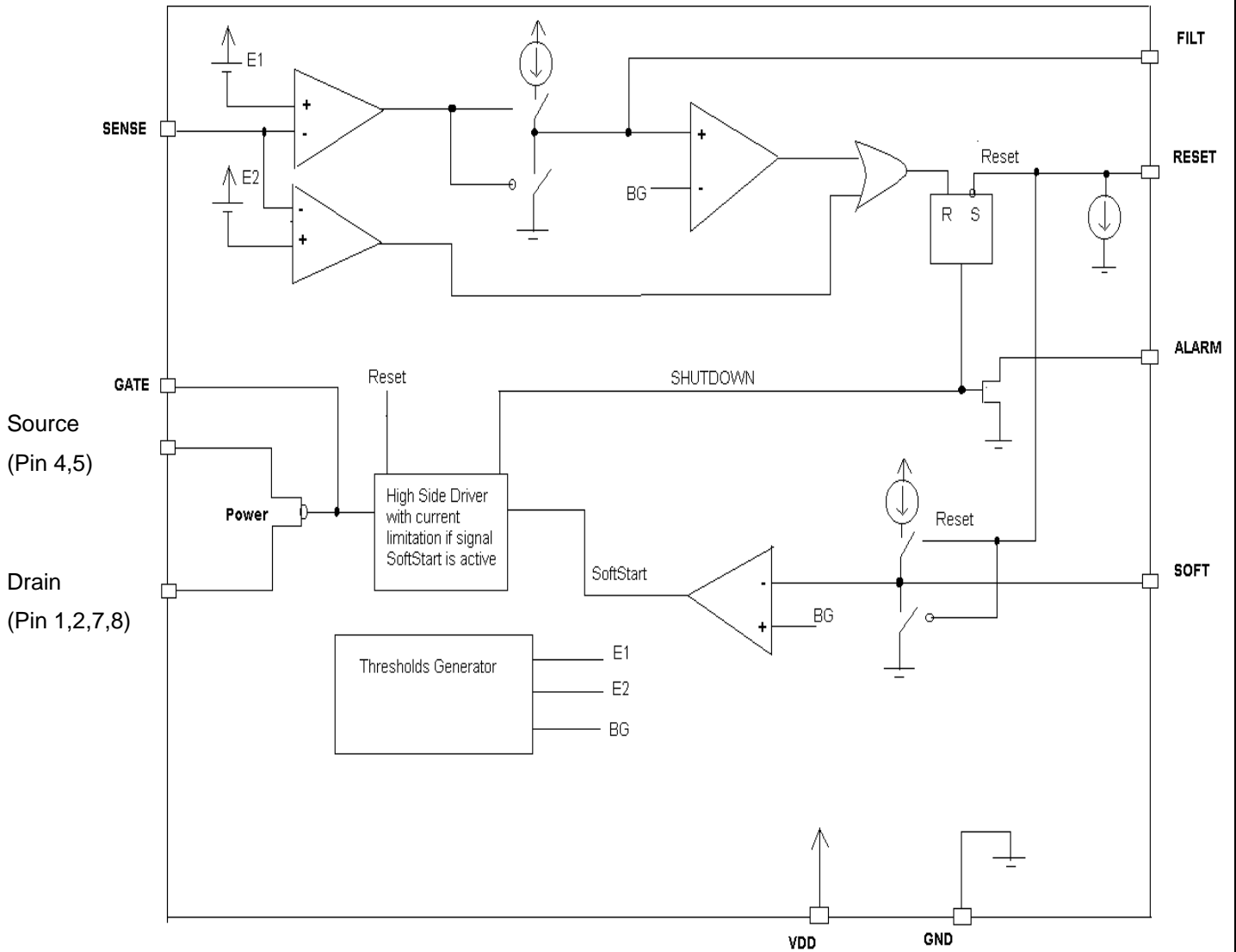
FILT	10	Pin dedicated to the programmability of the filtering overcurrent time with a capacitor connected to ground	Analog Pin
SOFT	9	Pin dedicated to the programmability of the soft start time (during which linear current limitation occurs) with a capacitor connected to ground	Analog Pin
SUB	3	Ground pin dedicated to the ground connection of chip back side. To be connected to GND pin externally	Ground pin.
SENSE	14	Pin dedicated to the sense for overcurrent monitor	Analog Input Pin

4.2 Package

The SELP is assembled in DIL16 Dual In line 16 pin Package. Frame: 6.4mm X 4.1mm
Hereafter the Bonding Diagram for the SELP



4.3 Block Diagram



5 ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Description	Max Value	Unit
VDDMAX	VDD	Maximum Voltage on Power Supply	6	V
Vpin	All Pins except VDD and GND	Maximum and Minimum Voltage	from -0.3V to VDDMAX+0.3	V
Pdissmax	SOURCE(Pin 4,5) DRAIN(Pin 1,2,7,8)	Maximum Allowed DC Power on the Internal Power Switch	300	mW
I _{maxpin}	All pins except SOURCE(Pin 4,5) DRAIN(Pin 1,2,7,8)	Max. sinked or sourced current allowed on pins	+/-10	mA
Short Circuit Duration	DRAIN(Pin 1,2,7,8)		continuous	
I _{maxpower}	SOURCE(Pin 4,5) DRAIN(Pin 1,2,7,8)	Maximum Peak Current due to Bondings	1.5	A
T _{operating}		Operating Temperature Range	-40 to 125	°C
T _{storage}		Storage Temperature Range	-55 to 150	°C

Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute rating conditions for extended periods may affect device reliability.

ESD specification: +-2KV human body model

6 ELECTRICAL CHARACTERISTICS

(VDD=3.3v +-10% or VDD=5V+-10%, Tamb from -40C to 125C, unless otherwise specified)

Symbol	Pin	Parameter Description	Test Condition	Min	Typ	Max	Unit
Rdson5	SOURCE Pin(4,5) DRAIN Pin(1,2,7,8)	On resistance of the internal power p-mos switch. Source(Pin4,5) are connected together, Drain(Pin 1,2,7,8) are connected together	Vsource= =Vsense=VDD=5V Idrain=100mA Power p-mos is ON (stby signal static high)	0.25	0.5	1	ohm
Rdson3			Vsource= Vsense=VDD=3.3V Idrain=100mA Power p-mos is ON (stby signal static high)	0.3	0.6	1.2	
Vth	VDD, SENSE	Threshold Voltage between VDD pin and SENSE pin for overcurrent warning at open drain pin ALARM and internal/external p-mos power switch off	VDD=5V or VDD=3.3V	90	120	150	mV
Iqq	VDD	DC current consumption un normal operation mode (no overcurrent nor stby)	VDD=5V STBY pin static HIGH No load is connected to pins DRAIN (1,2,7,8)			500	uA
Istby	VDD	DC current consumption during stby mode	VDD=5V STBY pin static LOW			10	uA
ifilt	FILT	DC current sourced from pin FILT versus ground when Vth is overcome	VDD=5V VDD-Vsense > Vth	5	10	15	uA
tfilt	FILT	Shut OFF time between Vth is overcome and ALARM pin is set	VDD=5V VDD-Vsense > Vth external Cfilt between FILT and GND 10pF	10	25	40	us

Symbol	Pin	Parameter Description	Test Condition	Min	Typ	Max	Unit
vlimit	VDD, SENSE	Soft Start Max. Drop	VDD=5V DRAIN(Pin 1,2,7,8) shorted to GND. SOFT pin floating. Stby pin high	90	120	150	mV
Vthlimit	SOFT	Threshold voltage on SOFT to make current limitation inactive	VDD=5V DRAIN(Pin 1,2,7,8) shorted to GND	1.05	1.25	1.35	V
vthfilt	FILT	Threshold Voltage to make the ALARM pin is set	VDD=5V DRAIN(Pin 1,2,7,8) shorted to GND	1.05	1.25	1.35	V
tsoft	SOFT	Time during which the current limitation is active after the rising edge on pin STBY	VDD=5V DRAIN(Pin 1,2,7,8) shorted to GND external Csoft capacitor 1nF	1	2.5	4	ms
isoft	SOFT	Current sourced from pin SOFT during tsoft	VDD=5V VDD-Vsense > Vth SOFT pin to GND	5	10	15	uA
Ipdwn	STBY	Pull Down Current on STBY pin	STBY=VDD=5V	5	10	15	uA
Vsat	ALARM	Saturation Low Voltage on pin ALARM when active	VDD=5V Ialarm = 500uA sinked by ALARM		0.2	0.4	V

7 APPLICATION NOTE

This section describes how to use SELP, especially the following graphs are significant for choosing the external sense resistor to fix the overcurrent value.

The resulting power supply furnished to the serviced device, is:

$$V_{res} = V_{dd} - (R_{external} + R_{dson}) * I_{ddq} \tag{1}$$

where $R_{external}$ is the external sense resistor, V_{dd} is the power supply for the SELP, I_{ddq} is the quiescent current for the serviced device and R_{dson} is the ON resistance of the internal or external p-mos power switch.

The resulting overcurrent threshold is fixed as an internal constant voltage threshold of 120mV divided by the external sense resistor:

$$I_{overcurrent} = 120mV / R_{external} \tag{2}$$

The maximum internal power dissipation is a function of the overcurrent threshold, and it is calculated as

$$P_{diss} = I_{overcurrent}^2 * R_{dson} \tag{3}$$

The filtering time for the internal or external pmos power is switched off is made as a current over an external capacitor. In general,

$$t_{filt} = C_{external} * I_{filt} * 2.5V / 100uA \tag{4}$$

The soft start time is made as a current over an external capacitor, and, in general:

$$t_{soft} = C_{external} * I_{soft} * 2.5V / 100uA \tag{5}$$

One can calculate the t_{soft} and the needed external capacitor by knowing the capacitor value connected on the power supply pin of the serviced device.

Taking into account that during the soft start time there is a current limitation at a value that is $I_{overcurrent} / 5$, one can calculate that, if C is the capacitor on the supply pin of the serviced device, this capacitor charges from 0V to V_{res} with a constant current $I_{overcurrent} / 5$ during the time:

$$t_{soft} = C * V_{res} / (I_{overcurrent} / 5), \tag{6}$$

and, using the formula (5), one can calculate the needed $C_{external} * I_{soft}$

Connecting the R_{sense} external resistor.

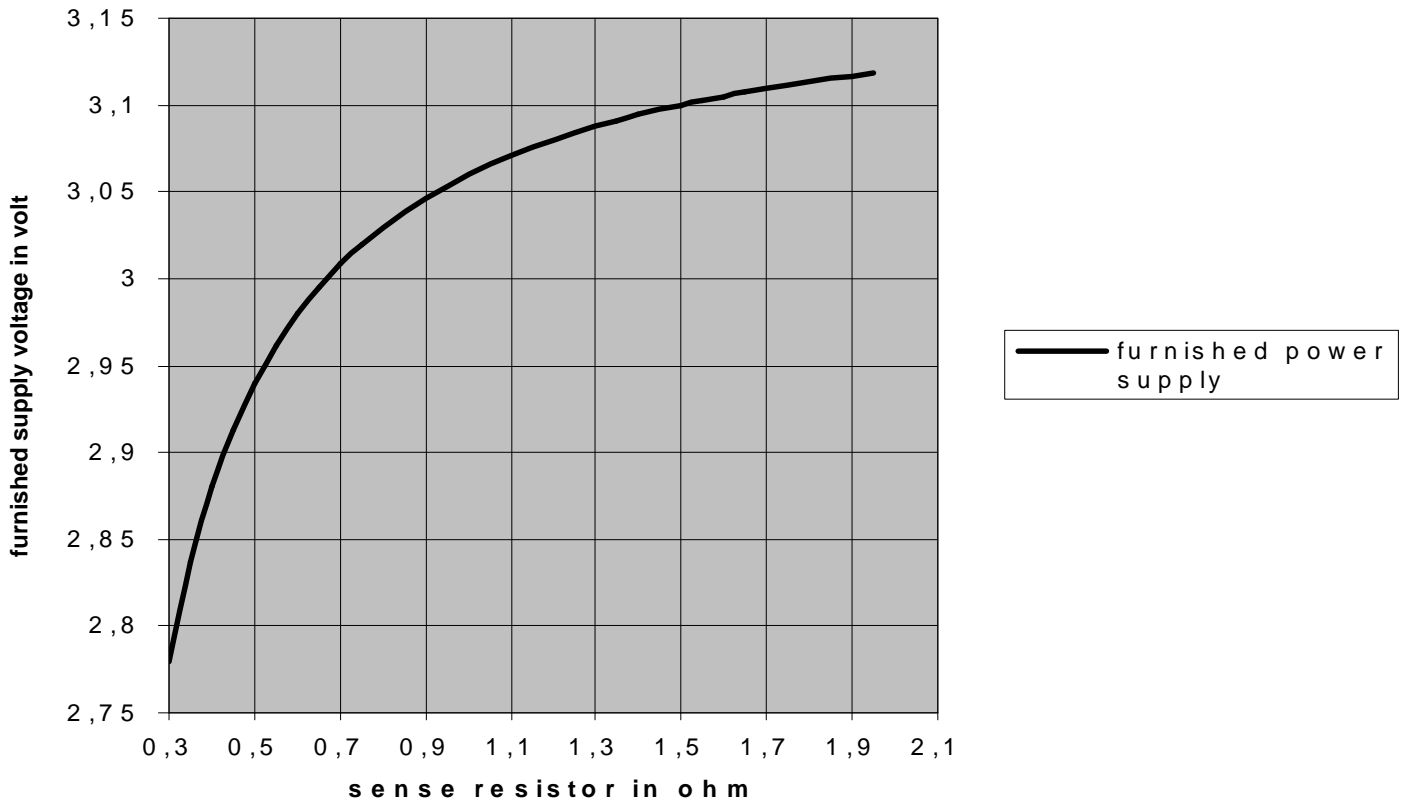
The external sense resistor has to be connected just between the pins VDD and SOURCE (4,5) connected together.

This avoids that additional current, not to be monitored, causes drops on the paths in series with the sense resistor: this could false -lower-the overcurrent protection threshold.

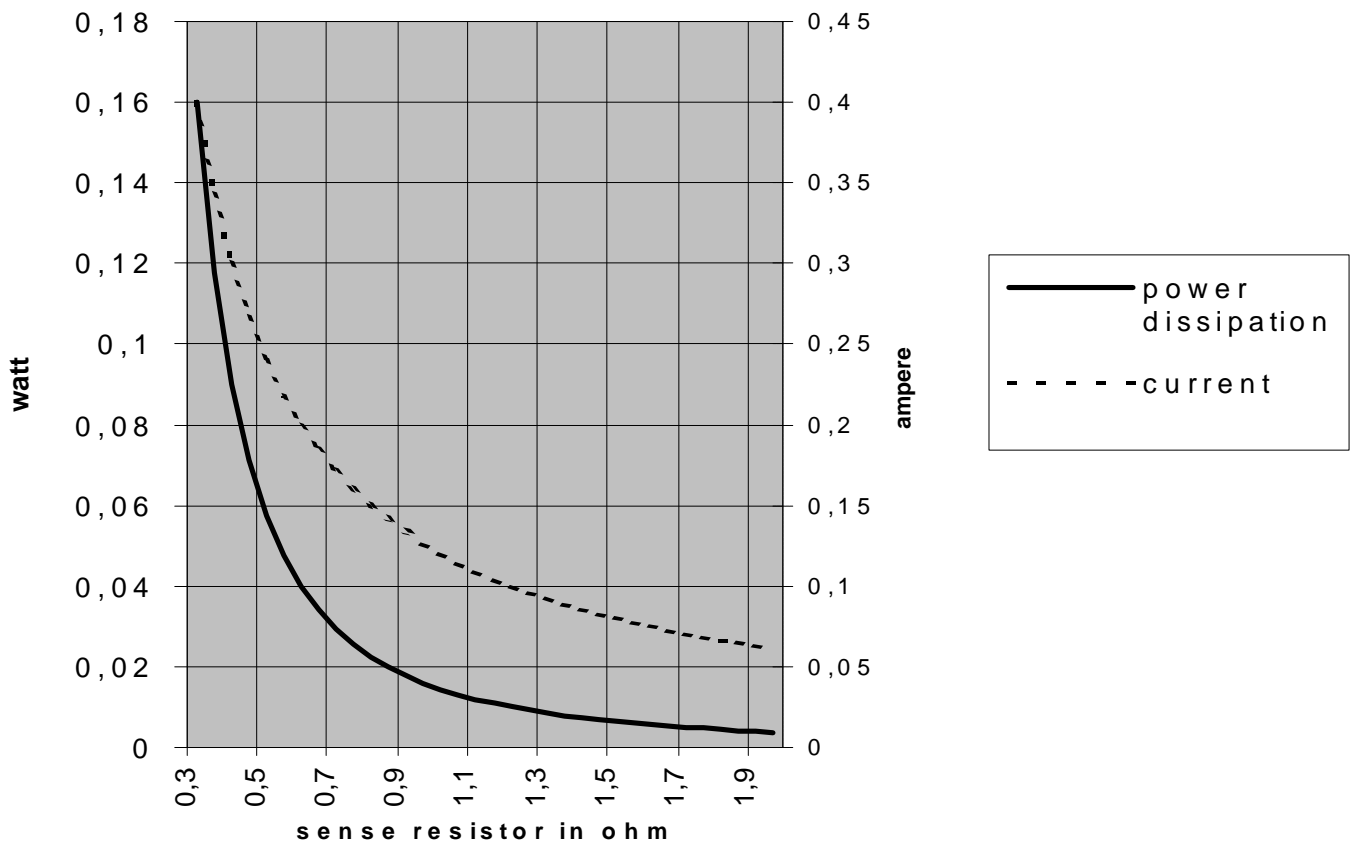
Connecting the external p-mos power switch.

The external p-mos power switch has to be connected between the pins SOURCE(4,5) GATE, DRAIN(1,2,7,8) with respecting the correspondence.

**Furnished Power Supply as a function of the external sense resistor: max R_{dson} of 1ohm is considered
typ threshold of 120mV is considered**



**Power Dissipation and Overcurrent Threshold as a function of external sense resistor: max R_{dson} of 1ohm is considered
typ threshold 120mV is considered**



8 CONTACT US

Aurelia Microelettronica – CAEN Microelettronica

operative office

Via Giuntini 13 - 56023 Navacchio PI - ITALY

Tel. +39.050.754260 - Fax +39.050.754261

E-mail: info@aurelia-micro.it URL: <http://www.caen.it/micro>

CAEN headquarters

Via Vetraia 11 - 55049 Viareggio LU - ITALY

Tel. +39.0584.388431 - Fax +39.0584.388959

